Oliver Hauck

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Background

GHz-range analog mixed-signal and digital fullcustom CMOS VLSI circuit design and layout, DCDC-conversion, asynchronous circuit design, high-speed pipelines, cryptography, number theory.

Working Experience

since 09/06: Infineon Technologies AG, Munich, Communications Solutions Business Unit
Working as mixed-signal design engineer on fully integrated GHz DCDC conversion for RF transceivers in 65nm CMOS.

05/01 – 08/06: Infineon Technologies AG, Munich, Chipcard Business Unit

01/04 – 08/06: Design lead and project manager for symmetric crypto coprocessor implementing secure AES (Advanced Encryption Standard) and DES in 0.13μm CMOS for new controller platform. Involved into security concept and design methodology. Worked on architecture, microarchitecture and fullcustom circuit design. Team has 6 members, budget 1M EURO.

05/02 – 12/03: Responsible for Data Encryption Standard (DES) coprocessor in 0.25μm and 0.13μm CMOS. Lead the design through tapeout til rampup and security certification. Patent pending for side-channel attack resistant flipflop circuit. DES currently integrated in $>$20 chipcard controller products.

05/01 – 04/02: Fullcustom designer for public-key cryptography coprocessor in 0.25μm CMOS performing modular multiplication with 2Kbit operands, $\approx$0.5M fullcustom devices. Responsible for circuit design, layout, simulation, and testchip tapeout.

Education

12/95 – 04/01: Doctoral studies at Integrated Circuits and Systems Lab, Departments of CS and EE, Darmstadt University of Technology
Advisor: Prof. Dr.-Ing. Sorin A. Huss

Doctoral Thesis: "Asynchronous Wave Pipelines for Energy Efficient Giga-Hertz VLSI"
Circuit styles for asynchronous wave pipelines are investigated. A new logic family called AWPCMOS is developed enabling latchless pipeline operation at 6 inverter delay cycle. A 1.0GHz 64b adder in 0.6μm CMOS and a 1.0GHz

270b elliptic curve crypto processor in 0.35μm CMOS are designed and fabricated. Other projects include Huffman coding, DCT and SRT division. Secured funding of followup project via DFG. Defense took place 24th April 2006. Graduated as "Dr.-Ing." with magna cum laude.

Teaching: Undergraduate digital logic design class; graduate class in VHDL modeling and synthesis. Thesis advisor of five MSc students, including two from IIT Bombay.

Publications: Nine papers, including seven on international IEEE conferences.

10/90 – 11/95: University of Karlsruhe, "Diplom" (MSc) in Computer Science, grade 1.8.

MSc Thesis: "Factoring large integers with elliptic curves in VLSI"
Advisor: Prof. Dr. Thomas Beth

Courses: VLSI (adv. digital design, adv. VLSI circuits, asynchronous design, signal processing, test, verification, synthesis); parallel computing architectures and compilers; theory (computability, complexity, neural nets, cryptography, number theory).

08/92 – 03/93 and 10/93 – 06/94: C-programming of a C-compiler frontend for a new parallel machine built at the school of CS at University of Karlsruhe.
Advisor: Prof. Dr. Walter Tichy

Skills

- English fluent written and orally.
- Cadence DF-II, Composer, Virtuoso XL Layout Editor, Custom Placer and Router, Analog Artist Environment, Spectre, Titan, Nanosim, Pathmill, Simplex power grid analysis, HP-83000 chip tester, SONNET EM simulation.
- C, Perl, VHDL.

Biographical Information

Personal data: born Aug 9th, 1969 in Neustadt an der Weinstrasse; German citizen; married; one son.

1980 – 1989: "Gymnasium" (High school); graduated top of school (grade 1.0).

06/89 – 08/90: Obligatory military service at the German Air Force.
