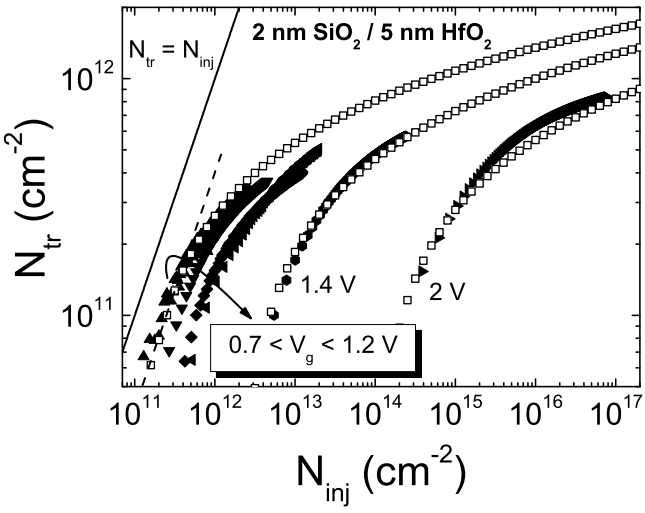

Figure 6.51: Trapped charge, N_{tr}, as a function of N_{inj} for several bias conditions (solid symbols). The open symbols show the trapped charge calculated by integrating the trapping probability in Fig. 6.50.

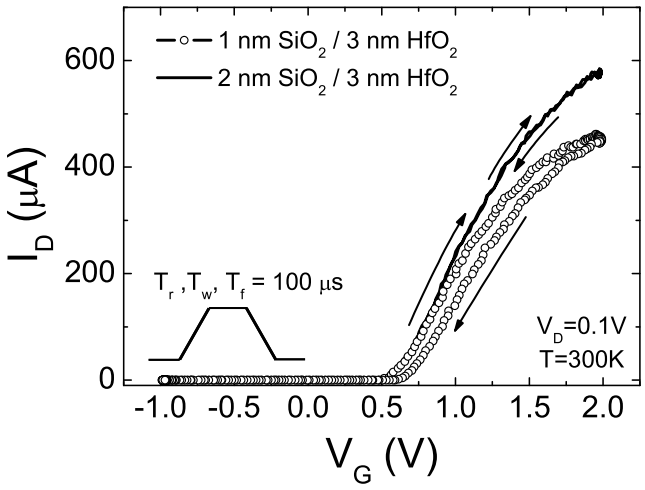

Figure 6.52: Transient I_D-V_G for 1 nm SiO_2 / 3 nm HfO_2 and 2 nm SiO_2 / 3 nm HfO_2. At the V_G=2V, the 2 nm SiO_2 / 3 nm HfO_2 stack shows no instability (see Fig. 6.53). The inset shows the pulse shape used to measure transient I_D-V_G characteristic.

6.2.8 Charge trapping versus relaxation of dielectric polarization

Dielectric relaxation losses in high-ε materials were proposed in the literature [62] as the cause for the threshold voltage instability. To clarify this point the injector

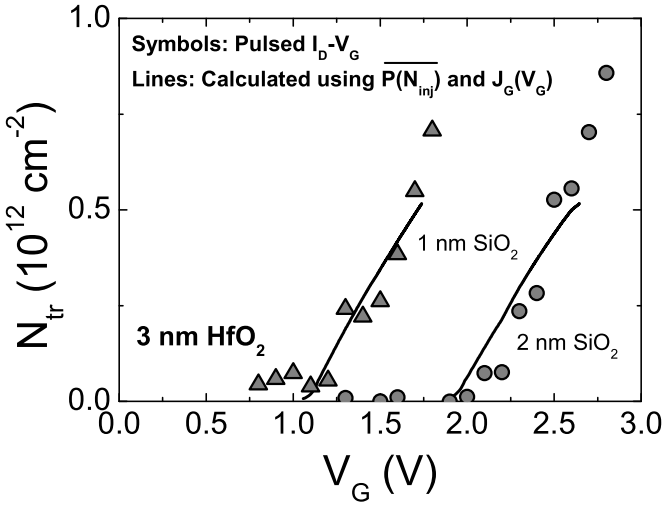

Figure 6.53: Comparison of the measured trapped charge (using the methods discussed in the context of Fig. 6.52) with the calculated trapped charge (using the apparent trapping probability of Fig. 6.50 and gate current data) in a 3 nm HfO_2 layer with 1 and 2 nm interfacial layers, respectively.

stacks previously introduced will be used where instabilities due to charge injection can be clearly separated from effects of dielectric polarization and its relaxation.

Samples with an EOT of ~ 2 nm were used in literature to illustrate the effects on the current transients and the V_{FB} or V_T shifts due to dielectric relaxation losses. To facilitate the discussion the shifts in the C-V characteristic due to gate stress are briefly summarized for the case of a thin interfacial layer and the injector stacks with a thick HfO_2 layer.

For the case of a thin interfacial layer in combination with thick HfO_2 the HF C-V characteristic again confirms the presence of electron trapping for positive gate bias (compare solid circles with triangles in Fig. 6.54). After stress at 3.8V a flatband voltage shift of close to $+1V$ is measured. This shift corresponds to an equivalent oxide charge of at least $5 \cdot 10^{12}/cm^2$, located near the Si surface. After applying a negative bias to the gate the initial V_{FB} recovers, indicating that the charge can be detrapped by a negative stress voltage. In addition, a significant stretch-out in the HF C-V characteristic is present after the negative bias stress which indicates the formation of interface states, similar as it has been observed previously for SiO_2 / Al_2O_3 stacks. It should be noted, that in the case of a thin interfacial layer carrier injection from the Si substrate already occurs at low positive gate bias. Therefore, the effects related to charge injection cannot easily be separated from the dielectric polarization effects which are linearly dependent on the oxide field [63].

When the interfacial layer thickness is increased there is no measurable V_{FB} shift in the low voltage regime, as can be seen in Fig. 6.55. As soon as charge injection occurs, $V_G > 7V$, the HF C-V characteristic rapidly shifts towards positive values. Since now F-N tunneling is used for charging, the injection field can be controlled very well. The field in the HfO_2 layer and the current density, however, are coupled.

Form the total voltage shift of 1V for the largest stress bias a stable trapped charge density of $\sim 8 \cdot 10^{12}/cm^2$ is calculated. This value is obtained when the charge is located at the SiO_2 / HfO_2 interface. (The charge centroid is assumed to be at $x = EOT_{HfO_2}/EOT$, where EOT_{HfO_2} is the contribution from the HfO_2 layer to the equivalent oxide thickness). This number is in reasonable agreement with the value obtained for the stacks with 1 nm interfacial oxide.

The pronounced distortion in the C-V characteristic in Fig. 6.55 is attributed to a high interface state density caused by poor interface passivation. The presence of defect states at the interface between the Si substrate and the thick SiO_2 layer is not expected to have a detrimental influence on the charge injection, so it is of minor significance for the discussion here.

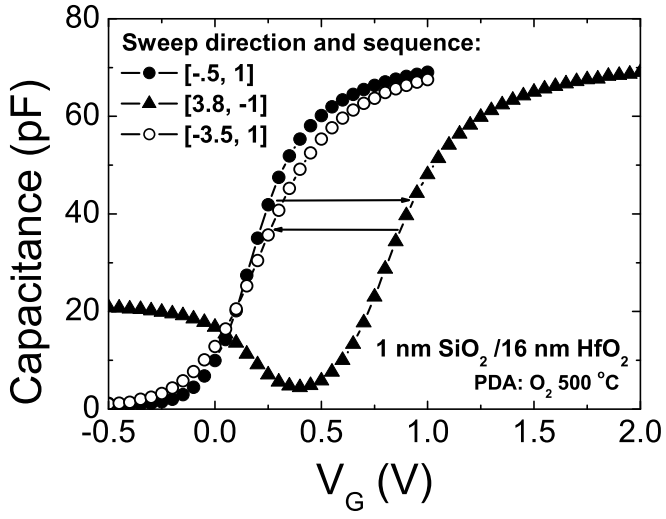

Figure 6.54: C-V characteristic of 1 nm SiO_2 / 16 nm HfO_2 before and after charge injection from the substrate and gate respectively. Positive C-V shift for substrate injection (V_G positive) due to electron trapping which recovers after applying a negative bias. Note the stretch-out in the HF C-V characteristic due to carrier injection from the gate.

The transient nature of the charge trapping was discussed in the previous section which causes a stretch out in the gate I-V characteristic at high current densities (see also Fig. 6.57). This feature is well known from the literature and is related to charge trapping (trapping ledge in the I-V characteristic). The magnitude of the I-V shift with respect to the calculated I-V curve saturates at a value of about 2.5V at a gate bias of $\approx$ 12.5V. From this shift, a much larger trapped charge density of $\sim 2 \cdot 10^{13}/cm^2$ is calculated, using the charge distribution model discussed above. If converted into a bulk density, values in excess of $10^{19} cm^{-3}$ are obtained.

To further quantify transient charging in the thick HfO_2 layer, a short diagnostic stress pulse at 13V was applied for 5 seconds and the gate current was monitored as a function of time after the voltage was reduced to accumulation condition of 3V (see Fig. 6.56). The different data sets were obtained with various integration settings on the parameter analyzer. Identical results are obtained and therewith any measurement artefact can be excluded. The results for the SiO_2 control, in Fig. 6.56, show that we indeed measure a current originating in the HfO_2 layer. It is

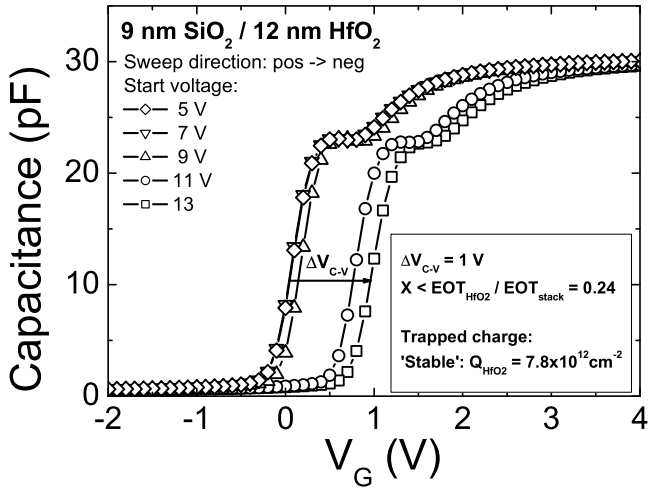

Figure 6.55: C-V characteristic of 9 nm SiO_2 / 12 nm HfO_2 using a sequence as indicated in the figure. A measurable C-V is observed when sufficient carriers are being injected through the thick SiO_2 layer ($V_G > 7V$).

interesting to note that the current decays proportional to t^{-1} at long times, with a possible deviation from that law at short times. Such transient current have been observed previously and have been interpreted in the context of charge trapping (for nitrides for example) [64] or in the context of dielectric relaxation [62].

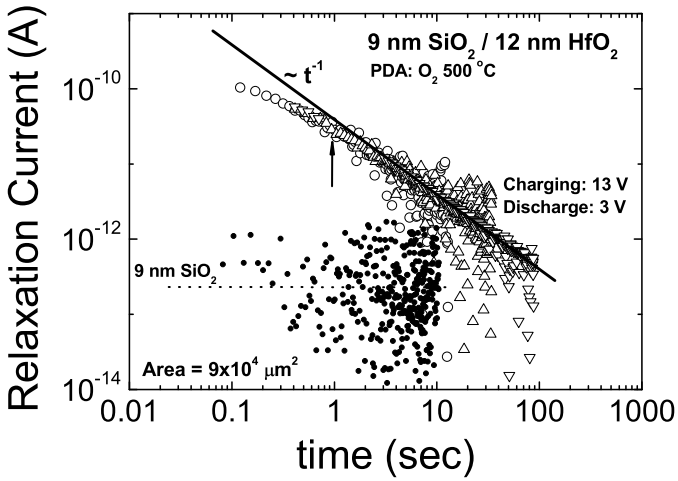

Figure 6.56: Transient current measured at $V_G = 3V$ after charge injection at $V_G = 13V$ for the gate stack shown in Fig. 6.57. The discharging current decays proportional to t^{-1}.

Based on the strong charge trapping observed in these stacks, we strongly favor

the interpretation in terms of charge trapping and detrapping. The comparison of the transient current and the gate current I-V for the injector stack, discussed in Fig. 6.57, further supports this interpretation. The bottom panel shows the transient current, measured at 3V in accumulation. The current values plotted were extracted from transient current traces as those shown in Fig. 6.56 at a time of 1s. In other words, the leakage current was measured 1 sec after the stress pulse was taken off. In the top panel the corresponding I-V characteristics are shown, where the negative bias trace was taken using light illumination. By comparing the data in the two panels for positive gate voltages, it is evident that a drastic increase in the transient current is measured at the same voltage where strong charge trapping is observed from the I-V traces. At lower positive voltages (below $\sim 9V$), where the I-V characteristics show ideal behavior (little charge trapping), the transient current is small and difficult to resolve. For negative gate bias, transient currents are much smaller but nevertheless significant in the range where current injection occurs. Possibly, this feature is also related to charge trapping. However, since n-type substrates were used for these measurements, some uncertainty remains because of depletion issues on n-type capacitor structures under negative gate bias. For conclusive measurements, p-type substrates with a top injector should be used. The fabrication of such structure, however, may be rather difficult.

If the transient currents were due to polarization only, a linear behavior with stress voltage at constant sense voltage would be expected. This is clearly not the case. If polarization and polarization relaxation does occur, the transient currents have to be measured at small voltages where trapping is minimal. As can be seen from the data in Fig. 6.57, the relaxation current is below the detection limit in these devices. Improved resolution would require even larger device structures, which were not available on our mask set.

In summary, the use of the injector stack allowed to confirm the cause for the measured instability in SiO_2 / HfO_2 dual layer gate stacks. No indication of an instability is observed when charging injection is minimized, whereas strong V_{FB} shifts and current-transients appear after large carrier injection. In the literature, these effects have been attributed to dielectric relaxation losses. The data presented here do not convincingly support this idea, whereas a strong indication for trapping related instabilities is given.

6.3 Impact of charge trapping on device performance

Charge trapping in high-ε materials not only causes V_T instabilities but also is responsible for performance degradation. To quantify the impact of charge trapping on the drive current degradation, and furthermore to correctly assess the channel carrier mobility in MOSFETs several techniques are described in the literature. In this section, an alternative technique is introduced which directly measures the inversion / trapped charge in MOSFETs and the drive current taking advantage of the same measurement speed. First, the technique will be verified using an oxide control and later it will be applied to SiO_2 / HfO_2 dual layer gate stacks.

6.3.1 Inversion Charge Pumping (ICP) and pulsed I_D-V_G technique

A common technique to extract the carrier mobility in MOSFETs is given by combining the split C-V with static I_D-V_G characteristics as described in Section 2.2.2.

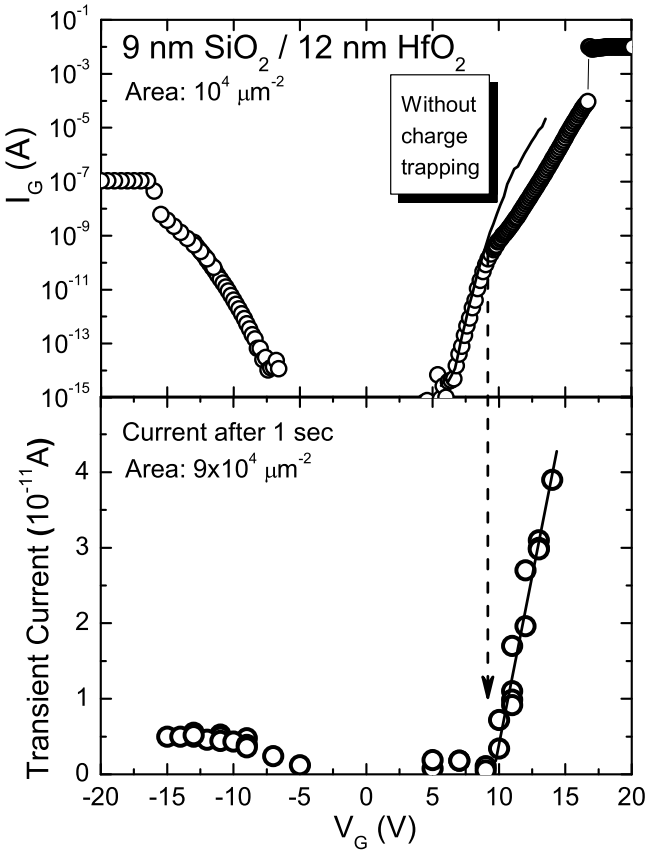

Figure 6.57: Current voltage characteristic for positive and negative polarity measured on 9 nm SiO_2 / 12 nm HfO_2 with poly-Si electrodes (upper figure). Transient current after 1 sec due to charge injection from either gate or substrate. Non-linearity in transient current coincides with onset of strong charge trapping for substrate injection.

The inversion charge wich is obtained by integrating the split C-V characteristic is directly compared with the drive current measured at low drain bias. The carrier mobility extracted by this comparison usually is plotted versus the effective Si field which is either calculated from the substrate doping (given in Section 2.2.2 Eq. 2.39) or obtained from the depletion capacitance.

In Fig. 6.58 typical split C-V and I_D-V_G characteristics are shown for a ~ 2 nm SiO_2 control sample.

From the data show in Fig. 6.58 the carrier mobility was extracted using the depletion approximation given in Section 2.2.2 by Eq. 2.40. A substrate dopant concentration of $5 \cdot 10^{17} cm^{-3}$ was used to calculate the effective Si field. In Fig. 6.59 the carrier mobility obtained from the SiO_2 sample is shown and compared with the universal mobility characteristic [12]. As can be seen, good agreement between the extracted carrier mobility on n-channel MOSFETs with the universal mobility characteristic is obtained in the high-field regime.

Mobility extractions based on the split C-V technique in combination with static

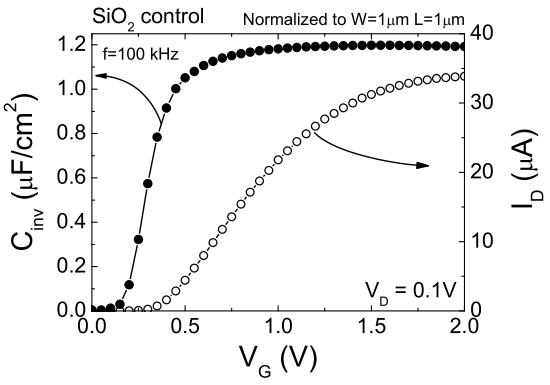

Figure 6.58: Conventional split C-V and I_D-V_G characteristic of a 2.1 nm SiO_2 control.

I_D-V_G measurements work well for conventional gate dielectrics. However, in case of high-ε materials this technique is not reliable due to the presence of strong charging effects during the quasi-DC measurements. To overcome this difficulty an alternative measurement technique is proposed which measures the inversion charge and drive current in the μs time range [65].

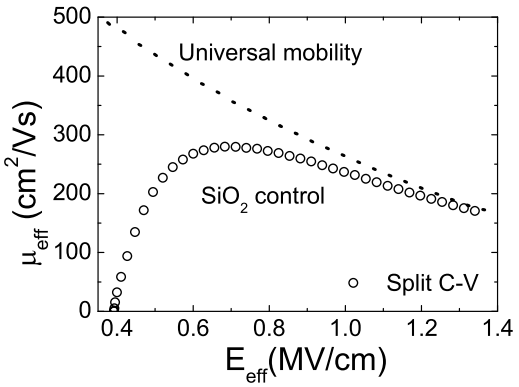

Figure 6.59: Electron mobility extracted for the SiO_2 control from the split C-V and the I_D-V_G data shown in Fig. 6.58 using the equations given in Section 2.2.2.

The proposed alternative technique for inversion charge measurements in MOSFETs is based on the geometrical component which is a parasitic effect in classical amplitude sweep charge pumping. To maximize the contribution from the geometrical effect long channel devices in combination with fast rise / fall times are used. In Fig. 6.60 the schematic measurement setup for Inversion Charge Pumping (ICP) is shown. Even though long channel devices are used, some fraction of the inversion charge still escapes back to the source / drain junction and does not contribute to the substrate current. By making use of the device symmetry the results can be corrected for this. Therefore, the charge pumping characteristic is measured contacting both junctions in one case and only one junction in the other case. The

complete inversion charge is then calculated using $N_{inv} = 2 \cdot N_{ICP_b} - N_{ICP_a}$, where the index a and b corresponds to the device configuration as shown in Fig. 6.60.

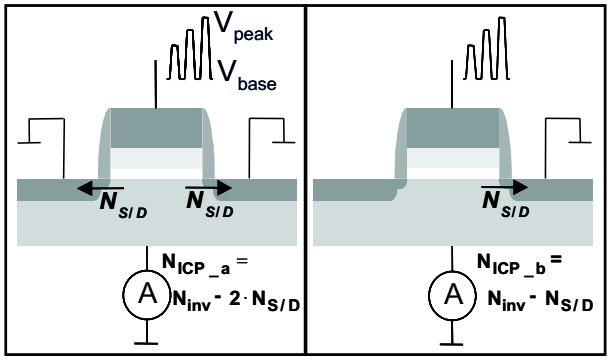

Figure 6.60: Schematics of the Inversion Charge Pumping (ICP) setup used to extract the inversion charge in long channel FETs.

The comparison of the inversion charge extracted from the split C-V (data Fig. 6.58) and the directly measured inversion charge by the variant of the charge pumping technique is shown in Fig. 6.61. The data in Fig. 6.61 are plotted on a linear and a logarithmic scale, to display the inversion and the sub-threshold regime simultaneously. Good agreement between the two techniques is obtained for the SiO_2 control.

In addition to the inversion charge, the drive current is measured on the same time scale using the pulsed measurement setup discussed in Section 5.2.3 using the same measurement speed as for charge pumping. Fig. 6.62 shows for the oxide control a comparison between the pulsed I_D-V_G characteristic and the conventional DC ramp measurement. Good agreement between the DC and pulsed measurement is evident. The small deviations in the characteristics may arise from a variation between different devices.

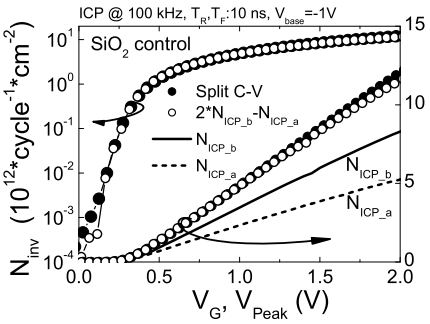

Figure 6.61: Comparison of inversion charge measured by conventional split C-V and by the ICP technique for the SiO_2 control using long channel ($100\,\mu$m) FETs. Data is plotted on linear and logarithmic scale.

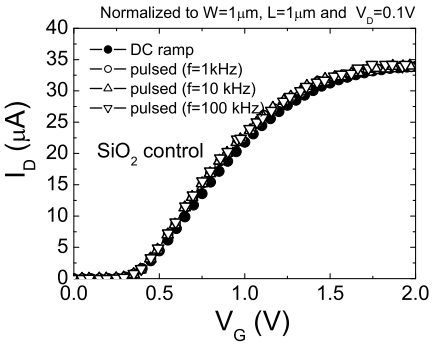

Figure 6.62: Pulsed I_D-V_G characteristic of the SiO_2 control using the measurement setup as discussed in Section 5.2.3. For comparison the DC result is shown using a parameter analyzer.

From the data shown in Figs. 6.61 and 6.62 the carrier mobility was extracted and plotted versus the effective Si field which was calculated in the same way as

in Fig. 6.59. As can be seen from Fig. 6.63 the carrier mobility obtained by the ICP in combination with pulsed I_D-V_G measurements is in good agreement with the conventional split C-V technique. The minor discrepancy in the peak mobility is most likely caused by the deviation between the pulsed and quasi-DC I_D-V_G measurement. However, the results for the SiO_2 control device demonstrate that ICP and pulsed I_D-V_G is an alternative procedure to extract the carrier mobility in MOSFETs which opens the window towards the μs time range.

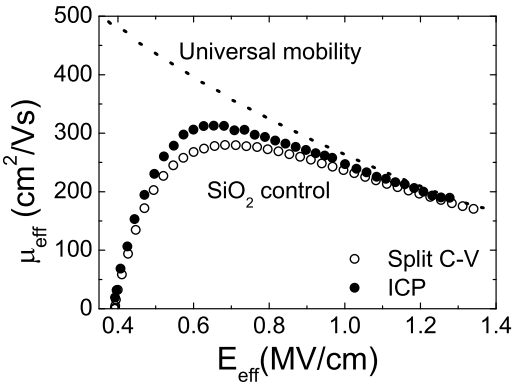

Figure 6.63: Comparison of electron mobility extracted from conventional ramp (Fig. 6.58) and pulsed (Fig. 6.61 and 6.62) measurement technique.

6.3.2 Mobility extraction in HfO_2 using ICP and pulsed I_D-V_G technique

In the previous section, an alternative technique was introduced to measure the inversion charge and the drive current in the μs time range. In the following, the combination of ICP with pulsed I_D-V_G measurements is used to assess the impact of charge trapping on the carrier mobility in SiO_2 / HfO_2 dual layer gate stacks with conventional poly-Si gate electrodes. From a conventional split C-V and I_D-V_G hysteresis measurement the severity of the charge trapping is clearly evident as shown in Fig. 6.64. To reduce charge trapping and to correctly account for the remaining charging effects, the ICP technique combined with pulsed I_D-V_G measurements were carried out at a frequency of 100 kHz or a charging time of 5μs.

Inversion charge pumping was performed on 20 μm×20 μm n-channel MOSFETs with a rise / fall time of 10 ns. Under these conditions the long channel is rapidly pinched-off, which forces a large fraction of the inversion charge to recombine in the Si where it can be measured as a substrate current. In Fig. 6.65 the normalized charge per cycle is shown for the measurement configurations shown in Fig. 6.60. Similar charge densities are extracted when the device symmetry is taken into account compared to the split C-V technique. However, the charge densities extracted by ICP still include the contribution from the trapped charge. To account for the trapped charge in the ICP technique, an additional charge pumping measurement using the amplitude sweep is required and was carried out on a short channel device (1 μm), where the geometrical effect is negligible. In Fig. 6.66 the contribution from electron trapping to the substrate current is shown for various frequencies / charging times. As can be seen, even at a frequency of 100 kHz there is still a significant

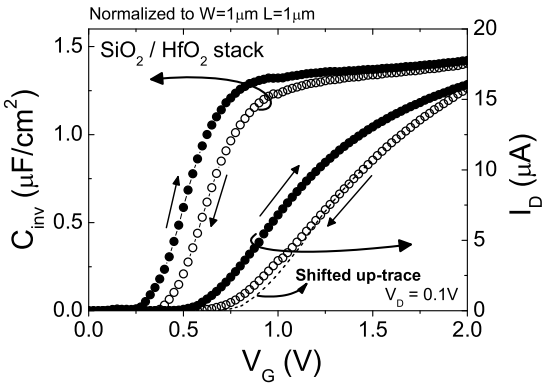

Figure 6.64: Split C-V and I_D-V_G characteristics for the SiO_2 / HfO_2 stack. A positive V_T shift is observed on the down trace due to electron trapping during the measurement.

contribution from charge trapping to the substrate current which needs to be considered. Furthermore, taking the carrier back diffusion into account, as described in detail in Section 6.2.5, the contribution becomes even more pronounced.

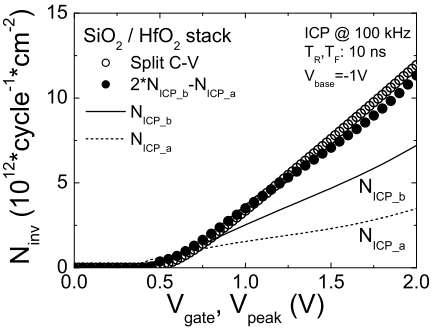

Figure 6.65: Comparison of inversion charge obtained from the split C-V (up trace in Fig. 6.64) with the charge measured by ICP in a long channel (20 μm) FET as described in Fig. 6.60.

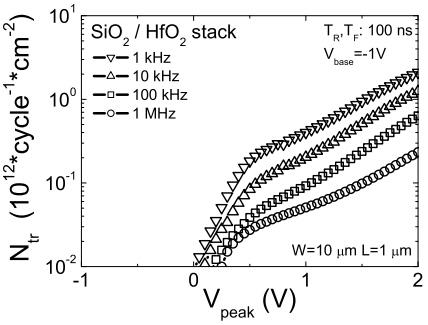

Figure 6.66: Trapped charge in the SiO_2 / HfO_2 stack measured in a short channel (1 μm) FET by the C-P technique using an amplitude sweep as described in Section 5.2.5 with long (100 ns) rise / fall times. No inversion charge is measured here.

In Fig. 6.67 the corrected inversion charge characteristics obtained by ICP are shown and compared to the integrated split C-V. The 1^{st} order correction was obtained by simply subtracting the measured trapped charge from $N_{inv} = 2 \cdot N_{ICP_b} - N_{ICP_a}$, whereas the 2^{nd} order correction considers the carrier back diffusion to the source / drain junction. When all these effects are taken into account, the determined inversion charge in the channel is significantly overestimated by the conventional split C-V technique, especially in the high field regime. Beside the inversion charge also the drive current of the MOSFET was measured under condition where charge trapping is strongly reduced. In Fig. 6.68 a comparison between the quasi-DC and the pulsed I_D-V_G characteristic is given. A significantly enhanced

drive current is measured when the measurement time is reduced, especially at large gate bias.

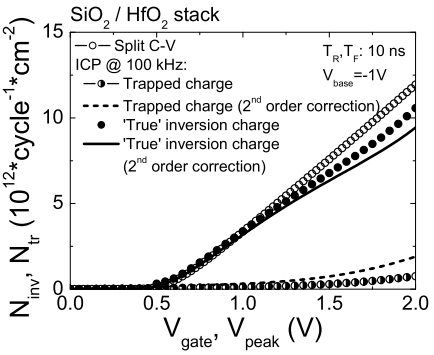

Figure 6.67: The "true" inversion charge in the SiO_2 / HfO_2 stack is calculated by subtracting the trapped charge (N_{tr} in Fig. 6.66 as measured and corrected for carrier back diffusion as discussed in Section 6.2.5) from data in Fig. 6.65.

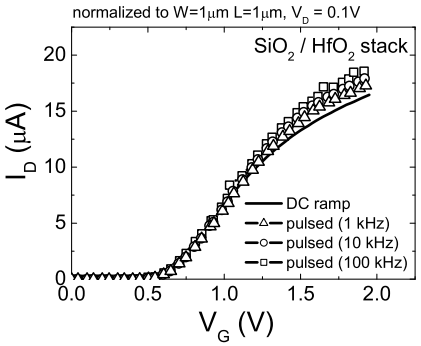

Figure 6.68: Pulsed I_D-V_G characteristic of the SiO_2 / HfO_2 stack using the measurement setup as discussed in Section 5.2.3. The ramp I_D-V_G characteristic (up-trace) is shown for comparison.

From the data shown in Figs. 6.67 and 6.68 the carrier mobility of SiO_2 / HfO_2 dual layer gate dielectrics was extracted and compared to the conventional method (data from Fig. 6.64). When applying the conventional ramp technique, a $\mu_{eff} \sim 100 cm^2/Vs$ is extracted, weakly dependent on the sweep direction. As can be seen, a $\sim 30\%$ larger mobility is obtained when charge trapping is minimized by the pulsed techniques. In view of global comparison it remains far below the values of the oxide control and cannot be explained by Coulomb scattering with fixed charge ($N_{OX} = 2.4 \cdot 10^{12}/cm^2$ as deduced from the initial V_T shift) and trapped charge ($N_{tr} = 8 \cdot 10^{11}/cm^2$) as measured in Fig. 6.66. This is illustrated by the two calculations [66] included in Fig. 6.69.

In summary, inversion charge pumping was introduced as an alternative method to measure the "true" inversion charge in MOSFETs. This method was used to extract the mobility in FETs with conventional and SiO_2 / HfO_2 dual layer gate dielectrics. It was demonstrated that the net-fixed charge and the trapped charge, responsible for the positive V_T shifts are not the primary cause for the strong mobility reduction. To explain the observed mobility reduction by Coulomb scattering [67] oxide charge densities in excess of $10^{13}/cm^2$ would be required. This is only possible if the gate stack contains roughly the equal amount of positive and negative charge. Alternatively, strong remote phonon scattering has been predicted for HfO_2 [68]. It can be speculated that the micro-crystalline structure of the HfO_2 layer may also contribute to the mobility reduction by causing potential fluctuations in the channel.

6.4 Summary

From the data presented in this section it becomes clear that not only the initial V_T control is of concern for integration of high-ε gate dielectrics but that the V_T stability during device operation is also a major issue. Some differences in the charge trapping behavior are certainly attributable to the details of the device fabrication

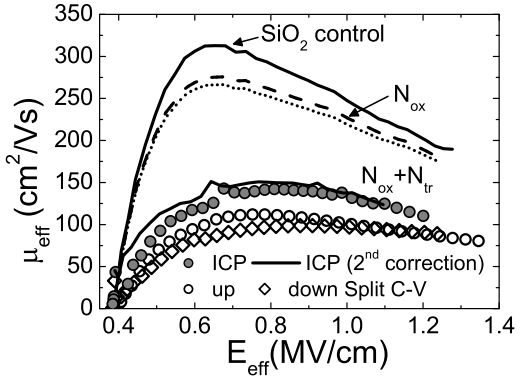

Figure 6.69: Comparison of electron mobility extracted from conventional ramp (Fig. 6.64) and pulsed (Fig. 6.67 and 6.68) measurements. SiO_2 control is shown for comparison. Calculated mobility curves (dashed / dotted lines) illustrate expected impact due to charge scattering (fixed (N_{OX}) and trapped (N_{tr}) charge).

process. However, a few general remarks can be made regardless of the high-ε material used.

Electron trapping in the high-ε layer is the dominant charging mechanism at positive gate bias. In case of Al_2O_3 layers it could be shown that high temperature annealing introduced shallow type of defects which cause strong transient charging effects. The transient effects require time resolved measurement techniques which were introduced here to assess the severity of the charge trapping in high-ε gate dielectrics. Furthermore, none of the process variation carried out in this study did substantially improve the charge trapping behavior.

For negative gate bias, positive charge trapping is observed in Al_2O_3 layers together with a rapid build up of interface states. This indicates that SiO_2 / high-ε gate stacks act like hot carrier injectors for this injection polarity. Therefore, instabilities related to Negative Bias Temperature Instability (NBTI) and Channel Hot Carrier Injection (CHCI) need careful attention.

Based on the electrical results a defect band model was introduced which can explain the qualitative behavior of the charging instability in conventional n-channel MOSFETs with SiO_2 / HfO_2 dual layer dielectrics. Moreover, the issue of dielectric relaxation losses in high-ε materials was addressed using the injector concept. The results obtained on injector stacks do not support the idea of dielectric relaxation effects being the primary cause for the V_T instability in MOSFETs with high-ε gate dielectrics.

Finally, the impact of charge trapping on the device performance was addressed. To do so, an alternative measurement technique was introduced which directly measures the inversion charge in MOSFETs (ICP). When combining ICP with pulsed I_D-V_G measurements the carrier mobility can be extracted at conditions were charge trapping is significantly reduced. The remaining trapping effects can be corrected for by using independent measurements on short channel devices.

Overall, it was found that the carrier mobility in n-channel MOSFETs increases by $\sim$ 30% when charge trapping is eliminated. However, the significantly lower mobility compared to the SiO_2 reference can not solely be explained by charge trapping.

7 Dielectric reliability

In the literature only few studies have discussed the reliability of stacked high-ε dielectrics so far [69, 70, 71, 72, 73]. In all these studies the stress methodology and the interpretation of the obtained results is based on the experience from thermally grown SiO_2 or SiON. The asymmetry in a dual layer stack with respect to carrier injection, defect generation and dielectric breakdown has not been considered so far. In this section, the dielectric reliability of SiO_2 / Al_2O_3 gate stacks with TiN electrodes is discussed in detail and some results are presented for SiO_2 / HfO_2 dual layer stacks.

7.1 Reliability of gate stacks containing Al_2O_3

The reliability of SiO_2 / Al_2O_3 gate stacks with TiN electrodes was investigated using constant current stress (CCS) as well as constant voltage stress (CVS). From voltage-time and current-time traces of CCS and CVS, respectively, the cumulative breakdown distributions were obtained. Furthermore the voltage acceleration was studied and a conventional extrapolation model was used for a 1^{st} order lifetime assessment.

7.1.1 Polarity dependent defect generation

The defect generation in SiO_2 / Al_2O_3 gate stacks was simply monitored using the current time traces during CVS. In Fig. 7.1 typical traces are shown for *as deposited* layers. Samples with different areas are superimposed, indicating negligible series resistance for all conditions studied. In all stacks, breakdown is hard and can easily be detected using a robust breakdown trigger criterion.

The time dependence of the stress current during CVS is consistent with the data presented in Section 6.1. In thin SiO_2 layers, an increase of the stress current towards breakdown is attributed to the generation of new defects. For gate injection, indeed a strong increase of the gate current is measured. The increase is due to positive charge trapping close to the Si substrate as discussed in Section 6.1.4. In addition, rapid interface state generation is present indicating trap generation in all Al_2O_3 layers studied. In conventional SiO_2 stacks the generation of interface

traps is not the cause for the dielectric breakdown. In dual layer stacks with a thin interfacial SiO_2 layer, however, the presence of interface trap generation is a clear sign for degradation of the interfacial layer, which in this case is likely the cause for triggering the dielectric breakdown of the entire stack. For substrate injection, electron trapping remains the dominant charging effect up to dielectric breakdown, as shown by the continuous current decrease in Fig. 7.1. For positive stress polarity, the generation of new defect sites appears to be masked by charge trapping in pre-existing defects.

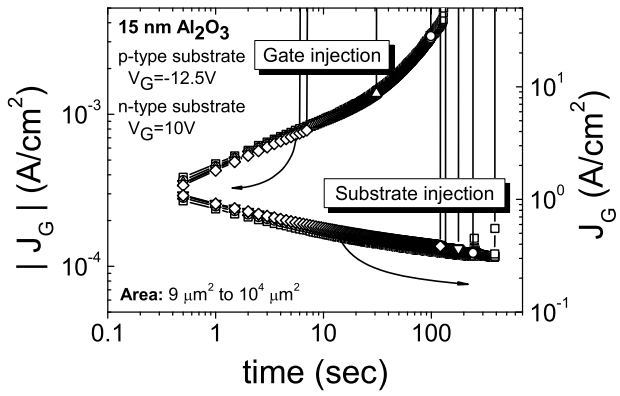

Figure 7.1: Stress current - time traces during CVS for 15 nm thick *as deposited* SiO_2 / Al_2O_3 using substrate and gate injection. Stress condition for substrate injection was $V_G = 10V$ and for gate injection $V_G = -12.5V$. Traces for capacitors with area ranging from 9 to 10^4 μm^2 are superimposed.

7.1.2 Breakdown distribution

From current-time traces like those in Fig. 7.1, time-to-breakdown (T_{BD}) and charge-to-breakdown (Q_{BD}) were obtained and plotted in the usual manner in a Weibull plot. In each case, five different areas ranging from 9 to $10^4 \mu$m^2 were measured for each sample including 29 sites across an 8-inch wafer. The Weibull slope (β) for T_{BD} and Q_{BD} was extracted using a maximum likelihood algorithm [27] including all measured areas for highest confidence of the extracted parameter values [74]. Due to the presence of non-negligible wafer non-uniformity, as discussed in Section 4.2.1, the maximum likelihood algorithm was extended by a variance analysis [75] to account for wafer non-uniformity. In this manner reliable values for the Weibull slope could be obtained for every split condition.

In Fig. 7.2 and 7.3 typical Weibull plots for gate and substrate injection are shown, respectively, for the *as deposited* Al_2O_3 layer. A large difference in the breakdown distribution is evident when comparing gate with substrate injection.

In Figs. 7.4 all Weibull slopes obtained for the *as deposited* SiO_2 / Al_2O_3 dual layer stacks are compared with Weibull slopes previously reported for conventional SiO_2 [28]. Results for CCS (β_{TBD}) and CVS (β_{TBD}, β_{QBD}) are included.

In case of substrate injection and CCS, the Weibull slope increases with Al_2O_3 thickness, indicating that the Al_2O_3 layer determines the breakdown of the entire stack. The dependence of the Weibull slope on thickness is similar to the SiO_2 case

and can be explained by the percolation concept [28]. In this model, traps generated in the Al_2O_3 build up a conduction path between the two interfaces and trigger the breakdown. For thicker oxides, more traps are needed to form the path, and, as a consequence the statistical distribution tightens.

Because of the strong charge trapping, the Weibull slopes for CCS ($\beta_{TBD} \equiv \beta_{QBD}$) and CVS ($\beta_{TBD}$, β_{QBD}) are significantly different. During a CVS, the current continuously decreases (see Fig. 7.1) and therefore the trap generation slows down. This stretches primarily the T_{BD} but also the Q_{BD} distribution resulting in a lower Weibull slope compared to CCS.

Contrary to the substrate injection stress, for gate injection the Weibull slope is low and independent of the Al_2O_3 thickness. This indicates that the interfacial layer mainly limits the dielectric reliability of the gate stack.

These oxide breakdown observations are consistent with charge trapping and degradation experiments shown in Section 6.1. In case of gate injection, a build up of interface traps is found, suggesting a fast degradation of the interfacial layer, resulting in early breakdown of this layer. In case of substrate injection, the interface trap generation is not observed, but instead electron trapping in the bulk of the high-ε layer dominates. Trap creation is expected to occur mainly in the Al_2O_3 leading to breakdown of this layer.

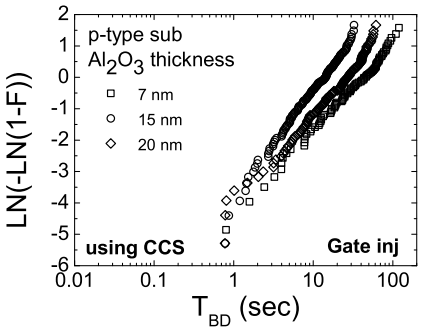

Figure 7.2: Weibull plot of T_{BD} for 7, 15 and 20 nm Al_2O_3 for gate injection using a CCS procedure. Low Weibull slope is obtained independent of Al_2O_3 layer thickness.

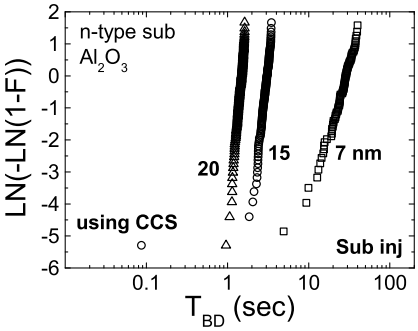

Figure 7.3: Weibull plot of T_{BD} for 7, 15 and 20 nm Al_2O_3 for substrate injection using a CCS procedure. A strong dependence of the Weibull slope on the Al_2O_3 layer thickness is consistent with the percolation concept.

Weibull slopes of high temperature annealed stacks are compared with those of *as deposited* SiO_2 / Al_2O_3 gate stacks in Fig. 7.5. Again, results for substrate and gate injection are compared. These data were collected using CCS on the same number of samples and capacitor areas as for the data in Fig. 7.4. The trends observed in the high temperature annealed samples are as follows: For gate injection no significant improvement after high temperature annealing in N_2 was seen with respect to Weibull slope. In case of substrate injection a significant reduction in the Weibull slope was obtained for high temperature annealed samples, indicating that the anneal modifies either the defect nature, or the defect generation in the SiO_2 / Al_2O_3 gate stack, which is expressed in a lower Weibull slope.

As aforementioned, by upgrading the maximum likelihood algorithm with a variance analysis, more accurate values for the Weibull slope could be extracted even in the presence of wafer non-uniformity. However, it was not possible to unambiguously test for possible bimodality. Therefore, a complementary study of

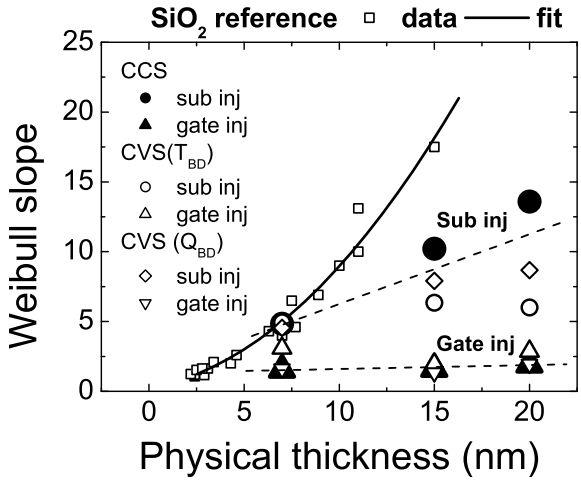

Figure 7.4: Weibull slope for charge-to-breakdown and time-to-breakdown versus Al_2O_3 thickness. Values for substrate and gate injection using CCS and CVS are compared. As reference, previous data obtained for SiO_2 is shown.

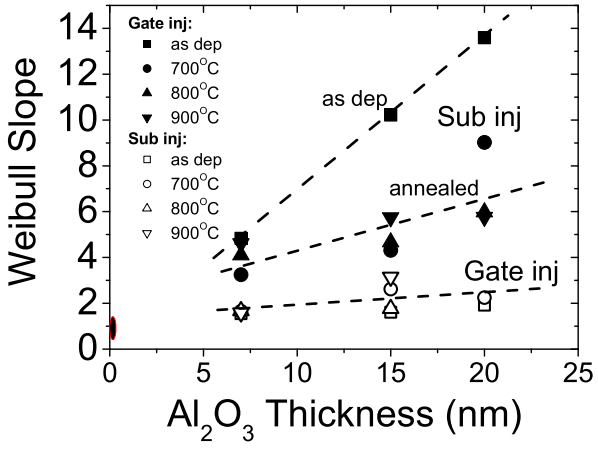

Figure 7.5: Weibull slope versus Al_2O_3 thickness for substrate and gate injection using CCS. For gate injection a shallow slope is obtained irrespectively of the Al_2O_3 thickness and annealing condition. For substrate injection the Weibull slope increases with the Al_2O_3 thickness, but the effect is reduced as compared to *as deposited* layers.

T_{BD} and Q_{BD} was carried out on a local area of the 8-inch wafer. For selected SiO_2 / Al_2O_3 gate stacks CVS was performed on a large number of devices using the same capacitor areas as in Figs. 7.4 and 7.5. By this means the influence of the wafer non-uniformity could be minimized. In Figs. 7.6 and 7.7 the Weibull plots for Q_{BD} of a 15 nm *as deposited* Al_2O_3 layer on a 1 nm SiO_2 interface is shown for

substrate and gate injection, respectively. In case of substrate injection no sign of a bimodal breakdown distribution was found. However, for gate injection clearly two competing breakdown mechanism were identified with statistically significantly different Weibull slopes. Possible causes for the bimodal distribution are the PVD TiN deposition process, which can introduce sputtering damage in the SiO_2 / Al_2O_3 gate stack or small variations of the interfacial oxide layer.

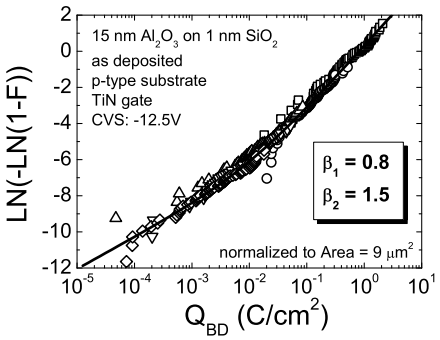

Figure 7.6: Weibull plot for charge-to-breakdown (Q_{BD}) for a 15 nm *as deposited* Al_2O_3 layer on 1 nm SiO_2 interface using CVS at $V_G = -12.5V$ (gate injection). A bimodal Weibull slope is obtained with $\beta_1 = 0.8$ and $\beta_2 = 1.5$.

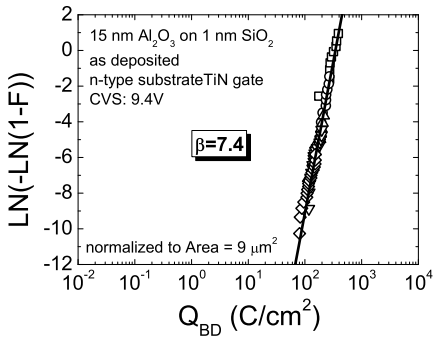

Figure 7.7: Weibull plot for charge-to-breakdown (Q_{BD}) for a 15 nm *as deposited* Al_2O_3 layer on 1 nm SiO_2 interface using CVS at $V_G = 9.4V$ (substrate injection). A monomodal Weibull slope is extracted with $\beta = 7.4$.

A direct comparison of the charge-to-breakdown distribution for substrate and gate injection, respectively, is shown in Fig. 7.8 for 7 and 15 nm Al_2O_3 layers. For 7 nm Al_2O_3 layers a higher charge-to-breakdown is measured compared to a 15 nm thick film for both injection cases. This trend is also observed in SiO_2. Furthermore, Q_{BD} also depends on the injection polarity. For gate injection significantly lower values are obtained compared to substrate injection, suggesting that not only the amount of injected charge during stress, but also the carrier energy or the defect generation mechanism play a critical role. Furthermore, the results obtained by the ramp I-V measurements shown in Section 4.1 are confirmed by the breakdown results shown here.

7.1.3 Lifetime prediction

The lifetime prediction of conventional CMOS circuits is based on accelerated reliability measurements which are extrapolated to operation conditions by an acceleration model. For selected SiO_2 / Al_2O_3 samples the breakdown measurements were carried out at different stress voltages using CVS stress. In Fig. 7.9 the T_{BD} for a normalized device area of $10^4 \mu m^2$ and a failure rate of 63% is shown. The experimental data were fitted using the voltage acceleration model given in Section 2.3.3. Good agreement between the model and the experimental data is obtained for the considered voltage range. To prove the validity of the acceleration model at low voltages (operation condition) long term stress measurement would be required, which are outside the scope of this work. However, from the data shown in Fig. 7.9 it is evident that depending on the stress polarity different voltage acceleration applies. A higher voltage acceleration was obtained for substrate injection ($\gamma = 5.9$ decades / V) compared to injection from the gate electrode ($\gamma = 4.4$). This again

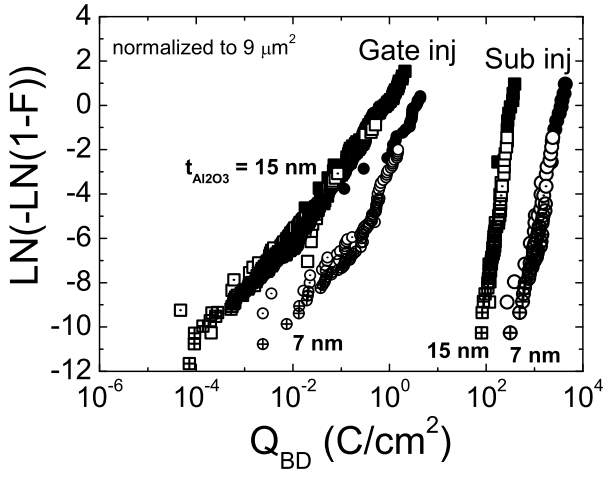

Figure 7.8: Weibull plot for charge-to-breakdown (Q_{BD}) measured on 7 and 15 nm Al_2O_3 layers for substrate and gate injection using CVS stress. For gate injection two failure modes can be distinguished.

shows that the inherent asymmetry of the gate stack has a strong impact on the reliability of high-ε materials.

In summary, a detailed analysis of the dielectric reliability of SiO_2 / Al_2O_3 gate stacks was carried out. The inherent asymmetry in the gate stack is also reflected in the dielectric reliability. For gate injection degradation of the interfacial layer is observed, whereas for substrate injection the breakdown is dominated by the Al_2O_3 layer. The asymmetry in the degradation was further reflected in a polarity dependence of the Weibull slope. For gate injection low Weibull slopes were obtained independent of the Al_2O_3 thickness, whereas for substrate injection β strongly increases with the thickness of the Al_2O_3 layer. The high temperature anneal showed some detrimental effects for substrate injection, but did not significantly change the behavior for injection from the gate electrode.

7.2 Reliability of gate stacks containing HfO_2

The reliability assessment for HfO_2 based gate dielectrics is focused on slightly different aspects compared to the SiO_2 / Al_2O_3 stacks. First, the impact of the gate electrode deposition on the device yield is discussed. Then the polarity dependence of defect generation is investigated using the charge pumping technique introduced in Section 5.2.5. The aim here is to separate interface degradation from defect generation in the bulk HfO_2 layer. Finally, breakdown distributions will be shown for SiO_2 / HfO_2 either with poly Si or TiN electrodes.

7.2.1 Device yield

The compatibility of high-ε materials with poly-Si gate processes is an important aspect for integration into a conventional CMOS process. In the literature, it has been shown that Zr-silicide is formed when integrating ZrO_2 with poly-Si electrodes resulting in high gate leakage currents [76]. The formation of Zr-silicide limited the

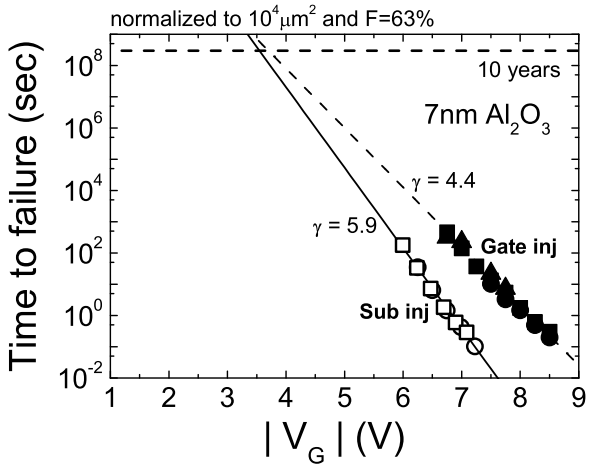

Figure 7.9: Voltage acceleration of 1 nm SiO_2 / 7 nm Al_2O_3 gate stacks. Constant voltage stress was applied on MOS capacitors ranging from 9 to $10^4 \mu m^2$. A polarity dependence of the acceleration factor γ is observed.

application of ZrO_2 as gate dielectric, shifting the focus to Hf based dielectrics. Although Hf-silicide formation has not been reported in the literature, several challenges remain for the integration of Hf based gate dielectrics with poly-Si electrodes [77]. In Fig. 7.10 typical I-V characteristics obtained on large area ($50\,\mu m \times 50\,\mu m$) capacitors are shown. Evidently, a large fraction of the measured samples show normal behaving current-voltage characteristic whereas for a few devices an enhanced gate leakage is observed. When plotting the cumulative fraction of the gate current at a certain gate voltage, as shown in Fig. 7.11, for different device areas it is obvious that small area devices have a lower time-zero failure probability. The yield versus device area, shown in Fig. 7.12, roughly indicates random defect distribution. Furthermore, from the example given in Fig. 7.10 two different failure modes are evident. One type of failure which leads to an enhancement in leakage current whereas the second type of failure corresponds to an ohmic conduction. When the dielectric thickness is scaled towards sub 1 nm EOT the failure mode which causes the enhancement in leakage current may not be detected anymore due to the presence of the large tunneling current. However, it is expected that the breakdown behavior of these gate stacks will be influenced by such weak spots.

The impact of device failure and its dependence on the device area becomes clearly evident when the device yield is plotted versus area, as shown in Figs. 7.12 and 7.13. In the figures various different processing conditions are compared. The growth of HfO_2 on a hydrogen terminated surface results in a high defect density, whereas on a OH termination higher device yield can be obtained. In addition, post deposition annealing strongly influences the leakage behavior. When assuming that a uniform defect density is the cause for the area dependence of the device yield shown in Figs. 7.12 and 7.13 defect densities ranging from 10^6 to $10^3 cm^{-2}$ and less are obtained. Such high defect densities are orders of magnitude too high for Very Large Scale Integration (VLSI). However, it is expected that process optimization can significantly improve the leakage behavior as for example given in Fig. 7.13.

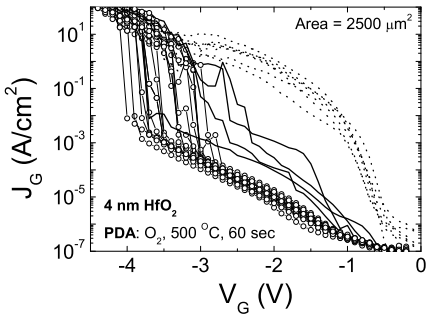

Figure 7.10: Current-voltage characteristic of $50\,\mu\text{m} \times 50\,\mu\text{m}$ capacitors measured on 29 sites across an 8-inch wafer. Open symbols indicated yielding devices, whereas solid lines indicate samples with enhanced leakage current and dotted curves reflect ohmic conduction.

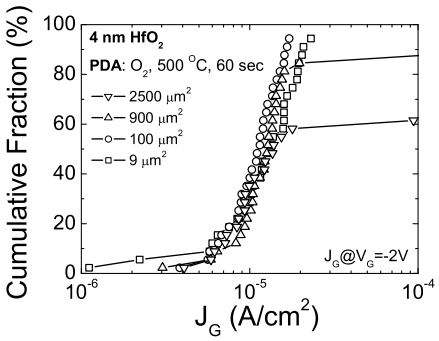

Figure 7.11: Cumulative fraction of the gate current at a gate voltage of $V_G = -2V$ for various capacitors as shown in Fig. 7.10.

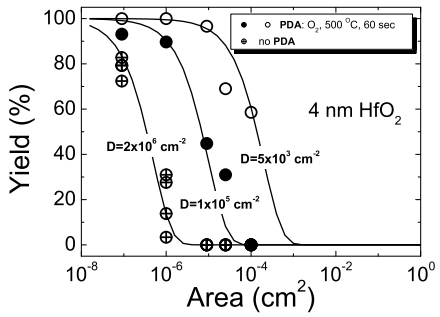

Figure 7.12: Device yield versus capacitor area for different processed HfO_2 layer as indicated in the figure. Lines correspond to a defect density considering Poisson statistic.

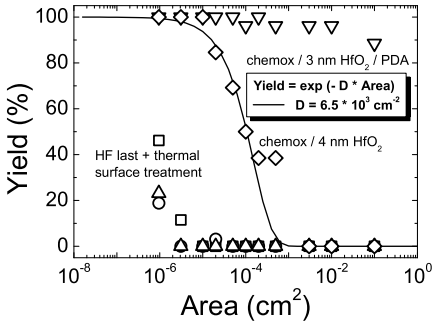

Figure 7.13: Device yield versus capacitor area for different processed HfO_2 layer as indicated in the figure. The line corresponds to a defect density considering Poisson statistic.

7.2.2 Polarity dependent defect generation

The defect generation in SiO_2 / HfO_2 dual layer stacks with conventional poly-Si gate electrodes was studied using n-channel MOSFETs. The use of a MOSFET devices in contrast to planar capacitor structures enables the application of additional characterization techniques to study the defect generation in the gate dielectric. Therefore, the charge pumping technique previously used to assess charge trapping in pre-existing defects is being applied to investigate the defect generation in SiO_2 / HfO_2 dual layer stacks. The conventional base level sweep is used to monitor interface state generation, whereas the amplitude sweep is more suited to provide information on the generation of bulk defect sites in the HfO_2 layer.

In Fig. 7.14 typical current time traces during CVS stress are shown for a 5 nm

HfO_2 layer deposited on a chemical grown SiO_2 interface. Significantly higher stress currents are measured for positive gate bias as a result of the asymmetry of the dual layer stack. Furthermore, at small negative gate biases ($V_G = -2V \ldots -2.5V$) the stress current decays which indicates a slow reversible charging process. For a stress bias of $V_G > -2.5V$ a steady state stress current is measured. When the stress bias is further increased strong fluctuations in the stress current can be observed prior to dielectric breakdown for both injection polarities similar to the behavior of SiO_2 / ZrO_2 stacks with TiN electrodes [78].

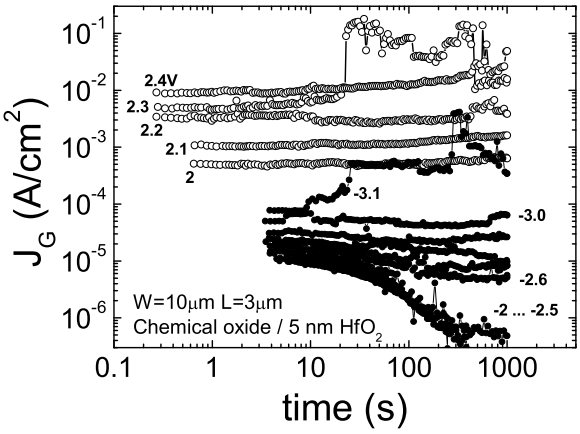

Figure 7.14: Stress current - time trace of a 5 nm HfO_2 layer deposited on a chemical grown SiO_2 interface using stress bias as indicated in the figure. The stress was performed on a single device with increasing gate bias.

After applying a CVS stress for 1000 seconds as shown in Fig. 7.14 charge pumping measurements were performed to measure the impact on interface and bulk defects using the conventional base level and amplitude sweep, respectively. In Figs. 7.15 and 7.16 interface state generation for gate and substrate injection are summarized for the stress conditions used in Fig. 7.14. As can be seen, after carrier injection from the gate electrode a more pronounced increase in interface states is measured compared to substrate injection. When comparing these results with SiO_2 / Al_2O_3 stacks with TiN electrodes the asymmetry in interface state generation is far less pronounced, however, the presence of an asymmetry indicates that also for HfO_2 gate stacks the injection polarity needs careful attention.

Furthermore, amplitude sweep charge pumping measurements were performed to investigate the formation of bulk defects in the HfO_2 layer. The results are summarized in Figs. 7.17 and 7.18 for the stress conditions shown in Fig. 7.14. The data clearly demonstrate that the generation of bulk defects in the HfO_2 layer strongly depends on the injection polarity. For gate injection basically no bulk defect generation is evident, whereas for substrate injection the charge pumping current strongly increases with increasing stress bias. Note that the amplitude sweep charge pumping not only measures the contribution from bulk defect sites but also the contribution from interface states. Therefore at low V_{Peak} values ($V_{Peak} = 0.2V \ldots 0.8V$) the dispersion in the charge pumping characteristic for gate injection (see Fig. 7.17) is caused by the interface state generation as shown in Fig. 7.15.

In summary, the degradation of SiO_2 / HfO_2 dual layer stacks with conventional poly-Si electrodes follows the same trend as seen for SiO_2 / Al_2O_3 stacks. For gate

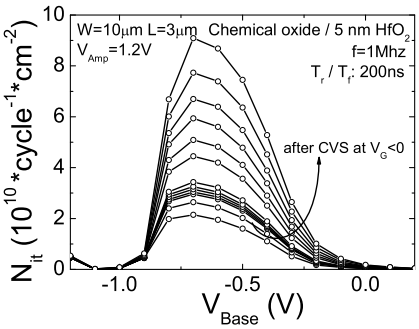

Figure 7.15: Interface state generation after CVS ($V_G < 0$V in Fig. 7.14) measured with charge pumping using conventional base level sweep. A significant increase in charge pumping current is found after carrier injection from the gate electrode.

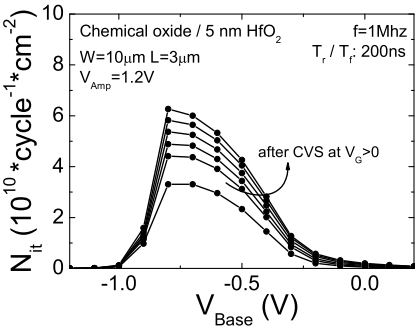

Figure 7.16: Interface state generation after CVS ($V_G > 0$V in Fig. 7.14) measured with charge pumping using conventional base level sweep. A less significant increase in charge pumping current after carrier injection from the Si substrate is seen compared to gate injection as shown in Fig. 7.15

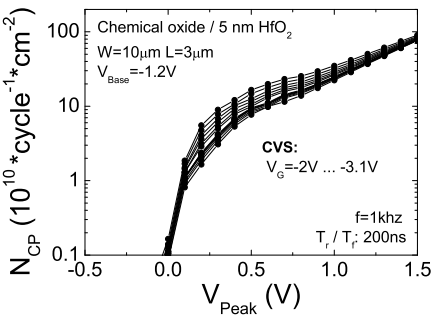

Figure 7.17: Bulk defect generation after CVS ($V_G < 0$V in Fig. 7.14) measured with charge pumping using the amplitude sweep using measurement conditions as indicated in the figure. Only a small increase in bulk defect density is measured for gate injection.

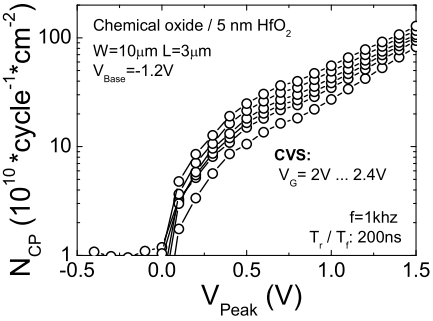

Figure 7.18: Bulk defect generation after CVS ($V_G > 0$V in Fig. 7.14) measured with charge pumping using the amplitude sweep using measurement conditions as indicated in the figure. A strong increase in bulk defect density is evident for substrate injection.

injection, degradation of the interfacial region is observed whereas for substrate injection bulk defect sites in the HfO_2 layer are being formed [79].

7.2.3 Breakdown distribution

Based on the similarities in the degradation of SiO_2 / Al_2O_3 and SiO_2 / HfO_2 gate stacks it could be expected that also the breakdown behavior of these stacks is following the same trends. Gate injection should yield low β values together with a low Q_{BD} due to the rapid degradation of the interfacial layer while for substrate injection based on the percolation concept a thickness dependence of β would be

expected. Therefore, substrate injection would be the appropriate polarity case to demonstrate intrinsic breakdown behavior of the HfO_2 layer. Due to the fact that initially the integration of HfO_2 layers with poly Si electrodes resulted in a severe yield loss on large area device structures as discussed in Section 7.2.1 the suitable hardware was not available to investigate the thickness dependence of the Weibull slope β. On the other hand, for SiO_2 / ZrO_2 stacks such thickness dependence was not seen which could lead to the conclusion that for both injection polarities breakdown of the interfacial SiO_2 layer determines the reliability of the entire gate stack [78]. This conclusion is not supported by the polarity dependent degradation experiments discussed in Section 7.2.2.

As previously mentioned, the use of poly-Si as gate electrode is reflected in the breakdown distribution as shown in Fig. 7.19. When the normalized T_{BD} or Q_{BD} is plotted using vertical area scaling, which means large area device correspond to a lower cumulative failure percentile, the extrinsic breakdown behavior of large area devices becomes clearly evident. When similar experiments are carried out on stacks with TiN electrodes no extrinsic breakdown mode is evident for similar device structures, as shown in Fig. 7.20.

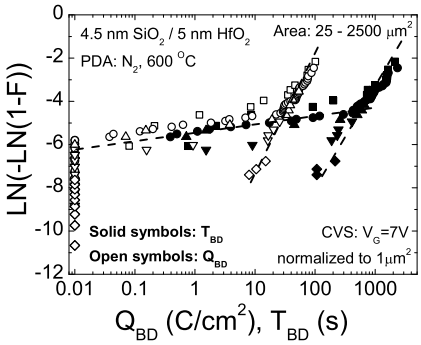

Figure 7.19: Weibull plot for Q_{BD} and T_{BD} obtained on SiO_2 / HfO_2 dual layer stack with poly-Si gate electrode. 'Intrinsic' breakdown behavior is only observed for small area devices.

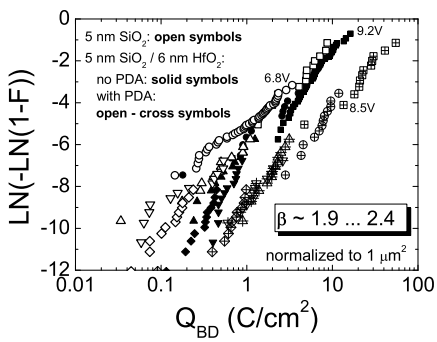

Figure 7.20: Weibull plot for Q_{BD} obtained on SiO_2 reference and SiO_2 / HfO_2 dual layer stacks with TiN gate electrodes. The extracted Weibull slope is ranging from 1.9 to 2.4.

The breakdown distributions shown in Figs. 7.19 and 7.20 were extracted from dual layer stacks with a 'thick' (4.5nm or 5nm) interfacial SiO_2 layer. However, the determined Weibull slope β was only $\sim$2. To demonstrate that the low β value for T_{BD} or Q_{BD} is intrinsic to the HfO_2 layer the defect generation rate was measured with the amplitude sweep charge pumping. Indeed a higher β value is obtained when considering the defect generation in the HfO_2 layer compared to simply using the Q_{BD} distribution [79]. A graphical illustration is given in Fig. 7.21. This indicates that for substrate injection trap generation in the HfO_2 layer is responsible for dielectric breakdown and the obtained β values for trap generation are consistent with the percolation model.

7.3 Summary

The dielectric reliability of dual layer high-ε gate stacks was investigated for substrate and gate injection. Based on the results shown here the breakdown behavior

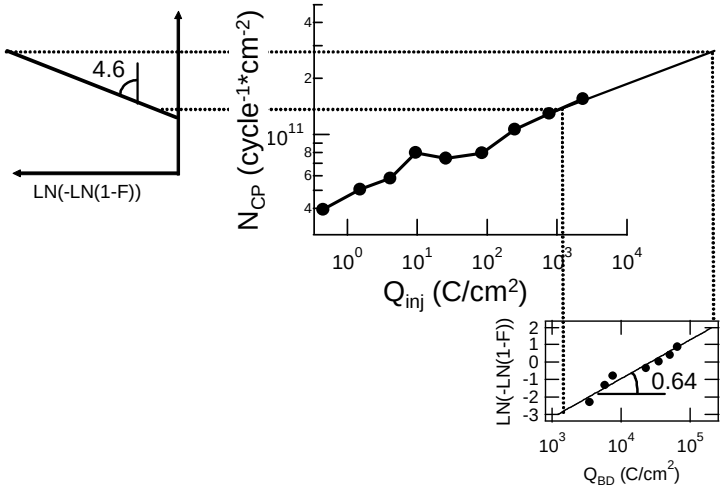

Figure 7.21: Graphical illustration of the HfO_2 trap density distribution constructed from the Q_{BD} distribution an the trap generation measured by C-P. Despite the low Q_{BD} Weibull slope, a step trap density distribution (N_{CP}) is found, indicating 'intrinsic' breakdown behavior [79].

of dual layer stacks strongly depends on the injection polarity. For gate injection a rapid degradation of the interfacial SiO_2 layer is observed which determines the reliability of the entire gate stack. Thus rather low β values for T_{BD} and Q_{BD} distributions are being extracted independent of the high-ε material used.

The situation for substrate injection, however, is more complex. In general, defect generation in the bulk of the high-ε layer is observed which can result in a strong thickness dependence in the β values for T_{BD} and Q_{BD} as expected from the percolation model. Indeed the experimental results obtained on Al_2O_3 layers confirm the expected trend. For other high-ε materials like ZrO_2 or HfO_2, however, this trend is not confirmed. A more detailed analysis on the correlation between defect generation and Q_{BD} distribution indicates that also for these materials the β value corresponding to the defect generation is significantly higher which indicates intrinsic breakdown behavior.

8 Conclusion

In this work, the electrical properties of two high-ε materials (Al_2O_3, HfO_2) deposited by ALD were investigated in detail. It was demonstrated that both Al_2O_3 and HfO_2 suffer from non-ideal behavior which prevents their application at present.

The primary aim of introducing high-ε materials into CMOS technologies is to reduce the gate leakage current. The magnitude of the leakage current reduction depends on the material properties and processing details such as interfacial layer thickness, dielectric constant, bandgap, band-alignment, post deposition treatment, gate electrode, etc. Indeed, for Al_2O_3 and HfO_2 a significant reduction in gate leakage is observed in comparison with the SiO_2 reference. However, a detailed understanding of the conduction mechanism (tunneling, trap assisted tunneling, Frenkel-Poole conduction, Schottky emission, ...) in high-ε materials is still missing. In this study, the focus was on the polarity dependence of the leakage current caused by the inherent asymmetry of the dual layer stack and the work-function difference between the gate electrode and the Si substrate. In 'thick' stacks, a significantly higher gate leakage current is measured for substrate injection compared to gate injection. With decreasing dielectric thickness ('thin' stacks) this effect gets less pronounced.

Intensive investigation of charge trapping in high-ε materials was carried out for SiO_2 / Al_2O_3 and SiO_2 / HfO_2 gate stacks. First of all, it could be demonstrated that the observed instabilities are not caused by dielectric polarization as proposed in the literature, but rather by trapping of mainly negative (positive) charge for substrate (gate) injection. For substrate injection, the initial probability for electron trapping was close to unity and the probability decays as a function of time following a power law relation with a slope of t^{-1}. The V_{FB} or V_T instability can be predicted by simply integrating the trapping probability. Furthermore, based on the electrical results a defect band model was introduced which qualitatively explains the experimental results. The defect band in the HfO_2 layer is located above the conduction band in the Si. Such a defect band moves rapidly in energy when the gate bias is changed due to the large difference in the dielectric constant between HfO_2 and SiO_2. This enables efficient charging (discharging) under positive (negative) bias. The origin of the defect band may be related to oxygen vacancies, water related defects such as OH (OH^-) or Cl impurities. Reducing the number of defects

will be of crucial importance for the successful application of high-ε materials in future CMOS technologies.

In order to correctly quantify the magnitude of the instability a methodology for charge trapping was established introducing pulsed measurement techniques (pulsed I_D-V_G, Charge Pumping) and "sense at stress" rather than "stress and sense". The novel measurement techniques yield equivalent results when the measurement conditions and device geometry are chosen carefully. To monitor improvements with respect to charge trapping it is necessary to apply the fast time resolved measurement techniques introduced here.

In addition, the effect of charge trapping on the MOSFET performance was investigated. To correctly account for the observed charging effects an alternative technique was developed which directly measures the inversion charge in MOSFETs (Inversion Charge Pumping (ICP)). When this new technique is applied to extract the carrier mobility in MOSFETs significantly enhanced mobility is obtained due to the reduction of charge trapping in the μs range enabling a proper correction of the remaining trapping effects. However, the still significant reduction of the carrier mobility compared to the SiO_2 reference cannot solely be explained by charge trapping. Other scattering effects (Remote Charge Scattering, Remote Phonon Scattering, ...) are likely responsible for the observed degradation.

Finally, the dielectric reliability of SiO_2 / Al_2O_3 and SiO_2 / HfO_2 gate stacks was studied. A strong correlation between charge trapping and dielectric reliability is evident. For gate injection, a rapid degradation of the interfacial SiO_2 is observed leading to breakdown of the entire gate stack. Thus, low β values are obtained independent of the thickness of the high-ε material. For substrate injection, defect generation in the bulk of the high-ε layer is present which results in a strong thickness dependence of the Weibull slope β for Al_2O_3 layers as predicted by the percolation theory.

Based on the results presented here it is evident that strong improvements in charge trapping and device performance are required for successful application of high-ε gate dielectrics in future CMOS technologies. The improvements may come from modifying the deposition technique, the dielectric material (Nitrogen and / or Silicon incorporation), applying the appropriate post deposition treatment or changing the integration scheme (conventional versus replacement gate process). The value of this contribution is based on the introduction of novel measurement techniques which allow to correctly assess and quantify the impact of charging effects on the stability and the performance of MOS devices with high-ε gate dielectrics. For a successful application the required improvements remain to be demonstrated.

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List of publications

Conference papers

1. R. J. Carter, E. Cartier, M. Caymax, S. DeGendt, R. Degraeve, G. Groeseneken, M. Heyns, T. Kauerauf, **A. Kerber**, S. Kubicek, G. Lujan, L. Patisano, W. Tsai, E. Young, "Electrical Characterisation of High-K Materials Prepared by Atomic Layer CVD" (invited), International Workshop on Gate Insulators, Tokyo, 2001.

2. **A. Kerber**, E. Cartier, R. Degraeve, L. Pantisano, Ph. Roussel, G. Groeseneken, "Strong Correlation between Dielectric Reliability and Charge Trapping in SiO_2 / Al_2O_3 Gate Stacks with TiN Electrodes", VLSI Technology Symposium, Honolulu, 2002.

3. P. J. Chen, E. Cartier, R. Carter, T. Kauerauf, C. Zhao, J. Petry, V. Cosnier, Z. Xu, **A. Kerber**, W. Tsai, E. Young, S. Kubicek, M. Caymax, W. Vandervorst, S. DeGendt, M. Heyns, M. Copel, P. Bajolet, J. Maes, "Thermal stability and device scalability of Zr-aluminate-based high-k gate dielectric", VLSI Technology Symposium, Honolulu, 2002.

4. **A. Kerber**, E. Cartier, R. Degraeve, Ph. Roussel, L. Pantisano, T. Kauerauf, G. Groeseneken, S. DeGendt and M. Heyns, "Charge Trapping and Dielectric Reliability in Alternative Gate Dielectrics, a Key Challenge for Integration" (invited), Workshop on Dielectrics in Microelectronics (WODIM), Grenoble, France, 2002.

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Curriculum vitae

Andreas Kerber was born in Schnann, Austria, on October 11. 1973. He graduated from the Technical Highschool (HTL) in Innsbruck, Austria, in 1992 with a major in communication engineering. From 1993 to 1999 he did his undergraduate study at the University in Innsbruck, Austria. For his diploma thesis he worked as an intern at Bell Laboratories / Lucent Technologies on the electrical characterization of ultra-thin gate oxides (1999 to 2000). In 2001, he received the diploma degree in physics from the University of Innsbruck, Austria. The same year he joined Infineon Technologies in Munich, Germany, as a member of technical staff. Currently, he is acting as the Infineon assignee to International Sematech at IMEC in Leuven, Belgium, where he is involved in the electrical characterization of alternative gate dielectrics for sub-100 nm CMOS technologies. In addition he is conducting his research towards a PhD in electrical engineering at the TU-Darmstadt, Germany, where he is focusing on the charge trapping and the dielectric reliability of high-ε gate dielectrics.