Electrochemical Gating of Oxide Nanowire Transistors at Low Operating Voltage

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Hiermit versichere ich an Eides statt, dass ich die vorliegende Arbeit selbständig und unter Verwendung der aufgeführten Hilfsmittel durchgeführt habe. Von mir wurde noch kein Promotionsversuch unternommen.

Karlsruhe, den 19.02.2013

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Abstract:

Single-crystal, one-dimensional (1-D), metal-oxide nanostructures are well known for their excellent electronic transport properties. Moreover, metal oxide-nanowire field-effect transistors (FETs) offer both high optical transparency and large mechanical conformability which are essential for flexible and transparent display applications. While the "on-currents" achieved with nanowire channel transistors are already sufficient to drive active-matrix organic light-emitting diode (AMOLED) displays; it is shown here in addition that application of electrochemical-gating (EG) to nanowire electronics reduces the operation voltage to ≤2 V. This opens up new possibilities for the realization of flexible, portable, transparent displays that can be powered by thin film batteries. Electrolyte gated field-effect transistors are fabricated with single crystalline metal oxide nanowires such as ZnO and SnO_2 as the channel and a composite solid polymer electrolyte (CSPE) is used as dielectric gating material. Excellent transistor performance and a very low-voltage operation (≤ 2 V) have been demonstrated. Practical use of such electrolyte-gated field-effect transistor (EG FET) devices is validated by their long-term stability in air. Moreover, due to the good conductivity ($\approx 10^{-2}$ S/cm) of the CSPE, sufficiently high switching speed of such EG FETs is attainable; a cut-off frequency in excess of 100 kHz is measured for in-plane FETs. Furthermore, thermal stability of the FETs is systematically examined up to 180 °C. Unchanged transistor characteristics are obtained up to 70 °C, short exposure at 110 °C is found acceptable, making such devices compatible with organic photovoltaics or various biomedical applications. Additionally, the solid polymer electrolyte developed in this study has great potential for future device fabrication using all-solution processed and high throughput techniques.

Abstrakt:

Einkristalline, eindimensionale (1-D), Metall-Oxid Nanostrukturen sind bekannt für ihre hervorragenden elektronischen Transporteigenschaften. Des Weiteren bieten Metall-Oxid Nanodraht Feldeffekt-Transistoren zusätzlich eine hohe optische Transparenz und eine gute mechanische Verformbarkeit. Diese Eigenschaften sind wesentlich für Anwendungen in flexiblen und transparenten Displays. Während der Strom im „on-state“ in Nanodraht-Transistoren bereits für die Anwendung in AMOLED Displays ausreicht, wird in dieser Arbeit gezeigt, dass durch den Einsatz des „electrolyte gating“ die Betriebsspannung auf $\leq$ 2V reduziert werden kann. Dies eröffnet neue Möglichkeiten für flexible, tragbare und transparente Displays, die von Dünnschicht-Batterien betrieben werden können. „Electrolyte gated“ Feldeffekt-Transistoren (EG FET) werden aus einkristallinen Nanodrähten aus z.B. ZnO oder SnO_2 als Kanal und einem Festkörper Polymer Kompositelektrolyt (CSPE) als Gate-Isolator hergestellt. Es wurden sowohl exzellente Transistoreigenschaften als auch eine sehr kleine Arbeitsspannung von $\leq$ 2V gezeigt. In der Praxis überzeugen solche EG FETs besonders wegen ihrer Langlebigkeit in Umgebungsbedingungen. Weiterhin ist wegen der guten Leitfähigkeit der CSPE ($\approx 10^{-2}$ S/cm) eine ausreichend hohe Schaltgeschwindigkeit solcher EG FETs erreichbar; es wurde eine maximale Frequenz von mehr als 100 kHz für „in plane“ FETs gemessen. Ferner wurden die FETs bei Temperaturen bis 180 °C systematisch untersucht; wobei bis zu einer Temperatur von 70 °C keine Änderungen in den Transistoreigenschaften festgestellt wurden. Auch eine kurzzeitige Temperaturerhöhung auf 110 °C beeinflusst die EG FETs kaum. Somit sind solchen Bauteile kompatibel mit organischer Photovoltaik und biomedizinischen Anwendungen. Zusätzlich bietet der in dieser Arbeit entwickelte CSPE in der Zukunft viele Möglichkeiten für vollständig gedruckte Bauteile mit hohem Produktionsdurchsatz.

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List of abbreviations and symbols

RFID	Radio frequency identification
AMOLED	Active matrix organic light emitting diode
LCD	Liquid crystal display
TFT	Thin film transistor
EDL	Electric double layer
FET	Field effect transistor
MOS	Metal oxide semiconductor
EG	Electrochemical gating
OS	Organic semiconductor
OFET	Organic field effect transistor
OPV	Organic photovoltaic
CNT	Carbon nanotube
TCO	Transparent conducting oxide
ITO	Indium tin oxide
CSPE	Composite solid polymer electrolyte
PC	Polycarbonate
DMSO	Dimethyl sulfoxide
PVA	Polyvinyl alcohol
PMMA	Poly(methyl methacrylate)
MIBK	Methyl isobutyl ketone
PEN	Polyethylene naphthalate
EBL	Electron beam lithography
CVD	Chemical vapor deposition
PVD	Physical vapor deposition
ALD	Atomic layer deposition
MBE	Molecular beam epitaxy
VLS	Vapor-liquid-solid

XRD	X-ray diffraction
GIXRD	Grazing incidence X-ray diffraction
SEM	Scanning electron microscopy
EDX	Energy dispersive X-ray spectroscopy
TEM	Transmission electron microscopy
HRTEM	High resolution transmission Electron microscopy
FFT	Fast Fourier transform
TGA	Thermal gravimetric spectroscopy
RIR	Reactive ion etching
GPA	Geometric phase analysis
UV	Ultraviolet
UV-Vis	Ultraviolet-visible
RT	Room temperature
UHV	Ultra high vacuum

Å	Angstrom
nm	Nanometer
at%	Atom percent
C	Specific capacitance
C_{dl}	Double layer capacitance
C_{in}	Insulator capacitance per unit area
c	Velocity of light
υ_{d}	Drift velocity
d	Diameter
d_{AVE}	Average diameter
d_{hkl}	Interplanar spacing for planes of Miller indices
E_{F}	Fermi energy
E_{g}	Band gap energy
q	Electric charge
e	Electron
h	Planck's constant
h, k, l	Miller indices for a Crystallographic plane
I_D	Electric source current
I_G	Electric gate current
L	Channel length
W	Channel width
k	Boltzmann constant
ε	Strain
ε_{r}	Dielectric constant
ε_0	Permittivity of free space
θ	Bragg diffraction angle
μ	Electron mobility
μ_{FET}	Field effect mobility
ρ	Electrical resistivity

R	Resistance
V_G	Gate voltage
V_D	Drain voltage
V_S	Source voltage
V_T	Threshold voltage
S	Subthreshold swing
g_m	Transconductance

Chapter 1

Motivation

Electronic and optoelectronic devices influence almost every aspect of human life, from simple domestic appliances and multimedia systems to communications, computing, and medical instrumentation. Given the demand for more user-friendly and versatile systems, among others, there are growing interests in the development of transparent and flexible devices. Novel next-generation electronics appliances and applications possibilities are being envisaged which require functionalities that are not possible to meet with traditional silicon technologies: for example there are already large demands and increasing interest towards large-area transparent sensors, active-matrix organic light emitting diode (AMOLED) display drivers, and invisible radio-frequency identification tags (RFID), electronic artificial skins, smart textiles and many others. [1,2,3–7] In this context, thin film transistors (TFTs) based on transparent metal oxides, have drawn enormous attention in recent years due to their excellent performance.[8–12] However, the devices based on inorganic thin films still suffer from limitations such as limited mechanical stress tolerance and insufficient bendability. In contrast, TFTs based on organic materials are much less prone to mechanical failure and show sufficient conformability to flexible substrates. Consequently, these concepts are being widely considered for flexible electronics, although most of the high-performance organic semiconductors show degraded performance when exposed to environmental moisture; especially, the electron conducting ones are found extremely sensitive to oxygen and moisture.[13] Furthermore, organic devices have lower mobility compared to their inorganic counterparts. In this regard, the high performance metal oxide nanowire-based field effect transistors (FETs) are one of the options fulfilling all

the requirements that are crucial for flexible electronics and hence have also become the subject of growing attention in recent years. Although the development of successful and efficient methods for the alignment of one-dimensional nanostructures is an issue not yet completely solved, there are several proposed experimental procedures for controlled positioning of nanowires/nanorods which could potentially lead to mature applications.

In addition to high transparency and flexibility, the envisioned future applications would also encompass wearable electronics i.e. battery compatible, portable devices with drive voltages limited to only a few volts.[14–17] Conventionally, a low operating voltage is attained by means of a gate dielectric which is composed of an ultrathin polymer such as a self-assembled monolayer,[17] or high-k dielectrics.[9] However, none of these materials are solution-processable and suitable for high-throughput technologies. As an emerging alternative, solid electrolytes have found their own place as a gate insulator in low operating voltage OFETs [18,19]. Provided that no electrochemical (redox) reactions take place at the electrical double layer (EDL) formed at the electrolyte-semiconductor interface, the ionic nature of an electrolyte allows electrons or holes to be accumulated at much lower operating voltages compared to traditional dielectric materials. A very high capacitance of the solid/electrolyte gate results from the fact that the ionic and electronic charges within this capacitive double layer are separated by a thin solvent layer which is of the order of only a few angstroms. However, in most electrochemically gated OFETs the switching speed is rather low and also the performance of the device degrades in ambient and humid environment.

In this work, we introduce a new approach to nanowire based FETs by incorporating composite solid polymer electrolytes (CSPE) as the gate-insulator to control the current through metal oxide single-nanowire transistors. This strategy simultaneously enables the low voltage operation, compatible with battery operation and complete solution processability. Furthermore, this approach ensures mechanical flexibility and high optical transparency. On top of that, unlike ionic liquids[20] which have been quite extensively studied as gate-insulators recently, the CSPE is found to be extremely stable at ambient conditions and the CSPE-gated nanowire FETs have shown long-term stability in air. It has also been shown recently, that a cut-off frequency of >10 MHz is attainable for high conducting solid polymer electrolytes.[21] In contrast to most of the organic semiconductor-based bendable electronic devices which suffer from limited temperature endurance, it is

shown that the metal oxide nanowire based electrochemically gated FETs (EG FETs) can stably operate up to a moderately high temperatures which may allow the direct integration into flexible organic photovoltaics (OPV).

In this thesis, the fabrication and characterization of high performance metal oxide nanowire transistors gated via CSPE is presented. In the future such structures could be used in fully transparent, flexible and battery compatible electronics. First, the current development of transparent and flexible nanowire field effect transistors, with a focus on the selection of dielectric materials and the corresponding potential application is described. The fabrication of nanoscale metal oxides in the form of nanowires for novel and highly versatile device fabrication is the focal point of this thesis. Using controlled growth based on vapor liquid solid (VLS) mechanism, single crystalline metal oxide nanowires, ZnO and SnO_2, with controlled and uniform diameters were synthesized. Both ZnO and SnO_2 nanowires have shown excellent electrical properties as the building blocks of EG FETs. Next, studies of the device performance with the focus on operation speed, environmental and thermal stability are presented. The fabricated EG FETs exhibit excellent performance with a comparatively high cut-off frequency ≥ 100 kHz, long-term stability ≥ 4 weeks and moderate temperature durability up to 100-110 °C.

Chapter 1 gives the motivation and overview of the research. Chapter 2 gives a brief research background including FETs and EG FETs, synthesis techniques of nanowires and literature review on nanowire based FETs. Chapter 3 reports on the synthesis of metal oxide nanowires via the VLS mechanism. In the following chapter the techniques used to fabricate nanowire based EG FETs are summarized. Chapter 5 and 6 contain the transistor characterization of the SnO_2 and ZnO nanowire based EG FETs along with the studies on the environmental stability.

Chapter 2

Literature review

2.1 Voltage controlled electronic transport through semiconductors

The metal oxide semiconductor field effect transistor (MOSFET) is one of the main building blocks of modern electronic and communication technologies which are used for amplifying or switching electronic signals. The term field-effect is used because for FETs, an electric field controls the flow of carriers (electrons or holes) through a single type of semiconductor material. Consequently, the FETs are sometimes referred to as unipolar transistor.

Introducing an insulating layer between the gate and the semiconducting film allows for accumulation or depletion of carriers through a control (gate) voltage and also reduces the *leakage/gate* current (increases the device input resistance). The insulator is typically made of an oxide (SiO_2, Al_2O_3 and HfO_2). This type of device is called a *metal-oxide-semiconductor FET* (MOSFET) or *insulated-gate FET* (IGFET). Figure 2.1 illustrates the schematic structure of a MOSFET. As it is shown a gate-oxide layer is deposited on a semiconductor film which is contacted with metallic source and drain electrodes. Ideally, the *source* and *drain* should form an ohmic contact with the semiconductor. The important device parameters are the *source-drain channel length* (L), the *channel width* (W), and the *insulator capacitance per unit area* (C_{in}).

The *bias voltage* (V_G) on the gate electrode either attracts or repels the majority carriers of the semiconducting film towards/from the channel (at the interface of insulator/semiconducting film). As V_G changes its polarity, the channel may get narrowed (depleted) or widened (enhanced), respectively. For instance, in case of an n-channel

MOSFET, positive *gate voltage* ($V_G > 0$) attracts electrons and repels holes from the channel towards the substrate, and therefore widens the channel and decreases the channel resistance. On the other hand, $V_G < 0$ makes holes to be attracted toward the channel. In other words, it narrows the channel and increases the channel resistance. The abbreviation for an n-channel MOSFET is NMOS, and for a P-channel MOSFET, PMOS.

The voltage applied between the *source* and *drain* contacts is referred to as the *drain* voltage, V_D. Generally, for a given V_D, the amount of current that can flow through the semiconductor film from the *source* to the *drain* contact is a function of the *gate voltage*, V_G. The semiconductor film and the gate electrode are capacitively coupled such that an application of a *bias voltage* at the gate induces a charge density modulation at the oxide/semiconductor interface. Most of these charges are mobile and move according to the applied *drain voltage*, V_D. Therefore, when a suitable *gate voltage* is applied, mobile charges are accumulated, and the transistor is in the "on-state".

As MOSFETs can both deplete the channel or enhance the channel, MOSFETs configuration are addressed based on the channel statues at $V_G = 0$. A *depletion mode device* (also called a 'normally-on' MOSFET) has already a conducting channel that gets smaller (narrowed) at application of a reverse bias voltage. Consequently, such a device conducts current at zero bias state. An *enhancement mode device* (also called a 'normally-off' MOSFET) does not conduct current when $V_G = 0$ and an increasing forward bias introduces/creates a channel that conducts current.

Two standard approaches are usually used to electrically characterize MOSFETs; either V_G is constant and V_D is swept to measure I_D versus V_D (IV) characteristics or V_D is constant and V_G is swept to analyze transfer characteristics (Figure 2.2)

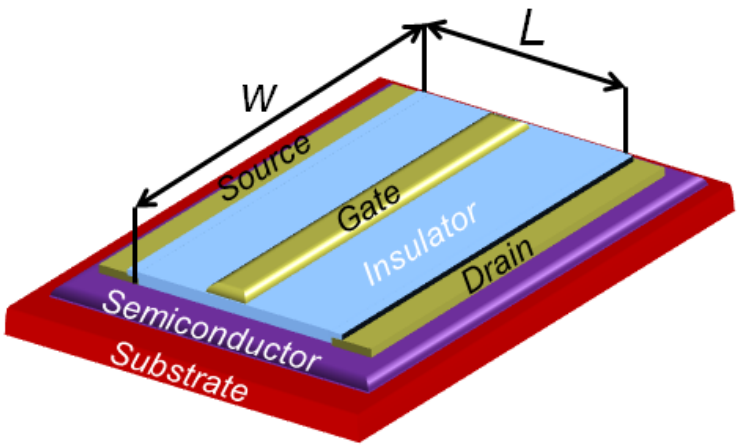

Figure 2.1 Schematic image of a MOSFET

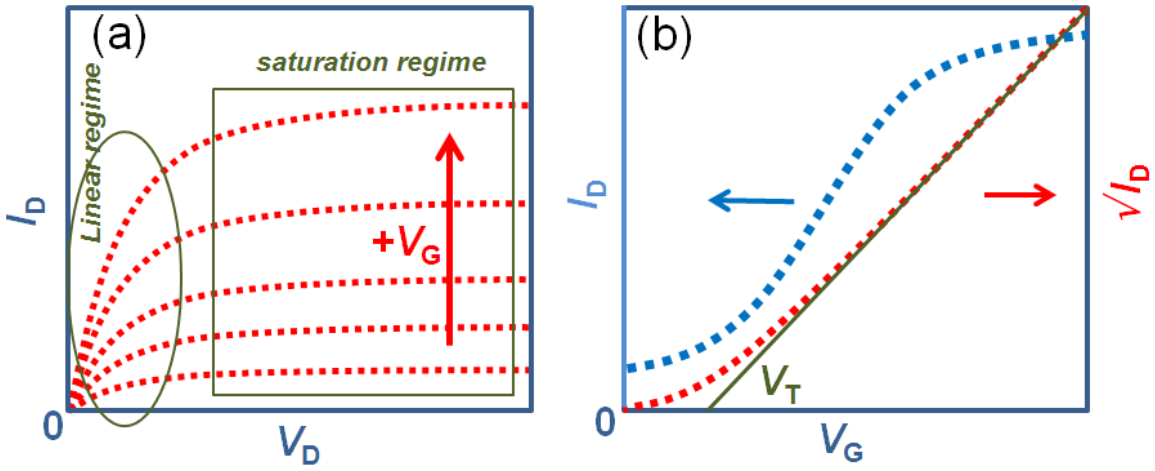

Figure 2.2 A typical FET characterization a) I_D versus V_D characteristic b) Transfer characteristic

Figure 2.2a shows IV characteristics of an *enhancement-mode* FET with n-type semiconducting channel at different (positive) *gate bias*. In contrast, Figure 2.2b shows transfer characteristic of the FET. The intercept of the extrapolated linear red curve with the *gate voltage* axis in the transfer characteristics defines the *threshold voltage* (V_T). Physically, the *threshold voltage* is defined as the *gate voltage* that is required for creating a conducting channel and allows the charge carriers to flow from the electrode (*source*/*drain*) into the channel.

The cross section of a MOSFET with n-type channel (NMOS) device is shown in Figure 2.3 in 3 different regimes under non-equilibrium condition with different magnitude

of applied *drain voltage*. Here, we assume that the *source* electrode is always grounded (V_S= 0 V) and the *gate voltage* is always larger than the *threshold voltage* so that the conducting channel is present. By applying a small *drain voltage*, a current can flow from the *source* to the *drain* through the conducting channel. The channel acts as a resistor, and the *drain* current, I_D, is proportional to the 'drain' voltage, V_D. In this regime the *drain* current is given by: [22]

$$I_D \approx \frac{W}{mL} C_{ox}\mu\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] \quad \text{for} \quad V_D << (V_G - V_T) \tag{2.1}$$

where the coefficient *m* is a function of doping concentration and insulator thickness and approaches unity by using very thin insulators or low-doped semiconducting channels which is the case in the current application. μ is the *carrier mobility* of electrons and is defined as υ_d/E in cm^2/Vs. Here υ_d and E are the *drift velocity* of electrons and the electric field along the conduction channel, respectively.

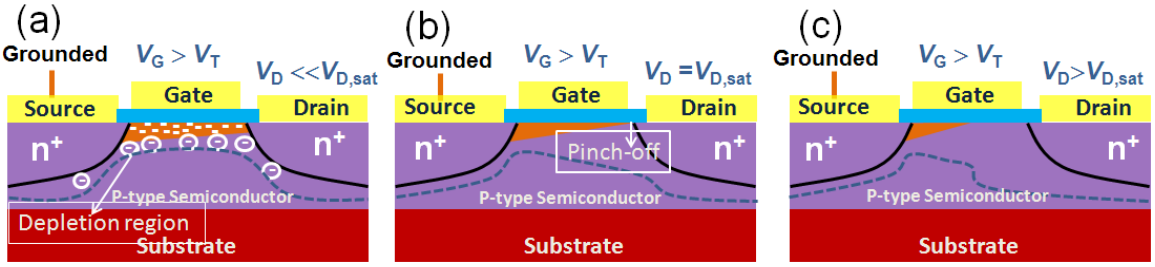

Figure 2.3 A cross-section structure of a MOSFET a) linear regime b) onset of saturation regime c) saturation regime

For smaller values of V_D, the quadratic factor in equation (2.1) can be ignored, and a linear dependence between V_D and I_D is obtained as shown in Figure 2.2a and equation (2.2):

$$I_D \approx \frac{W}{mL} C_{ox}\mu(V_G - V_T)V_D \tag{2.2}$$

As V_D increases, once it approaches $V_G - V_T$, the channel depth at the contact point of the channel and *drain* approaches zero; in other words, the conducting channel at the vicinity of the *drain* is pinched off (Figure 2.3b). If V_D further increases, ($V_D \geq V_G - V_T$) the pinch-off point starts to move towards the *source*. However, the voltage difference over the

induced channel (from of pinch-off point to the *source*) remains the same as $V_{D,sat}=V_G-V_T$ and, therefore, I_D remains constant or saturated.[22] At this point the *drain current* ($I_{D.sat}$) is given by:

$$I_D \approx \frac{W}{2mL} C_{ox}\mu(V_G - V_T)^2 \qquad \text{for} \quad V_D > (V_G - V_T) \tag{2.3}$$

The *field-effect mobility*, μ_{FET}, is calculated from equation (2.3), which shows the squared dependency of I_D with respect to V_G. It also suggests that I_D is no longer a function of V_D.

The other important parameter is *transconductance* which is calculated from the saturation region (refers to equation 2.3) and is computed as follows:

$$g_m = \left.\frac{dI_D}{dV_G}\right|_{V_D \rangle V_{D,sat}} = \frac{W}{mL}\mu C_{ox}(V_G - V_T) \tag{2.4}$$

The *sub-threshold slope* (*S*) is a criterion which shows the efficiency of the *gate voltage* to modulate the '*Off*' and '*On*' state of current, i.e., how abruptly the device turns '*On*' from the '*Off*' state, with respect to the change in *gate voltage*. It depends not only on the nature of the semiconducting channel but also on the chemical composition, dielectric properties and capacitance of the device. It is an important parameter and is desired to be small for low-power operation. The theoretical limit (60 mV/dec) shows the minimum possible value of *sub-threshold slope* which can be achieved in an ideal condition.

The sub-threshold voltage is given by:

$$S = \ln(10)\frac{dV_G}{d\ln(I_D)} = \ln(10)\frac{kT}{q}\left(1+\frac{C_D}{C_{ox}}\right) \tag{2.5}$$

where, C_D, is the depletion capacitance and C_{ox} is the gate insulator or the dielectric capacitance (electrolytic capacitance in the present case). In an ideal case of infinite dielectric capacitance the *sub-threshold slope* is simplified to:

$$S = \ln(10)\frac{kT}{q} \tag{2.6}$$

This equation gives the minimum theoretical value of ~ 60 mV/decade at room temperature (300 K). In order to reach a value close to the theoretical limit, it is necessary to have an ideal semiconductor-metal contact, a very high-quality semiconductor, a high-quality semiconductor-dielectric interface and a high capacitance of the dielectric.

2.2 Electrochemical gating

In the previous section, the principle of field-effect transistors has been presented. It has been shown that the conductance of semiconducting films can be controlled by the application of a voltage across a dielectric (metal oxide) between gate and semiconductor channel.

Alternative gating approach exploits the fact that the noble metals and the chemically inert semiconductors, when immersed in an electrolyte, develop a charged solid-electrolyte interface. In the absence of any chemical reaction this interface, known as electrical double layer, is functionally analogous to a charged plate capacitor. Thus, in a similar way like in dielectrically gated FET, an electric field applied across the semiconductor/electrolyte interface can either accumulate or deplete charge carriers, controlling conductivity of the semiconducting channel. This gating strategy, with the electrolyte substituting solid dielectric in FET, is commonly referred to as *electrolytic-gating*, *electrochemical-gating* or *electrostatic gating*. It should be stressed here that this technique is completely different from *electrochemical doping* of a semiconducting layer by chemical reactions where faradaic currents across the solid/electrolyte interface are present. With the *electrochemical doping* approach the conductivity of the semiconductor is modulated via reduction/oxidation reactions,[23] however, such methods are usually very slow due to the involvement of chemical reactions and not likely to be long-time reversible. The distinction between *electrolyte gating* and *electrochemical doping* is similar to the difference between the functioning of electrolytic capacitors and batteries. Therefore, at this stage the *electrolyte-gating* approach followed in this study needs to be clearly differentiated from the *electrochemical doping* activity. In fact, in order to ensure pure *electrolyte-gating* and to avoid occurrence of any chemical reaction, a careful selection of the supporting electrolyte, electrode materials and a precise control of the *gate voltage* has always been done in this study. A clear picture of the above explanation has been illustrated in figure 2.4.[24]

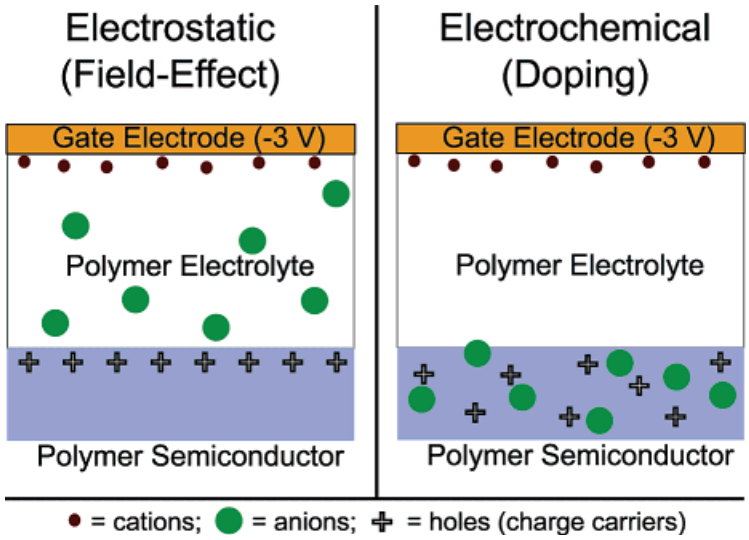

Figure 2.4 Schematic image of the difference between electrostatic and electrochemical doping of a semiconducting layer.[24]

The idea of *electrochemical gating* basically rests in the presence of an *electrical double layer* at the interface of an electrolyte and a solid electrode. Once a solid electrode is immersed in an electrolyte solution a surface charge develops on the solid and attracts the ions with opposite polarity. However, the ions are not uniformly distributed through the electrolyte. The ion concentration is higher near the interface and smeared out away from the interface. Thus, there is a thin but finite layer of the liquid in the vicinity of the interface which is electrically different from the extended liquid.

There are several theoretical models of the solid-liquid interface which are briefly explained below:

2.2.1 Helmholtz double layer

This model assumes that the electrode surface charge is neutralized by immobilized counter ions of opposite sign attracted to the electrode. The overall result is two layers of charge (the so-called *charge double layer*) and a potential drop which is confined to this region in the electrolyte only. The picture is analogous to an electrical capacitor which has two plates of charge separated by an atomic scale distance. The electric potential falls linearly from its surface value, Φ, to zero in the bulk solution over a definite thickness of counter ions. However, the Helmholtz double layer does not satisfactorily explain all the features, since it hypothesizes rigid layers of charges of opposite sign which do not happen in reality.

2.2.2 Gouy-Chapman double layer

Gouy and Chapman suggested that due to random thermal motion the counter ions cannot be immobilized. Therefore, the charged surface can be balanced with an equal number of ions of opposite charge which are spread out in the electrolyte. In other words, counter ions are not rigidly held, but tend to diffuse into the electrolyte. Contrary to the rigid double-layer scenario the potential falls very slowly into the bulk of the electrolyte. However, this model also has some limitations. It assumes that ions behave as point charges and there is no physical limit for the ions in their approach to the electrode surface.

2.2.3 Stern modification of the diffuse double layer

The Stern model modifies the Gouy-Chapman diffuse double layer and to some extend is a combination of the aforementioned models. It is assumed that some of the ions are immobilized on the surface but there are not enough of them to fully neutralize the surface charge. Therefore the rest of the surface charge is neutralized by a diffuse layer similar to the one presented in Gouy-Chapman model. The diagram in figure 2.5 gives a visual comparison of all the models.

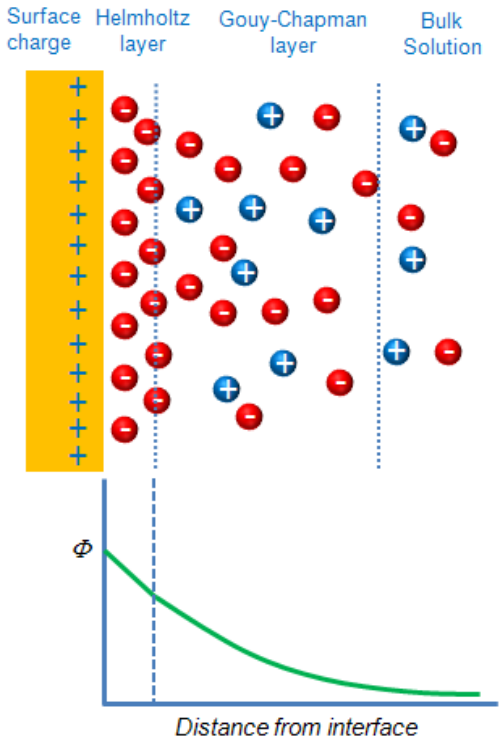

Figure 2.5 Model of the electrical double layer

2.3 Channel material, morphology and geometry

In transistor applications, apart from technological fabrication issues, the most critical parameters are *electrical conductivity*, *carrier mobility*, *environmental stability* and *morphology* of the channel material. Therefore, it may be essential to discuss different channel materials and their morphology with respect to their functionalities in electronic devices. Channel materials are basically semiconductors which are divided into two main categories, inorganics and organics.

Most of the inorganic semiconducting materials have high electron mobility and great stability. Among them, the best-known channel material is silicon; it is abundant and, consequently, cost effective. Moreover, one can easily grow silicon oxide over silicon just by thermal treatment and SiO_x works as an excellent gate dielectric with very low *leakage*. The doping possibility of silicon to provide equally good quality and high *mobility* n-type and p-type semiconductors for MOSFET (CMOS) technology has been an additional key to the success of silicon-based electronics. Silicon channel transistors have been fabricated with silicon being amorphous,[25] single crystalline[26] or polycrystalline.[7] Amorphous silicon (a-Si) and polycrystalline thin films have been traditionally used in active-matrix LCDs and photovoltaic devices [27–29, 30–33] The next important group of channel materials are III-V compound semiconductors such as GaAs, InP, GaP and GaN. III–V compound semiconductors show very high electron *mobility* and *substantially* higher than silicon, and have been used in a number of well-established commercial technologies, such as RF transistor technologies and especially in optoelectronic devices. For instance, InAs and InGaAs are of great interest for a variety of high-speed digital logic applications.[34] However, none of these well-established and frequently used high-performance semiconducting materials are appropriate for transparent and flexible electronics.

In this regard, carbon-based materials, organic semiconductors (OS) and inorganic oxide semiconductors are being studied in recent times as a suitable alternative. Nanocarbon materials such as carbon nanotubes (CNTs) and graphene are one of the candidates as they have excellent *mobility*.[35] CNTs have found many applications in electronics, photonics and sensors as well.[36–38] There are still many challenges, such as purification and product cost in the way to develop them worldwide.[39] Nevertheless, there is great interest to use CNTs as transparent electrodes in modern touch screens.[40]

Organic semiconductors (OS) are hardly used for practical purposes but have been widely studied in recent times as the active channel in transistors. OS usually show low electron *mobility* and they also suffer from limited *stability* in ambient oxygen and moisture. For instance, the best FET *mobility* reported for n-channel organic FET (OFET) was in range of 0.45 to 0.85 cm^2/Vs.[41] In case of p-channel OFET, *mobility* values in the range of 0.1 to 5 cm^2/Vs have been reported.[42,43] However, OFETs attracted considerable attention due to their potential low-cost application in large area and flexible electronics. Oxide semiconductors are also intriguing materials due to their relative large intrinsic electron *mobility*. Thanks to their wide band gap, most of them are transparent in the visible optical region and therefore can be used to realize transparent electronics, including transparent displays. Transparent conducting oxides (TCOs), such as indium-tin oxide (ITO), Al-doped zinc oxide (AZO), and indium zinc oxide (IZO), are well known and easily fabricated materials using versatile technologies. The inorganic materials show high *mobility* and fascinating electronic performance when prepared via e-beam evaporation or sputtering, i.e. techniques which result in dense thin films.[44,45,46] On the other hand, these thin film materials have a lack of *reliability* in flexible electronics and the production techniques are expensive. Therefore, one can think of amorphous or nonporous thin films which can be prepared through solution processing, such as wet chemical routes, which allow the deposition on bendable substrates.[47] Unfortunately, this approach results in thin films with lower electron *mobility*.[48,49,11]

Therefore, one-dimensional (1-D) nanostructures of transparent oxides can be the structure of choice as they fulfill the stringent requirements. Consequently, such structures have drawn great attention recently, as they are inherently flexible and in many cases single crystalline. This makes them fascinating candidates for manufacturing high-performance transparent flexible electronics. Moreover, due to their large surface-to-volume ratio and size confinement the dimensions are comparable to the mean free path, coherence length and screening length of the charge carriers. Size dependent factors have great impact on the performance of chemical/biosensors, quantum conductance and ballistic conduction and consequently lead to unique and novel applications in optics,[50] electronics[51] and sensors.[52] In the literature, one can find different types of quasi/1-D nanostructures, such as nanobelts, nanosprings/nanohelixes, nanopropellers, nanorings, nanobows,

nanobranches, nanotubes, nanorods and nanowires. Some examples of the impressive variety of 1-D nanostructures are shown in Figure 2.6.[53]

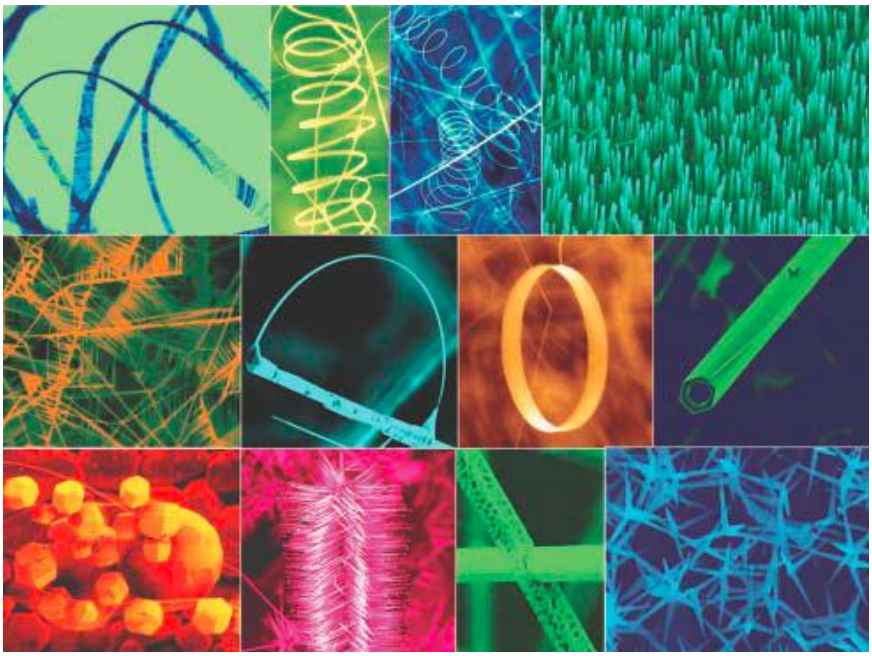

Figure 2.6 A survey of different morphologies of 1-D nanostructure materials [53]

In the present work, the focus is on wire-like 1-D nanostructures. The 1-D nanostructures are distinguished by different classification: nanowhiskers and nanorods are straight with aspect ratios (length/diameter) less than 10, while nanowires and nanofibers are usually bent with aspect ratios greater than 10. Also, nanofibers are thicker than nanowires (typically, more than 200 nm). In the literature the nanowires are described by a thickness in range of 2 to 200 nm, and lengths spanning from hundreds of nanometres to millimetres.[54]

Many kinds of nanowires made from different materials, including IV, II-V[55, 56] and III-V[57, 58] group semiconductors, metals[59–61] as well as metal oxides[62–69] have been produced until now. Parallel to the success with group IV, II-V and III-V compound nanowires, semiconducting oxide nanowires, such as ZnO, SnO_2, CdO and In_2O_3, have become increasingly important and considered as candidates for smart and functional materials. They are composed of anions and cations with mixed valance states accompanied by ion deficiencies (vacancies).[70] Thus, their optical, electrical, chemical and magnetic

properties can be controlled in many ways by manipulating either one or both of these structural characteristics.

2.4 Nanowire synthesis techniques

Many fabrication methods have been explored and established to synthesize 1-D nanostructures. They fall into three main categories; (a) spontaneous growth, (b) template synthesis and (c) lithography. The first two categories are considered as bottom-up approach while the third is a top-down approach. Compared to "top–down" nanofabricated device structures, "bottom–up" synthesized nanowire materials offer better control of the nanowire diameter, which is a critical parameter for the device as it defines the channel width. The nanowire diameter is often below the resolution limits of even the highest quality e-beam lithography systems.

The Spontaneous growth results in the formation of single crystalline nanowires or nanorods due to a preferential crystal growth direction depending on the crystal structure and surface properties of the nanowire materials while template synthesis produces polycrystalline structures or even amorphous nanowires.

The spontaneous growth occurs by means of a phase transformation, a chemical reaction or release of stress to reduce the free energy of the system. Anisotropic growth happens when a preferential growth direction of the crystalline structure exists and no growth takes place in any of the other directions. Some of the most prevalent techniques in this category are solution-based growth routes, such as, hydrothermal synthesis,[71–73] solvothermal synthesis[74–76] and sol-gel mediated reactions.[77, 78] However, the poor crystallinity and the presence of defects in nanowires synthesized using these methods have a negative influence on the performance of the devices.[79] Several vapor transport-based growth techniques have been reported which lead to single crystalline nanowires with almost no imperfections. They include physical vapor deposition (PVD),[80, 81] molecular beam epitaxy (MBE),[82] and laser ablation,[68, 83] where the vaporous agent is provided either from a solid target, i.e laser ablation or a liquefied target, i.e. MBE. In chemical vapor deposition (CVD),[84–87] the gaseous reactants are generated by decomposition of a metalorganic precursor. Thus, the different growth techniques from the vapor phase can be distinguished by the way the growth material is supplied and deposited on the substrate.

Among the various mechanisms utilized for growing the nanowires, a well-known and efficient method is the vapor-liquid-solid mechanism (VLS) proposed by Wagner and Ellis published in 1964.[88] This growth mechanism has been used to explain the growth of whiskers, nanowires, and carbon nanotubes. Basically, any unidirectional growth with a liquid mediating phase (i.e. liquid metal seed particle as a catalyst) and precursors supplied from a vapor phase is considered to grow by the VLS growth mechanism. This mechanism is also referred to when unidirectional growth results from any three-phase system. Some examples are vapor–solid–solid (VSS),[89] solid–liquid–solid (SLS),[90] solution–liquid–solid (SLS),[91] supercritical-fluid-solid-solid or supercritical-fluid-liquid-solid (SFSS or SFLS),[92] growth processes.

2.4.1 Vapor-Liquid-Solid (VLS) mechanism

In the VLS growth, a second phase material commonly referred to as either impurity or catalyst is introduced with the purpose to direct and confine the crystal growth along one direction. In theory, material A would deposit on a substrate B if the condition $\gamma_B > \gamma_A + \gamma^*$ is achieved, where γ_A is the surface energy of the material to be deposited, γ_B is the surface energy of the substrate material, and γ^* is the interfacial energy. In order to meet this inequality, deposition sites with high surface energy are desired. Therefore, it is a common practice to deposit a metallic thin film as a catalyst to mediate VLS growth.

At a given growth temperature the catalyst forms a liquid droplet reducing its free energy by alloying with the vaporized metal. At certain vapor pressure, absorbed material enriches the catalyst droplets, and then precipitates at the growing surface/interface resulting in one-directional growth.

There are many requirements and conditions to be met for controlled VLS growth:

1. Selection of the right catalyst using equilibrium phase diagrams with the goal to provide a liquid alloy with the material of interest. This gives the necessary information on a specific composition (catalyst, growth material) and synthesis temperature to achieve co-existence of liquid alloy and solid 1-D material.
2. Presence of a catalyst in the form of a cluster which eventually determines the diameter of the final 1-D nanostructure and localizes the vaporized material at the end of the growing nanowire.

3. The liquid catalyst alloy cluster serves as a preferential site for absorption of the vaporized material (i.e., there is a much higher sticking probability on liquid rather than on solid surfaces). When the partial vapor pressure of 1-D material is high enough the liquid catalyst is moderately supersaturated. Next the adsorbed material partially precipitates, solidifies and becomes the nucleation site for crystallization which in turn results in preferential 1-D growth in presence of vaporized material.
4. The equilibrium vapor pressure of the catalyst over the liquid alloy droplet must be sufficiently small to avoid (or minimize) evaporation of the catalyst from the droplet.
5. The catalyst must be chemically inert to avoid any chemical reactions with the growing species.
6. The interfacial energy plays an important role; the wetting characteristics influence the diameter of the nanowire. For a given volume of the liquid droplet, a small wetting angle results in a large growth area and large nanowire diameter.
7. In order to provide a unidirectional growth the solid-liquid interface must be well defined crystallographically.

The synthesis of Si nanowire can be considered as an example to illustrate the VLS mechanism. The desired catalyst, Si:catalyst composition, and growth temperature of a nanowire can be determined by examining the Si-rich region of binary catalyst-Si phase diagrams. For example, the Au-Si phase diagram (Figure 2.7) shows a broad phase above 363 °C near to the Si-rich region where Au and Si in liquid phase coexist.

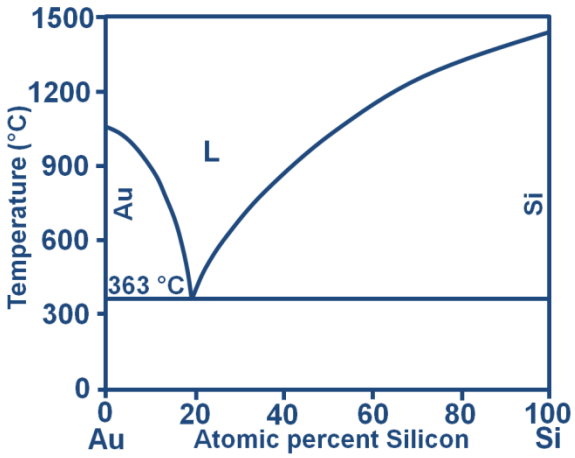

Figure 2.7 Phase diagram of different metal-Si systems

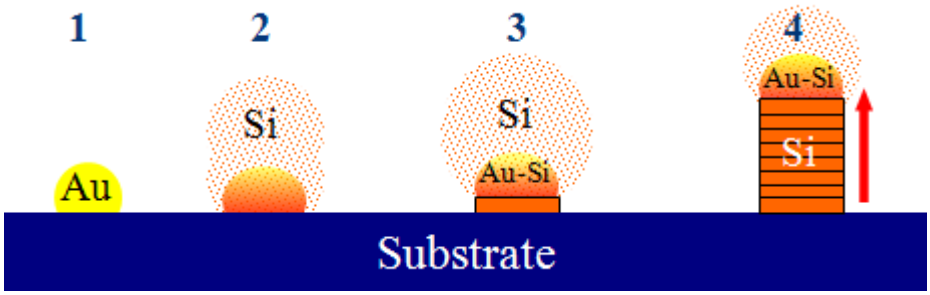

Figure 2.8 Illustration of the VLS growth mechanism

At a certain growth temperature above the eutectic point of the Si-Au system, the vaporized Si species preferentially condenses in the vapor-solid interface of the catalyst until a liquid alloy droplet is formed as shown in Figure 2.8, step 2. Step 3 shows that at a relatively high Si vapor pressure the condensation of vaporized Si in the alloy droplet can be continued even when the droplet is supersaturated with Si. Subsequently the supersaturated Si species separates out of the droplet and precipitates at the liquid-solid interface of the substrate where it immediately solidifies as it has a melting point higher than the growth temperature. The first nucleated Si layer thus produced then onsets epitaxial and unidirectional growth of the solid phase Si nanowire as far as the Si vapor is supplied constantly. (Figure 2.8 step4).

2.4.2 Nanowire size control

As previously mentioned, the VLS growth process has been considered as an effective technique for the synthesis of semiconducting nanowires with well defined geometries. Based on the VLS growth mechanism, unidirectional growth is supported by metallic catalysts under aforementioned conditions, where the catalytic metal transforms to its liquid alloy (liquid phase). The diameter of the nanowires is likely to be determined by the size of the alloy droplet, which in turn is governed by the original catalyst dimension.[93] Consequently, to get the desired radial dimension of the nanowires, the size and distribution of the catalysts (clusters) must be controlled and determined.

Several approaches have been suggested to determine the catalyst primary size and consequently the diameter of the growing nanowires:

The most common way is to deposit Au thin films of different thickness on a substrate to obtain gold catalyst nanoparticles directly or by subsequent annealing of the thin

films.[94] At a moderate temperature well below melting point the Au thin film disaggregate to separated nanoparticles due to dewetting phenomenon. This phenomenon is more pronounced when ultra thin films are prepared via vapor deposition techniques since as-deposited atoms are not really localized but move on the surface of the substrate within a limited range of few nanometers. As a result the prepared thin film is unstable (metastable) and incline to transform (dewet) to islands, clusters or nanoparticles when annealed to a temperature at which constituent atoms obtain enough mobility to be transported on the surface of substrate.[95] Simpkins *et al.* utilized e-beam lithography to control the size distribution of the catalyst nanoparticles. After e-beam writing and defining the catalyst size thermal evaporation was used for metallization followed by lift off and thermal annealing. [96] In another experiment performed by Bogart *et al.*, a series of anodized porous alumina membranes was implemented to determine the catalyst size.[97] A similar technique was also used by Lee *et al.*. The catalyst size and the size distribution was controlled by means of nanoporous alumina templates which were used as the nanoscale stamps for printing of catalyst nanoparticles.[98] Mark *et al.* produced monodisperse catalyst nanoclusters and used them as the seeds to control the diameter of the nanowires.[99]

Generally, the methods should be selected with caution to avoid several common drawbacks such as nanoparticle agglomeration or catalyst size variation.[98]

2.5 Previous reports on nanowire FETs

The development of one-dimensional nanostructure electronics (i.e. nanowire-based FETs) over the last two decades has introduced a powerful class of materials. Through controlled growth and organization, opportunities for novel nanoscale photonic and electronic devices including large area displays, transparent and invisible electronics, smart windows, optical and UV sensors and solar cells etc. are opened.

There are several causes that have contributed to development of nanowire-based FET research. Firstly, semiconductor nanowires can be prepared in high-yield with reproducible electronic properties as required for large-scale integrated systems.[100, 101] Secondly, the single crystalline structures reduce carrier scattering and result in higher carrier mobility compared with other non-1D nanostructures of similar size.[102] Thirdly, owing to the high aspect ratio of nanowires, the electrical integrity of nanowire-based electronics can be intensively scaled down, a feat that has become increasingly difficult to achieve with

conventional TFTs.[103] Finally, nanowires can function both as active devices and interconnects and thus have the potential to provide simultaneously two of the most critical functions in any integrated nanocircuitry.[104]

In this section the broad arrays of nanowire-based FETs available, their preparation procedures and operating features that could enable new and diverse applications in present-day and future electronics will be discussed.

In general, nanowire-based FETs can be fabricated in four major types of gate configurations: back-gate, top/omega-shaped, side-gate and wrapped/surrounding-gate. The back gate configuration is the traditional structure due to its fabrication simplicity; however, it lacks precision control of individual channel segments and poses some additional difficulties with the device integration as well as weak capacitance coupling. In contrast, top and surrounding gate structures demand more complicated fabrication processes, but they have demonstrated enhanced device characteristics and significantly increased integration density due to their higher coupling capacitance.

2.5.1 Back-gate nanowire FETs

When the gate is directly placed on the substrate followed by the insulator film and the active channel, respectively, the device is identified as a back-gate FET. Generally, a combination of a Si/SiO_2 gate/semiconducting nanowire is used to build back-gate nanowire FETs.[105–107] The typical field-effect mobility of a back-gate device falls in the range of 3-80 cm^2/Vs with an *On*/*Off* ratio of around 10^4–10^6. As the nanowire lies on top of a flat dielectric substrate, the back gate capacitance can be calculated based on the cylinder-on plate model:[53, 54, 109]

$$C_{back} = \frac{2\pi\varepsilon_r\varepsilon_0 L_{NW}}{\cosh^{-1}(1+h/r_{NW})} \tag{2.7}$$

where L_{NW} is the nanowire channel length, r_{NW} is the nanowire radius, h is the thickness of the dielectric, and ε_r is the relative dielectric constant of the gate dielectric. The dielectric needs to be thin to achieve effective gate operation; however, thinner dielectric may result in significant leakage current and device failure.[110] Furthermore, Si/SiO_2 gated devices operating at high voltage would prevent them from applications in portable and battery compatible electronics. To overcome this, using high-k dielectric materials can ease the

demand on thickness, without inducing leakage current or causing dielectric breakdown, and also leads to devices performing at lower operating voltage (≤ 5-6 V). For example, HfO_2 dielectric with much higher *k* value (*k* = 16) than SiO_2 (*k* = 3.9) can be prepared readily on Si substrate by metal–organic molecular beam epitaxy method.[111] Other dielectrics such as Al_2O_3 (k = 9),[112, 113] and organic polymer[16] have also been used as an effective gate dielectric layer.

2.5.2 Top/Omega shape gate nanowire FETs

Although back-gate configuration has mostly been adopted in nanowire FETs fabrication, the top-gate structure of nanowire FET offers local gating response with precise control.[114, 115] In addition, localized top-gate electric field requires less field strength to efficiently regulate the channel conductivity and can result in an *On/Off* ratio at least two order of magnitude higher than the back-gate FETs. In this configuration, the *source–drain* contacts are first patterned on a selected nanowire as the FET channel, followed by the deposition of a gate dielectric. Lee *et al.* used Ni/Ti as contact electrodes and deposited 30 nm thick Al_2O_3 gate dielectric by atomic layer deposition (ALD).[116] The gate dielectric layer forms an omega (Ω) shape to enhance the gate performance.[117] In an experiment performed by Keem *et al.* nanowires are transferred onto a hexamethyldisilazane (HMDS) thin film of 50 nm thickness which are spin-coated on top of a thermally oxidized Si substrate. Subsequently, positive photoresist is deposited on the nanowires. After designing the *source* and *drain* using UV photolithography and development, Ti/Al metals are deposited via thermal evaporation. The photoresist and HMDS are removed in distilled water. At the next stage, thin Al_2O_3 layer is deposited conformably on the channel part by ALD, in order to surround the nanowire. It is demonstrated by cross sectional TEM that Al_2O_3 (as gate oxide) deposited on a ZnO nanowire forms an omega shape gate FET with *On/Off* ratio of 10^7 as depicted in Figure 2.9.[117]

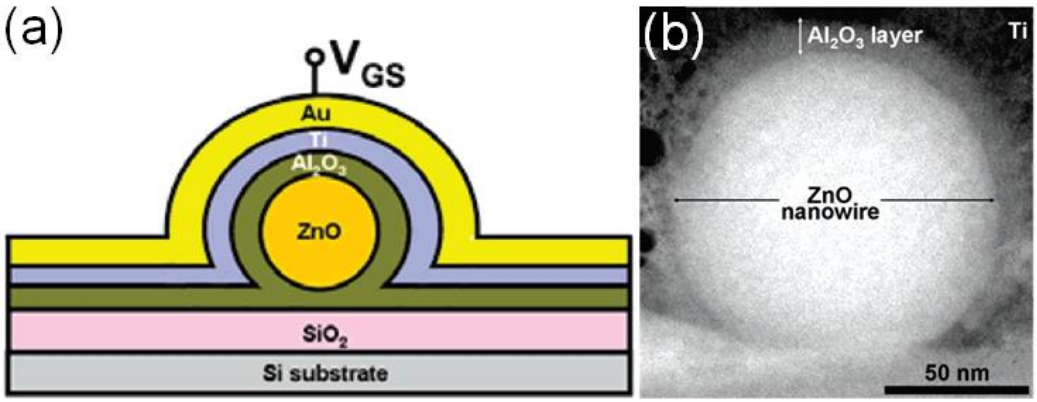

Figure 2.9 (a) Schematic cross sectional view and (b) cross sectional TEM image of the omega shape gate FET.[117]

In such a configuration, the top-gate capacitance is expressed by the cylindrical model in the following way:

$$C_{top} = \frac{2\pi\varepsilon_r\varepsilon_0 L_G}{\ln(1 + r_G / r_{NW})} \tag{2.8}$$

where L_G is the length of the nanowire under the gate dielectric, r_{NW} is the nanowire diameter, and r_G is the outer diameter of the surrounding dielectric layer.[118] By using high-*k* dielectric material and adjusting the r_G/r_{NW} ratio, a large gate capacitance can be achieved, yielding improved *transconductance* and *On/Off* ratio over the common back gate configuration.

2.5.3 Surround/Wrap gate nanowire FETs

In surrounded/wrapped gate nanowire FETs, the nanowire is wrapped/surrounded by an insulator or dielectric. In this case the nanowire should be placed on the substrate with a gap in between or in an ideal case oriented vertically on the substrate to let the dielectric or insulator material cover the channel of the FETs.

Researchers at NASA have successfully fabricated vertically aligned ZnO nanowires, both p- and n-type vertical-surround-gate FETs (VSG-FET).[119] As illustrated in Figure 2.10 the ZnO nanowires are vertically grown on conducting silicon-terminated silicon carbide (SiC) substrate via VLS mechanism. SiO_2 as gate dielectric is coated around the nanowire via CVD, followed by the deposition of the gate electrode (Cr). An additional SiO_2 layer is deposited by CVD followed by chemical mechanical polishing to remove the gold

catalyst and define the vertical channel length of the device. The top *drain* electrode (Cr) is subsequently patterned on top of the nanowire. In this work an *On*/*Off* ratio of > 10^4 and > 10^3 has been reported for the n-VSG-FET and p-VSG-FET, respectively.

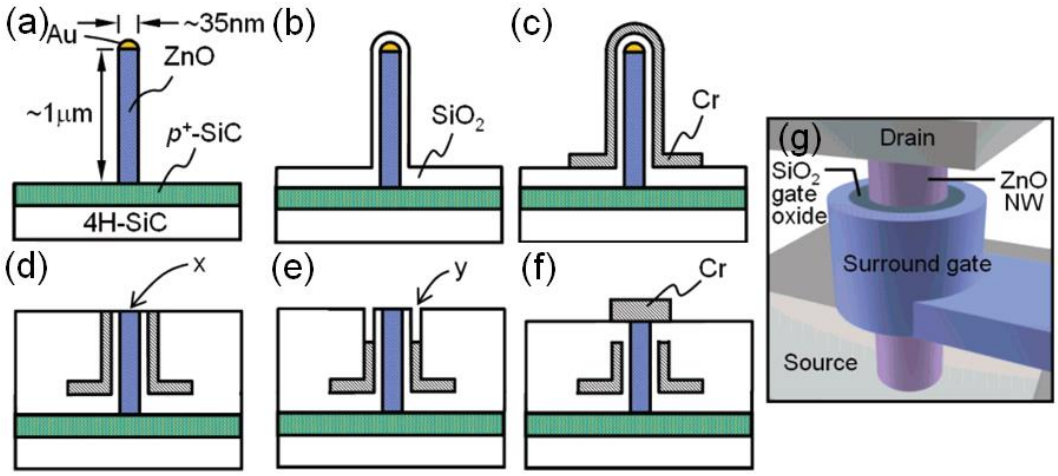

Figure 2.10 Preparation of vertical surround-gate field-effect transistor (VSG-FET) (a) A vertical ZnO nanowire which is grown on p⁺-SiC/4H-SiC substrate. The underlying p⁺-SiC layer acts as the bottom source while the vertical ZnO nanowire performs as the active hole channel. (b) The nanowire is coated with SiO_2 via conformal chemical vapor deposition (CVD) to provide the surround gate oxide. (c) Deposition of Chromium (Cr) via conformal ion-beam evaporation which surrounds the gate oxide serves as the gate electrode. (d) In order to form an active channel length formation SiO_2 is deposited on the substrate by CVD and completely encapsulated the nanowire and is followed by chemical mechanical polishing (CMP) to remove the excess SiO_2 and gold catalyst at the tip of the nanowire. (e) A selective Cr wet etching is carried out to remove the Cr partially and define a desirable gate length. (f) The recess is filled by SiO_2 via CVD, followed by CMP to expose only the tip of the ZnO nanowire to Cr deposited on top as the *drain* electrode (g) A 3D graphical view of the critical components of VSG-FET.[119]

Another elaborate procedure is studied in the experiment carried out by Zhang *et al.*[120] Al_2O_3 as gate oxide is deposited on vertically grown Ge nanowires followed by deposition of Al by means of magnetron sputtering which leads to core-shell $Al/Al_2O_3/Ge$ nanowires with approximate cylindrical geometry. The nanowires are then harvested and transferred on a new substrate and coated with PMMA. Lithographic patterning is

performed to open small windows to cut away the Al and Al_2O_3 layers that surrounded the nanowires via wet chemical etching. The directional electron-beam evaporation is used to complete the *source* and *drain* contacts. Finally, the second step of e-beam lithography followed by metal evaporation is carried out to place the gate. The whole procedure is schematically shown in Figure 2.11. The electrical property of the surrounding gate Ge nanowire FETs exhibits p-type characteristics (due to light, unintentional p-doping during the growth) with an *On/Off* current ratio of 10^5 at V_D= 0.5 V.

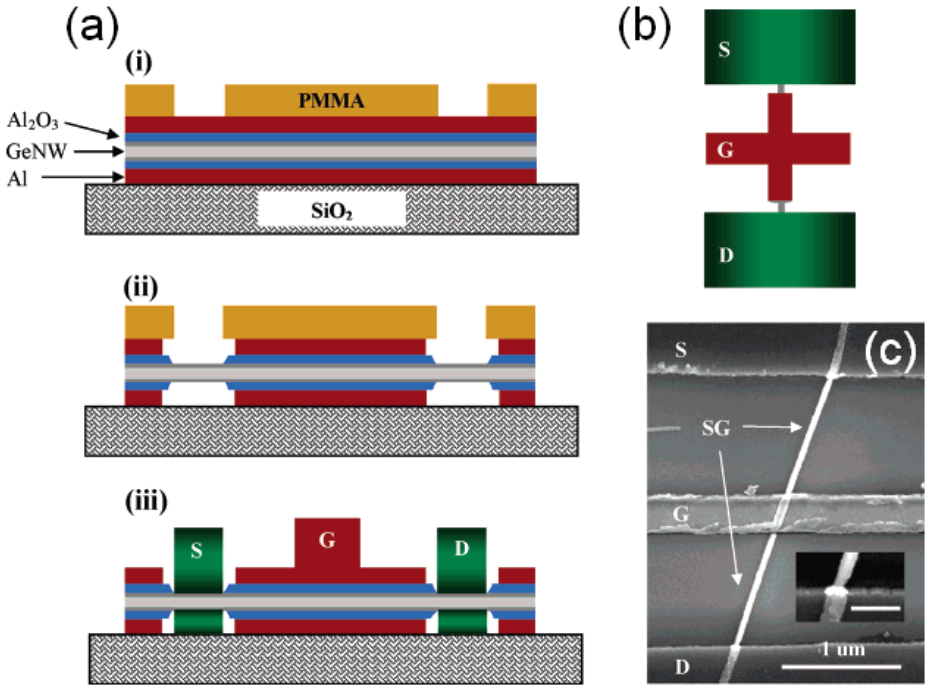

Figure 2.11 Surround-gate nanowire transistors with self-aligned *source/drain* and *gate*. (a) Schematic cross-sectional views of the key fabrication steps: (i) e-beam lithography patterned PMMA to design *source* and *drain* contacts over the core-shell nanowire; (ii) KOH etching was used to remove Al and Al_2O_3 shells in the contact regions (notice undercutting in the outer shells); (iii) directional Ti deposition on *source* and *drain* regions, lift-off, followed by patterning of Pt *gate* electrode as surround gate. (b) A schematic top view of the surround-gate device. (c) A SEM image of a surround-gate device. The surround-gate (SG) metal shell is contacted by the Pt gate line (in the middle) and extends to the edges of the *source/drain* electrodes.[120]

In another example, similar to the above mentioned work, Dhara *et al.,*[121] reported high performance nanowire FETs. They harvested the grown nanowires and transferred

them onto a different substrate which was already coated with an e-beam resist polymer beforehand. Subsequently, another layer of e-beam resist with different molecular weight was deposited to sandwich the nanowires. Following two steps of e-beam lithography, firstly the dielectric material and secondly the *source, drain* and gate electrodes were deposited. (Figure 2.12) The authors show capacitance-voltage (C-V) measurements performed at room temperature to determine the capacitance coupling between the wrap-gate electrode and the nanowire. A capacitance value of ~1.5 fF/m and a high field-effect mobility of 2500–2800 cm^2/Vs were reported.

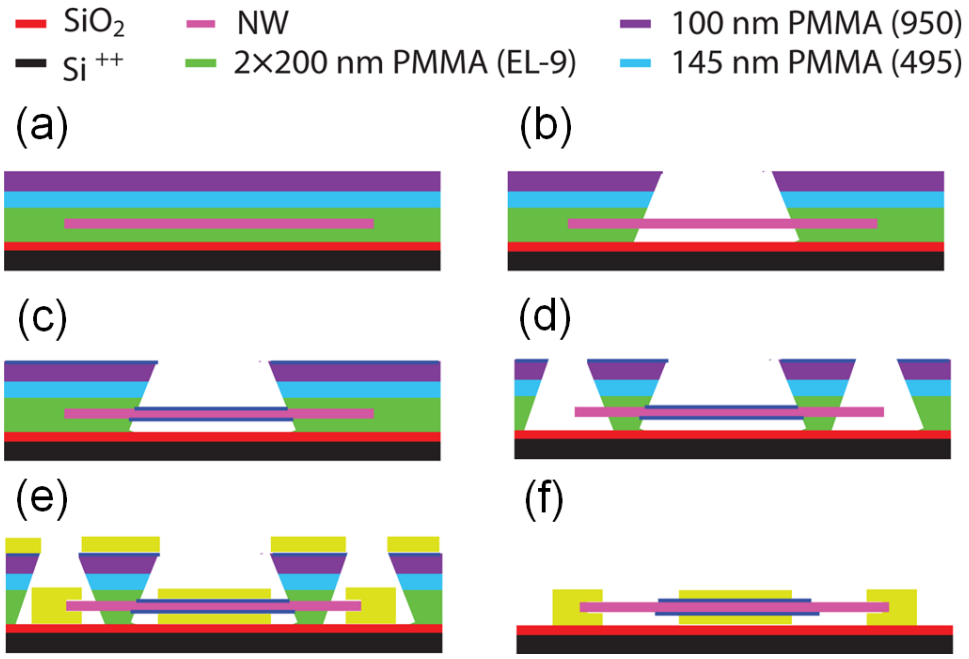

Figure 2.12 Schematic view of lithography performed for fabricating wrap-gate devices. (a) Sandwiched nanowire between polymer e-beam resists of different molecular weights. (b) Patterning of gate electrode (c) deposition of HfO_2 by ALD. (d) Patterning *source* and *drain* areas (e) Chromium and gold deposition via DC magnetron sputtering to form *source* and *drain* electrodes (f) lift off in acetone to remove the polymer resist and metal layers.[121]

In the surround/wrap-gate nanowire-based FET configuration, the gate capacitance is calculated based on the cylindrical model as mentioned previously for FETs with top-gate configuration.

$$C_{top} = \frac{2\pi\varepsilon_r\varepsilon_0 L_G}{\ln(1 + r_G / r_{NW})} \tag{2.9}$$

To investigate whether it is a reasonable assumption to consider the cylindrical model to calculate the dielectric capacitance for Top/omega shape gate FETs, Li *et al.* studied electrical characteristics of surrounding-gate FET and omega-shaped-gate nanowire FETs.[122] Using three-dimensional quantum correction simulation they calculated several parameters like the *On/Off* current ratio, *turn-on resistance*, *sub-threshold slope* (*S*), drain induced barrier lowering (DIBL), and *gate capacitance*. These parameters were compared for a 5 nm nanowire based MOSFET with the surrounding-gate (100% coverage) and omega-shaped-gate structures (70% to 80% coverage), respectively. According to their calculations, it was found that the characteristic difference between the surrounding-gate and omega-shaped-gate MOSFETs with 70% coverage is insignificant. Therefore, the cylindrical model can be safely used for both the omega-shaped -gate FETs and the surrounding-gate FETs.

2.6 Instrumental techniques

2.6.1 X-ray diffractometry (XRD)

X-ray diffractometry is a multi-purpose, non-destructive analytical technique used to identify the crystallographic structure and phase composition of materials as well as differentiate single crystal from polycrystalline or amorphous materials.

Considering a polycrystalline specimen or powder sample with a random distribution of different (*h,k,l*) planes, only planes reflecting the incident X-ray which meet a specific interference condition result in diffraction pattern. Figure 2.13 schematically shows the geometry of the XRD measurement. When an incoming monochromic X-ray beam strikes the crystalline planes in a crystalline specimen at an angle θ, diffraction can arise under a specific condition defined by Bragg's law. The wavelength λ of the X-ray beam is typically in the range of a few angstroms which is perfect for analyzing the structural characteristics of materials. Bragg's law gives a relationship of the distance (d) between two successive atomic layers in a crystal, from which the X-ray beam reflects, with an integer number n of wavelength and can be given as:[123]

$$n\lambda = 2d_{hkl}\sin\theta \tag{2.10}$$

where n is an integer, λ is the wavelength of the incident wave, d is the spacing between the planes in the atomic lattice, and θ is the angle between the incident X-ray and the planes where X-ray has been reflected.

Bragg's law was derived by the English physicists Sir W.H. Bragg and his son Sir W.L. Bragg in 1913 to explain why the cleavage faces of crystals appear to reflect X-ray beams at certain angles of incidence (θ, λ).

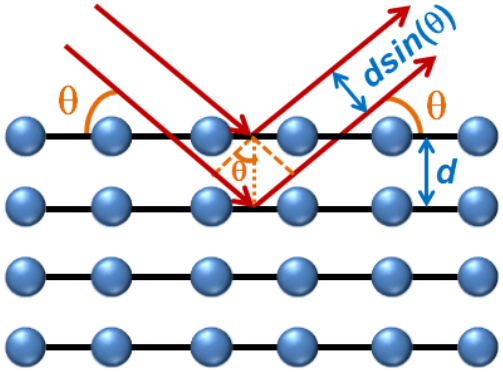

Figure 2.13 Illustration of X-ray diffraction defined by Bragg's law

A Bragg reflection (diffractogram) can be described based on its position (in Radian or degree), maximum intensity, total intensity (integrals intensity), full width at half maximum (FWHM), reflection profile and asymmetry. Based on these parameters for the whole range of a measurement the crystal structure of the materials can be described.

Therefore, complete information about crystallographic structure and often about phase composition of the sample can be achieved through X-ray diffraction pattern by the angle-dependent positions and relative intensities of the resultant reflected peaks.

2.6.2 Scanning electron microscopy

Scanning electron microscopy (SEM) is extensively used to provide large area and high-resolution images of materials. The advantage of SEM is that sample preparation is relatively easy. The system typically also provides energy dispersive X-ray spectroscopy (EDX or EDS) for elemental analysis. Therefore, SEM is a valuable alternative compared to optical microscope when images with high resolution are demanded on a day-to-day basis. A SEM image is constructed by scanning a highly focused electron beam (primary electrons) with energies in range of 1-20 keV across a specimen and detecting the secondary or back scattered electrons ejected from the scanned area. The secondary electrons originate from

the top 5-50 nm of the specimen by the primary electrons or other secondary electrons and provide information on the topography and, to a lesser extent, elemental distribution in the sample.

The primary electrons penetrate the specimen and collide with constituent atoms. After the interaction between incident electrons and the specimen, the primary electron will continue along a new trajectory; this effect is known as scattering, and results in a tear-shaped reaction volume as shown in Figure 2.14, in which all scattering events take place.[124]

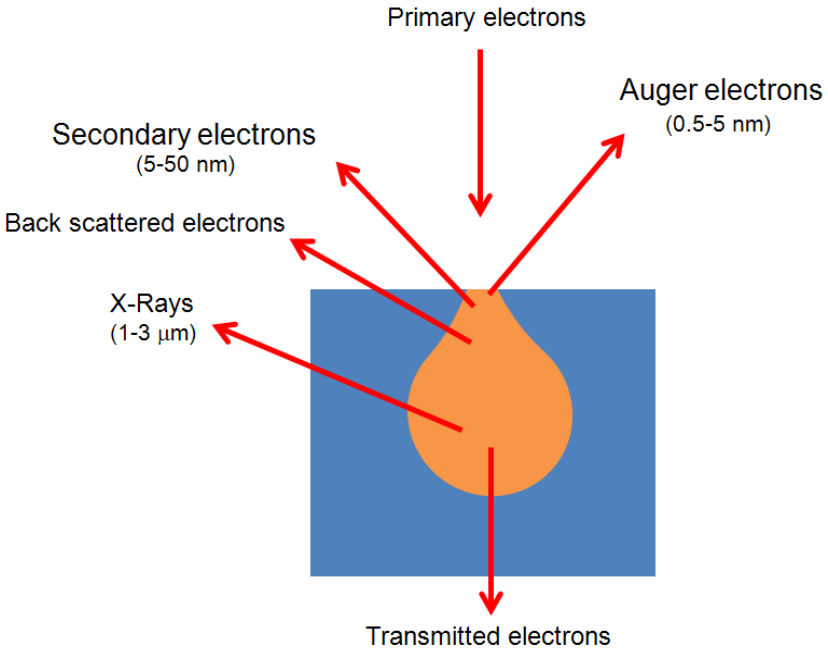

Figure 2.14 Signals resulting from electron-material interaction

Topographical images are mainly provided by secondary electrons which are attracted by a detector, hit a scintillator, and trigger the emission of photons. These photons are then amplified by means of a photomultiplier. Several electrons are thus produced for every photon resulting in a significant amplification. Signal conversion begins with the amplifier in the detector and ends with the image on the display screen.

2.6.3 Transmission electron microscopy

The transmission electron microscope (TEM) works under the same basic principles as the optical microscope however TEM uses electrons instead of light. Since electron wavelength is much lower than wavelength of light it results in a resolution thousands time better than a light microscope, in order of few angstrom.

The resolution δ of any sort of microscope is defined as the minimum distance between two points discernible from one another. It can be calculated using the Abbe's theory of image formation for optic systems. For incoherent light or electron beam the equation is given as follow:[125]

$$\delta = \frac{0.61.\lambda}{\mu \sin \beta} \quad \text{(Rayleigh criterion)} \tag{2.11}$$

where λ is the wavelength of the light, μ is the refractive index of the medium and β the maximum angle between incident and deflected beam. For optical microscopy, the resolution is therefore limited by the wavelength of light (410-660 nm). The X or γ rays have lower wavelength but unfortunately high-performance lenses necessary to focus the beam to form an image do not exist yet (however, X-rays can reveal structural information of materials by diffraction techniques). In 1923, De Broglie showed that all particles have an associated wavelength linked to their momentum:

$$\lambda = \frac{h}{mv} \tag{2.12}$$

where m and v are the relativist mass and velocity, respectively, and h the Planck's constant. In 1927, Hans Bush showed that a magnetic coil can focus an electron beam in the same way that a glass lens can for light. Five years later, a first image with a TEM was obtained by Ernst Ruska and Max Knoll.[125] In a TEM, the electrons are accelerated through vacuum in the column of a microscope by means of a high voltage (100-1000 kV) to a velocity approaching the speed of light (0.6-0.9 c); they must therefore be considered as relativistic particles. The associated wavelength is five orders of magnitude smaller than the light wavelength (0.04-0.008 Å). However, due to the magnetic lens aberrations, the convergence angle of the electron beam is confined to 0.5° and the TEM resolution is reduced to the Å

order. However, this resolution enables material imaging and structure determination at the atomic level.

The accelerated electron beam is projected on the specimen of interest by means of condenser lens system. The specimen must be thin enough (< 200 nm) to allow the incident electrons pass through it. Depending on the density of the material some of the electrons are scatter or deflected from the beam and the rest travel through the specimen. Next, the transmitted electron beam is directed and, focused via an objective and aperture lens system respectively and eventually projected onto an electronic imaging device by means of series of projection lenses which results in a magnified image of the sample.

TEM is used to get outstanding image resolution via high-resolution transmission electron microscopy (HTEM) or scanning transmission electron microscopy (STEM) analysis. It is also possible to characterize crystallographic phases, crystallographic orientation (by diffraction mode experiments), and produce elemental maps (using EDX or EELS).

2.6.4 Energy dispersive X-ray spectroscopy

Energy dispersive X-ray spectroscopy (EDS or EDX) is a chemical microanalysis technique used in combination with scanning electron microscopy (SEM) or transmission electron microscopy (TEM). An EDX system includes a sensitive X-ray detector cooled by liquid nitrogen, and software to collect and analyze energy spectra. Owing to the advanced software one can readily identify elements constituting the investigated sample.

As shown in Figure 2.14 the interactions between the electrons and the material give rise to different kinds of signals such as secondary electrons, back scattered electrons and X-rays. Since the atomic energy states are quantized, the X-ray energy spectrum represents the signature of the atoms.[126] An EDX spectrum is a superposition of background produced by the Bremsstrahlung X-rays and characteristic peaks of the chemical elements present in the material. The identification is quite straightforward for elements beyond carbon when the peaks do not overlap. For lighter elements, Auger electron spectroscopy is often needed. If there is an overlap of the peaks, a deconvolution step is required which may result in poor resolution for close elements.

The spatial resolution of EDX is determined by the penetration and spreading of the electron beam in the specimen[127] (Figure 2.14). Both the accelerating voltage of the

electron and the mean atomic number of the analyzed sample influence the spatial resolution of the X-ray signal. Better spatial resolution is achievable for ultra-thin (~100 nm) specimens, in which the beam does not spread out so much. Such specimens can be analyzed in a transmission electron microscope (TEM) with an X-ray spectrometer attached, also known as an analytical electron microscope or AEM.

2.6.5 Thermogravimetric analysis

Thermogravimetric analysis (TGA) measures the amount and rate of weight change of a material as a function of temperature or time in a controlled atmosphere. Measurements are used primarily to determine the decomposition products of materials and to predict their thermal stability at temperatures up to 1000 °C. The technique can characterize materials that exhibit weight loss or gain due to decomposition, oxidation, or dehydration. TGA can elucidate following issues:

- Thermal stability of materials
- Oxidative stability of materials
- Lifetime and durability of a product
- Decomposition kinetics of materials
- Stability of materials under reactive or corrosive atmosphere
- Moisture and volatile constituents of materials

A TGA comprises a sample pan that is supported by a precision balance. The pan is inside a furnace and can be heated or cooled during the experiment while the weight of the sample is being recorded. An inert or reactive gas flows into the chamber over the material and exits through an exhaust.

If TGA is provided with a vacuum system (Vac-TGA) it allows a material to be analyzed under different pressure conditions as low as 5 Torr. Vac-TGA gives a more accurate look into volatiles, degradation, and degassing of materials such as films, composites, epoxies, etc.

TGA can also be equipped with a mass spectrometer to determine the elemental composition of the material under test.

2.6.6 Mass spectroscopy

Mass spectrometry is a technique that measures the masses of individual molecules that are ionized. So far, mass spectrometry has undergone tremendous technological improvements allowing for its application to analyze proteins, peptides, carbohydrates, DNA, drugs, and many other biologically relevant molecules. Due to ionization sources such as electrospray ionization and matrix-assisted laser desorption/ionization (MALDI), mass spectrometry has become an irreplaceable tool in the biological sciences. A mass spectrometer determines the mass of a molecule by measuring the mass-to-charge ratio (m/z) of its ion. In a mass spectrometer, the sample molecules are ionized in the ionization source Ions are electrostatically directed into a mass analyzer where they are separated according to m/z. Then the separated ions are digitized and detected by an ion detector. The detector converts the ion energy into electrical signals, which are then transmitted to a computer. The result of molecular ionization, ion separation, and ion detection is a spectrum that can provide information on the molecular mass..

Chapter 3

Nanowire growth and characterization

In this chapter, the synthesis of different kinds of oxide nanowires on Si substrates (100) via a catalyst-mediated vapor-liquid solid (VLS) process is presented. In general, the VLS needs a reaction chamber into which the reaction gases can be introduced in a controlled manner. In the present experiments, the nanowires are grown in a quartz tube which serves as the reaction chamber being located in a horizontal furnace. As shown in Figure 3.1, the quartz tube has one open end, which makes it possible to load the source materials and substrates inside. The open end is then sealed by a quartz cap by means of a rubber O-ring. The length of the quartz tube is adjusted in order for the closed end to reach exactly the center of the furnace. A gas pipe inside the quartz tube allows the carrier gas to enter into the reactor exactly at the hot end (as shown in Fig. 3.1) and then to flow towards the open cold end of the reactor. Additionally, a second thinner second tube, also closed at one end, with about one-fourth of the reactor-tube diameter is placed concentrically inside the reactor with the open end facing the cold end of the furnace (see Figure 3.1).

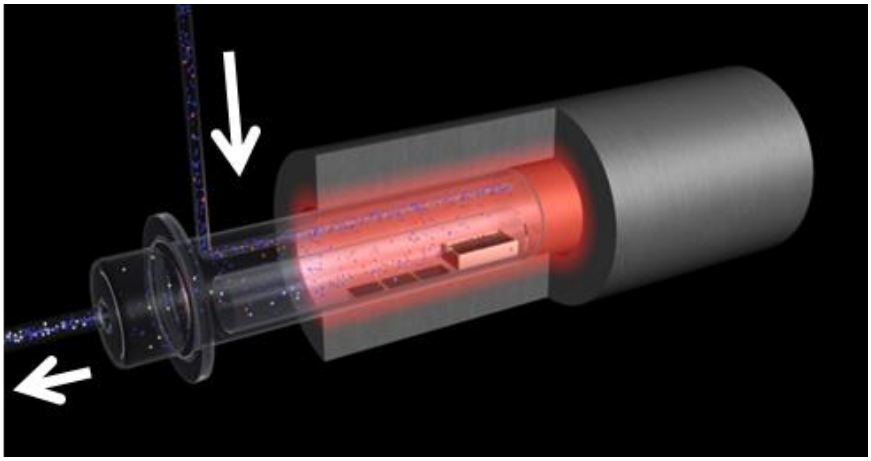

Figure 3.1 3D schematic of the quartz tube (reactor) used for nanowire growth

The source material is placed inside an alumina crucible at the closed end of the thinner tube, i.e. at the end with the higher temperature. Silicon substrates coated with Au catalyst nanoparticles are placed downstream (at a distance of 10-50 mm) from the alumina crucible. Using this experimental setup, the parameters controlling the nanowire growth can be varied. The variation of the carrier gas flow rate and the pressure inside the reactor allows having different partial pressures of the metal vapor and the oxygen gas along the small diameter tube, starting from the highest metallic vapor concentration at the closed/hot end to highest oxygen pressure at the open/cold end. Therefore, with this setup it was relatively easy to obtain the optimal parameters for the ideal conditions for nanowire growth.

3.1 Substrate preparation

As mentioned in section 2.4.2 the size of the catalyst particles and their distribution play a key role in the growth process and in determining the thickness of the resulting nanowires. In this experiment, gold is used as the catalyst to grow nanowires via VLS mechanism. Gold is selected as the catalyst (growth seed) as it does not react with oxygen or any other oxides as the heat of the formation of Au_2O_3 is ~ 39 kcal/mol .[128] Gold has also widely been used for growing metal oxides and some other semiconducting nanowires owing to the broad liquid phase region that exists in its equilibrium phase diagram with these nanowire materials. Two different approaches were implemented to control the diameter of the nanowires. These will be discussed in the following two subsections.

3.1.1 Deposition of the gold thin film

Molecular beam epitaxy technique (MBE) was used to deposit gold thin films with different thicknesses. The gold thin films of 4 nm, 2 nm, 0.5nm and 0.2 nm were prepared under defined deposition parameters which are summarized in Table 1. The deposition was carried out on a Si (100) substrate at room temperature.

Table 3.1 Deposition parameters for MBE coated gold thin films

Film thickness (nm)	Base pressure ($\times 10^{-10}$ mbar)	Growth rate (nm/s)
4	9.4	0.03
2	8	0.03
0.5	6	0.03
0.2	7	0.013

The substrates were then annealed at 500 °C in air atmosphere for 1 hour in order to achieve hemispherical gold nanoparticles with a homogeneous distribution on the substrate. Figure 3.2a shows that the as-prepared gold thin films with a nominal thickness of 4 nm are not uniform but form a network of gold islands. After annealing, as shown in figure 3.2 b, the gold thin film transforms into gold nanoparticles, which later act as catalysts during the VLS growth of nanowires.

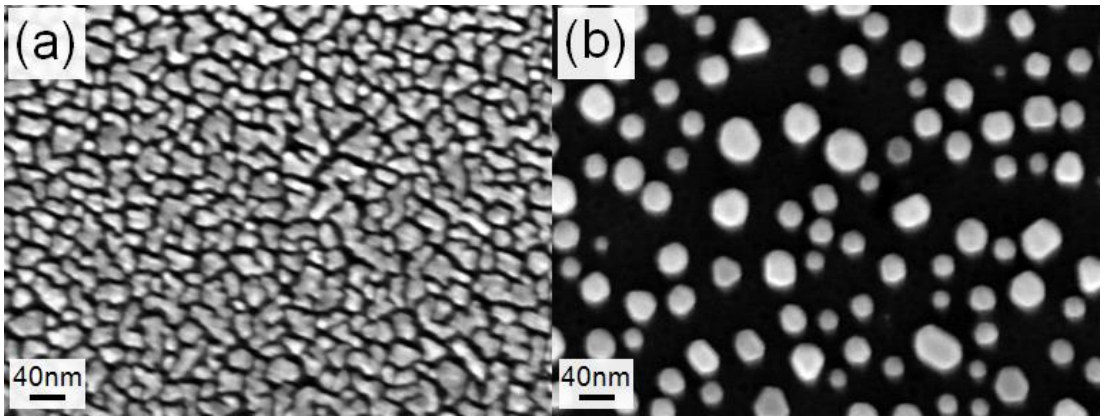

Figure 3.2 a) As prepared MBE coated gold thin film with nominal thickness of 4 nm and b) presence of gold nanoparticle after annealing the thin film at 500 °C for 1 hour in air atmosphere

Figure 3.3(a-d) show representative SEM images of the Au catalyst nanoparticles after annealing of MBE grown Au films deposited on Si substrates. The films have clearly converted into gold nanoparticles with average diameters of ~ 29, 12, 4 and 3 nm, for the nominal film thicknesses of 4, 2, 0.5 and 0.2 nm, respectively. The variation of the distribution of catalysts on the substrates with respect to the different thicknesses is clearly shown in Figure 3.3. The average size of the catalyst nanoparticles shrunk with decreasing the nominal thickness of the gold thin films. However, further reduction of the thickness of the gold thin films from below 0.2 nm, did not result in a noticeable change of the catalyst size as well as their internal spacing. For this ultra-low nominal film thickness, the catalysts are found densely packed and it has not been possible to control the catalysts distribution by further reduction of the film thickness.

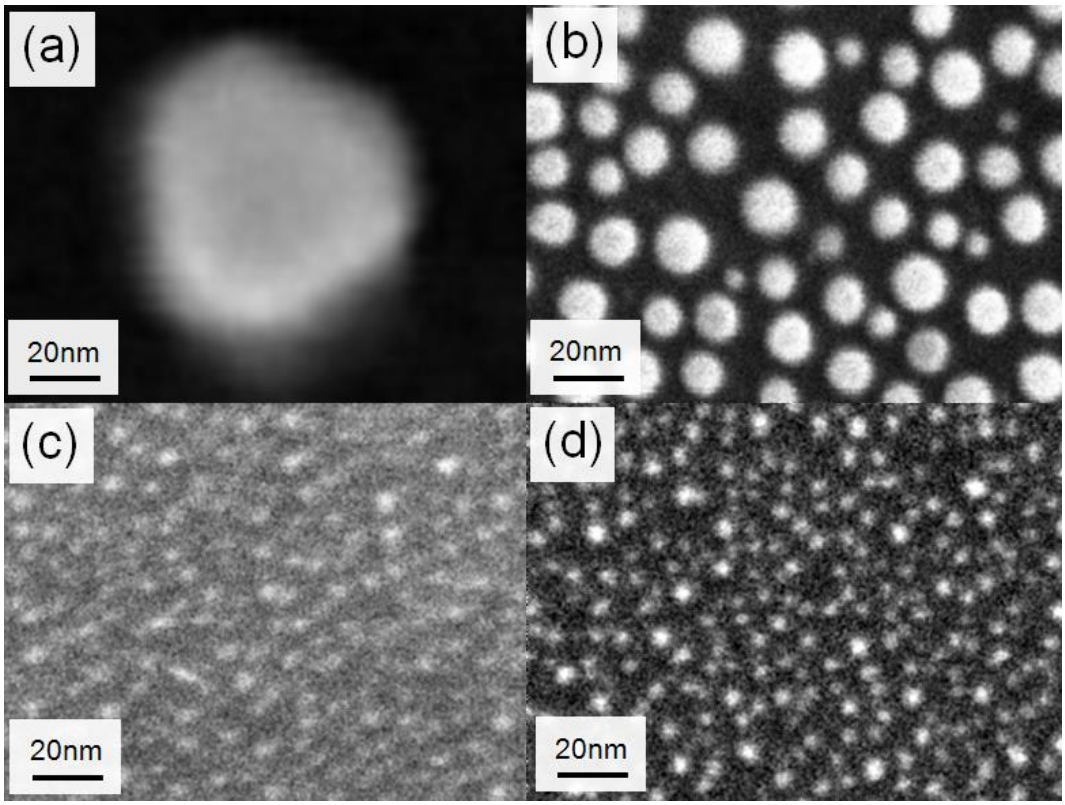

Figure 3.3 SEM images of gold thin films deposited by MBE with nominal thickness of a) 4 nm, b) 2 nm, c) 0.5 nm and d) 0.2 nm after additional annealing at 500 °C

Figure 3.4 shows the size distribution of the catalyst nanoparticles prepared from annealed gold thin films. It is shown (Figure 3.4) that catalysts with average size (d_{Ave}) of 4

nm and 3 nm with a small standard deviation (σ) of 1.5 nm and 1.2 nm were obtained. Utilizing the 2 nm, 0.5 nm and 0.2 nm thin films, nanowires with average thickness of 30 nm, 31 nm and 23 nm, respectively, could be grown. The SEM images and the diameter size of the grown nanowires are shown in Figure 3.5. Evidently, the diameter of the nanowires is much larger than the size of the catalyst nanoparticles (especially true for the small 3 and 4 nm catalyst nanoparticles). Most likely, this is caused by the coalescence of narrowly spaced liquid alloy catalyst clusters which expand during adsorption of the metallic vapors; hence resulting in thicker nanowires.

One way to circumvent this problem could be to distribute the catalysts farther from each other, i.e., to increase the inter-particle spacing of the gold clusters. While annealing of MBE grown films is an uncontrolled process and such engineered distribution of catalysts are difficult to achieve in this manner, such well-distributed catalyst coverage on Si-substrates have been achieved by dispersing functionalized gold nanoparticles with 2-4 nm average particle size on silanized substrates.

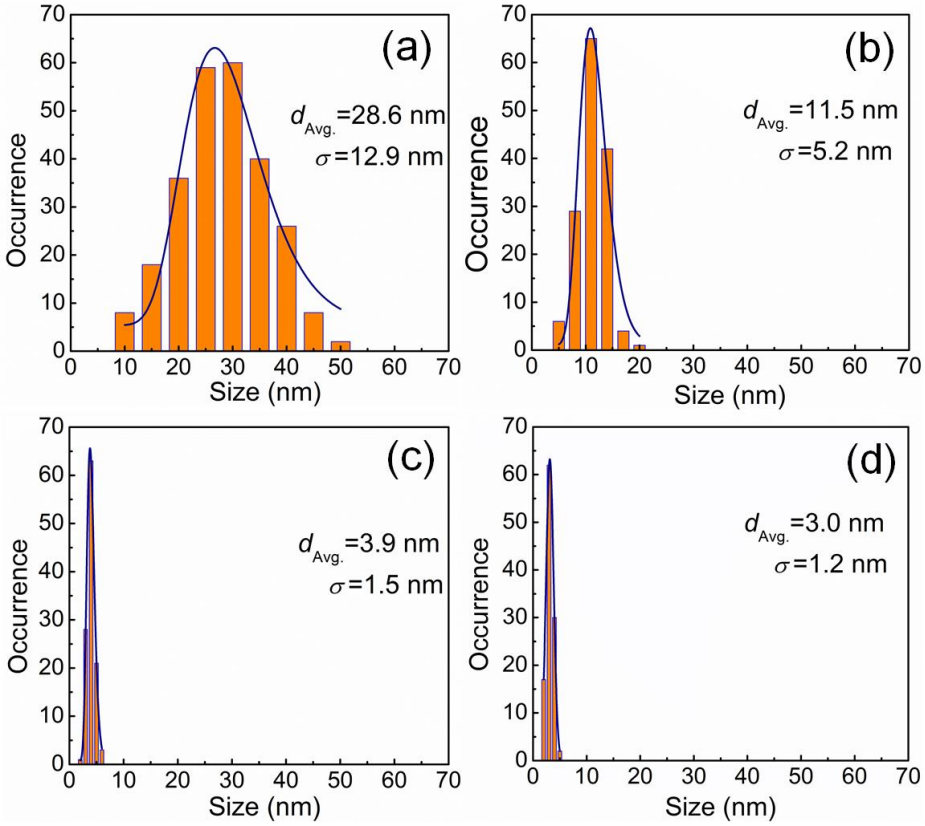

Figure 3.4 Histograms of the size of the catalyst nanoparticles produced by annealing MBE coated gold thin films with nominal thickness of a) 4 nm b) 2 nm c) 0.5 nm d) 0.2 nm

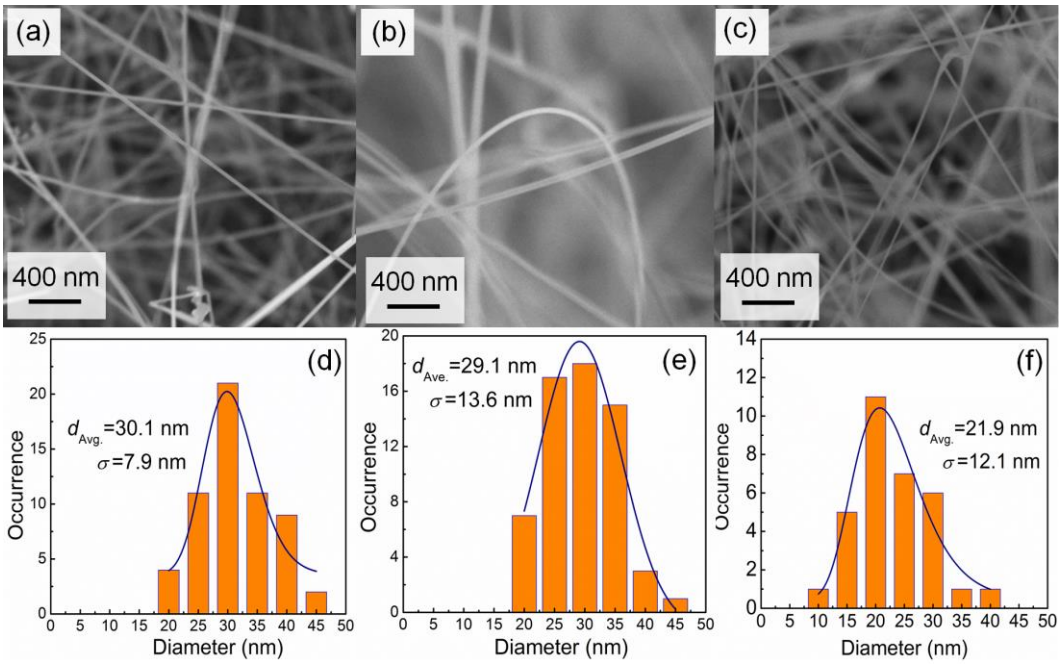

Figure 3.5 SEM images of SnO_2 nanowires with average diameters of a) 30 nm b) 29 nm and c) 22 nm. (d, e and f) The histograms show size deviation of the grown nanowires on substrates coated with 2 nm, 0.5 nm and 0.2 nm catalysts

3.1.2 Gold nanoparticle dispersion

In this approach functionalized gold nanoparticles dispersion (diameter: 2-4 nm) are dispensed on a silanized Si substrate. This method provides well-distributed gold nanoparticles on the silicon substrates with sufficient inter-particle spacing to prevent coalescence of liquid catalyst-metal alloys during metal vapor condensation. The silanization process is shown as a schematic in Figure 3.6. In order to create adsorption sites on the substrates for functionalized gold nanoparticles the silicon wafers are soaked several times in a piranha solution bath. Piranha solution hydroxylates the surface of the wafers and consequently creates adsorption sites for silanol groups on the surface at the next stage. The hydroxilated substrates are then rinsed with distilled water and blown by dry nitrogen and placed in a vacuum desiccator lid facing downside. Few drops of tri-methoxy silane are also introduced in the vacuum desiccator. The substrates are kept in vacuum atmosphere for about ~3 hours to ensure that enough tri-methoxy silane was adsorbed on the substrates.

The treated substrates are then immersed into the dispersion of functionalized gold nanoparticle for 24 hours. Subsequently, the substrates are washed with toluene and ethanol.

In this process as-made gold nanoparticles dispersion without any further modification has been used. The process is found quite versatile, when more/less catalysts and denser/fewer distribution is favored, the gold nanoparticle concentration and/or immersion time can be modified accordingly. Finally, after annealing at 400°C to remove any surfactant and residual organics, substrates are ready to be used.

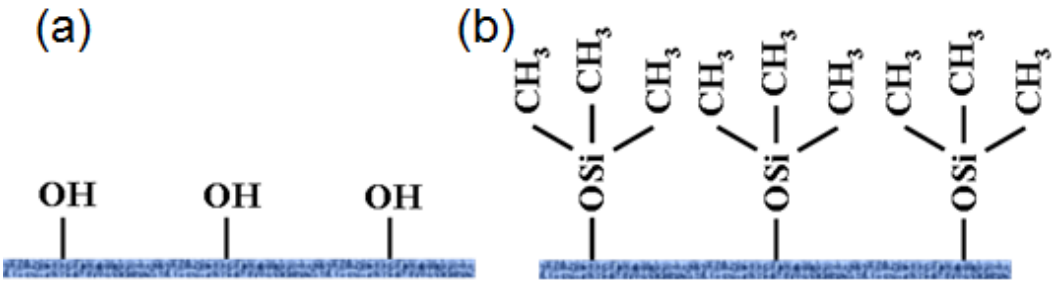

Figure 3.6 a) A hydrophilic silicon substrate b) Silanized substrate

The high magnification SEM images of the dispensed gold nanoparticles on the substrate are shown in Figure 3.7 (a and b). It can clearly be seen that the density of catalysts is much lower than in the previous case of annealed Au film (for comparison, see Figure 3.3 (c and d)). For a shorter immersion time of 12 hours Figure 3.7 (b) shows a significant decrease of the density of Au nanoparticles on the substrate. The lower magnification SEM images shown in Figure 3.8 (a and b) give a larger view of the distribution of the catalyst nanoparticles on two substrates.

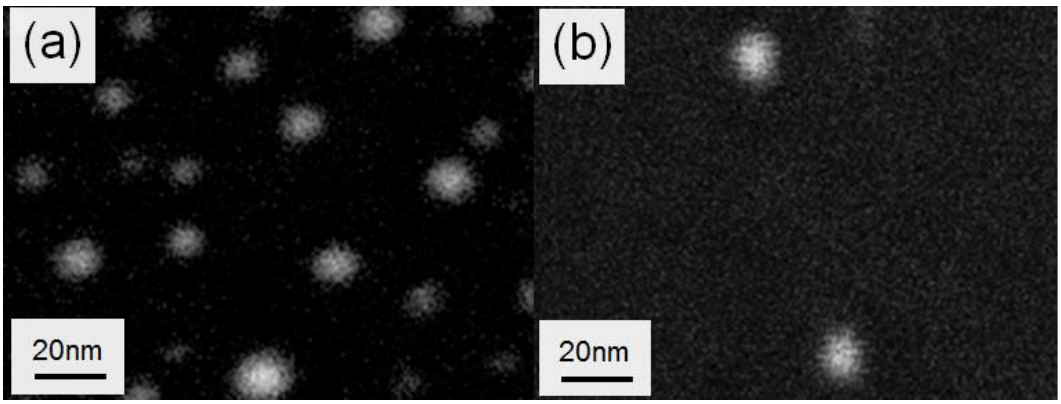

Figure 3.7 High magnification SEM images of catalysts distribution at immersing time of a) 24 hrs b) 12 hrs

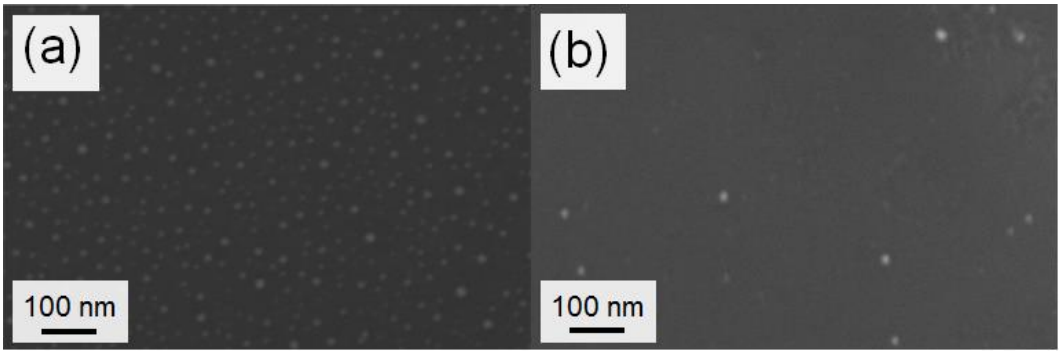

Figure 3.8 Low magnification SEM images of the distribution of catalyst nanoparticles after immersing time of a) 24 hrs b) 12 hrs

The substrates with a shorter immersing time (12 hrs) result in rather low yield of nanowires which is not practical (Figure 3.9 (a) and (b)). The as-prepared SnO_2 nanowires on the substrate with longer immersing time (24 hrs) are observed to have a high yield by SEM, as shown in Figure 3.10 (a). Figure 3.10 (b) also shows the size distribution of the nanowires. As expected, the average size of the nanowires is decreased to an average value of 12 nm with the largest diameters less than 25 nm. Although dispersed gold nanoparticles with average sizes in the range of 2-4 nm are used as catalyst, the size distribution of the nanowires is not narrow and their diameters ranges from 4 to 25 nm. This can be accounted to agglomeration of gold nanoparticles after landing on the silanized substrate.

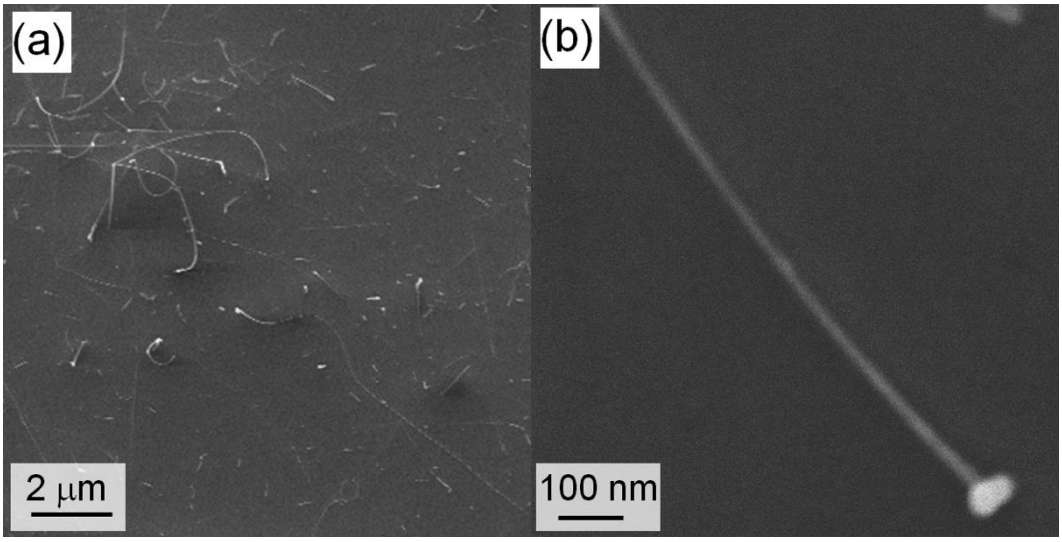

Figure 3.9 a) Low magnification SEM image of SnO_2 nanowires grown on silanized substrate with immersing time of 12 hrs b) High magnification SEM image of a single SnO_2 nanowire on the as mentioned substrate.

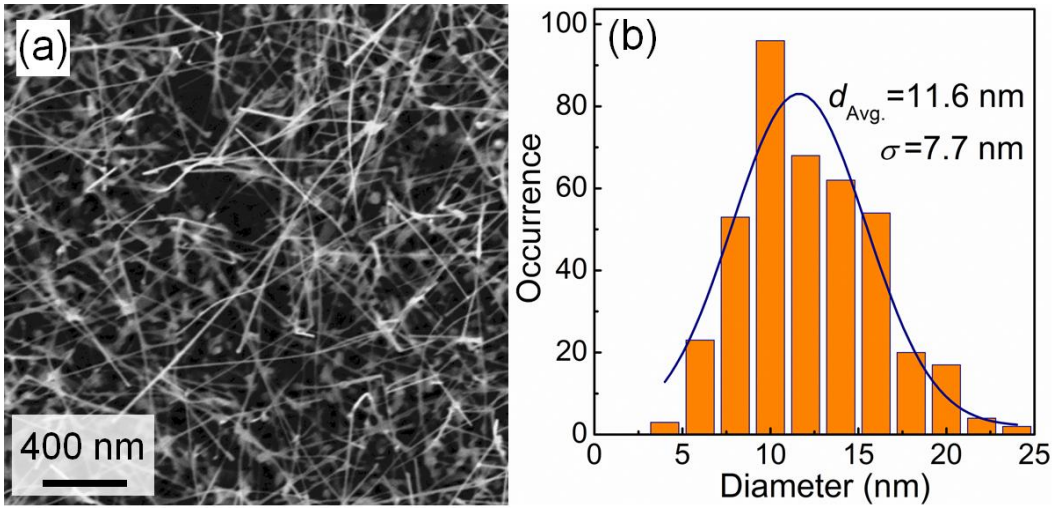

Figure 3.10 a) SEM image of SnO_2 nanowires grown on silanized substrate b) size deviation of the grown nanowires on silanized substrate.

3.2 Undoped nanowires

3.2.1 Synthesis of ZnO nanowires

Zinc oxide (ZnO) nanowires as a typical II-VI semiconductor belong to the best candidates for fabrication of high performance devices owing to their physical properties such as intrinsic transparency with a large band-gap (~3.37 eV) and large charge carrier mobility (~230 cm^2/Vs),[129] in addition the low-cost compared to other alternatives, non toxicity and environmentally friendly properties.[130, 131] Consequently, ZnO nanowires have attracted great attention as a promising functional material and have been considered as building blocks for UV lasers,[132] light emitting diodes,[133] electrochromic and field emission devices,[134, 135] sensors, field effect transistors[136] and solar cells[137]. In order to explore the capacity of ZnO nanowires for the present approach, it is important to master the synthesis of ZnO nanowires in single crystalline form and to study the electronic properties. Here, the vapor-phase transport process is used to grow ZnO nanowires via the vapor liquid solid (VLS) mechanism.

A thoroughly ball-milled mixture of ZnO (99.999% purity, Sigma Aldrich) and graphite powder (99.9% purity, Chempur) with a weight ratio of 1:3 is used as the source material. The reaction is sensitive to the amount of surface contact between ZnO and carbon grains since it defines the active area of the reaction.[138] Consequently, the mixing process was performed by ball milling at 150 rpm for 3 hours. 100 mg of the prepared powder was weighted and placed in an alumina crucible. In this experiment, the annealed MBE coated gold thin film of 0.5 nm, on silicon substrate, was used as a catalyst. After loading the source materials, the substrates were placed 10 to 20 mm downstream from the source into the smaller inner tube and the complete system was evacuated to 1 mbar under a 10 sccm flow of carrier gas (1 vol. % O_2 and 99 vol. % Ar) and was kept under continuous evacuation for about 45 minutes in order to make the reaction atmosphere free from any polluting or unwanted gaseous species. Next, the reactor was introduced into the tube furnace which was pre-heated to 945 °C. Immediately, after insertion of the tube, the temperature of the furnace was rapidly lowered down to 910 °C. The reactor was then kept at this temperature for about 10 minutes and subsequently moved out of the furnace and allowed to cool down to room temperature. After this synthesis procedure, a dense white layer of as-grown ZnO nanowires was observed on most of the substrates. The experimental

parameters for growing ZnO, SnO_2, In_2O_3 and Sn-In_2O_3 nanowires are summarized in table 3.2.

The generation of Zn vapor involves complex processes which are sensitive to the furnace temperature, the oxygen partial pressure and the ZnO:C powder ratio. When a mixture of ZnO and graphite is heated to a temperature higher than 900 °C, the carbothermal reaction between ZnO and graphite occurs, as shown in equation (3.1).

$$ZnO(s) + C(s) \rightarrow Zn\ (v) + CO\ (v) \quad (3.1)$$

Zinc has a high vapor pressure and evaporates at low temperatures (about 400 °C) and reacts readily with oxygen due to its high chemical activity.[139] Therefore the oxygen concentration/partial pressure in the growth chamber is a critical parameter and must be controlled via adjusting the total pressure and gas flow. On the other hand, depending on the oxygen partial pressure, oxygen causes a series of reactions between carbon and oxygen, leading to the formation of CO and/or CO_2 as described by the following chemical reactions:

$$2C + O_2 \rightarrow 2CO \quad (3.2)$$

$$2CO + O_2 \rightarrow 2CO_2 \quad (3.3)$$

Therefore, depending on the amount of CO an oxidation reaction with Zn at temperatures higher than 900 °C may take place, affecting the amount of Zn vapor which was already produced via carbothermal reduction of ZnO.[140]

Zinc condensation is influenced by the local deposition temperature, total pressure, the amount of Zn vapor and the oxygen partial pressure. Zinc re-oxidation and condensation processes during the super-saturation of the Zn–Au droplet alloy follows:

$$2Zn + O_2 \rightarrow 2ZnO \quad (3.4)$$

If the system pressure is too low, Zn vapor may be over supersaturated, and consequently the vapor deposits not only on the surface of the Au catalyst but also at the surface of the substrate, resulting in formation of three-dimensional grown nanostructures.

Product		Source		Ratio	Source weight	$T_{initial}$ (°C)	$T_{process}$ (°C)	$t_{process}$	Ar (sccm)	Ar:O_2 99 : 1 (sccm)	P (mbar)	Au coated Substrate
ZnO		ZnO(99.999 % Sigma Aldrich)	Graphite powder (99.9% purity, Chempur)	1:3	100	945	910	10 min	0	10	1	0.5 nm
SnO_2		SnO (99.9% purity, Alfa Aesar)	Graphite powder (99.9% purity, Chempur)	1:3	100	965	925	10 min	0	40	1	0.5 nm & dispersed
In_2O_3	A	In_2O_3 (purity 99.99%, Chempur)	Graphite powder (99.9% purity, Chempur)	1:3	100	900	900	2 hrs	100	0	10	4 nm
	B	In_2O_3 (purity 99.99%, Chempur)	Graphite powder (99.9% purity, Chempur)	1:3	100	930	930	10 min	0	10	1	0.2 nm
Sn-In_2O_3		In (99.99%, Sigma Aldrich)	Sn (99.8% , Sigma Aldrich)	9:1	100	955	925	10 min	0	10	1	0.2 nm

$T_{Initial}$: The initial set temperature of the tubular furnace before reactor insertion
$T_{Process}$: The stabilized temperature to commence reaction
$t_{process}$: Deposition time

Table 3.2 A brief description of the parameters and conditions of metal oxide nanowires growth via VLS growth

From the Ellingham diagram (Appendix A); reaction 3.1 occurs only when the temperature is higher than 970 °C, whereas in our experiments, the furnace is heated just to 910 °C. It is possible that the local temperature is high enough for reaction 3.1 due to the heat of reaction (reaction 3.2). Therefore the heat is absorbed locally by the source materials (ZnO and graphite) and possibly facilitates the reaction (reaction 3.1) to produce Zn vapor. On the other hand, local concentration of CO could also increase, which could hinder the Zn vapor generation. Therefore, choosing the proper deposition parameters is very difficult in the presence of these two effects. For instance, reaction 3.1 may not fully take place when the O_2 partial pressure is very low and as a result insufficient Zn vapor is released to reach a reasonable super-saturation point, and as a consequence, production of ZnO nanowires is not possible.

Once the partial pressure of O_2 is increased, additional O_2 can react with CO to form CO_2 (reaction 3.3), which lowers the concentration of CO and generates heat as well. Both of these effects facilitate reaction 3.1. Therefore, super-saturation of Zn vapor can be reached, leading to growth of high quality aligned ZnO nanowires. However, when the partial pressure of O_2 is further increased, additional O_2 could immediately react with Zn vapor generated from the source materials to form 3-dimensional ZnO nanostructures.

The XRD measurements of as-grown ZnO nanowires are presented in Figure 3.11. The first three diffraction peaks can be easily identified as $(2\bar{1}\bar{1}0)$, (0002) and (1120) reflections, when compared to the XRD pattern of bulk polycrystalline ZnO which possess a wurtzite hexagonal structure (ICSD No. 031060). The absence of any spurious diffraction peaks confirms formation of phase pure ZnO nanowires. The reflection which belongs to the single crystalline Si substrate is marked in red. Figure 3.12 also shows the energy dispersive X-ray spectroscopy (EDX) which was performed to further support the phase purity.

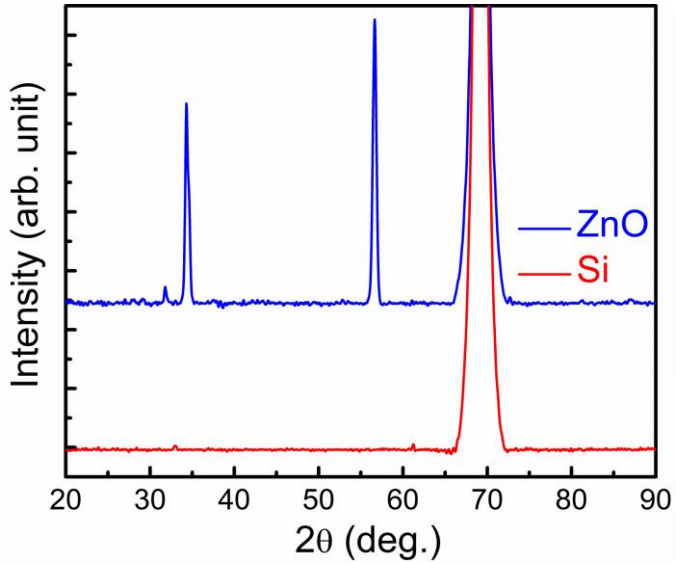

Figure 3.11 XRD pattern of ZnO nanowires

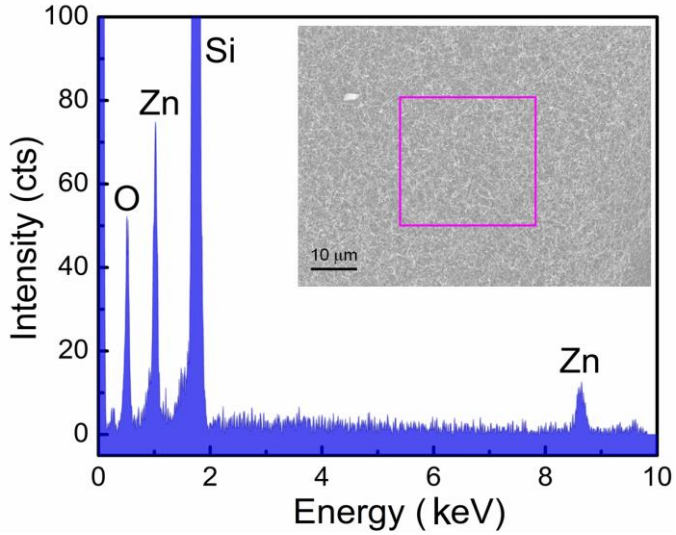

Figure 3.12 EDX spectrum obtained from the squared area indicated in the insert where nanowires are grown

Scanning electron microscopy (SEM) images (a characteristic image is shown in Figure 3.13 a) were acquired on the as-grown samples which show ZnO nanowires and also gold catalysts on top of each nanowire confirming the VLS growth mechanism. The average nanowire diameter is determined from SEM images and is found to be approx. 23 nm (Figure 3.13 (b)).

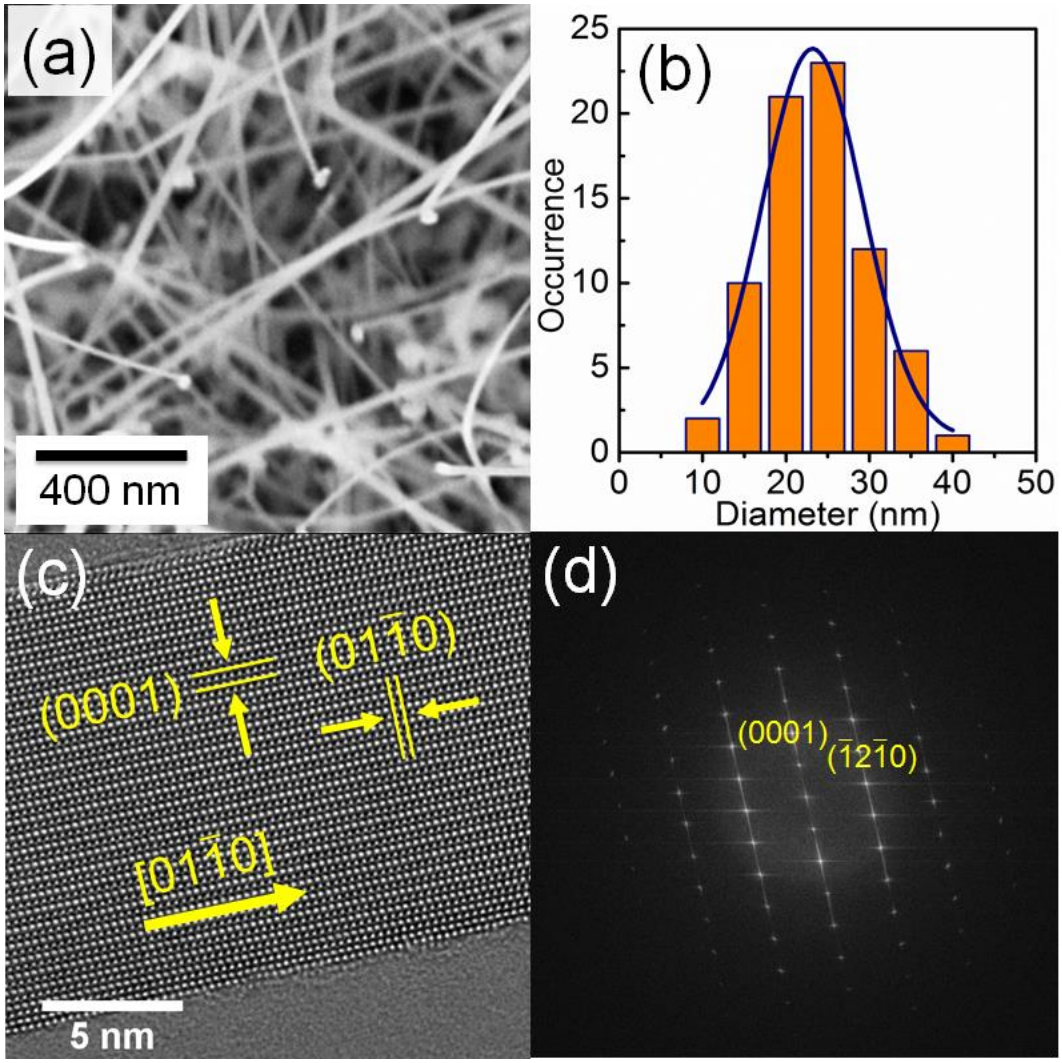

Figure 3.13 a) SEM image of the as prepared ZnO nanowires; b) Histogram of diameter of the zinc oxide nanowires; c) HRTEM image of a single ZnO nanowire; d) Fast Fourier Transformation of the HRTEM image which is shown in the left.

Figure 3.13c shows a high-resolution transmission electron microscopy (HRTEM) image of a single nanowire which undoubtedly confirms the single crystallinity. The fast Fourier transform (FFT) of the HRTEM image (e.g., Figure 3.13 (d)) shows that the growth direction of the nanowires, in most cases, is perpendicular to the (01$\bar{1}$0) planes which translate to [01$\bar{1}$0] growth direction in hexagonal wurtzite lattice structure of ZnO. In many instances during the TEM experiments, the ZnO nanowires were found to be remarkably bent as shown in Figure 3.14a (the bending radius, r_b< 6 μm in this particular case). The resulting strain was attributed mainly to the elastic lattice distortions, because no plastic

deformation ε_{xx} was observed in any of the HRTEM images taken (Figure 3.14 (b)) along the curvature of the bent nanowires. In order to further examine the elasticity and mechanical robustness of the super-flexible nanowires, the strain tensor component, ε_{xx}, (Figure 3.14 (c)) and rigid-body rotation (Figure 3.14 (d)) of the bent segment of the nanowire (Figure 3.14 (b)) was calculated using geometric phase analysis (GPA).[141] Figure 3.14 (e) shows the strain profile (strain tensor component ε_{xx}) measured across the bent segment of the nanowire which is indicated by the black rectangle in Figure 3.14 (c). Compressive and tensile strain is found in the lower and the upper part of the nanowire respectively, and a total strain difference of 2.5% is observed. Additionally, a profile of the rigid-body rotation was measured along the length of the nanowire (as indicated by the rectangular box in Figure 3.14 (d), which shows a rotational gradient of the nanowire axis of about 2.5° from one end to the other, already within approx. 30 nm of length segment. Therefore, it may be concluded from the GPA analysis that the nanowires can be moderately bent without causing any plastic deformations, such as dislocations or other defects.

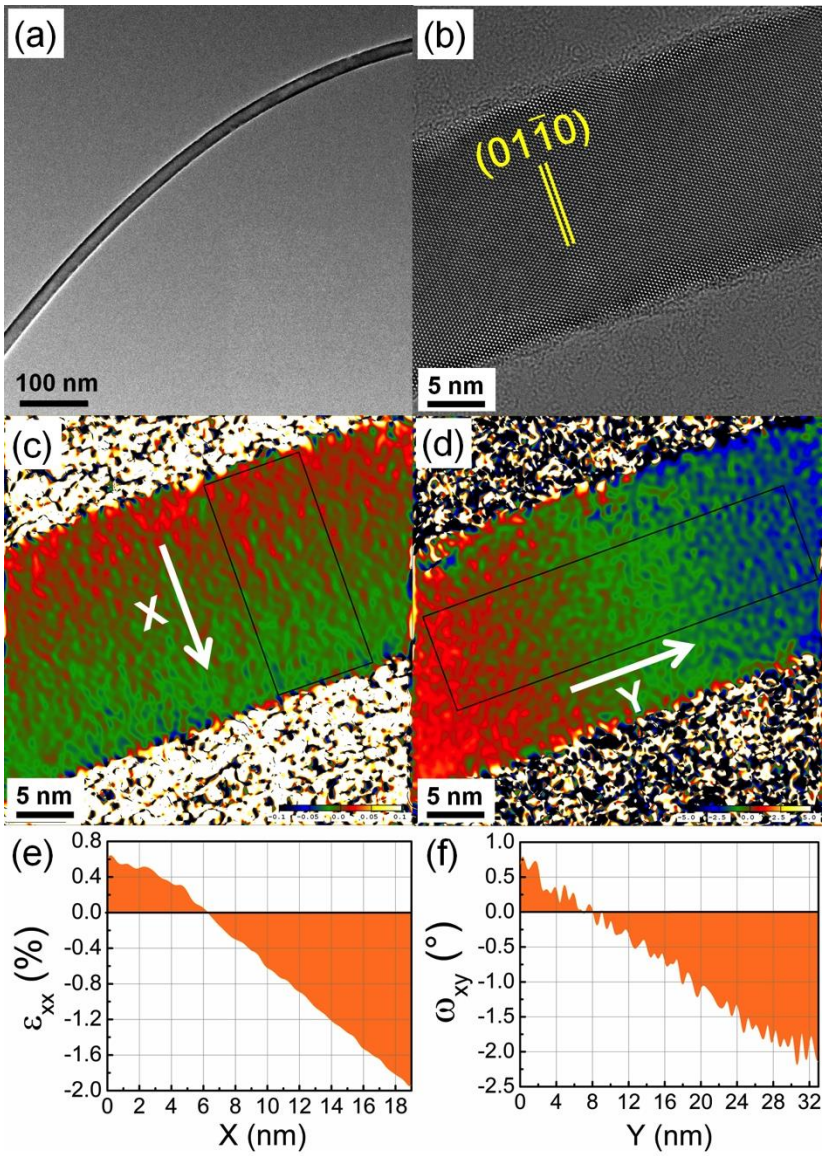

Figure 3.14 (a) TEM image of a typical bent ZnO nanowire; (b) HRTEM image along the curved part of the nanowire; (c) strain map showing the strain tensor component ε_{xx}; (d) rotation map showing the rigid-body rotation (strain tensor component ω_{xy}); (e) strain profile of ε_{xx} measured across the nanowire and averaged over the width of the rectangular box as indicated in (c); (f) rigid-body rotation measured along the nanowire and averaged over the width of the box as indicated in (d).

3.2.2 Synthesis of SnO_2 nanowires

Tin dioxide (SnO_2) is a n-type, wide-bandgap, metal-oxide semiconductor with a direct bandgap of ~ 3.6 eV at 300 K.[142] Nanowire transistors using SnO_2 nanowires as active channels have been investigated recently.[143, 144] They can be used as the building

blocks for constructing high-performance nanodevices, such as field emitters,[64] solar cells,[145] photoconductors[146] and gas sensors[147] etc. as well.

The growth procedure is similar to that described in section 3.1.1 for preparing ZnO nanowires. The source materials (tin monoxide and graphite mixture) and experimental parameters are given in table 3.2. In this experiment silicon substrates were either coated with gold via MBE or decorated with colloidal gold nanoparticles. The substrates were placed 10 - 50 mm downstream from the source material. Dense randomly oriented tin oxide nanowires were obtained as the final product on all the substrates.

The carbothermal reduction of tin monoxide follows the chemical reaction:

$$2SnO\ (s) + C\ (s) \rightarrow 2Sn\ (v) + CO_2\ (v) \qquad (3.5)$$

The ratio of carbon to stannous oxide was selected to be 3:1 to keep the reaction environment highly reducing so that the metallic tin vapor formation could be favored. The Sn vapor was transported and condensed onto the gold catalysts to form Sn-Au alloy droplets. As the droplet became supersaturated, crystalline SnO_2 nanowires were formed by the reaction between Sn and O_2 or CO_2.

Figure 3.15, shows XRD pattern of phase-pure SnO_2 nanowires obtained in a typical synthesis experiment. All the peaks can be indexed with tetragonal rutile structure and the corresponding diffraction peaks of SnO_2 (ICSD No. 031060).

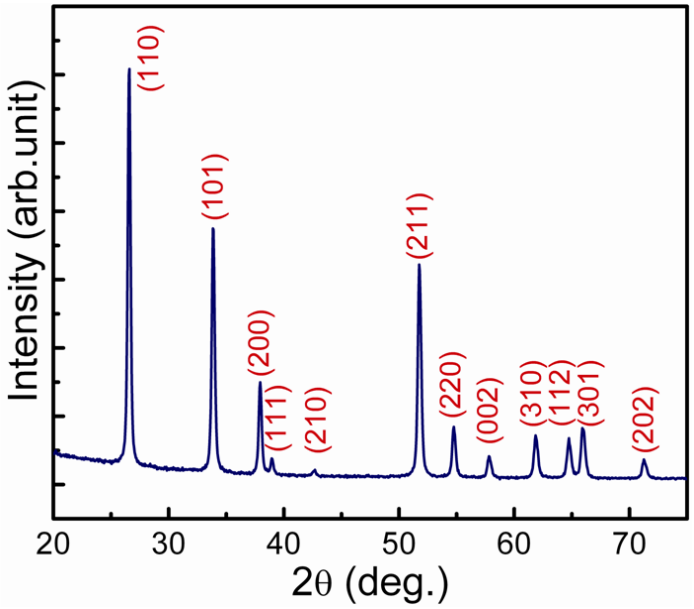

Figure 3.15 XRD pattern of SnO_2 nanowires

Scanning electron microscopy (SEM) images as shown in Figure 3.16 (a) illustrate high density SnO_2 nanowires with spaghetti-like morphology. The nanowires have an average diameter of 20 nm and are typically tens of micrometers long (see Figure 3.5 (c) and (f)).

High-resolution transmission electron microscopy (HRTEM) images of several individual nanowires undoubtedly confirm the single crystallinity of the nanowires and the absence of any line or planar defects. There is no indication for the formation of an amorphous layer at the surface of the nanowire (Figure 3.16 b). The growth direction is found to be [101]. The lattice parameters value of 2.68 Å and 4.77 Å shown in the inset of Figure 3.16(b) corresponds to (101) and (400) crystallographic planes in tetragonal rutile structure of SnO_2.

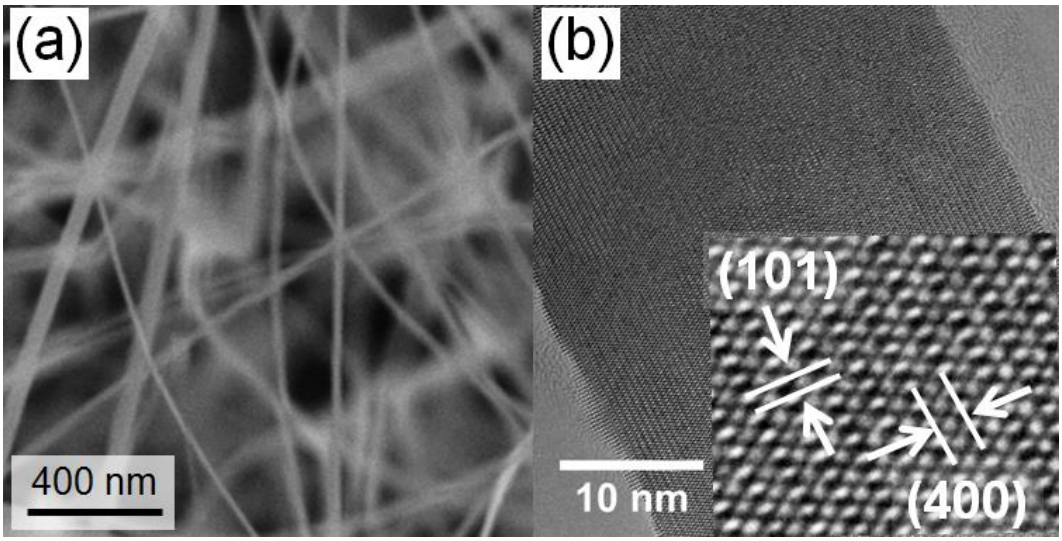

Figure 3.16 (a) SEM image of a bundle of SnO_2 nanowires on the 2 Å gold thin film coated on silicon wafer; (b) HRTEM of an individual SnO_2 nanowire showing the single crystalline nature over large distances. The inset shows a higher resolution with the [101] growth direction of the tetragonal rutile lattice of SnO_2.

As discussed in section 3.1.2, it is possible to obtain ultra-thin nanowires, when functionalized gold nanoparticle dispensed Si substrates are used for the growth. The SEM image in Figure 3.17 (a) shows the morphology of these nanowires which are considerably thinner and shorter than the nanowires grown from MBE/made catalysts which are shown

in Figure 3.16 (a). Again, the HRTEM imaging shown in Figure 3.17 (b) confirms that the nanowires are single crystalline and free from any defects.

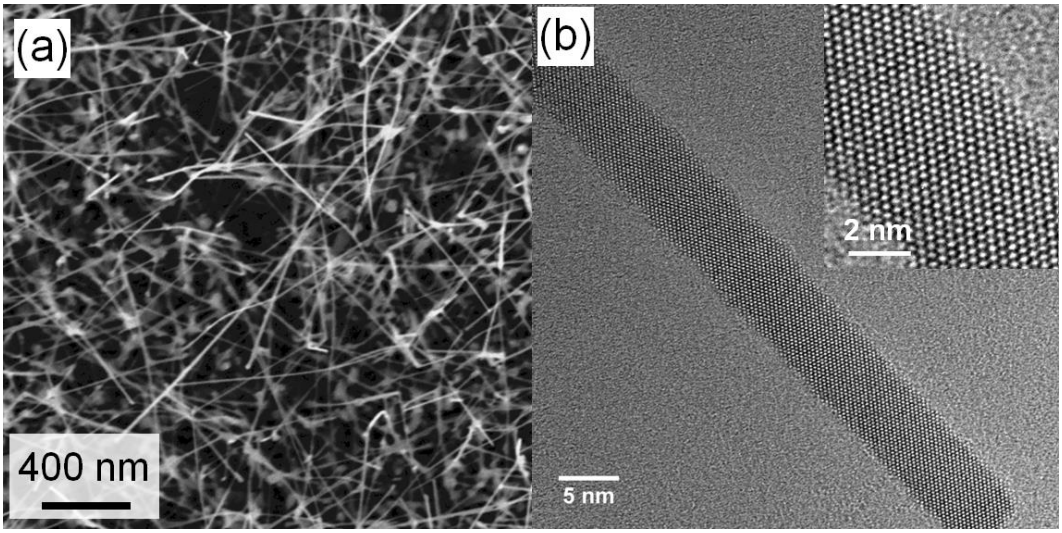

Figure 3.17 (a) SEM image of a bundle of SnO_2 nanowires on a substrate covered with gold on a silicon wafer; (b) HRTEM of an individual SnO_2 nanowire showing the [101] growth direction of the tetragonal rutile lattice of SnO_2.

To confirm the VLS growth mechanism the bulged tips of the nanowires were analyzed qualitatively with transmission electron microscope energy dispersive X-ray spectroscopy (TEM-XEDS). As shown in Figure 3.18 (a), the catalyst at the tip of the nanowire is clearly discernible and one can acquire a X-ray spectrum from the catalyst by focusing the electron beam on the tip of the nanowire. The EDX data shows strong signals of Sn, Au and Cu in the spectra as depicted in Figure 3.18 (b). The presence of Cu can be related to the use of a copper grid as the sample holder. Since the growth process is stopped abruptly after a specific time, there is still considerable amount of Sn in the gold nanoparticle at the tip of nanowires.

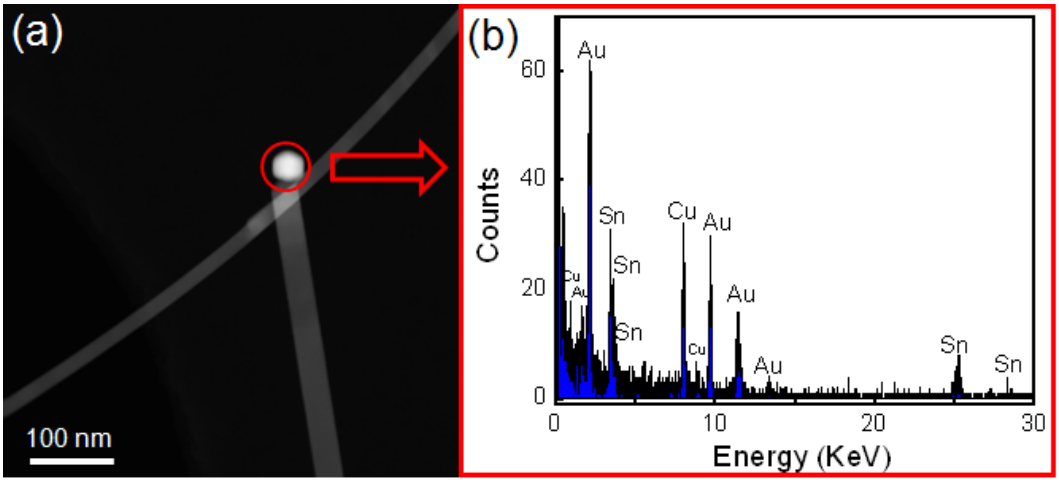

Figure 3.18 (a) TEM image of an individual SnO_2 nanowire showing a catalyst on the tip of the nanowire (b) EDX spectrum of the tip region.

3.2.3 Synthesis of In_2O_3 nanowires

Indium oxide (In_2O_3), as a wide band gap semiconductor with a direct band gap of 3.6 eV and indirect band gap of about 2.6 eV, has attracted much attention owing to its distinctive optical, chemical, and electronic properties and its importance for applications in solar cells,[148] biological sensors,[149] gas sensors, field emission[150] and optoelectronics, etc.[151, 152] In this context, there is increasing interest in the synthesis and investigation of the properties of low-dimensional In_2O_3 structures. Already various In_2O_3 nanostructures have been fabricated by vapor and solution routes, such as nanotubes,[153] nanowires,[154] nanorods,[155] nanobelts,[156] nanoflowers, nanosheets,[157] nanocubes,[158] and nanopyramids.[159]

Two parallel procedures, based on VLS mechanism with different conditions, are adopted to synthesize different nanostructures including microtowers, nanotowers, nanopillars, nanopyramids, nanorods and nanowires. The synthesis conditions are given in table 3.2. In **procedure A**, five silicon wafers coated with 4 nm gold films were placed downstream at a distance of 5, 10, 30, 60 and 90 mm, called A1 to A5, respectively. Prior to the thermal reaction, a carrier gas (Ar with purity of 99.9999) at a flow of 100 sccm under a pressure of 10 mbar was introduced into the system for 45 min. Keeping the flow and pressure unchanged, the reactor was loaded in the preheated furnace at 900 °C. The temperature instantly dropped to 850 °C and was subsequently ramped up to 900 °C in 5

min. Next, the reactor was pulled out after 2 hrs and cooled down to room temperature while the carrier flow and the pressure remained unchanged. After reaction, a layer of yellowish product was found on the silicon wafers. In **procedure B**, the synthesis root is the same as in procedure A, however the flow, gas carrier, pressure, reaction temperature, time and thickness of gold thin film on the substrate were changed to 10 sccm of 99 % Ar and 1 % O_2, 1 mbar, 930 °C, 10 min and 0.2 nm respectively. For simplicity, the substrates are referred to as B1 to B5 for the downstream location at a distance of 5, 30, 70 and 100 mm, respectively.

The morphologies of the obtained nanostructures were characterized by scanning electron microscopy (SEM). Figure 3.19 shows a low-magnification image of as prepared products in experiment A, which reveals how different nanostructures are achievable depending on the distance of the substrates from the source. Microtowers, nanopyramids were observed on the substrates (i.e. A1, A2 and A3) which were placed at a distance of 5 to 30 mm from the source (Figure 3.19 (a-c) and Figure 3.20 (a-c)). A type of irregularly tapered nanotower is found on the substrate (A4) positioned at 60 mm from the source (Figure 3.19 (d) and Figure 3.20 (d)) and finally a nanorods structure is obtained on the last substrate (A5) which is placed 90 mm from the source as shown in Figure 3.19 (e) and 3.20 (e) and (f).

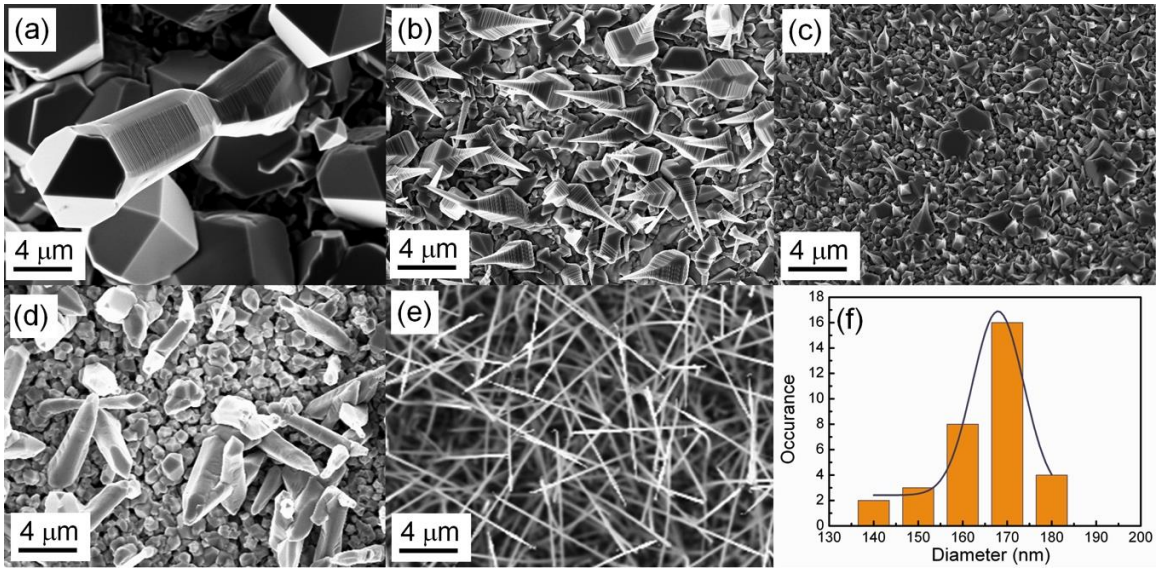

Figure 3.19 Low magnification SEM images of a) microtowers, b and c) nanopyramids d) tapered nanotowers e) nanorods and f) Size deviation of nanorods diameter. (Figure a, b, c, d, e are corresponding to the substrates A1 to A5, respectively)

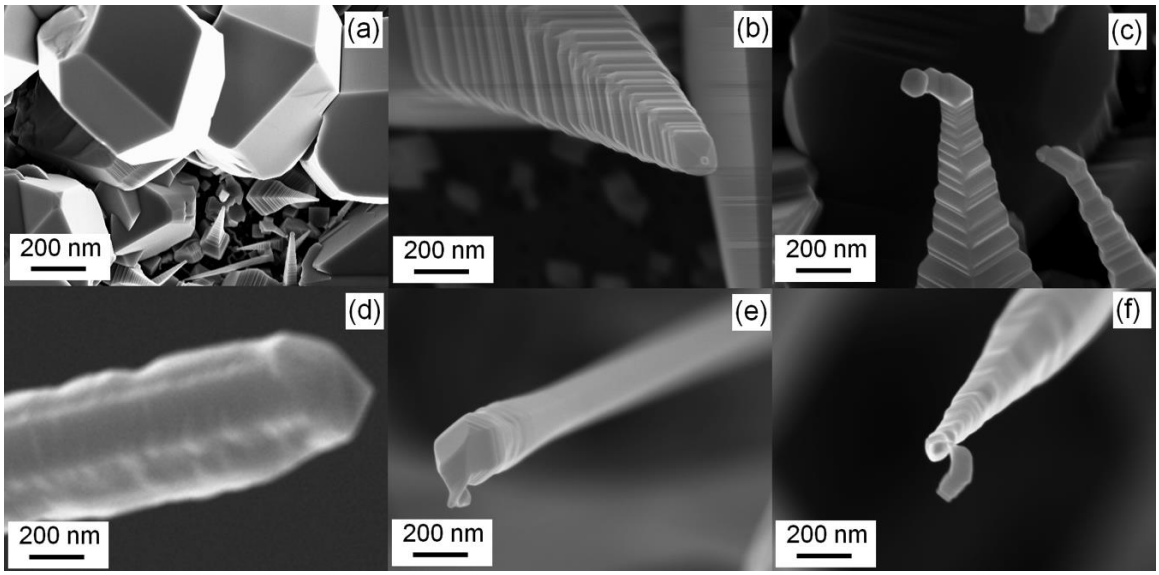

Figure 3.20 High-magnification SEM images a) microtowers b and c) nanopyramids d) nanotower e and f) nanorods which give close-up images of the tip and body of the nanostructures. (Figure a, b, c, d and e & f are corresponding to the substrates A1 to A5, respectively)

The average size of the nanorods (on A5 substrate) is calculated to be of 173 nm and their diameter size distribution is shown in Figure 3.19(f). The high resolution SEM images (Figure 3.20) show that there is a particle on the tip of every nanostructure except for microtowers and nanotowers as indicated in Figure 3.20 (a) and (d).

High-resolution SEM images (Figure 3.20 (a), (c) and (d)) also reveal that the nanopyramids consist of many layers of linked octahedral segments with a truncated bottom and a tip ended with an imperfect octahedron cap. While, catalyst particles can be seen at the tip of the nanopyramids, the gradual increasing size from the tip to the bottom and the segmented appearance of the truncated octahedrons along the growth direction could not be satisfactory explained by the VLS mechanism. In this regard, it can be noted that Yan *et al.* has proposed that one dimensional growth is usually controlled by a VLS mechanism and the lateral growth is controlled via a vapor-solid (VS) mechanism.[160]

The carbothermal reduction process generates liquid and vapor phases of the indium species via the simplified set of reactions:[161, 162]

$$In_2O_3\ (s) + C\ (s) \rightarrow In_2O\ (v) + CO_2\ (v) \qquad (3.6)$$

Since no oxygen is introduced into the system separately the reaction which may result in epitaxial growth of In_2O_3 nanowires is as follows:

$$In_2O\ (v) + 2In_2O\ (v) \rightarrow In_2O_3\ (s;\ nanowire) + 4In\ (l) \qquad (3.7)$$

In this procedure not all the vapor species are incorporated in 1-D growth through the gold catalyst but also some are adsorbed on the surface of the growing nanostructures. When the gold catalyst is supersaturated with growth species, the precipitation and the oxidization took place successively which results in 1-D growth while at the same time part of the In vapor was transported onto the side plane and resulted in the radial and epitaxial growth of the nanostructures.

The vapor pressure and surface energy have surely played an important role in controlling the resultant nanostructure morphology. Higher supersaturation of vapor species (due to their higher vapor pressure) can be expected in the vicinity of the central heating zone. Consequently, around the substrate A1 which is close to the source, the vapor pressure of indium was much higher than the vapor pressure around the substrate A5, which was farther away from the source. On the other hand, the crystallographic structure of In_2O_3 is bcc and three of its low-indexed planes have a growth rate relationship of $r_{<111>} < r_{<100>} < r_{<110>}$ according to $\gamma_{\{111\}} < \gamma_{\{100\}} < \gamma_{\{110\}}$ (γ is the surface energy), the reason for the one dimensional growth of the oxide.[163] Although, the difference of surface energies among {110}, {100}, {111} facets can lead to their different growth rates, the high vapor pressure at the vicinity of the source diminishes the effect of the surface energy difference on the growth. As a result, the crystal growth rates perpendicular to {111}, {100}, and {110} facets become comparable to the octahedron growth model as shown in Figure 3.21. This explains the geometry of the constituent segments of the nanopyramids having a shape of truncated octahedron.[160] The competitive growth of vapor species at the interface of solid–liquid (catalyst droplet and In_2O_3 segment) and epitaxial growth on the surface of the nanostructure will induce the formation of this kind of nanopyramids. The increasing size of the nanotower from tip to bottom is attributed to the different growth time. The segments produced in the early stages at the bottom part are exposed to vapor species longer than those recently produced and therefore possess a larger size.

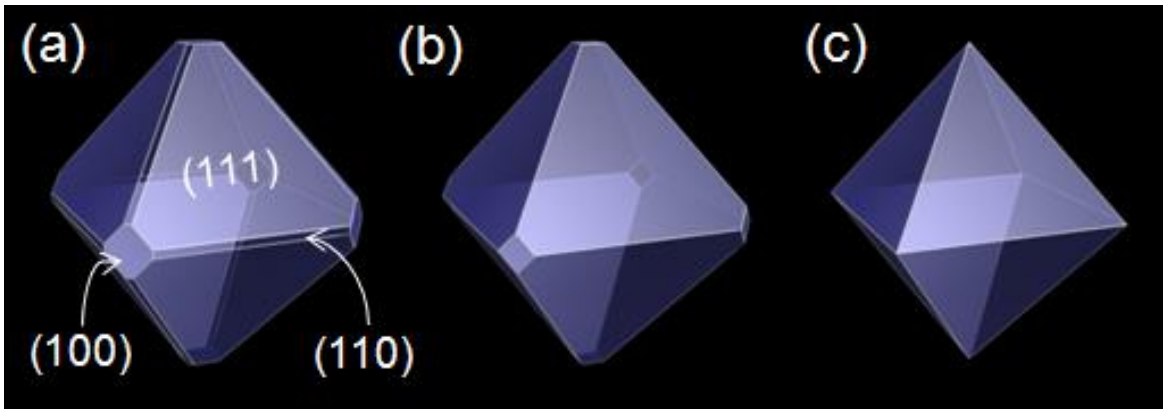

Figure 3.21 A schematic image of a) truncated octahedron with three crystallographic facets b) truncated octahedron with two crystallographic facets and c) perfect octahedron one set of crystallographic facet as a model for VS lateral growth of In_2O_3 pyramids.[164]

In case of microtowers and nanotowers which are found on the substrates A1 and A4 (Figure 3.19 (a) and (d)), no catalyst particle was observed on their tip (Figure 3.20 (a) and (d)). A plausible reason could be that the octahedral particles can also be deposited on the silicon wafer and lead to both one dimensional and lateral growth via self-catalytic VLS and VS mechanism, respectively, without any contribution from the gold catalyst nanoparticles. In this complex mechanism, the abundant indium vapor can be deposited onto the gold particles on the silicon substrate and due to the high supersaturation of indium, the formed particles are found to be indium rich. In this process gold nanoparticles may just play the role of potential deposition sites but may not contribute to the VLS mechanism. The absorbed species transported from the vapor phase, maintained the growth of the particles and considering the growth rate relationship of $r_{<111>} < r_{<100>} < r_{<110>}$, the low-energy planes {111} can be expected to be the facets of the octahedra at tip of the micro and nanotowers.

While the reaction is taking place, abundant reagent species absorbed onto the truncated octahedron under VS mechanism leading to lateral growth while part of the absorbed species is transferred to the (100) plane to maintain the 1D growth along the [100] crystalline direction. This mechanism results in the production of micro- or nanotowers as well as nanopyramids.

Once indium nucleation occurred either in the catalyst droplets or on the silicon surface and at high indium vapor pressure, there was a high chance of 3-D growth (1-D +

lateral). When moving away from the source, where the In vapor pressure becomes lower, nanorods appeared to prevail with minimum lateral growth (Figure 3.19 (e)).

Nanorods with two different geometries at their tips are distinguishable in the high resolution SEM images in Figure 3.20 (e) and (f) corresponding to the SEM image in Figure 3.19 (e) which has been taken from the substrate (A5) in procedure A. It can be seen that diameter of both types of nanorods have a uniform size along the entire length except the tip, which in one case (Figure 3.20 (f)) exhibits a gradually increasing size from the tip to the bottom and the other one is tapered. The presence of spherical particles at the tip of each nanowire proves that the growth mechanism is according to the VLS mechanism. The results of the EDX analysis performed to obtain the composition of the catalysts and the existence of indium and gold at the tip of a nanorod is demonstrated in Figure 3.22.

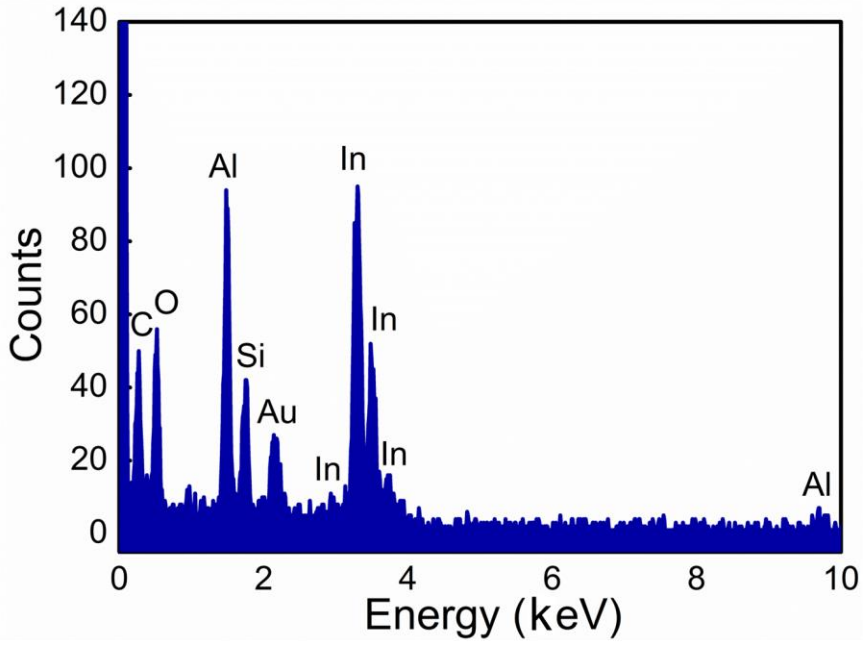

Figure 3.22 EDX spectrum of the catalyst on the tip of a single In_2O_3 nanorod showing the In-K_α, Al-L_α, O-K_α lines.

The morphology of the nanostructures grown on 0.2 nm MBE coated gold thin film in the procedure B are shown in Figure 3.23. Nanopillars with a rectangular cross section have grown on the substrate closest to the source as indicated in Figure 3.23 (a). The significant lateral growth can again be explained by the VS mechanism. Relatively thin nanowires and a few thick nanorods were obtained on the other three substrates. A closer

look also reveals that the nanowires possess a rectangular cross section (i.e. inset of Figure 3.23 (c)). In procedure B, additional substrates decorated with gold nanoparticles were loaded in the reactor beside the aforementioned substrates. As shown in Figure 3.24 only sporadic nanostructures including nanocubes and few nanorods were found on these substrates at a low yield. This result implies firstly that the nanowire growth on 0.2 nm gold substrate follows the catalyst mediated VLS mechanism and secondly, the growth of nanowires depends on the thermodynamic limit determined by the minimum radius of the metal-liquid droplets.[165]

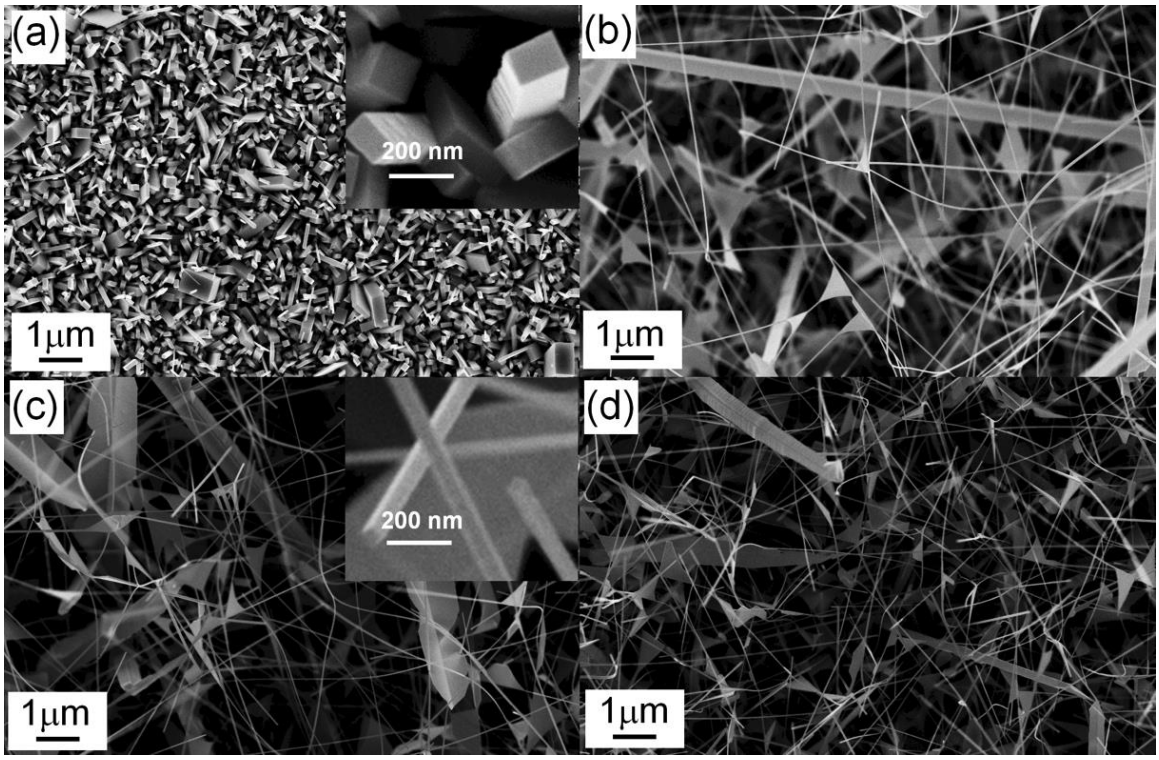

Figure 3.23 Low magnification SEM images (high magnification is shown as inset) of a) nanocubes on the first substrate b-d) nanowires on the second to forth substrates

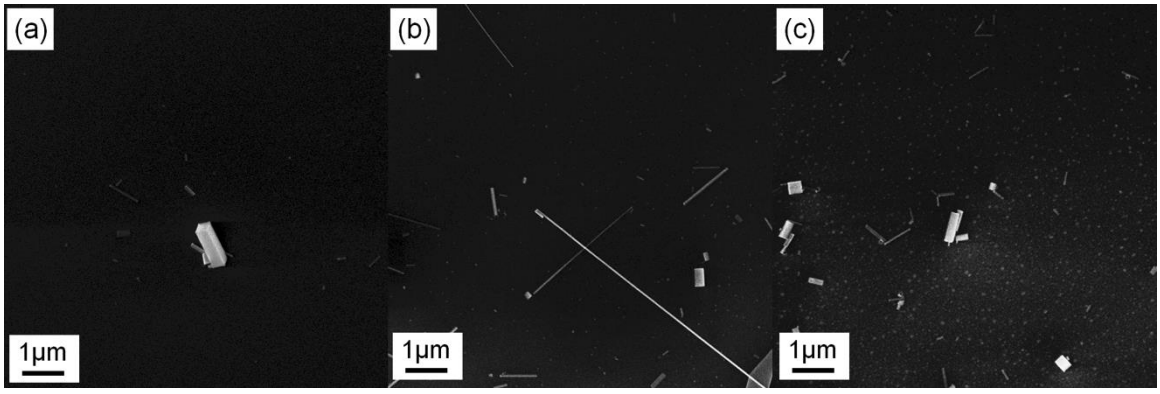

Figure 3.24 Low magnification SEM images of gold nanoparticle decorated substrates a) nanocubes on the first substrate b-d) nanowires on second and third the substrates

The average diameter of the nanowires are calculated to be 45 nm and 40 nm for the closest (B2) and farthest substrate (B4), respectively. The diameter size distributions of the nanowires for these two samples are shown in Figure 3.25. As mentioned before the presence of thicker nanowires is due to tendency towards lateral growth under higher indium vapor pressure.

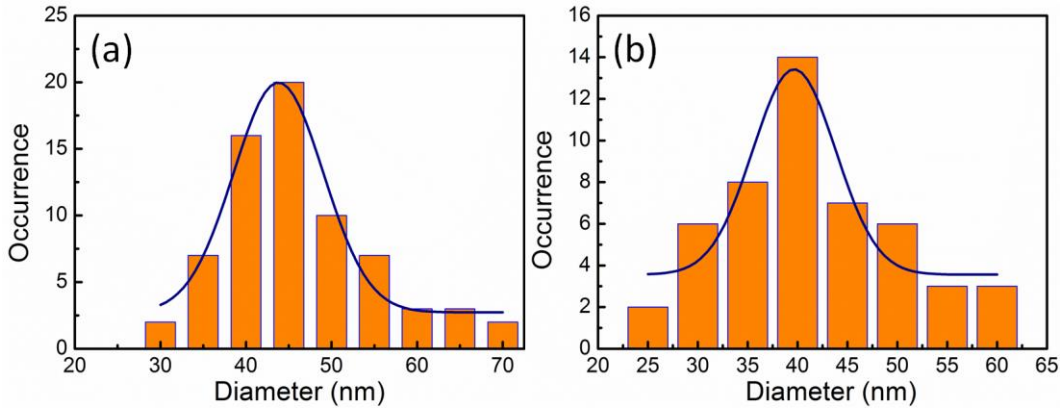

Figure 3.25 Diameter size deviations of nanowires for a) nanowires grown on substrate B2 b) nanowires grown substrate B4

Grazing incidence X-ray diffractometry (GIXRD) measurements were performed to probe the crystal structure and phase purity of the In_2O_3 nanowires. This method was chosen to avoid any reflection from the silicon substrate. Figure 3.26 shows a typical XRD pattern of the In_2O_3 nanowires on Si substrate. All the sharp diffraction peaks can be indexed to a

body-centered cubic (bcc) structure which is consistent with the bulk cubic-In_2O_3 (ICSD 050846) and no other impurity peaks were detected.

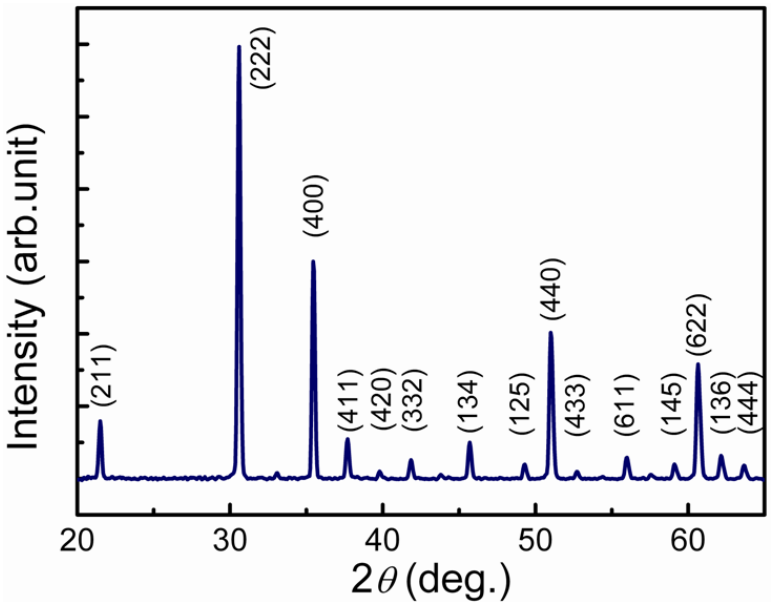

Figure 3.26 GIXRD spectra of the harvested In_2O_3 nanowires

HRTEM image of a single In_2O_3 nanowire is shown in Figure 3.27 (a). It reveals that the spacing of the two vertical group crystallographic planes are all 0.252 nm, which correspond to the (400) and (040) planes of body-cubic In_2O_3. Fast Fourier transform (FFT) of the HRTEM image shown in Figure 3.27 (b) confirms the growing direction of In_2O_3 nanowires along [100].

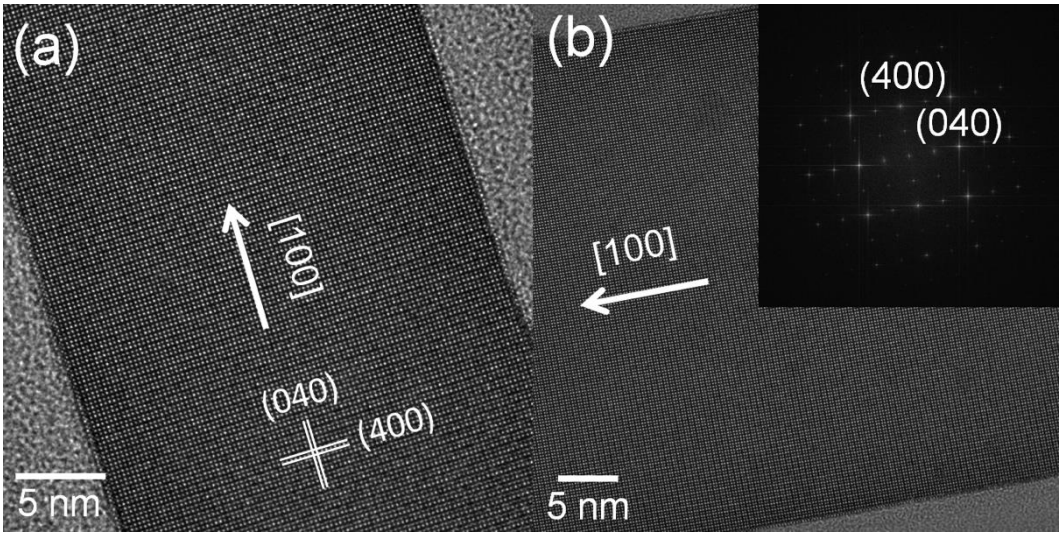

Figure 3.27 (a) HRTEM images of a nanowire with higher resolution showing the lattice fringes. (b) HRTEM images of the In_2O_3 nanowire (The inset is the corresponding FFT pattern of the nanowire)

3.3 Doped nanowires (ITO)

In the present studies the metal oxide nanowires are typically not intentionally doped, and the charge carriers are normally generated by structural defects such as oxygen deficiencies. As a result, the nanowires behave as wide band gap semiconductors.[69] Of course, intentional doping can greatly modify the device properties and lead to new device applications. One such example is tin-doped indium oxide (ITO), in which metal-like behavior is achieved when In_2O_3 is degenerately doped by Sn. Due to its high conductivity and high transmittance in the visible spectral region,[166] ITO has become by far the most important transparent conducting oxide material, and ITO films have found applications in various optoelectronic devices such as flat panel displays,[136] solar cells,[167] and light-emitting diodes.[168] However, the homogeneous introduction of dopants into the lattice while preserving the structural integrity of the nanowires is still a major challenge in the synthesis of metal oxide nanowires. Therefore, the ability to produce highly crystalline ITO nanowires may potentially further enhance the performance of integrated electronics by using these nanowires as electrodes.

The ITO nanowires were synthesized on (100) Si substrates by a catalyst-mediated vapor-liquid solid (VLS) process in which the Sn and In source materials were provided by a

vapor transport method. Indium powder (99.99%, Sigma Aldrich) and tin powder (99.8% , Sigma Aldrich) with weight ratio of 9:1 were first mixed thoroughly using a mortar inside a glove box with an argon atmosphere and loaded in an alumina crucible. As the source materials can easily be oxidized, the reactor chamber was sealed in the glove box and transferred into a horizontal tube furnace. The rest of the preparation set-up is similar to the previous ones mentioned already. Details are given in table 3.2.

The crystal structure of the as-synthesized nanowires was analyzed by GIXRD. Four major diffraction peaks, as shown in Figure 3.28, are found. These are indexed as (222), (400), (440) and (622) crystal planes of a cubic structure with a lattice constant of a = 1.01 nm (from ICSD 050846). It should be noted that the peaks of SnO_2 or any other spurious phase were not observed.

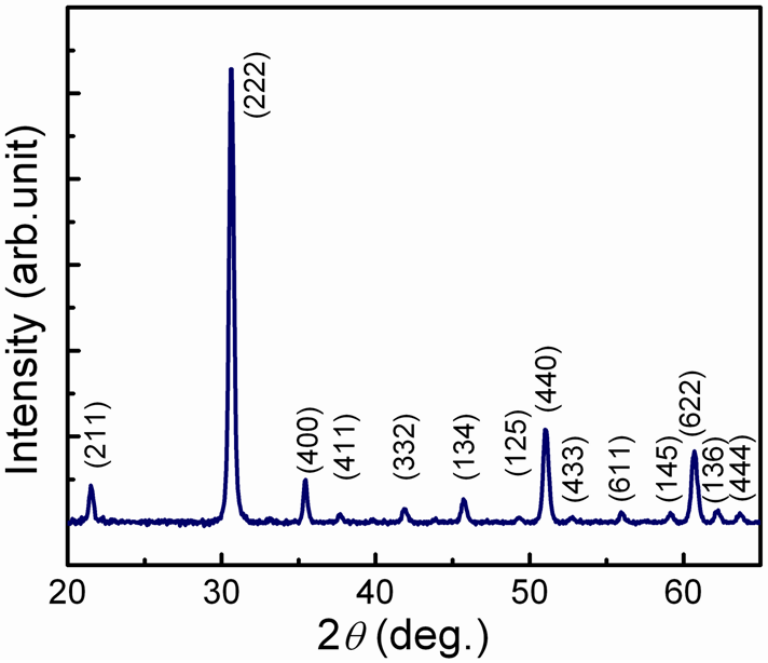

Figure 3.28 GIXRD spectra of the as-synthesized Sn doped In_2O_3 (ITO) nanowires

Figure 3.29 (a) shows a typical SEM image of the as-synthesized material on the Si substrate, showing the general morphology with nanowires of diameters in the size range from 20 to 35 nm (Figure 3.29 (b)) and lengths of several micrometers. On examination with SEM, spherical-shaped particles are found at the tips of the ITO nanowires, some of which

are marked with red arrows in Figure 3.29 (a). This observation is a clear evidence that the growth of ITO nanowires is controlled by the VLS mechanism.

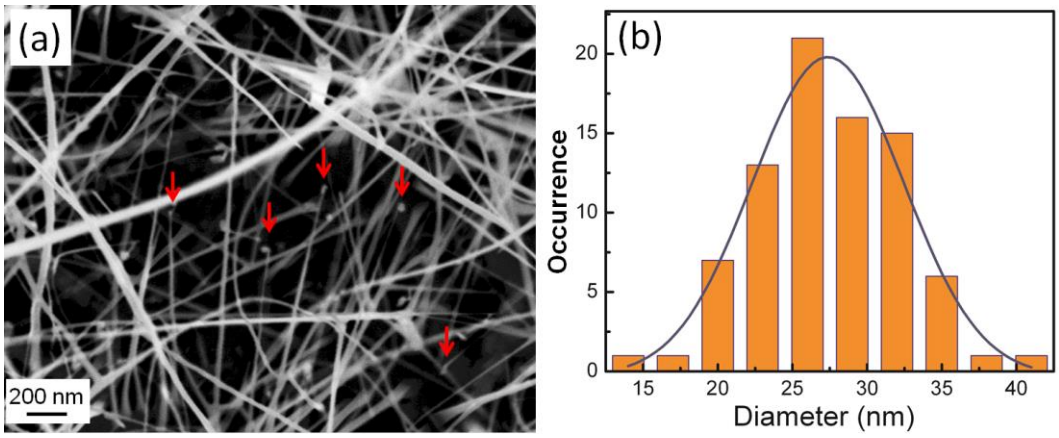

Figure 3.29 a) SEM image of Sn doped In_2O_3 nanowires prepared via VLS mechanism b) distribution of the diameters of the nanowires

The high crystallinity of the ITO nanowires is further confirmed by HRTEM analysis. Figure 3.30 (a) shows HRTEM image which reveals a perfect single crystalline single ITO nanowire with an interplanar spacing of 0.253 nm grown in the [100] direction.

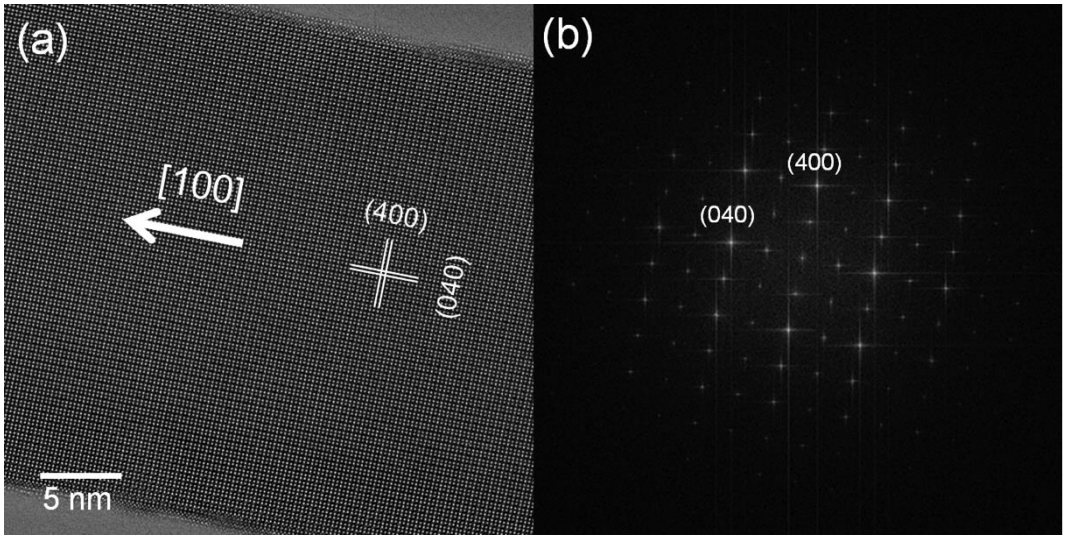

Figure 3.30 a) HRTEM images of the ITO nanowire; b) the corresponding FFT pattern of the nanowire

In order to check whether Sn is actually incorporated in these nanowires, the EDX analysis was performed in STEM mode to examine the composition of individual nanowires.

Figure 3.31 shows the EDX spectra from the two selected areas on the nanowire. Figure 3.31 (a-b) show spectra acquired from two selected rectangular areas along the nanowire, one at the edge and the other at the center to evaluate the doping concentration as well as any possible elemental segregation on the surface of the nanowire. EDX analysis shows that the nanowire contain In, Sn, and O, Au and Si with the composition In/Sn atomic ratio of 87.7:12.3 and 85.8:14.2 at the middle and edge of the nanowire, respectively. The Au and Si peaks come from the gold grids and the Si substrate where nanowires are grown. The TEM sample was prepared by tapping the substrate onto the grid which may have caused falling of a few Si fragments on the TEM grid. The evaluated atomic ratios of In/Sn are almost the same all around the nanowire.

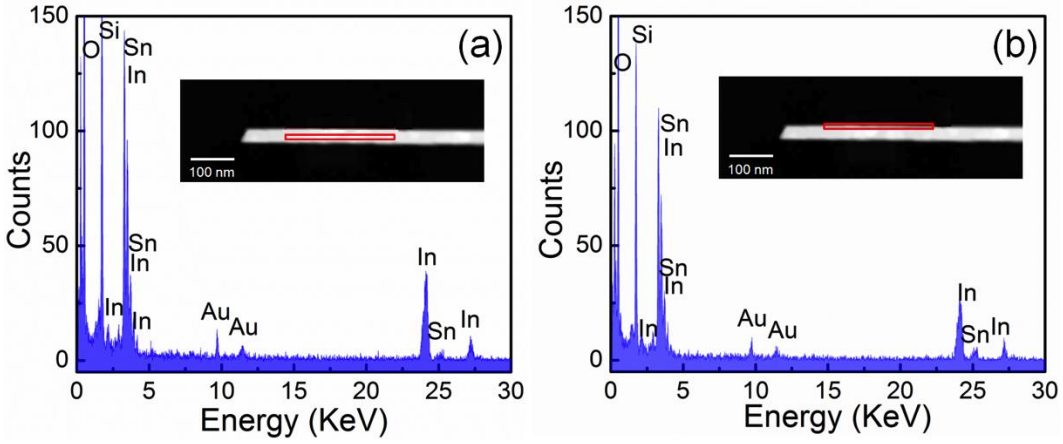

Figure 3.31 EDX spectrum of the catalyst on the (a) middle and (b) edge of a single Sn doped In_2O_3. The inset shows the surveyed area

Chapter 4

Preparation of nanowire electrochemically gated FETs

4.1 Device preparation

In order to build the nanowire based, electrochemically-gated field-effect transistors (EG FETs), the as-grown nanowires were transferred from the growth substrate (donor) onto the oxygen plasma-cleaned receiver (Si/SiO_2wafer) substrate. The receiver substrates were previously patterned with electron beam lithography (EBL) using alphabetically signed polygonal shaped markers. Thus, several individual nanowires could be selected and their positions could easily be addressed using SEM.

The substrates were cleaned using reactive ion etching, RIE, (Oxford Instruments, Plasmalab 80 Plus) under oxygen plasma atmosphere at room temperature. The etching pressure, gas flow, power and etching duration were 0.13 mbar, 10 sccm, 30 W and 2 min, respectively. After transferring and addressing the desired nanowires, 200 nm poly(methyl methacrylate), PMMA , (A4.5 950k, Allresist) was spin coated on the receiver substrate as an e-beam resist and subsequently cured at 165 °C for 30 min. Next, EBL was used to design and pattern the passive structures onto the addressed nanowires. The EBL written samples were developed using methyl isobutyl ketone (MIBK) to solve and remove the e-beam exposed part for metallization. Two deposition techniques were used in order to build the passive structures from suitable materials which could provide excellent electrical contacts to the nanowires. In this context, a brief definition of semiconductor-metal ohmic contact is given. Ohmic contact is defined as a metal-semiconductor contact in which there is an unrestricted transfer of majority carriers from one material to another, i.e., the contacts have

negligible resistance compared with the total resistance of the device and do not limit the current. In the first case, DC sputtering was employed to deposit tin doped indium oxide (ITO) at room temperature with an approximate thickness of 30 nm onto the nanowires in order to ensure ohmic contacts with the ZnO nanowires. The deposition parameters, such as DC power, working pressure and argon flow, were selected to be of 100 W, 0.001 mbar and 30 sccm, respectively. These deposition conditions and parameters were chosen as optimum growth conditions for preparing the ITO thin films with minimum resistivity of 2.7×10^{-4} Ωcm. In the other technique e-beam evaporation was used to deposit Ti/Al metals with an approximate thickness of 5/40 nm onto the SnO_2 nanowires. The Ti and Al crucible temperatures were set to nominal values of 1640 °C and 1150 °C, respectively; hence, the deposition rate of 0.25 nm/min and 4 nm/min was established for Ti and Al correspondingly. The substrate was cooled down by flowing liquid nitrogen and kept always around -130 °C to avoid any agglomeration of deposited Al clusters on the substrate to attain a uniform thin film. The base pressure and deposition pressure were around 10^{-10} mbar and 10^{-9} mbar.

Table 4.1 Working functions of the deposited metals and semiconducting channels

Materials	Work function (eV)	Ref.
Ti	4.33	[169]
Al	4.28	[170]
ITO	3.5-4.3	[171]
n-SnO_2	4.7-5.7	[172]
n-ZnO	4.45	[173]

According to Table 4.1, the contact between ZnO and ITO is ohmic since the work function of ZnO is smaller than the work function of the metallic ITO ($\Phi_{ITO}<\Phi_{ZnO}$) and similarly for the contact between SnO_2 and Ti as $\Phi_{Ti}<\Phi_{SnO2}$.

The contact electrodes, such as the *source*, the *drain* and the *in-plane gate* electrodes are constructed in the way that the distance between the *source* and the *drain* electrode is usually kept around 1-2 μm whereas the distance of the *gate* electrode from the nanowire channel is maintained at approximately 10 μm. At the next step the remaining e-beam resist (PMMA)

was lifted off using acetone as a remover and ultrasonication for 1 min. At this stage, the nanowires had ohmic contact with the electrodes and were ready to be introduced to the printer for electrolyte printing. The schematic image as well as optical picture of the device is shown in figure 4.1.

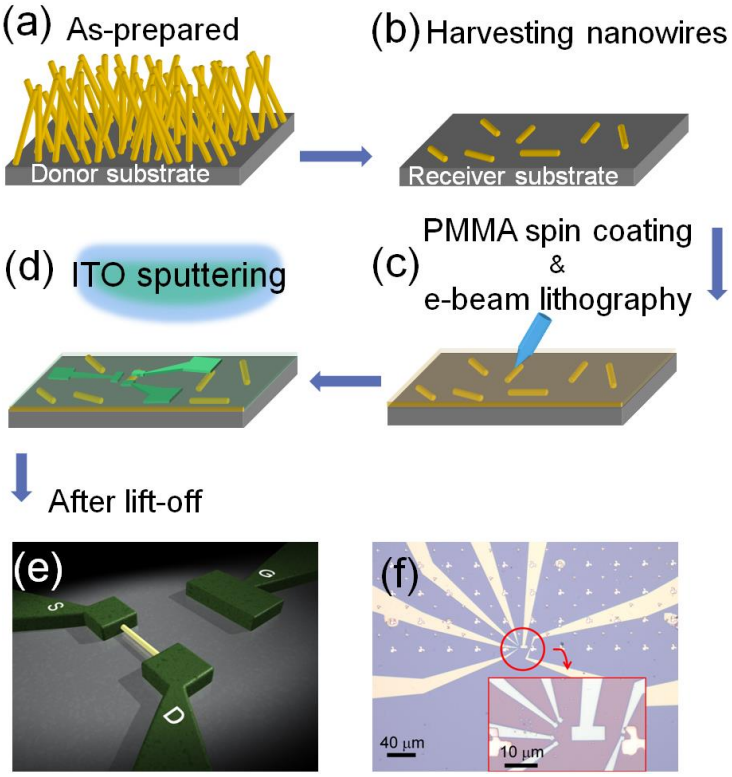

Figure 4.1 Schematic representation of the device preparations steps; a) as-prepared nanowires on a donor substrate; b) the nanowires are transferred to the receiver substrate by simple physical contact method; c) spin coating of PMMA as the positive resist to perform e-beam lithography; d) after the development, the electrodes are deposited by ITO sputtering; e) and f) the schematic and optical view of the device geometry after the lift-off

4.2 CSPE synthesis and printing

A new approach was introduced in order to have both electrolytic-gating and all-solid-state device simultaneously. This has been accomplished by utilizing a composite solid polymer electrolyte (CSPE) as the gate-insulator for the transparent conducting oxide (TCO) single nanowire transistors which resulted in low voltage operation and high performance, at the same time. CSPE, used as the gate insulator, is composed of synthetic polymer

(poly(vinyl alcohol) (PVA), average mol. wt. = 13.000-23.000) 98% hydrolysed, Sigma-Aldrich), a plasticizer (propylene carbonate (PC), anhydrous, 99.7%, Sigma-Aldrich), a supporting electrolyte/salt (lithium perchlorate, $LiClO_4$, anhydrous, 98% Alfa Aesar) and a solvent (dimethyl sulfoxide, DMSO, anhydrous 99.9% Sigma-Aldrich). All of these are used as received and without any additional purification. In order to prepare the CSPE, first PVA was added to DMSO and the solution was then stirred and heated continuously to 80-100 °C for several hours until the mixture became a homogeneous sol. Then lithium perchlorate was dissolved in PC and added to the PVA solution. The complete mixture was then stirred at room temperature for at least 12-24 hours to obtain a completely single phase, clear and homogeneous solution (liquid electrolyte) which was ready for dispensing/solution casting/printing. For the optimum performance of the polymer gel electrolyte, the PVA:PC:$LiClO_4$ ratio was kept at 30:63:7. In order to ensure easy printability, the weight of DMSO was usually taken 5-6 times larger compared to the total weight of all other components together.

The electrolyte was usually dispensed or ink-jet printed in the liquid form and was solidified by evaporation of the excess solvents. Because of the high boiling point of the DMSO and PC, the room temperature vapor pressures are low; consequently, a significant amount of solvent remains trapped inside the polymeric network in the dried form of the electrolyte. This effect in turn results in a high value of conductivity of the solid polymer electrolyte of about 10^{-2} S/cm.[174]

A Dimatix DMP 2831 ink-jet printer with piezoelectric nozzles and nozzle diameter of 21.5 μm is used to print the electrolyte on the channel of the device. The printed droplet always covered the nanowire channel completely and the in-plane gate electrode partially. For experimental simplicity all the transistors reported in this study were prepared as in-plane FETs, as shown in Figure 4.2.

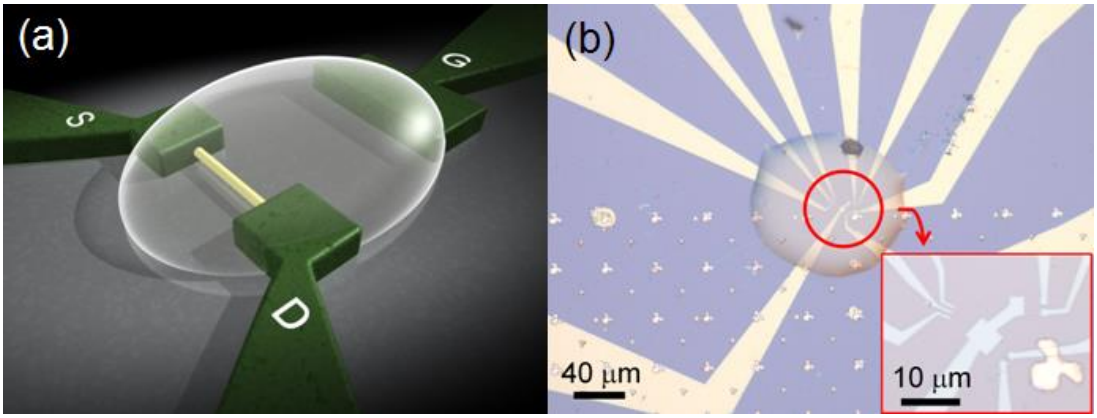

Figure 4.2 a) schematic and b) optical view of the EG FET device after ink-jet printing of the CSPE which covers the nanowire transistor channel completely and the gate electrode partially

Chapter 5

Electrical characterization of electrochemically-gated nanowire FETs

5.1 Static characterization

5.1.1 SnO_2 single nanowire EG FETs

The transistor characteristics of an electrochemically-gated single SnO_2 nanowire field-effect transistor (EG FET) are presented in Figure 5.1. These electrical measurements were carried out at room temperature (25 °C) and under ambient conditions. As can be seen from the transfer curve (Figure 5.1a), the nanowire-channel FET's show a behavior similar to an *accumulation-mode* n-type metal-oxide-semiconductor field-effect transistor (MOSFET) with excellent transistor characteristics.

At zero gate bias, a complete *Off*-state is recorded around zero gate voltage (V_{ON} ~ 0.24 V) with an *Off*-current much less than one picoampere. Owing to the high *double-layer capacitance* of the electrolyte, a large *On*-current of several microamperes can be driven even though the applied gate voltage is always limited to ≤ 2 V.

On the other hand, this constraint in applied gate voltage prevented any faradaic currents from flowing through the gate which, in fact, makes it similar to a regular electrochemical capacitor. This fact is further supported by the excellent insulating property of the electrolyte with only ultra-low and ideal capacitor-like constant gate currents (I_G) of few tens of picoamperes (Figure 5.1a).

The specific transconductance ($g_m = dI_D/dV_G$) is found to be extremely large, 714 μS/μm, the sub-threshold slope ($S = dV_G/d(\log I_D)$) is defined as the gate voltage that is necessary to alter the drain current by one order of magnitude is calculated to be only 74 mV/decade. Such a high *transconductance* and a small value of *sub-threshold slope* indicate extremely high field-induced mobility of the single-crystalline channel of the nanowire transistor and quite efficient gating by the CSPE; a direct result of an atomically smooth channel-insulator interface which is typical of electrolytic insulators. The *threshold voltage* (V_T) of all the measured FET's was always positive (accumulation-mode operation), while the V_T of the device presented in Figure 5.1a is calculated to be 0.63 V.

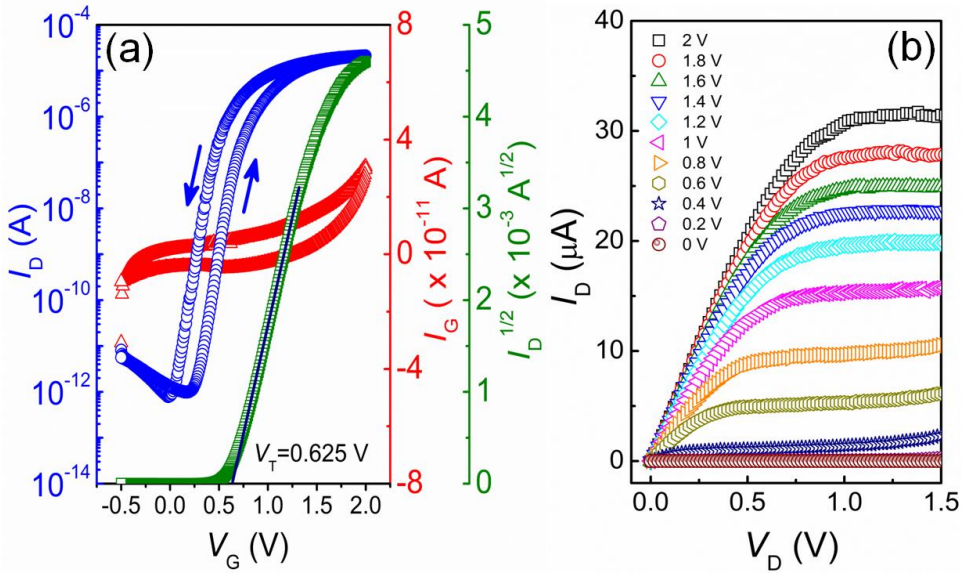

Figure 5.1 (a) Transfer characteristics of a typical SnO_2 nanowire channel EG FET device, the applied drain voltage is V_D= 0.5 V, the blue circles, the green squares and the red triangles represent the *drain current*, the square root of the *drain current* and the *gate current*, respectively. The *threshold voltage* (V_T) is calculated to be 0.625 V; (b) *drain current-drain voltage* (I_D-V_D) output characteristics of the same device, measured with V_D up to 1.5 V, while the *gate voltage* (V_G) is varied between 0 to 2 V in every 0.2 V steps.

Figure 5.1b shows *drain current-drain voltage* characteristics of the SnO_2 nanowire EG FET, where the *gate voltage* (V_G) is varied between 0 to 2 V and the *drain voltage* is swept from 0 to 1.5 V. The output characteristic reveals current saturation (~ 30 μA) at high V_D and an excellent linear behavior at low V_D indicating low resistance of the ohmic contacts formed between the SnO_2 nanowire and metallic (Ti) *source/drain electrodes*.

Field-effect mobility (μ_{FET}) of a transistor at its saturation regime ($V_D > V_G - V_T$) can be calculated from the following equation which has been derived from equation (2.3):[59]

$$\mu_{FET} = \frac{I_D \times 2L}{W \times C_{DL} \times (V_G - V_T)^2} \tag{5.1}$$

where L, the channel length; W, the channel width; I_D, the *saturated drain current* at the *gate voltage* V_G and V_T, the *threshold voltage*. For the presented EG FET device, the *specific capacitance* of the dielectric (C) in equation (4.1) is considered to be equal to the *double layer capacitance* (C_{DL}) of the electrochemical capacitor. C_{DL} has been calculated with the cylindrical capacitor model which is composed of the nanowire and is surrounded by the solid polymer electrolyte:[118]

$$C_{DL} = \frac{2\pi\varepsilon_0\varepsilon_r L_G}{\ln(1+\frac{l}{r})} \tag{5.2}$$

where, ε_0, the permittivity of the free space, ε_r, the dielectric constant of the electrolyte solvent, r, the radius of the nanowire and l, the dielectric thickness of the electric double layer (EDL) which can be considered to be 1 nm unless it is for an extremely diluted electrolyte which is definitely not the case here.[175–177] The dielectric constant of the solvent of the electrolyte is taken to be 5, because Dzhavaichidze *et al.*[178, 179] have shown earlier that regardless of the bulk dielectric constant, the dielectric constant of a solvent/medium very close to a solid (electrode) surface (at the vicinity of EDL) reduces to 5. A simple test is performed in order to experimentally support their conclusion. Two identical (identical electrode size, geometry and inter-electrode distance) electrochemical cells are constructed with sputtered ITO electrodes and 0.1 M $LiClO_4$ electrolytes, the solvent of electrolytes have been dissimilar though, ethyl acetate, EA ($\varepsilon_r = 6$) and propylene carbonate, PC ($\varepsilon_r = 65$), respectively. Intentionally, two solvents with significantly different dielectric constants have been chosen. Electrochemical cyclic-voltammetry performed with these cells within the adsorption-free purely capacitive potential region of -0.1 to +0.1 V. It can easily be seen from Figure 5.2 (a-d) that irrespective of the potential scan rate the charging current (Figure 5.2a) and hence the accumulated charge (Figure 5.2b-d) (i.e. capacitance or

polarizability) have always been found almost identical for two electrolytes containing solvents that have largely different relative permittivity (ε_r).

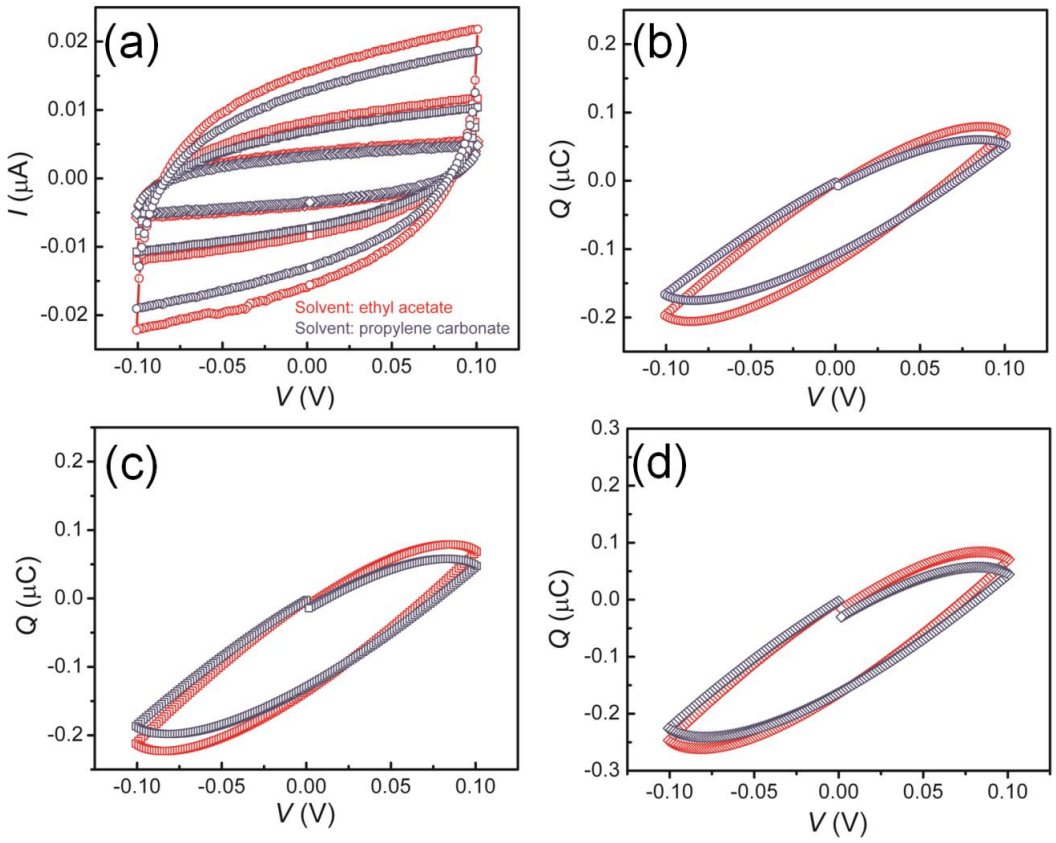

Figure 5.2 Cyclic voltammetry performed with ITO thin film electrodes of identical size and similar inter-electrode distance for two non-identical electrolytes of the same strength but different solvents. The electrolytes have been 0.1 M $LiClO_4$ solution of ethyl acetate, EA (ε_r = 6) (red symbols) and propylene carbonate, PC (ε_r = 65) (blue symbols), respectively; (a) cyclovoltammograms with a potential sweep rate of 10, 5 and 2 mV/s are marked with round (–), square (∀) and prism shaped (M) symbols, respectively. (b-d) accumulated charge on the electrodes for scan speed of 2, 5 and 10 mV/s, respectively.

Using equation 5.1, the *field-effect mobility* (μ_{FET}) for the transistor shown in Figure 5.1 is calculated. The channel length (L) and the channel width (W) are 973 nm and 34 nm, respectively. For the presented EG FET device, the *specific capacitance* of the electrolyte insulator is considered analogous to the *double layer capacitance* (C_{DL}) of the electrochemical capacitor. It was calculated considering the cylindrical capacitor geometry as given by equation 5.2 and was found to be between 4.5 and 5 μF/cm^2, for all the fabricated nanowire-

channel FET devices that are summarized in table 5.1. On the other hand, the *field-effect mobility* of the present FET device is obtained from equation 5.1 and 5.2 and found to be 207 cm^2/Vs.

The *On/Off* ratio, saturated *On*-current, *transconductance* and *sub-threshold slope* of 10 individual devices are summarized in Figure 5.3 (a-b). Devices from D1 to D10 used nanowires of slightly different diameters; however, attempts were made to keep the channel length of the devices constant at approximately 1 μm. The channel geometry for ten devices is given in table 5.1. All devices show an *On/Off* ratio in excess of 10^5, with a few of them exhibiting a ratio larger than 10^7; the *On*-currents are always around 10 μA, however, as high as 40 μA in some devices. Although small scatter in the *transconductance* values were observed, the *sub-threshold slope* values were found to be quite consistent; about or less than 100 mV/dec.

Table 5.1 Geometry of the SnO_2 EG FET's channel

Device name	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
***W*(nm)**	27	27	30	34	40	40	51	51	53	61
***L*(nm)**	953	902	934	973	937	895	927	973	939	910

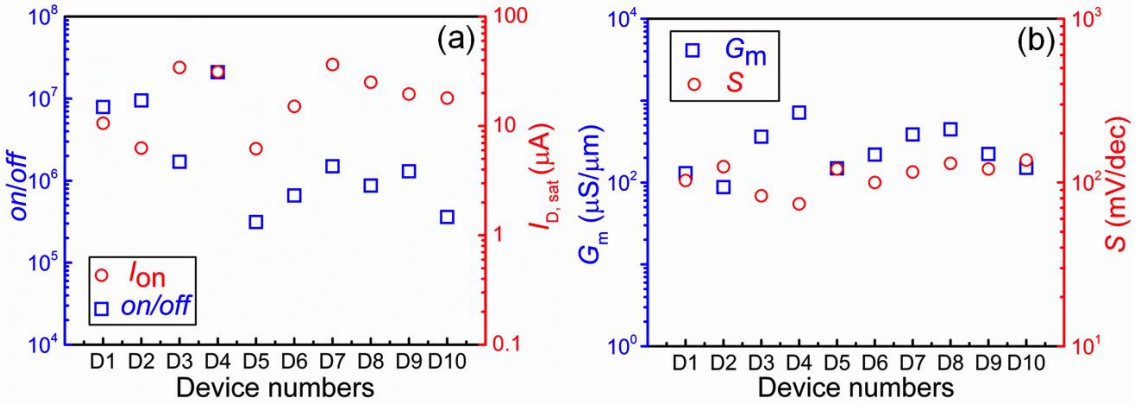

Figure 5.3 Transistor characteristics of several SnO_2 nanowire EG FETs fabricated with identical process parameters; a) *On/Off* ratio and *saturated drain currents*; and b) calculated *transconductance* (G_m) and *sub-threshold slope* (*S*) of several EG FETs with slightly non-identical channel geometries is plotted.

5.1.2 ZnO single nanowire EG FETs

The transistor characteristics of a ZnO single nanowire EG FET device are shown in Figure 5.4. The transfer curve shown in Figure 5.4a illustrates the behavior of a normally-off electron conducting (n-type) metal oxide semiconductor field-effect transistor (MOSFET). As already explained in section 5.1.1, the low operation voltage (≤ 2 V) ensures complete electrostatic field-effect operation and suppression of any faradaic currents.

The excellent insulating property of the CSPE confines the *gate currents* (I_G) to a few tens of picoamperes. Similar to single SnO_2 EG FET discussed in the previous section the ideal capacitor-like constant gate-leakage (Figure 5.4a) confirms the character of the current as capacitive charging current from the passive structures/contact electrodes and not a real *gate leakage*.

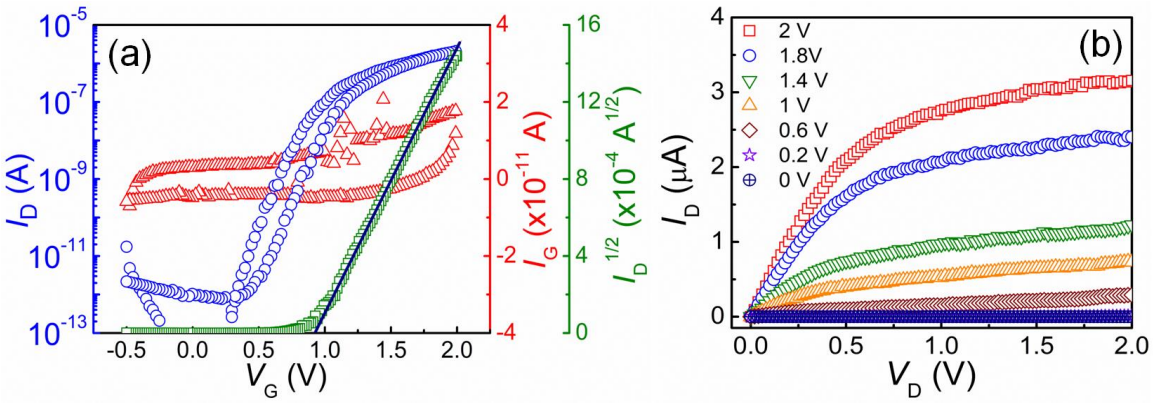

Figure 5.4 a) Transfer characteristics of a typical ZnO nanowire channel EG FET device, the applied *drain voltage* is V_D= 0.5 V, the blue circle, the green square and the red triangle symbols represent the *drain current*, the square root of the *drain current* and the *gate current*, respectively. The *threshold voltage* (V_T) is calculated to be 0.93 V by extrapolating the linear part of the $I_D^{1/2}$; (b) *drain current-drain voltage* (I_D-V_D) output characteristics of the device, while the *gate voltage* (V_G) is varies from 0 to 2 V.

The *transconductance* (g_m) of the device with 18 nm diameter of the nanowire channel (channel width) is found to be 155 μS/μm. The *sub-threshold slope* (S), on the other hand, is found to be 115 mV/decade. The *threshold voltage* (V_T) of all the measured FETs was always positive while the V_T of the device presented in Figure 5.3a was calculated to be 0.93 V. This indicates an *accumulation-mode* operation of the ZnO nanowire channel transistors which in

combination with an ultra-low value of the *Off*-current opens possibilities for low-power logic operations.

Figure 5.3b shows *drain current-drain voltage* characteristic of the ZnO EG FET, where the gate voltage (V_G) is varied between 0 to 2 V and the *drain voltage* is swept from 0 to 1.5 V. The output characteristic reveals quite decent *current saturation* at high V_D and a superb linear behavior at low V_D indicating low resistance of the ohmic contacts formed between the ZnO nanowire and the ITO *source/drain* electrodes. The transistor already shows a high *saturation current* (~3 μA) at values V_D= 0.5 V and V_G= 2 V indicating that the EG FETs are quite suitable for ultra low-voltage applications and may be compatible with thin film batteries.

Therefore, using equation (5.1) and (5.2), the *field-effect mobility* of the present FET at its saturation regime ($V_D > V_G$-V_T) is calculated to be of 61.7 cm^2/Vs. However, a maximum value of 98 cm^2/Vs for the *field-effect mobility* was obtained for another device demonstrating that an increase of μ_{FET} can be achieved by further process optimizations.

Furthermore, the *On/Off* ratio, saturated *On*-current, *threshold voltage* and *field-effect mobility* of 10 individual devices are summarized in Figure 5.5. Key transistor parameters of several ZnO nanowire EG FET devices are also given in table 5.2.

Table 5.2 Geometry of the ZnO EG FET's channel

Device name	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
***W*(nm)**	18	21	21	28	31	32	32	38	45	51
***L*(nm)**	940	950	952	950	1000	954	1900	1600	1700	1900

It should be noted that there is not much spread in device characteristics when the nanowire diameter is varied or the channel length is doubled. On the other hand, devices with very similar geometries (such as D1-D3, or D4 and D5) show little variation in the device performance. This may come from dissimilar nanowire-electrode contacts in different devices. With further optimization in the fabrication steps, a better control over the nanowire-electrode contacts may be possible, leading to all-identical devices for similar device geometries.

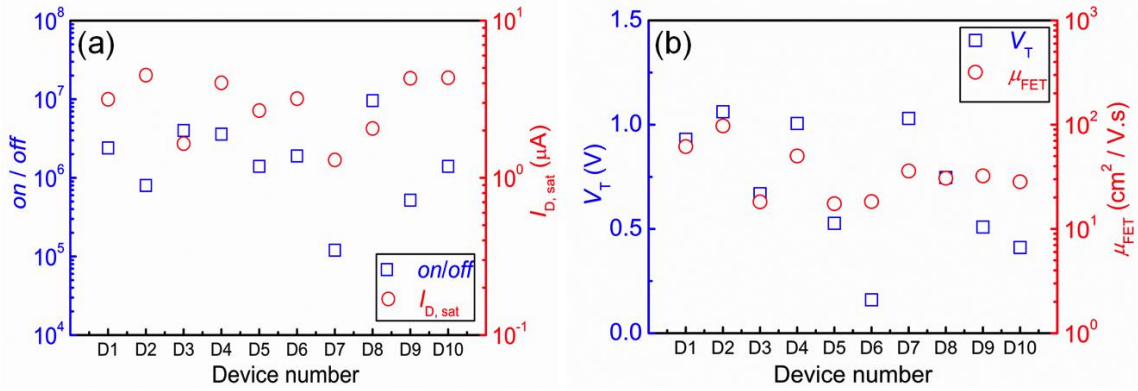

Figure 5.5 Statistical presentation of transistor characteristics of ZnO nanowire EG FETs; a) *On/Off* ratio and the *saturated drain currents*; and b) the *threshold voltages* (V_T) and the computed *field effect mobility* (μ_{FET}) values of several EG FETs with little non-identical channel geometries.

As a test of applicability the single nanowire transistor with the transfer characteristics as shown in Figure 5.4 (channel length = 940 nm and nanowire diameter = 18 nm) were also used to build a *rectifying diode* and a simple MOS *inverter* (NOT *logic gate*). The electrical characteristics are shown in Figure 5.6. The *rectifying diode* is built simply by short-circuiting the *drain* and *gate* electrode and using the two terminals (the *source* electrode and shorted *gate-drain* electrode) as the terminals of a *p-n* junction diode (as shown in the inset of Figure 5.6a). The *rectification ratio* was always more than three orders of magnitude; for example, the rectification ratio of 6.6×10^3 and 3.4×10^3 is observed for an input voltage of ± 1.8 V and ± 2 V, respectively. In addition, the measured *threshold voltage* of the transistor can be corroborated by this diode configuration, with a linear fit of the forward biased diode response, as shown in Figure 5.6a, which results in a completely identical value of V_T= 0.934 V. The simple MOS *inverter* (NOT *logic gate*), on the other hand, was fabricated with a constant load external resistor (R_L= 10 MΩ) as shown in Figure 5.6b, inset. The voltage transfer characteristics (VTC) was recorded for the supply voltage (V_D) of 1 to 2 V with 0.2 V increments and the input voltage (V_G of the transistor) was swept from 0 to $V_G = V_D$. The resulting output voltage variation is shown in Figure 5.6b. The *inverter* response to switching was clearly observed; for example, when the input voltage V_{in} was varied from 0 to 2 V for V_D= 2 V, the transition voltage was at 0.68 V. At this voltage, the voltage transfer characteristics should show $V_{in} = V_{out}$. When V_{in} is at logical 0 (V_{in}= 0 V), the driver FET is

cut off and the output voltage (V_{out}) is close to V_D (logical 1), similarly V_{in} being at logical 1 (V_{in}= V_D= 2 V), the driver transistor switches ON with much lower resistance compared to the load and the V_{out} turns to logical 0, i.e. close to 0 V. A sharp switching of output swings was observed, which corresponds to gain values (dV_{out}/dV_{in}) of around 10, considerably large for an unipolar single-transistor NMOS *inverter* (Figure 5.6b). It is shown that even without equally good performance *p*-type MOSFET (PMOS), the single-transistor *inverter* operates quite outstanding as a *logic device*.

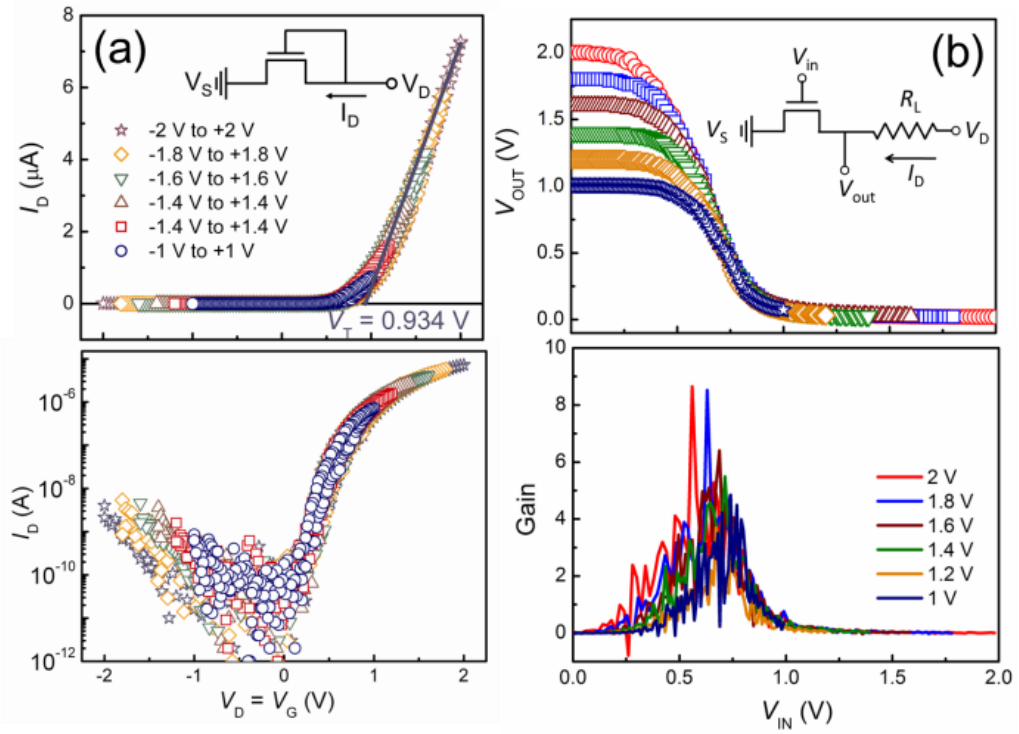

Figure 5.6 a) Electrical characterization of a diode fabricated by short circuiting the *gate* and the *drain* electrode (as shown in inset) of the previously mentioned ZnO nanowire EG FET device, the *rectification ratio* of more than 10^3 is observed for all the input voltages and an identical V_T value of 0.934 V has been obtained by extrapolating the linear part of the forward bias to I_D = 0; b) the voltage transfer characteristics and signal *gain* (dV_{out}/dV_{in}) of the *inverter* logic gate based on a CSPE gated ZnO nanowire FET and a load resistor of R_L= 10 MΩ, under different V_D and input voltage (from 1-2 V with every 0.2 V increments); the inset shows the circuit diagram of the *inverter*

5.2 Dynamic characterization

In this section, one of the most important finding of the present study is discussed. The commonly encountered concerns about applicability of the electrochemically-gated FETs relate to their switching speed. It is often argued that although devices with large *field-effect mobility* can be realized, they are usually of limited applicability as the speed of EG FETs are actually governed by the ionic conductivity of the electrolyte.[180] This argument is of course partially true and especially valid for FETs with such high μ_{FET} as presented in this work, however, our recent studies involving the charging time of the electrochemical capacitors shows that for CSPE with a conductivity of 10^{-2} S/cm, attaining over MHz cut-off frequency may not be a problem for FETs with the right top-gate geometry and electrolyte thickness of several hundreds of nanometers.[174] Here, the experimental confirmation of the frequency dependent effective capacitance calculations which were presented earlier are shown.[174]

A semiconductor characterization system (*Keithley 4200-SCS*) equipped with pulse measure units (PMU) and low current modules (RPM) was used to measure the time-resolved FET switching of a zinc oxide EG FET where the *source* electrode was grounded, a constant potential of 2 V was applied to the *drain* and the potential at the *gate* was pulsed between -1 V to 2 V. Correction for the parasitic capacitive currents from the passive structures was made by subtracting the *drain current* recorded for the zero *drain voltage*. The results are plotted in Figure 5.7 (a-b) where Figure 5.7a shows the variation in the *gate potential* and Figure 5.7b illustrates the resultant *drain current* switching. An exponential fitting of the *rise* and the *fall* currents gives the characteristic relaxation *rise* (τ_1) and *fall* (τ_2) times which are 9.5 μs and 0.88 μs, respectively. A larger *rise* time compared to the *fall* time has also been reported earlier; in fact it has always been observed that electrochemical charging takes considerably longer period than discharging.[13, 181] Taking the inverse of the charging time the *cut-off frequency* (f_T) of the device is calculated to be larger than 100 kHz. It is important to note that the zinc oxide EG FET measured in this geometry is an in-plane transistor with a channel-gate distance larger than 10 μm. This leaves a large range for further improvement in speed and an increase in f_T to the MHz regime just by a reduction in the *gate*-channel distance which can be easily achieved using a top-*gate* geometry. This is simply due to the fact that the *electrochemical capacitors* are part of *RC* circuits; and hence the

relaxation time varies linearly with a decrease in the electrolyte resistance (*R*); while the later scales with inter-electrode (i.e. gate-channel) distances.[175]

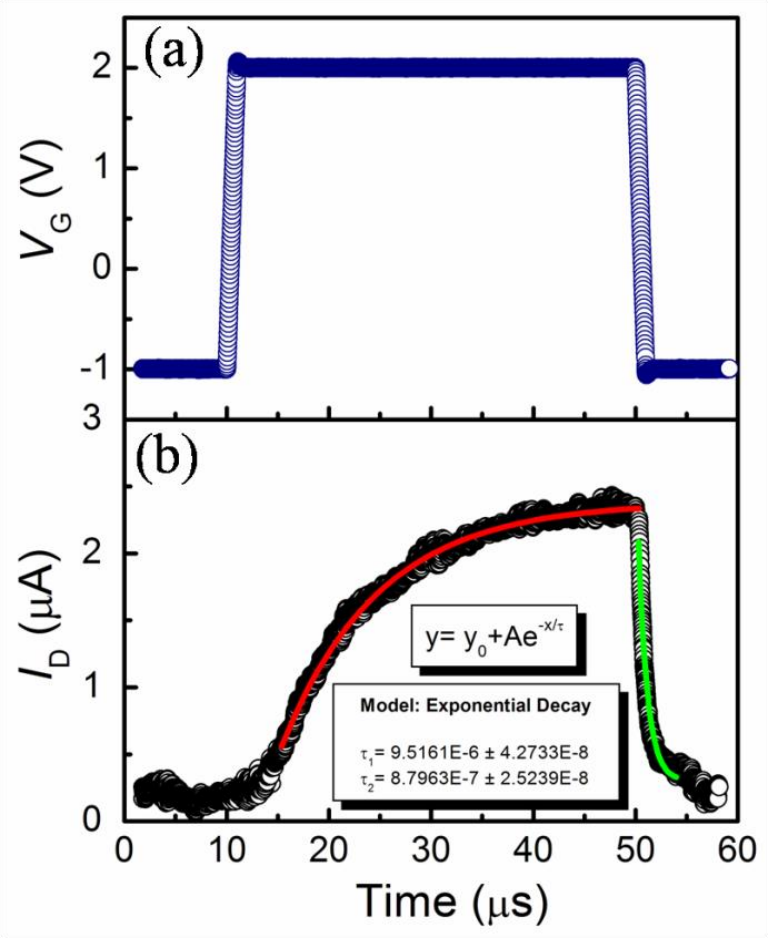

Figure 5.7 Time-transient measurement showing the switching speed of a single zinc oxide nanowire EG FET device; (a) the gate voltage V_G is pulsed from -1 to 2 V, (b) the corresponding response of the *drain current* (I_D) is recorded and both are plotted with respect to elapsed time, the *rise* and *fall* segments of the *drain currents* are separately fitted with exponential decay equations in order to obtain the charging (*rise*) and discharging (*fall*) time of 9.5 μs and 0.88 μs, respectively.

Chapter 6

Environmental stability of EG FETs

The *reliability* issues, i.e. the *long-term* performance *stability* in ambient conditions, represent the first and foremost concerns for any kinds of electrical device. This issue becomes more pertinent in case of flexible and low voltage operated devices; for example, organic semiconductors as FET channel (especially the electron conducting ones),[182] or ionic liquid/ion-gel as gate dielectric degrade extremely rapidly in the presence of oxygen or water moisture.[20] Therefore, the demonstration of stable operation of low voltage, portable devices at ambient condition for sufficiently long measurement time is an important issue for applications.

Furthermore, *thermal stability*, another interesting aspect of *reliability* tests, has not really been explored for this sort of electronics up to now. Therefore, in this chapter *environmental* and *thermal stability* of single nanowire based EG FETs both will be explored.

6.1 Long term stability

It is definitely worth to note in the context of applications that the composite solid polymer electrolyte used in the present study is extremely stable at ambient conditions. Figure 6.1 clearly shows that an electrochemical capacitor consisting of ITO electrodes and the CSPE as the dielectric retains 97% of its initial charge/capacitance after one month exposure to air.

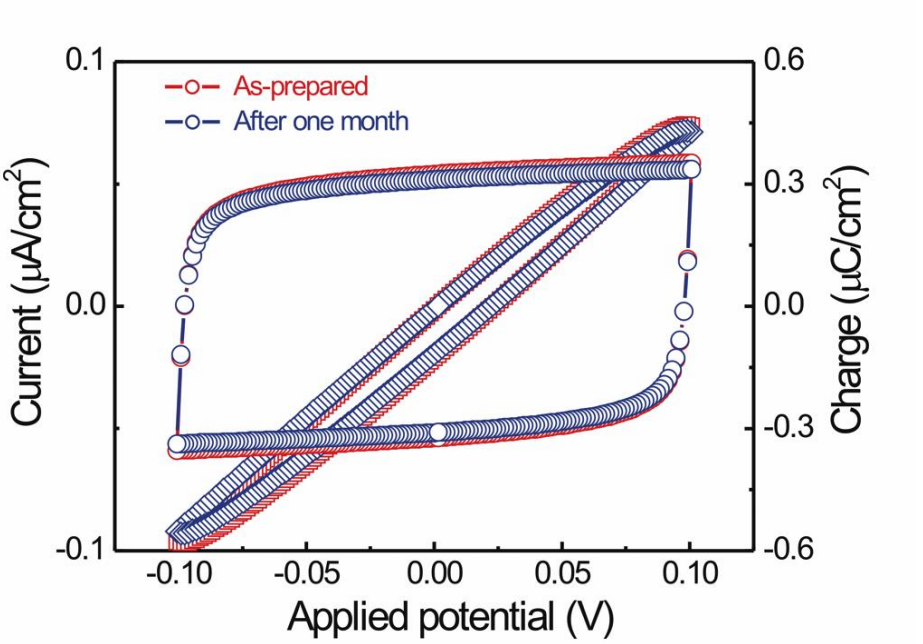

Figure 6.1 Cyclic voltammetry measurements showing the *long-term stability* of polarizability or capacitance of the composite solid polymer electrolyte in air. Sputtered ITO working and counter electrodes have been used for the experiment. The circle and square symbols indicate the current density and the specific charge density on the electrodes, respectively.

On the other hand, *air stability* and *long-term reproducibility* of four EG FETs are illustrated in Figure 6.2 which shows transfer curves in the as-prepared condition and after twenty days in air without any additional protective film. As a noticeable observation, the *threshold voltage* can be seen to change by a small amount with a maximum value of around 200 mV; however, there was not any clear trend or preferred direction of this *threshold voltage* shift; hence it may not be related to certain physical effects in the nanowire FETs. On the other hand, no significant increase in hysteresis was observed, in fact, in some cases the hysteresis was found to decrease with time. Additionally, as a general trend for all the measured devices, a small decrease in the gate leakage (may relate to further drying of the electrolyte) and a 2-3 fold increase in *saturated drain current* ($I_{D,sat}$) was recorded, which signifies that even an increase in μ_{FET} is possible after several weeks of exposure to air.

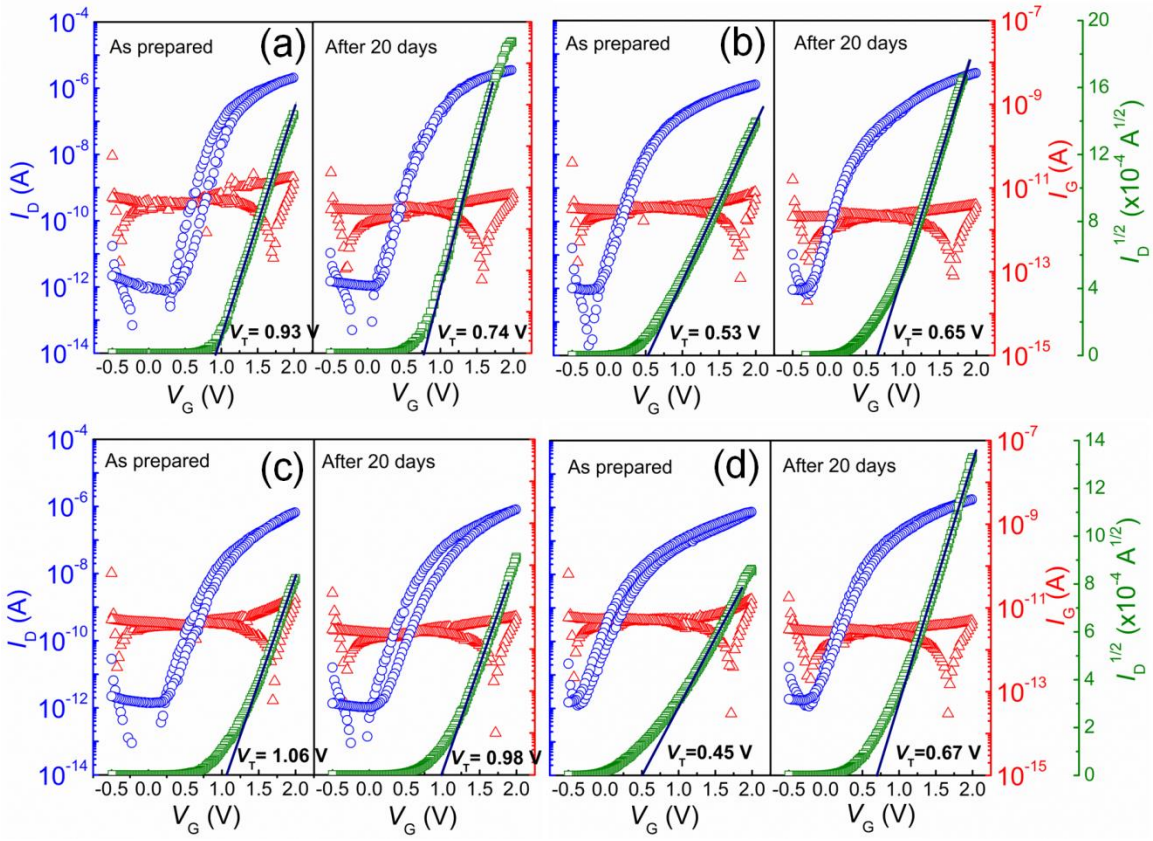

Figure 6.2 (a-d) Transfer curves of randomly selected, four individual EG FET devices measured immediately after device fabrication and after 20 days aging in air showing *long-term stability* of the nanowire channel EG FETs and especially outstanding *stability* of the CSPE in air ambience.

In addition to above-mentioned measurements, *long-term air-stability* and retention of the FET characteristics of a single individual ZnO nanowire EG FET device is shown in Figure 6.3. The transfer curves are measured immediately after fabrication and after several weeks show similar FET characteristics. The *leakage* or *charging currents* (I_G) decrease by a negligible amount with time, however, the *saturated drain current* is found to remain unchanged or even increased. Consequently, the transistor characteristics either remain the same (such as μ_{FET}) or even improve with time (such as *transconductance*, G_m, *sub-threshold slope*, S).

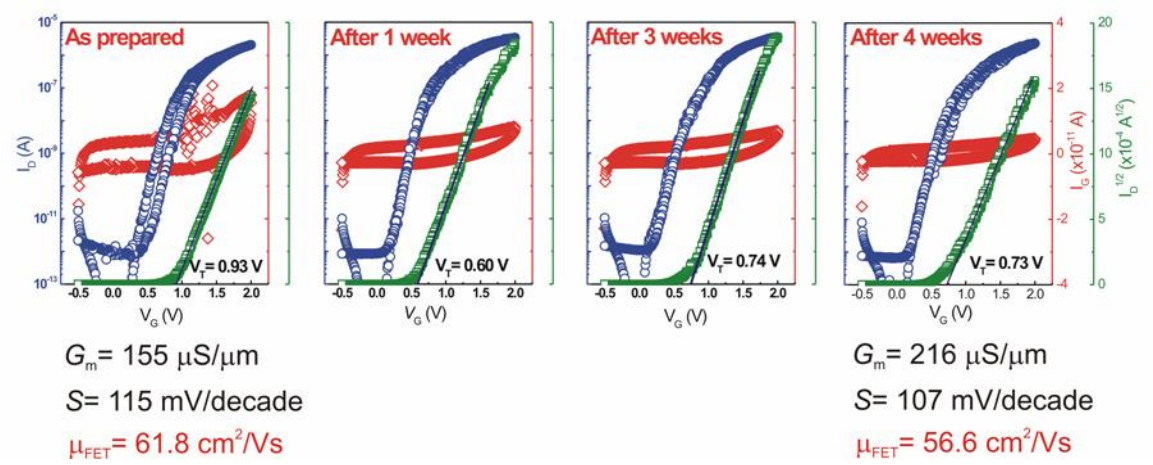

Figure 6.3 Transfer characteristics of an individual EG FET device measured after the aging times indicated in the figure.

6.2 Temperature stability

One of the critical points that relates to the application versatility of FETs with very low operating voltage is their temperature stability. In this section high temperature resilience of such SnO_2 nanowire based EG FETs has been investigated when the substrate temperature of the devices was systematically varied from room temperature up to 180 ºC (the upper temperature threshold was chosen equal to the short-term exposure limit of the inexpensive polyethylene naphthalate (PEN) polymer substrates).

In this study, the transfer characteristics of the devices were first measured at room temperature (25 °C) and then the temperature of the silicon chip was raised from 30 °C to 180 °C in 10 °C increments with an interval of 20 minutes at every step. The transfer curves of a typical SnO_2 nanowire EG FET device measured at sixteen different temperatures are plotted in Figure 6.4. In order to demonstrate the high *reproducibility* of the phenomena taking place during the heating of the EG FET devices, a similar dataset for another device is shown in Figure 6.5. As mentioned in chapter 5, at room temperature, SnO_2 single nanowire EG FETs behave analogous to normally-off *accumulation mode* NMOS. It can be seen for all the devices which are heated to high temperatures that the nanowire channels get increasingly thermally doped and the *threshold voltage* shifts to lower potentials, as the temperature is raised. Temperature dependence of *threshold voltage* shift has also been reported previously for metal oxide thin film transistors (TFTs).[183, 184] Until 70 ºC, the devices still operate in the *accumulation mode* but above 80 - 90 ºC, the *threshold voltage* gradually shifts to

negative values making them *depletion-mode* FETs (Figure. 6.4 and 6.5). However, up to 110 - 120 ºC, the shape of the transfer curves, the *On*-currents and the *On*/*Off* ratios are retained; additionally, the hysteresis is small up to this temperature range. Above 110 - 120 ºC the hysteresis and the *Off*-currents increase significantly; the increase of the latter parameter also decreases the *On*/*Off* ratios. The EG FET channels are composed of tin oxide, a material of excellent *stability* (beside, the concentration of intrinsic carriers being a function of temperature) in air. At elevated temperatures, most of the observed changes in transistor characteristics while heating can safely be attributed to the corresponding changes in the CSPE.

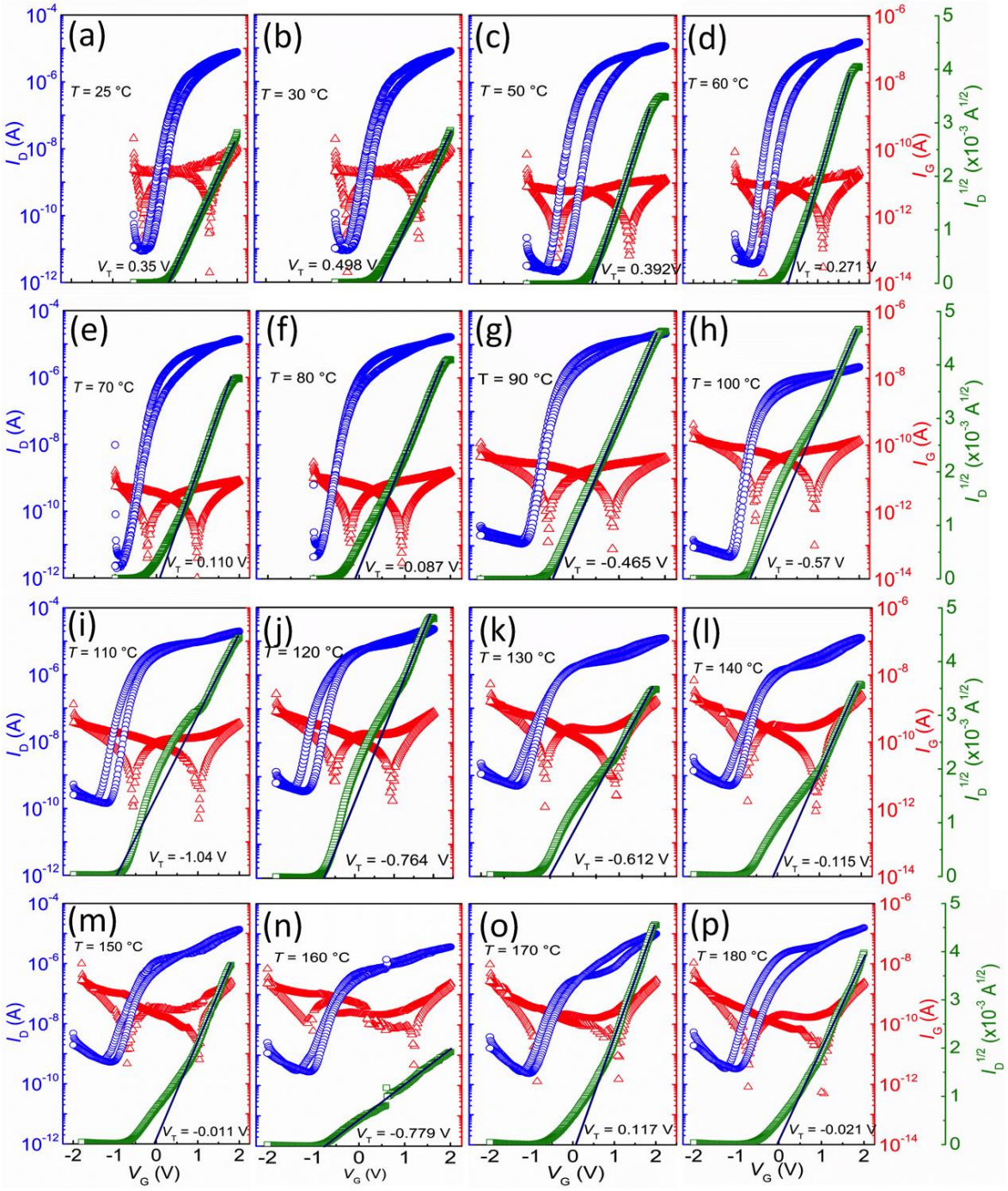

Figure 6.4 Transfer characteristics of a single SnO_2 nanowire EG FET device, the applied *drain voltage* is V_D= 0.5 V, the blue circles, the green squares and the red triangles represent the drain current, the square root of the *drain current* and the *gate current*, respectively. Figures (a-p) show the gradual change in the performance parameters (V_T, I_G, $I_{On\text{-}sat}$ and *On/Off*) of the device with the increase in operating temperatures from 25 °C to 180 °C at every 10 °C steps.

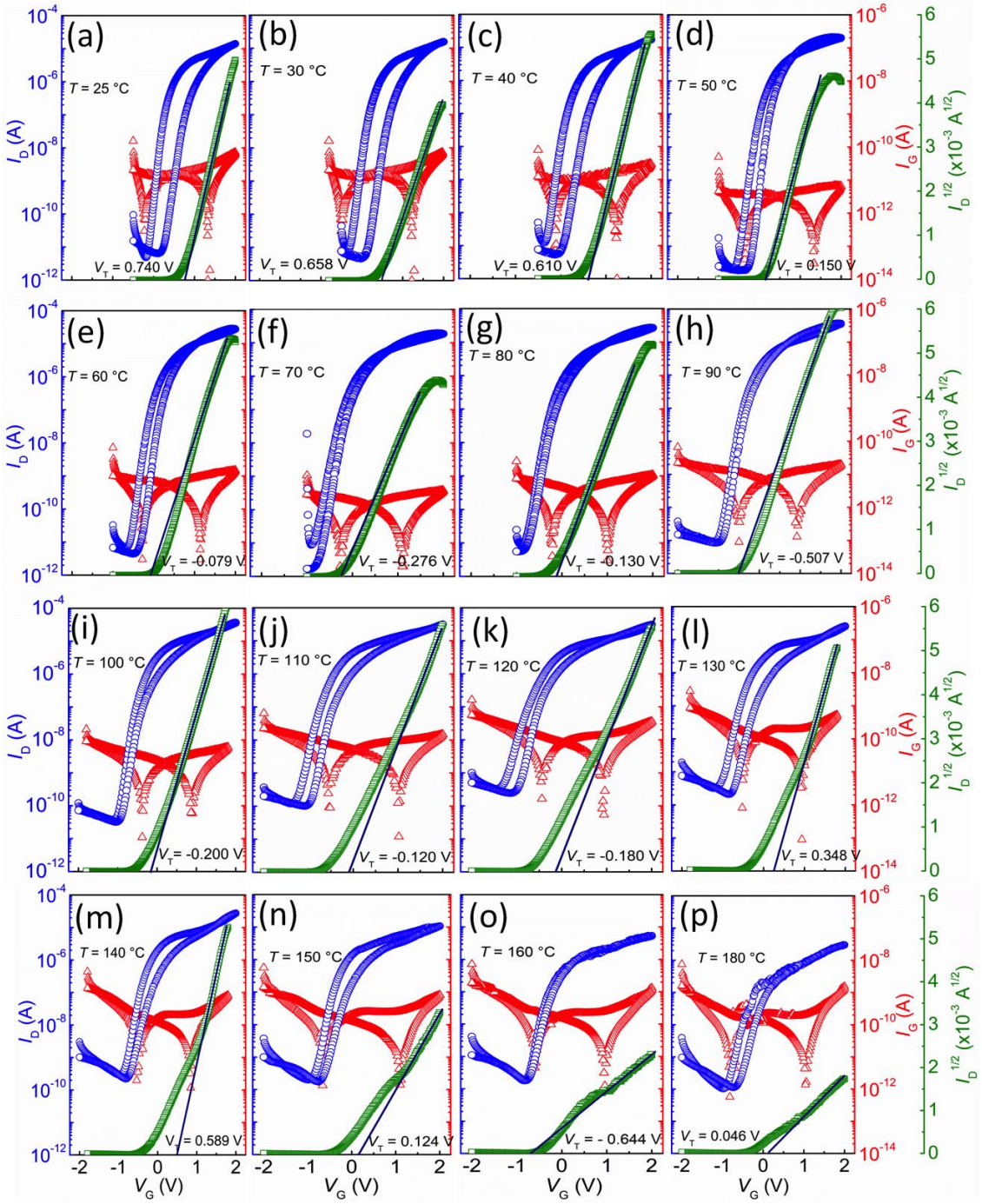

Figure 6.5 Similar temperature dependent transfer curves measured for another identical single SnO_2 nanowire EG FET device showing reproducibility of the measured phenomena.

In order to study the *thermal stability* of the CSPE thermal gravimetric analysis (TGA) is carried out (Figure 6.6). The measurements were performed with a *Setaram* thermal analyzer *SENSYS evo* TGA-DSC equipped with a *Pfeiffer OmiStar* mass spectrometer for the

analysis of the evolved gas. The samples were prepared by drying around 50 mg of liquid electrolyte in an aluminum crucible under ambient conditions (i.e. in air and at room temperature) for about two weeks. The TGA measurement was performed in an inert helium atmosphere.

The temperature in the analyzer was ramped from room temperature to 180 °C with a heating rate of 5 °C/min and then maintained at 180 °C for 1 hour. Until 90 °C, the *mass loss* was insignificant, corresponding well to the undistorted transfer curves shown in Figure 6.4 and 6.5. The majority of the mass loss (as high as 30 %), occurred within the temperature range from 90 - 180 °C. However, the severe *mass loss* during temperature ramping was followed by a stable mass during the holding period at 180 °C (Figure 6.3a). In order to examine the origin of the lost mass, mass spectroscopy was simultaneously carried out during the TGA measurement. Mass spectra recorded (Fig. 6.3b) in the temperature range from 30 to 90 °C reveal desorption of small amounts of adsorbed moisture/water molecules (the CSPE was exposed to air for drying for at least 2 weeks prior the TGA analysis) and a fraction of vinyl alcohol monomers with characteristic signals at m/Z = 44, 45. Above 110 °C DMSO and PC were also detected by mass spectrometry with the signals at m/Z = 63, 78 and m/Z = 57, respectively. This indicates that the PVA polymeric network/cages of the CSPE seem to get disturbed or even ruptured thereby allowing sudden and rapid evaporation of the solvents (DMSO and PC) (Figure 6.3b). Thereafter, most likely, the desorbed solvents account for the majority of the *mass loss*. In order to further corroborate the nominal/insignificant *mass loss*, i.e. negligible degradation of the CSPE at lower temperatures, another identical CSPE sample was separately heated to 60 °C for about 60 hours (Fig. 6.6c). Interestingly, the total *mass loss* took place immediately within the first hour and thereafter the sample mass remained unchanged. Furthermore, the complete *mass loss* was found to be not more than 1 % even after 60 hours of measurement (matches well with the other TGA measurements, Fig. 6.6a); this mass loss can again be attributed to the desorbed moisture from the CSPE.

In conclusion, TGA and mass spectroscopy analysis show the correlation between the temperature dependence of the transfer characteristics and the *temperature stability* of the CSPE. It is observed that up to moderate temperatures (60-80 °C), the electrolyte remains unchanged, loosing only a small (≤ 1 %) amount of adsorbed moisture while the transfer

curves are also unaffected and no significant increase in the gate leakage can be observed. However, at higher temperature, thermally activated carriers in SnO_2 channels make the devices normally-on (*depletion-mode* MOSFET) and the gate leakage increases noticeably. Above 110 °C, however, the CSPE structure partially ruptures allowing quick evaporation of the trapped solvent. A corresponding effect in the performance of SnO_2 EG FETs can be seen immediately as the transfer curves get distorted.

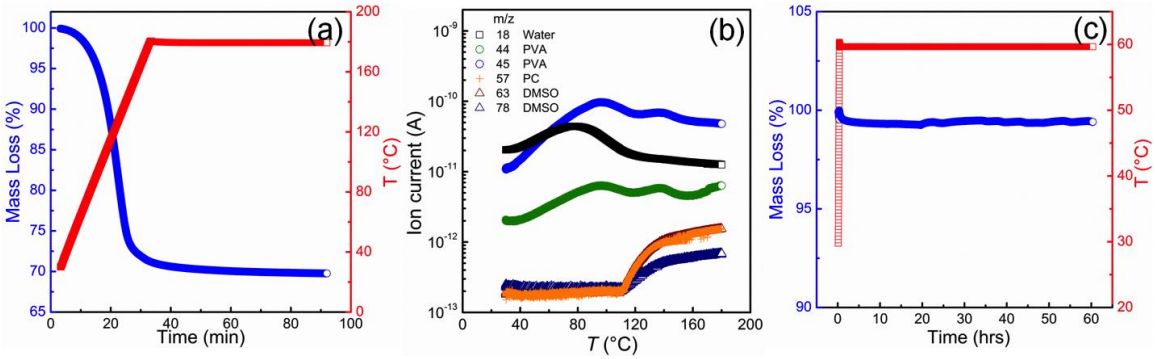

Figure 6.6 (a) Percentage *mass loss* and temperature versus time for the CSPE which is heated in thermo-gravimetric analyzer for a temperature range from 30 °C to 180 °C with a heating rate of 5 °C/min and then kept at 180 °C for 1 hour; (b) Corresponding *mass spectroscopy* of the CSPE performed under helium flow of 20 ml /min, the spectrometer signal corresponding to mass fraction of the desorbed species are listed in the figure; (c) TGA of the CSPE is performed again by heating the electrolyte at 60 °C for 60 hrs, the sample is heated from 30 °C to 60 °C with a heating rate of 2 °C/min.

Chapter 7

Conclusions and Outlook

7.1 Conclusions

In this thesis the concept of *electrochemical-gating* and its compatibility to nanowire-based transistors has been explored. Throughout the course of this work, metal oxide nanowires have been synthesized and several EG FETs have been designed, fabricated and characterized. Transistor characteristics have been measured at room and moderately elevated temperatures to examine the *thermal stability* of the devices. Time dependent device characteristics have been tested to evaluate the *long-term environmental stability*. The main results and observations are summarized below:

I. A series of high quality single crystalline metal oxide nanowires have been successfully prepared via the VLS technique. Undoped systems, such as ZnO, SnO_2 and In_2O_3 or doped systems, such as Sn-doped indium oxide, ITO, nanowires have been prepared with high quality, single phase and free of defects. Both the size and the distribution of the catalyst nanoparticles are found to play a key role in determining the diameters of the nanowires. Dispersions of gold nanoparticles were found to be the best option for controlling the diameter of the nanowires, as well as their production yield. Finally, ultra-thin SnO_2 nanowires with diameter as small as 6 nm and average diameter of 12 nm have been produced and have shown excellent electrical performances.

II. Remarkable bendability of ZnO nanowires has been demonstrated in this study by using the geometric phase analysis (GPA) technique. It has been shown that the

nanowires can be bent without introducing any defects as a result of plastic deformation, such as dislocations or other defects.

III. Electrochemically-gated field-effect transistors with a channel composed of single-crystalline high-mobility semiconducting nanowires, such as ZnO and SnO_2 nanowires have been fabricated. The devices are prepared on commercial silicon wafers; however, owing to the low processing temperatures and high flexibility of the active components, the devices can be considered compatible to the inexpensive and flexible substrates, such as polymers, cellulose, etc. It has been shown that the EG FET devices show excellent transistor characteristics and can be operated at drive voltages as low as 2 V or less.

IV. High *field-effect mobility* close to the intrinsic value of the single-crystal oxide semiconductor, excellent *transconductance* and *sub-threshold slope* close to theoretical limit have been obtained for the EG FET devices.

V. The temperature dependent transfer curves of the single SnO_2 nanowire EG FETs as well as TGA analysis of the CSPE demonstrate the possibility of using such transparent and flexible FET's for a long time at moderate temperatures of up to 60 - 70 °C. Even short term occasional exposure to higher temperatures in the range of 100 - 110 °C is acceptable without breaking the devices. Unlike the ionic liquids which are frequently used by many researchers for their high capacitance, the CSPE examined and utilized in this work has been found simultaneously to have a high capacitance value, 4-5 $\mu F/cm^2$. This value is much larger than any existing gate dielectric and also quite stable under ambient conditions. The ZnO nanowire EG FETs show no noticeable degradation after an exposure of 3-4 weeks in air.

It is also shown that single nanowire based EG FETs based on CSPE can operate at a moderate frequency of 100 kHz with an in-plane transistor geometry. The *switching frequency* may further increase to the MHz range by changing to top gate configuration. It can also be concluded that the *electrochemical gating* approach is not a limitation in improving the transistor performance.

7.2 Outlook

The vapor-liquid-solid (VLS) synthesis of nanowires ensures high quality, single phase, single crystalline and identical dimension of 1-D nanostructures. However, the yield of the process is not high and hence it is not suitable for nanowire alignment tests, building multi-wire devices or for scaling up such nanowire EG FETs. Therefore, the production of nanowires at a large scale is essential and would have significant impact on their potential application or usability in novel electronics. Usually, the synthesis is easier to control in small volumes, expanding to larger scale increases process control problems and reproducibility as well as alteration in output quality. Therefore, one of the important issues is the large-scale and large quantity production of nanostructures.

Physical vapor deposition (PVD) and chemical vapor deposition (CVD) have been widely employed to synthesize single crystalline nanowires. However, the high-temperature vapor-phase approach involved in these techniques makes them expensive and energy-consuming. Thermal or chemical wet methods are better candidate for fabricating nanowires because they occur under mild conditions (aqueous solution, atmospheric pressure and <100 °C) as well as allowing for the tuning of the crystal morphology via changes in the solution conditions or the introduction of small organic molecules during the growth process.[185–189]

The next important issue towards future development of such devices would be to avoid lithography techniques in order to have high-throughput fabrication of completely solution-processable high-performance FET's. In this regard, several ways of one dimensional nanostructure assembly or alignment (e.g., nanorods[190], nanowires[191–194]) have already been reported in the literature. Recent work on random mixtures of semiconducting nanowires has also been performed along these lines.[195, 196] With the success of such alignment processes, one would be able to directly convert the present research results into inexpensive, high-throughput fabrication of low voltage operated, portable transparent and flexible electronics.

Another important issue needing immediate attention is to grow high quality *p*-type nanowires with high electrical performance so that equally good quality PMOS devices can be built towards fabrication of CMOS circuitry in order to ensure high electrical gain and low power loss in such nanowire EG FET based logics.

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Appendix A

Ellingham Diagram

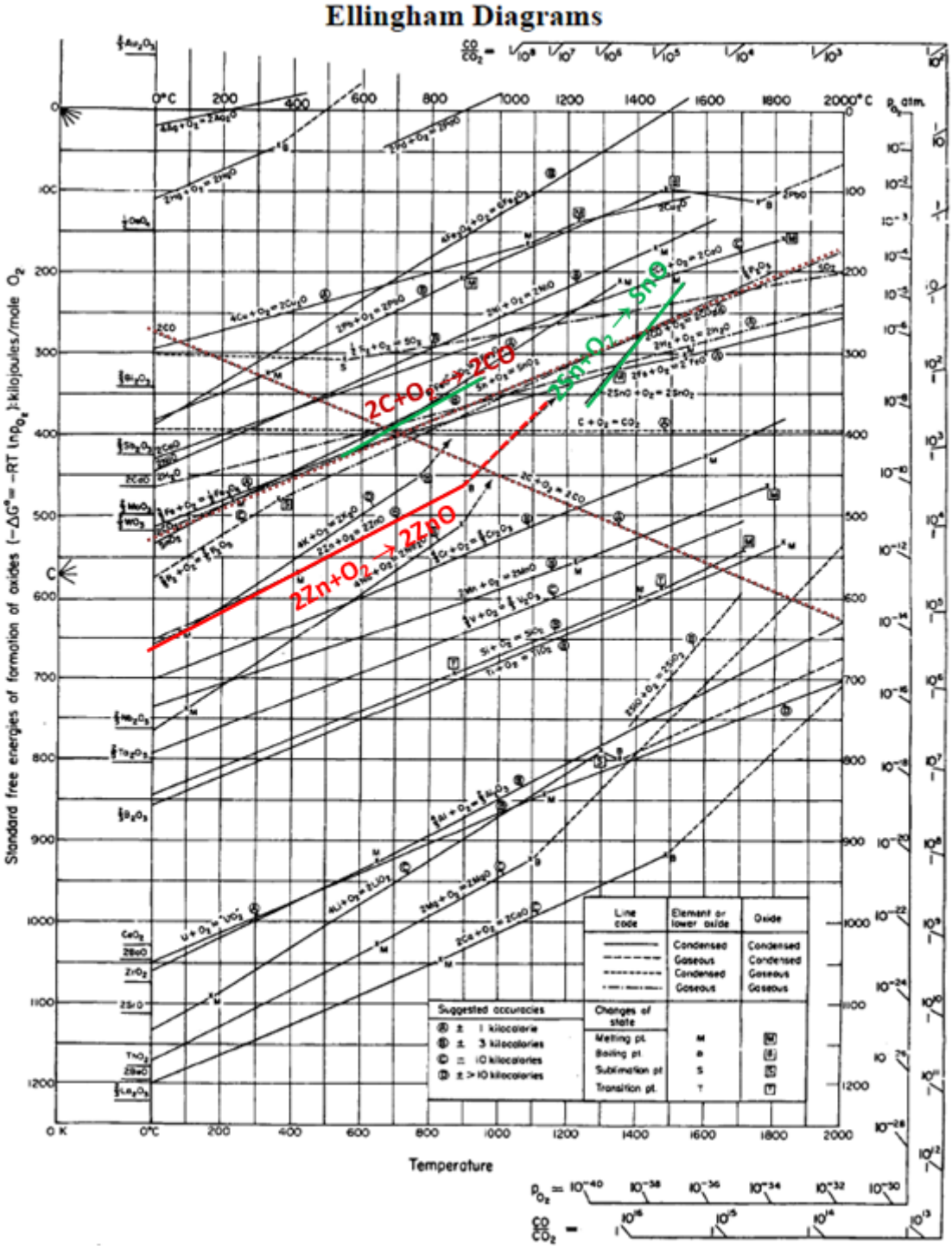

Figure A. Ellingham Diagram

An Ellingham diagram is a plot of ΔG versus temperature. Since ΔH and ΔS are essentially constant with temperature unless a phase change occurs, the free energy versus temperature plot can be drawn as a series of straight lines, where ΔS is the slope and ΔH is the y-intercept. The slope of the line changes when any of the materials involved melt or vaporize.

Free energy of formation is negative for most metal oxides, and so the diagram is drawn with

ΔG=0 at the top of the diagram, and the values of ΔG shown are all negative numbers.Temperatures where either the metal or oxide melt or vaporize are marked on the diagram.

A given metal can reduce the oxides of all other metals whose lines lie above theirs on the diagram. For example, the $2Zn + O_2 \rightarrow 2ZnO$ line lies below the $2C + O2 \rightarrow 2CO$ line at temperature ≥ 950 °C, and so carbon can reduce zinc oxide to metallic zinc. Since the $2C + O_2 \rightarrow 2CO$ line is downward-sloping, it cuts across the lines for many of the other metals. This makes carbon useful as a reducing agent, because as soon as the carbon oxidation line goes below a metal oxidation line, the carbon can reduce the metal oxide to metal.

Appendix B

UV-Vis spectroscopy and an optical image showing the high transparency of the composite solid polymer electrolyte has been shown in Figure B.

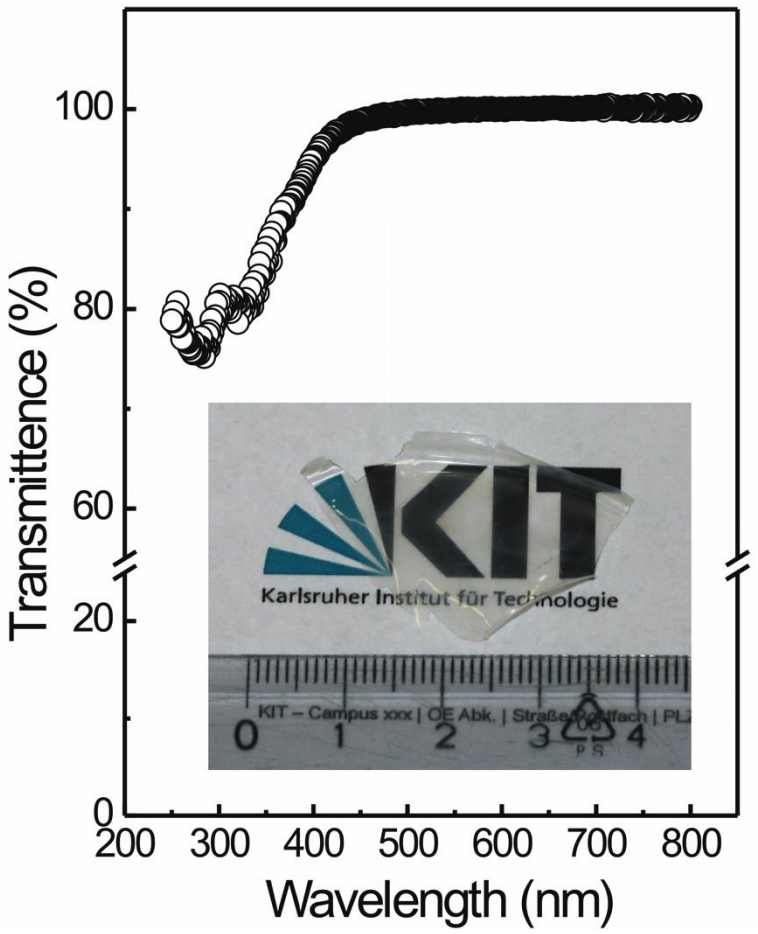

Figure B. UV-Vis spectroscopy and an optical image (inset) show high transparency of the CSPE at the visible wavelengths.

The optical transparency of the CSPE is investigated with UV-VIS spectroscopy. It can be seen from Figure B that the electrolyte is nearly 100 % transparent in the visible spectrum range and even shows around 80 % transparency in the UV regime of the spectrum, down to the experimental limit of 250 nm wavelength of the incident light.

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Publications

- **B. Nasr**, Zh. Zhao-Karger, D. Wang, R. Kruk, H. Hahn, S. Dasgupta,"High temperature operation of electrochemically-gated SnO_2 nanowire field-effect transistors" *J. Mater. Chem. C,* **1**, 2534, (2013).

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