Fully Integrated Autonomous System-on-Chips with Wireless Energy and Data Transmission

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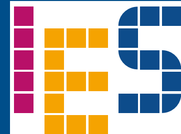

Electrical Engineering and Information Technology Department

Integrierte Elektronische Systeme

Fully Integrated Autonomous System-on-Chips with Wireless Energy and Data Transmission

Accepted doctoral thesis by Dominic Korner

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Abstract

Integrated autonomous **S**ystem-**o**n-**C**hips (SoCs) with wireless data and energy transmission enable applications in areas that were previously inaccessible due to size constraints or the lack of an energy source. Depending on the transmission medium, the integration of an energy source and communication into the **A**pplication-**S**pecific **I**ntegrated **C**ircuit (ASIC) requires specialized circuitry. Ideally, an autonomous SoC consists of a single ASIC, requiring no external components for operation, making it hereby particularly small.

This work focuses on developing, designing, and fabricating autonomous SoCs with the smallest possible size and as few external components as feasible while still being capable of energy and data transmission. Four different ASICs have been designed and fabricated for three different applications. Two fabricated ASICs use ultrasound for energy and bidirectional data transmission, whereas the other two ASICs use visible light for energy and unidirectional data transmission.

The ultrasonic-powered systems presented are a **S**ensor-**i**ntegrated **M**achine **e**lement (SiMe) and a medical smart implant. The SiMe can generate a power of $60\,\mathrm{mW}$, providing power to sensors even in fully encapsulated metal enclosures deep inside the machine. The medical smart implant focuses on minimal-sized implants for the human body.

External piezoelectric crystals, required for ultrasound, consume much space compared to the size of an ASIC. Visible light as an energy and data carrier offers the possibility to integrate all components into a single die by using on-chip solar cells. The presented system for discovering novel drug candidates with an ASIC tag uses visible light as an energy and data carrier, and therefore requires no external components. It operates at a high illumination intensity of $10\,\mathrm{Mlx}$, decreasing the overall system size to a minimum. A single solar cell generates voltages of up to $0.7\,\mathrm{V}$, which is not enough to supply the ASIC. Instead of charge pumps, which consume energy and chip area, a serialization of solar cells in a **S**ilicon-**o**n-**I**nsulator (SOI) technology provides the required supply voltage. To predict the power generated by the solar cell array on the ASIC, different types of solar cells are fabricated and measured. Light encountering the ASIC generates leakage current on the p-n junctions in sensitive circuitry. A countermeasure was taken to reduce the light-induced leakage currents: Measurements show a reduction of the leakage current by over $90\,\%$ when using a metal shield and give instructions on how to design it.

This thesis provides design and implementation recommendations for autonomous SoCs with wireless energy and data transmission. It considers light and ultrasound transmission principles for energy and data, as well as provides a system architecture overview for the implementation. The fabricated ASICs prove the effectiveness of the presented recommendations.

Zusammenfassung

Neuartige integrierte autonome **S**ystem-**o**n-**C**hips (SoCs) mit drahtloser Energie- und Datenübertragung ermöglichen Anwendungen in Bereichen die bisher aufgrund von Größenbeschränkungen oder dem Fehlen einer Energiequelle unzugänglich waren. Je nach verwendetem Übertragungsmedium, erfordert die Integration von Energiequelle und Kommunikation in den **A**pplication-**S**pecific **I**ntegrated **C**ircuit (ASIC) spezielle Schaltungen. Im Idealfall besteht der autonome SoC ausschließlich aus einem einzigen ASIC ohne weitere externe Bauteile zu benötigen und ist dadurch besonders klein.

Diese Arbeit befasst sich mit der Entwicklung und Herstellung von autonomen SoCs mit der kleinstmöglichen Größe und so wenig wie möglichen externen Komponenten, wobei sie dennoch Energie und Daten übertragen können müssen. Es wurden vier verschiedene ASICs für drei verschiedene Anwendungen entwickelt. Zwei der hergestellten ASICs verwenden Ultraschall für eine bidirektionale Datenübertragung, während die anderen beiden ASICs sichtbares Licht für eine unidirektionale Datenübertragung verwenden.

Bei den ultraschallbasierten Systemen handelt es sich um ein **S**ensor**i**ntegriertes **M**aschinen**e**lement (SiMe) und ein Implantat für den menschlichen Körper. Das SiMe kann eine Leistung von bis zu $60\,\mathrm{mW}$ in einem hermetisch geschlossenen Metallgehäuse bereitstellen und somit eine stabile Versorgung von Sensoren mit Strom im Inneren von Maschinen gewährleisten. Das medizinische Implantat hingegen ist besonders auf eine minimale Größe ausgelegt.

Im Vergleich zur Größe eines ASICs brauchen externe piezoelektrische Kristalle viel Platz. Sichtbares Licht als Energie- und Datenträger hingegen eröffnet die Möglichkeit, alle erforderlichen Komponenten mithilfe von On-Chip Solarzellen in einen einzigen Chip zu integrieren. Das vorgestellte System für die Wirkstofffindung in der Medizin nutzt sichtbares Licht zur Energie- und Datenübertragung und benötigt daher keine externen Komponenten. Um die Größe des Systems weiter zu minimieren, arbeitet es mit einer hohen Lichtstärke von $10\,\mathrm{Mlx}$. Eine Herausforderung ist hierbei, dass eine einzelne Solarzelle eine Spannung von bis zu $0.7\,\mathrm{V}$ erzeugt. Diese Spannung reicht nicht für die Versorgung eines ASICs aus. Um Ladungspumpen welche Energie und Chipfläche benötigen zu vermeiden, können zur Erzeugung der Versorgungsspannung stattdessen Solarzellen in einer **S**ilicon-**o**n-**I**nsulator (SOI) Technologie in Reihe geschaltet werden. Um die erzeugte Leistung des Solarzellen-Arrays vorherzusagen, werden verschiedene Solarzellen gefertigt und vermessen. Licht, das auf den ASIC trifft, erzeugt Leckströme in den p-n-Übergängen. Eine Metallabschirmung sorgt für eine Verringerung der Leckströme um über $90\,\%$.

Diese Arbeit gibt Designempfehlungen für autonome SoCs mit drahtloser Energie- und Datenübertragung. Es werden Licht und Ultraschall und die dafür benötigte Systemarchitektur vorgestellt. Die gefertigten ASICs zeigen die Wirksamkeit der vorgestellten Empfehlungen.

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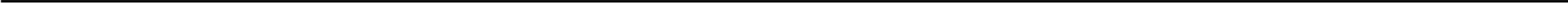


List of Abbreviations

AC	**A**lternating **C**urrent
ADC	**A**nalog-to-**D**igital **C**onverter
AM	**A**mplitude **M**odulation
ASIC	**A**pplication-**S**pecific **I**ntegrated **C**ircuit
BB	**B**uilding **B**lock
Box	**B**uried **ox**ide
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
DAC	**D**igital-to-**A**nalog **C**onverter
DC	**D**irect **C**urrent
DRAM	**D**ynamic **R**andom **A**ccess **M**emory
EEPROM	**E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory
ESD	**E**lectro**s**tatic **D**ischarge
ESR	**E**quivalent **S**eries **R**esistance
FDA	U.S. **F**ood and **D**rug **A**dministration
FM	**F**requency **M**odulation
FPGA	**F**ield **P**rogrammable **G**ate **A**rray
IC	**I**ntegrated **C**ircuit
LDO	**L**ow-**D**rop**o**ut
LED	**L**ight-**E**mitting **D**iode
LNA	**L**ow **N**oise **A**mplifier
MIM	**M**etal-**I**nsulator-**M**etal
MOS	**M**etal-**O**xide-**S**emiconductor
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor
MPPT	**M**aximum **P**ower **P**oint **T**racking
MTP	**M**ultiple-**T**ime-**P**rogrammable

NVM	**N**on-**V**olatile **M**emory
OOK	**O**n-**O**ff **K**eying
OTP	**O**ne-**T**ime-**P**rogrammable
PCB	**P**rinted **C**ircuit **B**oard
PTAT	**P**roportional **t**o **A**bsolute **T**emperature
PVT	**P**rocess, **V**oltage, **T**emperature
RF	**R**adio **F**requency
RFID	**R**adio **F**requency **Id**entification
S-parameter	**S**cattering-**p**arameter
SiMe	**S**ensor-**i**ntegrated **M**achine **e**lement
SMD	**S**urface-**M**ounted **D**evice
SoC	**S**ystem-**o**n-**C**hip
SOI	**S**ilicon-**o**n-**I**nsulator
SPI	**S**erial **P**eripheral **I**nterface
SRAM	**S**tatic **R**andom-**A**ccess **M**emory
USB	**U**niversal **S**erial **B**us
UV	**U**ltraviolet
VNA	**V**ector **N**etwork **A**nalyzer

List of Symbols

Symbol	Unit	Definition
A	m^2	Area
C	F	Capacitance
c_{3333}^E	$\mathrm{N\,m^{-2}}$	Electroelastic coefficient
d	m	Diameter of a piezoelectric crystal
e	C	Elementary charge
f	Hz	Frequency
f_p	Hz	Parallel resonance frequency
f_r	Hz	Resonance frequency
f_s	Hz	Series resonance frequency
h	$\mathrm{kg\,m^2\,s^{-1}}$	Planck constant
I	A	Current
I_L	A	Load current
I_s	A	Reverse-bias saturation current
I_{SC}	A	Short circuit current
k		Number of ASICs
l	m	Length
m		Number of stages in a split and pool synthesis
N		Number of generated compounds
N_r	Hz m	Frequency constant of a piezoelectric crystal
P	W	Power
Q	C	Charge
R	Ω	Resistance
R_L	Ω	Load resistance
S		Scattering parameters
s		Different building blocks in a split and pool synthesis
T	K	Temperature
t	s	Time
V	V	Voltage
v		Resonating mode
V_{OC}	V	Open circuit voltage
V_T	V	Threshold voltage of a MOSFET
Z	Ω	Impedance

Symbol	Unit	Definition
λ	m	Wavelength
ρ	$\mathrm{kg\,m^{-3}}$	Volumetric mass density
τ_x	m	Thickness of a piezoelectric crystal
Φ	$\mathrm{m^{-2}\,s^{-1}}$	Photon flux density
Ω^v	Hz	Dimensionless eigenfrequency

Part I.

Introduction to Autonomous System-on-Chips

1. Introduction

In 1959, Jack Kilby patented his idea of the first **I**ntegrated **C**ircuit (IC) [1]. However, it would be unfeasible to mass produce the IC since it still required gold wires for the connection of the individual transistors. A few months later, Robert Noyce invented the first silicon IC based on an idea from Jean Hoerni [2]. The following years showed that the number of components in an IC is increasing exponentially. In 1965, Gordon Moore predicted a yearly doubling of components on each chip [3]. Ten years later, he renders his statement more precisely to a doubling of components every two years [4]. This forecast was true for about 50 years but the doubling of components is slowing down recently, as Moore stated in 2015 [5]. New concepts have to be explored for further scaling of **C**omplementary **M**etal-**O**xide-**S**emiconductor (CMOS) ICs [6].

To achieve a higher level of integration, additional functions have to be included in an IC, which were formerly discrete components on a **P**rinted **C**ircuit **B**oard (PCB). Integrating additional components like sensors, analog, and digital circuits into a single silicon chip is called More than Moore [7]. By integrating additional functionality into a chip, the size of the overall system becomes significantly smaller. Additionally, the energy efficiency can be increased by omitting no longer required connections and power supplies on the PCB, although these components do not follow Moore's law itself. Such systems are called **S**ystem-**o**n-**C**hips (SoCs). Figure 1.1 shows the building blocks of SoCs with a digital controller, which follows Moore's law, and various analog components, which do not scale so well with smaller transistor sizes. The analog block has to provide different functions on the SoC, for example, reference voltages, power-on reset, and clock sources. Besides these functions, circuitry for energy management, energy harvesting, and communication interfaces have special demands on the **A**pplication-**S**pecific **I**ntegrated **C**ircuit (ASIC) and might require special process technologies. The reduced size for the overall systems is of the highest importance and enables new application fields in space-limited environments.

This thesis presents ASIC-based communication systems powered solely wirelessly with no external power supply. Four fabricated ASICs for three application areas are introduced in this work. Each ASIC is optimized for its application, demonstrating fully integrated autonomous system-on-chips with wireless energy and data transmission.
Two ASICs use ultrasound for energy and data transmission. The presented **S**ensor-**i**ntegrated **M**achine **e**lement (SiMe) focuses on high power ultrasound transmission through a metal enclosure in a compact format, while the smart implant focuses on the overall size of the system. Ultrasound requires external piezoelectric crystals, which consume additional space inside the system. To develop even smaller systems, visible light can be chosen. The developed light-powered ASIC

for the discovery of novel drug candidates integrates solar cells directly into the ASIC. Since the power receiver is integrated into the ASIC, no external components are required, making it a single-chip solution and herewith extremely small. However, light induces leakage currents in the circuitry on the ASIC, a metal shield for counteracting this effect is presented.

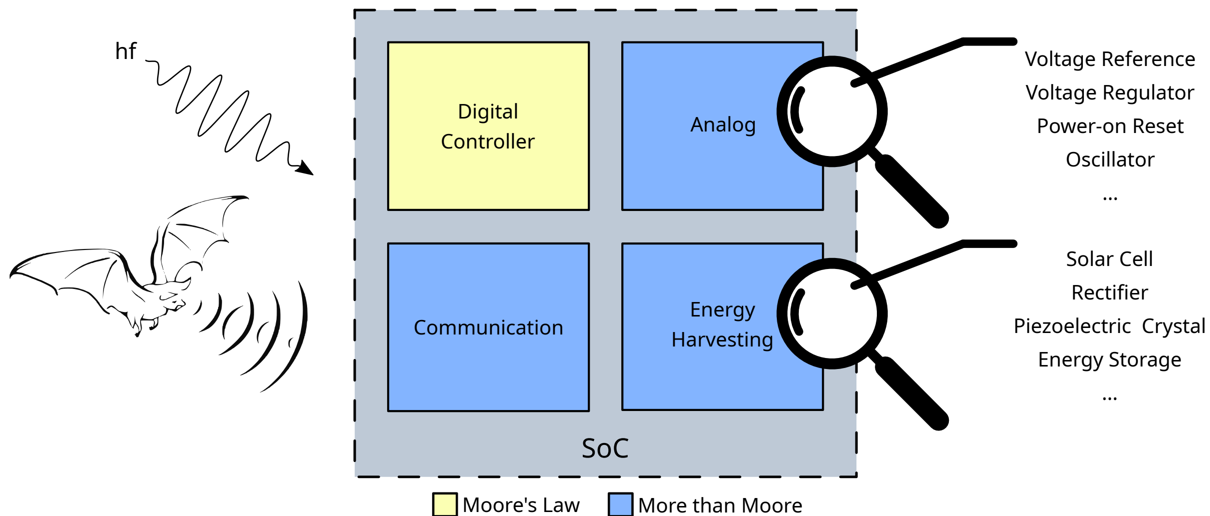


Figure 1.1.: Building blocks of fully integrated autonomous system-on-chips with wireless energy and data transmission.

1.1. Research Scope and Contribution

This thesis investigates the integration of energy autonomous systems into a single ASIC, including a power management system and a communication interface. A key aspect is ultrasonic and solar energy transmission including data transfer using as few external components as possible. This work presents three different applications, with individually designed and manufactured ASICs for their best performance in the particular use case. As a result, the following research questions are dealt with and answered:

- **How to minimize the overall system size using autonomous self-powered SoCs?** A smaller system allows new areas of application that can be accessed as a result of the reduced size.

- **Is it possible to integrate autonomous SoCs with wireless energy and data transmission into a single ASIC?** More than Moore technologies provide a suitable basis for the integration of such systems into a single ASIC.

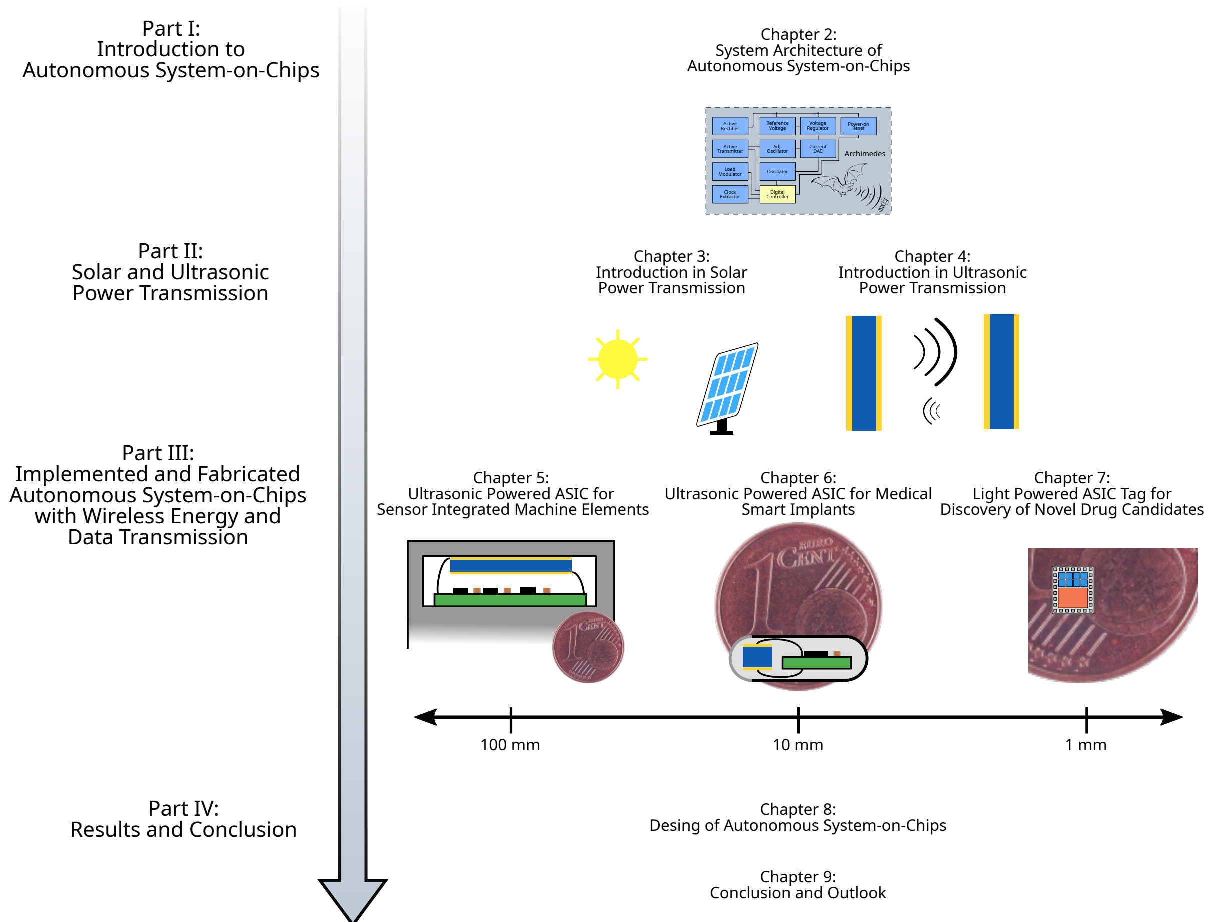


Figure 1.2.: Outline of this thesis.

- **How can the power supply be integrated into the ASIC?** External elements like antennas or solar cells consume a large area of the system. Integration directly on the ASIC would decrease the overall system size significantly.
- **How to counteract light-induced leakage currents on the ASIC?** Light generates leakage currents on a p-n junction in the ASIC causing low power circuits to consume more energy than necessary.

1.2. Thesis Outline

The outline of this thesis is illustrated in Figure 1.2. After the brief introduction in Part I, Chapter 2 focuses on the general system architecture of autonomous integrated systems and explains the required system components for integration. Part II introduces ultrasound and solar energy harvesting for ASICs in Chapters 3 and 4.
Part III presents four manufactured ASICs, each designed for a different application. Chapter 5 shows an ultrasonic-powered SiMe. It is optimized for high energy transfer, as well as high data throughput. Chapter 6 introduces a smart implant powered by ultrasound. Due to a size limit of $2\,\mathrm{mm} \times 2\,\mathrm{mm} \times 10\,\mathrm{mm}$, the ASIC integrates everything except a piezoelectric crystal and an energy storage. Because of the small piezoelectric crystal, the system focuses particularly on low power consumption. Chapter 7 presents the smallest system in this thesis that does not need any external components. It integrates all necessary components like energy harvesting, communication, and memory into one single ASIC. Its energy supply and communication are based on visible light, making the system extremely small, with an area of only $8.16\,\mathrm{mm}^2$. Particular focus is put on low power consumption and light-induced leakage.
Part IV presents the findings of the fabricated ASICs. Chapter 8 gives recommendations for designing autonomous systems with wireless energy and data transmission on an ASIC scale. Finally, Chapter 9 concludes the presented designs and gives an outlook for future developments and research in this field.

2. System Architecture of Autonomous System-on-Chips

Autonomous SoCs with wireless energy and data transmission in space-limited applications require a high degree of integration to fit the system in the designated place. These systems cover various application areas, such as ultrasonic implants for the human body to record health data or wirelessly powered integrated machine elements to monitor a machine [8, 9]. This chapter provides a brief overview of wireless power transfer techniques and the integrated components in the SoC. Figure 2.1 shows the general system architecture of an autonomous SoC.

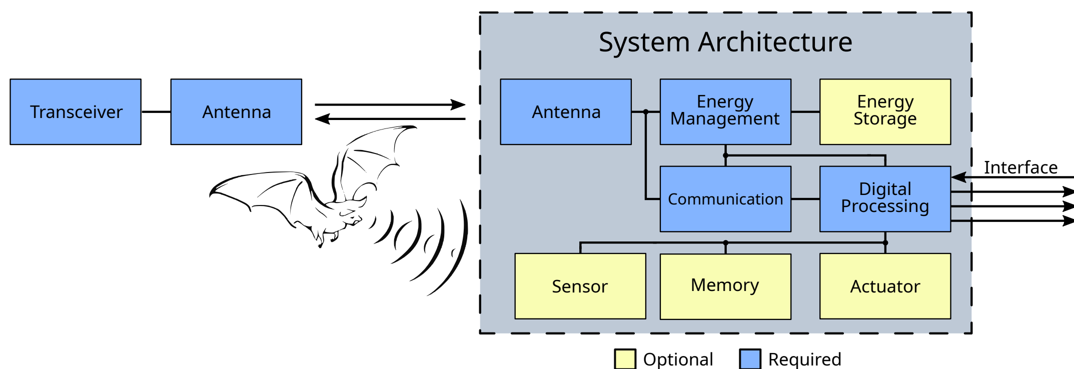


Figure 2.1.: System architecture for energy autonomous SoCs with wireless energy and data transmission and the required and optional components.

These systems have a similar architecture as a basis, including an external transceiver for energy and data transmission. It requires an antenna to receive the energy and the data sent by the external host. Connected to the antenna is an energy management circuit, to convert the power received by the antenna to voltages suitable for the ASIC. In most cases, this circuit has to rectify an **A**lternating **C**urrent (AC) voltage and stabilize it. Additionally, reference voltages are often required for supplying sensitive analog circuitry. An energy storage might be necessary, depending on the application of the system and the continuity and quantity of the delivered power. Besides energy, the antenna also receives data for communication. It is the purpose of the communication module to decode the received data. If bidirectional communication is desired, the module also has to include a transmitter. A digital processing circuit is implemented to process the received data and if necessary to execute received commands. It can consist of

a state machine, particularly designed for one purpose, or a microcontroller, which gives more flexibility. Depending on the application, the digital processing unit can connect various optional internal or external components, including but not limited to sensors, memories, or actuators. The following Section 2.1 introduces different wireless power transfer methods, while Section 2.2 explains the required components in such systems.

2.1. Wireless Power Transfer

There are multiple methods to supply integrated autonomous SoC with wireless power, but not all of them are suitable for energy transmission. Subsequently, different wireless power transfer techniques are summarized and rated with regard to the suitability for integrated autonomous SoCs.

2.1.1. Inductive Coupling

Inductive power transfer is widely used as energy transfer in household appliances, like toothbrushes or the well-known Qi interface standard for wireless power transfer [10]. It is based on Faraday's law of induction, discovered in 1831 by Michael Faraday [11]. A magnetic field is generated with a wire coil, while a second coil converts the magnetic field back to an AC voltage. A study for biomedical implants shows that for small systems, which are of particular interest in this thesis, inductive energy transfer is outperformed by ultrasonic energy transfer for receiver diameters smaller than $3\,\mathrm{mm}$. At source-receiver distances higher than $14\,\mathrm{mm}$, ultrasound is even more efficient than receivers with a size of $5\,\mathrm{mm}$ or smaller [12].

2.1.2. Capacitive Coupling

Capacitive coupling between two electrodes uses the electric field to transfer energy. The transmitter electrode plates are driven with a high frequency AC voltage, which induces a voltage on the receiver plate. Although this technique is rarely used for end-consumer products due to the high voltage and frequency required, recent research has shown capacitively coupled power transfer techniques for low power implants [13, 14]. For capacitive plates with a size of $20\,\mathrm{mm} \times 20\,\mathrm{mm}$ and a distance of $3\,\mathrm{mm}$, a power transmission of up to $100\,\mathrm{mW}$ was achieved in compliance with safety guidelines for human tissue [15].

2.1.3. Ultrasound

Sound waves with a frequency of more than $20\,\mathrm{kHz}$ are called ultrasonic waves. Ultrasound is known for measuring distances, detecting objects, cleaning objects, or as a non-invasive imaging tool in medicine [16]. Piezoelectric crystals provide an efficient method for converting electrical signals into ultrasonic waves and vice versa. For frequencies above around $1\,\mathrm{MHz}$, piezoelectric crystals become small enough, i.e. longest dimension below $1\,\mathrm{mm}$, to be used as power and

communication device in the human body. For example, a piezoelectric crystal cube with an edge length of $750\,\mu m$ at a frequency of $1.85\,MHz$ can receive up to $350\,\mu W$, in compliance with the U.S. **F**ood and **D**rug **A**dministration (FDA) safe density limit of $7.2\,mW\,mm^{-2}$ for the transmitter [17].

2.1.4. Electromagnetic Waves

History has given different names for the electromagnetic spectrum. Sorted from a long to short wavelength, it includes radio waves, microwaves, infrared light, visible light, ultraviolet light, X-rays, and gamma rays [18]. Radio waves, microwaves, infrared, and visible light in limited intensity are considered harmless to most organisms including the human body. Therefore, these electromagnetic waves represent a possible transmission medium and are considered in more detail.

Radio Waves and Microwaves

In 1887 Heinrich Hertz discovered the existence of radio waves [19]. The size of antennas required for an efficient transmission for radio and microwaves depends on the wavelength and the antenna type. An often-used dipole antenna needs a wire length of half the wavelength, which results in an antenna length in the range of a few mm to one meter. Increasing the frequency and hereby decreasing the antenna size is an option, but the attenuation of the electromagnetic wave in human tissue will increase with the frequency. Small implants proved to work with a harvesting coil diameter of $2\,mm$ at a depth of $5\,cm$ while receiving a power of $200\,\mu W$ at a transmit power of $500\,mW$ [20].

Infrared and Visible Light

Infrared and visible light have a wavelength from $400\,nm$ to $10\,\mu m$. To receive and convert light to electricity, solar cells offer a high energy conversion efficiency. Additionally, solar cells can be directly integrated into an ASIC due to the silicon substrate. Energy densities of up to $12\,W\,cm^{-2}$ are demonstrated. By increasing the light intensity higher energy densities are possible, practically only limited by the heating of the ASIC by the incident light [21].

2.2. Required Components in Wireless-Powered ASICs

The previously mentioned architecture of wirelessly powered SoCs is divided into four major building blocks, shown in Figure 2.2. The antenna converts the received energy, which could be electromagnetic waves or a different method, into an electrical voltage. The subsequent energy management block provides a stable **D**irect **C**urrent (DC) voltage for the operating circuit. It usually includes a rectifier circuit, a **L**ow-**D**rop**o**ut (LDO), and a reference voltage generator, as well as an energy storage. A communication module incorporates a receiver and transmitter to implement a bidirectional communication interface. At last, a digital processing block handles

communication and potential additional tasks like sensor management. The following subsections will dive into further detail of each building block.

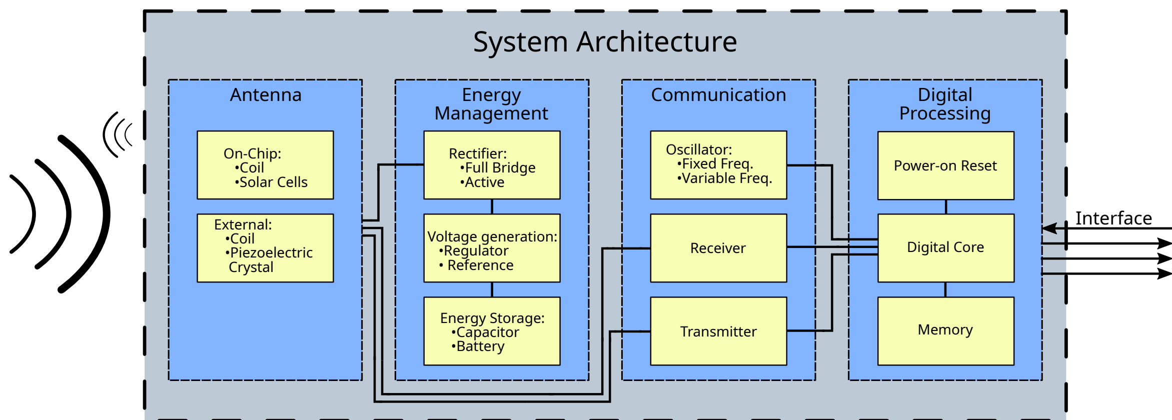


Figure 2.2.: Detailed building block for wireless-powered SoCs.

2.2.1. Antenna

In general, there are two possibilities for placing the antenna: On-chip antennas (internal) integrated into the system or off-chip antennas (external) as an additional device connected to the system. On-chip antennas have the big advantage of being very small compared to external ones, at the expense of energy efficiency and maximum range.

Internal

A standard CMOS process only allows coils or solar cells as a direct implementation. It limits the received signals to electromagnetic waves for the wavelength of radio waves, microwaves, and light. In each case the die size limits the maximum size of the antenna, leading to a small energy yield.

External

External antennas extend the application area to other transmission methods like ultrasound by using a piezoelectric crystal or inductive and capacitive coupling at the expense of a larger device. Additionally, larger antennas have a higher sensitivity compared to internal antennas and can therefore still work with lower energy densities.

2.2.2. Energy Management

The energy received by the antenna is often a high frequency AC voltage with low amplitude, therefore the first block for energy management is a rectification circuit. This is not a requirement if solar cells are used. The rectified voltage needs an LDO for stabilization. Additional voltage references provide an accurate voltage for the analog components. The optional energy storage provides a stable voltage or energy for the ASIC in phases without active energy transmission or for short bursts of increased power consumption i.e. sensor activation or data transmission.

Rectifier

As mentioned previously most methods using an antenna will convert the input to a high frequency AC voltage with low amplitude and require a rectification circuit. In general, there are two possibilities for rectifying an AC voltage: passive or active rectification circuits. Passive rectification with diodes is simple and reliable but lowers the output voltage by at least one diode drop voltage. For a full bridge rectifier with two diodes in the conduction path, it increases the voltage drop to two diode drop voltages. That would decrease the obtainable output voltage by approximately $0.7\,\mathrm{V}$ or $1.4\,\mathrm{V}$ for silicon diodes. While Schottky diodes would have a lower drop voltage they are often not available in CMOS processes. This would limit the usable energy significantly and decrease the overall energy efficiency. An active rectifier can replace the diodes with transistors, lowering the drop voltage significantly. Naturally, the active control mechanism has to be fast enough to switch the transistors according to the AC voltage, which makes it hard to build active rectifiers for **R**adio **F**requency (RF) applications that have very high frequencies. However, this is a common choice for ultrasound applications as they operate with lower frequencies [22].

Reference Voltage Generation

Analog and digital circuitry need a stable supply voltage to operate in the given specifications. A reference voltage circuit can provide a stable voltage reference to the ASIC. Depending on the necessary precision of the reference voltage and the allowed maximum power dissipation, a solely **M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor (MOSFET)-based reference or a more stable bandgap voltage reference is suitable. Compared to bandgap voltage references, a MOSFET-based reference usually has a smaller area and a lower power consumption [23]. If precision is the main concern and power or area are less important, a bandgap reference has a more process-robust reference voltage [24]. Since the reference circuits usually operate with a constant current, a bias current can be derived for components on the ASIC. Important to note here is that these currents usually are not temperature compensated. With a working reference voltage, an LDO can supply the circuit with a stable supply voltage.

Energy Storage

If the application has phases with no active power transmission or short bursts with high power consumption, an energy storage has to supply the system to prevent a non-intermittent operation.

Since on-chip capacitors are usually only fabricable in the range of a few picofarads, this will only allow the charge to be buffered for a short time. Therefore, an external solution is unavoidable for buffering the supply voltage for longer times. In general, three different technologies as an external energy storage exist that are suitable for energy autonomous systems: (super)capacitors, rechargeable batteries, or primary batteries. The systems developed in this thesis receive energy wirelessly. Since primary batteries cannot be recharged, they are not suitable for the task of momentary energy storage and are therefore not further discussed here. Supercapacitors are a form of capacitors with a higher energy density compared to a ceramic or electrolytic capacitor. However, supercapacitors have a higher **E**quivalent **S**eries **R**esistance (ESR) and subsequently a lower maximum charge and discharge rate, which is not a significant problem in this application since our overall currents are small [25]. The self-discharge rate is typically around $1.8\,\%$ per day, making a supercapacitor realistically suitable for storing energy for about one month [26]. The energy density is low, with only up to $10\,\mathrm{W\,h\,L^{-1}}$, compared to a modern lithium-ion battery cell with up to $100\,\mathrm{W\,h\,L^{-1}}$ for small-sized cells [27, 28]. Additionally, lithium-ion batteries have a lower self-discharge rate of about $4\,\%$ per month. In terms of cycle life, a supercapacitor can reach more than 50000 cycles, whereas a lithium-ion battery can survive up to 5000 cycles [25].

In summary, there exist two different energy storage technologies that are suitable for energy autonomous systems. A capacitor may be sufficient for systems with only short operation times. For higher operation times in the range of days, higher cycle lifetime, or broader temperature range a supercapacitor is preferred. For systems that need to operate without an external power transmission for longer than a month, rechargeable batteries feature a higher energy density or a more compact solution.

2.2.3. Communication

To establish a communication with the SoC, a receiver and transmitter are required. Additionally, a clock source for transmitting data is necessary.

Receiver

A receiver decodes the data from the wireless transmission path. In many applications, the data rate to the SoC has a low priority since only simple commands are sent to the system. The energy consumption and chip area on the other hand play a major role, making an easy decodable modulation like **O**n-**O**ff **K**eying (OOK) preferable.

Transmitter

The transmitter handles the encoding and physical output to the antenna to send data over the transmission path. In general, two different transmission schemes are possible: Either an active or a passive transmission scheme. The active transmission possesses a power amplifier and actively transmits bursts of power to the antenna containing the data payload. If power requirements do not permit the active scheme, a passive data transmission can manipulate the incoming waveform

and change the reflected signal. This is called backscatter communication. While this requires less energy than an active transmission, the achievable data rate and range usually decrease compared to an active transmission. Also, the active external transducer has to detect changes in the reflectivity to decode the returned data.

Oscillator

The oscillator provides a constant frequency to the receiver, transmitter, and digital core. It typically operates with a frequency below $10\,\mathrm{MHz}$ to minimize system power consumption due to switching losses. LC oscillators and ring oscillators typically operate in much higher frequencies while the LC oscillator requires an additional on-chip inductor. Crystal oscillators always need a large external crystal and thus are unsuitable for energy autonomous systems. For frequencies below $10\,\mathrm{MHz}$, relaxation oscillators are a common choice because of their low power consumption [29]. The frequency can be made adjustable by tuning the input current of the relaxation oscillator, making it especially useful for generating a signal for a **F**requency **M**odulation (FM) transmitter.

2.2.4. Digital Processing

The digital processing block controls the entire SoC, including receiving and transmitting data, evaluating sensor data, and handling the power management circuit. Additional analog blocks for generating a power-on reset and an optional memory are possible.

Power-on Reset

At the start-up of the SoC, the digital core needs a proper power-on reset. Different kinds of reset systems have to be implemented, depending on the power source and application. For the ultrasonic-powered systems presented in this thesis, a classical voltage-sensitive circuit detects a rising supply voltage and releases a reset signal after an additional delay. A voltage-sensitive power-on reset is not sufficient for light-powered systems because of the voltage-current characteristic of solar cells. Here, a resistive load checks if enough power is present. If that is the case, the power-on reset releases the circuit.

Digital Core

All implemented digital cores in this thesis are synthesized from Verilog code. A place and route tool transfers the synthesized netlist to a layout integrated into the SoC. They incorporate multiple state machines to fulfill the individual tasks. The clock frequency is as low as possible, in this thesis below $500\,\mathrm{kHz}$, to save as much power as possible. Besides controlling the receive and transmit process of the SoC, the digital core has an external interface for debugging or to connect an external microcontroller for further functionality. This microcontroller can use the SoC as a power source and data transceiver. If the application requires a high amount of memory, an additional memory interface for external memory can be integrated.

Memory

Depending on the application, the digital core needs external or internal memory. In general, two types of integrated memory exist: Volatile memory like **S**tatic **R**andom-**A**ccess **M**emory (SRAM) or **D**ynamic **R**andom **A**ccess **M**emory (DRAM), which loses its information without power, and **N**on-**V**olatile **M**emory (NVM), which can retain its data without a power source. Since electrical power is usually not constantly available in energy autonomous systems, this section focuses on NVMs. NVMs are divided into two kinds of memories: **O**ne-**T**ime-**P**rogrammable (OTP) memory, which can programmed only once, or an **M**ultiple-**T**ime-**P**rogrammable (MTP) memory, which allows multiple program cycles [30, 31]. **E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory (EEPROM) and flash memory belong to the MTP category and are available in many technologies. By depositing a charge on a floating gate, the threshold voltage of a MOSFET changes, and thus the stored information persists. The stored information can be deleted by removing the charge trapped on the floating gate. In contrast to an MTP memory, an OTP memory stores the information by changing a device permanently, typically by a controlled destruction of a specific device for writing data. The information is then readable an infinite number of times from the device. As storing elements, Zener diodes, metal traces, and gate oxides are possible. Unfortunately, burning Zener diodes or metal tracks is an energy-intensive task that typically involves currents in the milliampere range. These high currents are not available in wireless-powered ASICs and are therefore unsuitable for this type of system. Implementing an EEPROM or destroying gate oxides for the creation of an OTP on the other hand, requires only currents in the range of microamperes. Unfortunately, storing charge on an EEPROM cell or destroying gate oxides requires a high voltage ranging from $5\,\mathrm{V}$ to $15\,\mathrm{V}$ for typical process technologies. If this voltage is not available in the system, a charge pump is required to generate the high voltages.

Part II.

Solar and Ultrasonic Power Transmission

3. Introduction to Solar Power Transmission

In 1839, A. E. Becquerel discovered the photovoltaic effect by illuminating a junction between an electrode and an electrolyte [32]. In 1905, A. Einstein proposed the idea of photons, which distribute the energy of light discontinuous in space instead of a continuous energy distribution, explaining Becquerel observations [33]. 35 years later, in 1940, R. Ohl demonstrated the first p-n junction, which generated a substantial voltage with the photovoltaic effect, leading to the first solar cell [34]. Only nine years later, in 1949, W. Shockley proposed a theory on p-n junctions, enabling the development of the bipolar transistor and subsequently many modern semiconductor devices [35, 36]. Today, solar cells are widely used as a source of renewable energies and are the primary means to directly convert sunlight to electricity. Photodiodes are based on the same working principle but are optimized for sensor applications to detect light. Therefore they are widely used in optical communication systems.

3.1. Photoelectric Effect

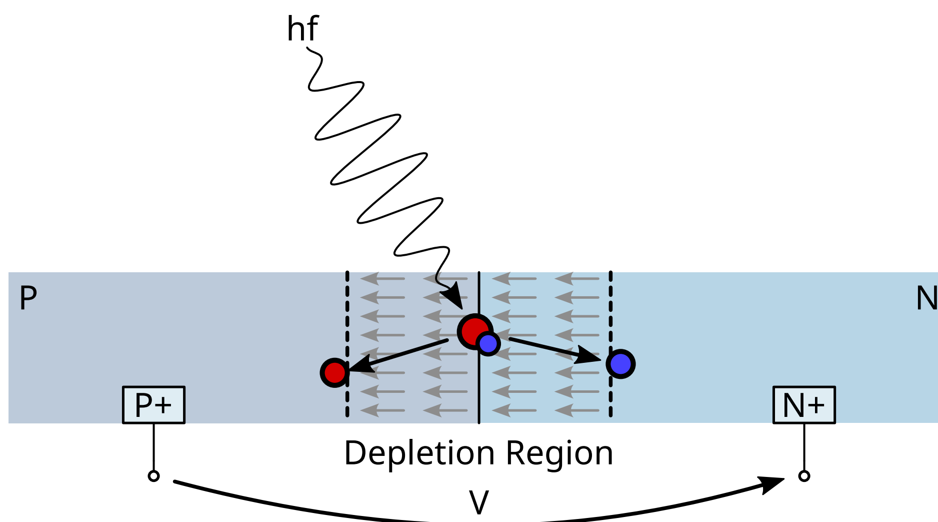


Figure 3.1.: Sectional view of a solar cell. A photon with sufficient energy (E=hf) excites a carrier, generating a photocurrent.

The photoelectric effect can be divided into two different effects: The external and the internal photoelectric effect. The external photoelectric effect describes the emission of electrons from a metal surface caused by the irradiation with **U**ltra**v**iolet (UV) light. The internal photoelectric effect, present in semiconductors, describes the generation of electron-hole pairs from photons. This effect can also occur for photons with a wavelength longer than UV light. Therefore, it is suitable for electrical energy generation from the sun. Figure 3.1 shows a sectional view of a basic solar cell or photodiode. It consists of a n- and p-doped semiconductor. When a photon excites an atom within a depletion region of a semiconductor, an electron will drift to the n-doped area, while the remaining hole drifts to the p-doped area. Since an electron is negatively charged and an atom missing an electron (the hole) is positively charged, the transfer of charges is considered a current. In this case, the generated current is called photocurrent. It is proportional to the incident illumination in a wide operating range. The ratio of incident light photons to generated electron-hole pairs is called the quantum efficiency. It depends on the device's dimensions, the doping concentration, how much light enters the semiconductor, the light wavelength, and many other parameters. Solar cells and photodiodes are basically from the same construction type, whereas solar cells are optimized for high energy conversion efficiency at a broad solar spectrum while photodiodes are designed for high quantum efficiency and low capacitance for high response speeds. The wavelength and the material determine how deep light penetrates the solar cell. Silicon as a typical semiconductor, has a light penetration depth of $1\,\mu m$ to $10\,\mu m$ in the visible light range from about $400\,nm$ to $780\,nm$ [37]. To excite an electron, the depletion region must be in the same depth as the light penetration depth to contribute to the photocurrent.

3.2. Simulation Model and Equivalent Circuit of a Solar Cell

For developing integrated solar cells, a working simulation model for a solar cell in a circuit is required, and thus an equivalent circuit. Figure 3.2(a) shows a solar cell with a connected load resistance R_L. Figure 3.2(b) substitutes the solar cell with an equivalent circuit, consisting of the ideal current source I_L in parallel with an ideal diode D_1. The current I_L derives from the excitation of electron-hole pairs, while the current I_D derives from the Shockley diode equation.

Figure 3.2.: Equivalent circuit for solar cells. Figure (a) shows a solar cell with a connected load resistance, and Figure (b) an equivalent circuit consisting of an ideal current source and a diode substituting the solar cell.

I_L can be calculated using

$$I_L(E_g) = Ae \int_{hf=E_g}^{\infty} \frac{d\Phi}{dhf} d(hf) \tag{3.1}$$

where A is the area of the solar cell, e the elementary charge, h the Planck constant, f the frequency of the photon, E_g the bandgap of the semiconductor, and Φ the photon flux density [37]. This simplified equation neglects the quantum efficiency of a real solar cell. The integral counts every photon with an energy higher than the bandgap of the semiconductor and adds one electron to the output current I_L.

The current through diode D_1 can be described by the Shockley diode equation [35]. By using Kirchhoff's law, the output current over the solar cell voltage can be expressed as follows [38]:

$$I = I_L - I_s \left(exp^{\left(\frac{eV}{kT}\right)} - 1 \right) \tag{3.2}$$

where I_s is the reverse-bias saturation current, k the Boltzmann constant, T the absolute temperature of the p-n junction, and V the voltage over the diode. With this equation, a characteristic load line can be simulated. Figure 3.3 shows the simulated load line for two different light intensities. The maximum power point is shown in green for the high illumination intensity. This point represents the maximal power output from the solar cell when the product of cell voltage and cell current reaches its maximum. It changes with the temperature and light intensity of the solar cell. Therefore, in solar power plants, an **M**aximum **P**ower **P**oint **T**racking (MPPT) algorithm changes the load to reach the maximum power output. I_{SC} marks the short circuit current, and V_{OC} the open circuit voltage of a solar cell, which is typically around $0.6\,\mathrm{V}$ to $0.7\,\mathrm{V}$ for silicon-based cells.

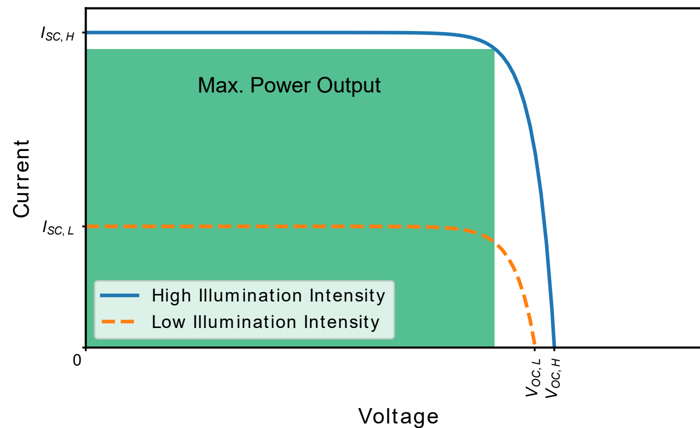


Figure 3.3.: Load line of a typical solar cell. It shows the current generated for two different light intensities and the maximum power point in green.

By adding a shunt resistor in parallel to the diode and a series resistor to the output in the equivalent circuit, more parasitic effects of a solar cell are modeled. Figure 3.4 shows the two

additional resistors. The parallel shunt resistor R_{SH} models defects in the crystal, non-ideal doping profiles, and other material defects that can lead to increased leakage currents in the p-n junction. Usually, this resistance is relatively high compared to the series resistance. The series resistance R_s models the resistance of the semiconductor material and contact resistances [39].

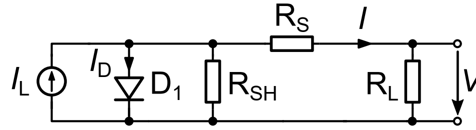


Figure 3.4.: Equivalent circuit for solar cells including a parallel and serial resistance for modeling parasitic effects.

Equation 3.2 can be extended with a parallel and series resistor to account for the additional parasitic effects, which results in the following equation:

$$I = I_L - \left(\frac{V + IR_S}{R_{SH}}\right) - I_s\left(exp^{\left(\frac{q(V+IR_S)}{kT}\right)} - 1\right) \tag{3.3}$$

3.3. Solar Cells for Integrated Circuits

Normal solar cells are manufactured in a specially created process, solely optimized for the highest power conversion efficiency and longevity of the produced solar cells. A typical CMOS process is optimized for the best transistor properties or the smallest gate length and not for solar cells. Therefore, the options for implementing solar cells are limited in a CMOS process. Figure 3.5 shows three different solar cell structures implementable in most CMOS processes. The typical light penetration depth for visible light is around 2 µm and every solar cell structure has a different p-n junction depth. The junction depth should be near the light penetration for a good-performing solar cell. Among other parameters like doping concentration and doping profile, the junction depth gives every solar cell a unique quantum efficiency. The resulting efficiency can only be measured on a fabricated ASIC since the exact manufacturing parameters are usually classified by the manufacturing fab and are unknown to an IC designer.

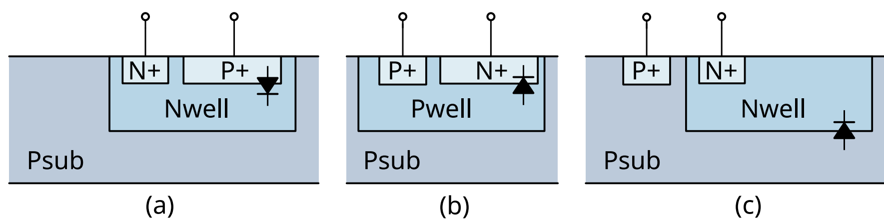


Figure 3.5.: Available solar cells in CMOS technologies: (a) Nwell/P+, (b) N+/Pwell, (c) Nwell/P-sub.

4. Introduction to Ultrasonic Power Transmission

The discovery of the piezoelectric effect dates back to 1880 when Jacques and Pierre Curie discovered that a mechanical deformation of tourmaline can cause the formation of an electrical voltage [40]. Since then, piezoelectric crystals have been used in a variety of applications such as crystal oscillators, ultrasound transducers, and sensors [41, 42, 43]. Figure 4.1 shows the simplified inner structure of a piezoelectric crystal lattice consisting of silicon and oxygen atoms. Since oxygen is more strongly electronegative than silicon, oxygen can be viewed as weakly negatively ionized while silicon is weakly positively ionized. A conductive coating on the top and bottom of the piezoelectric crystal provides a contact electrode. In Figure 4.1(a), the crystal is without any external loads, whereas a mechanical force compresses the crystal in Figure 4.1(b). Compressing the crystal with an external force shifts the positive charges C_{Q+} of the silicon atom, as well as the negative charges C_{Q-} of the oxygen atom. Where in 4.1(a), the charges C_{Q+} and C_{Q-} are congruent, in 4.1(b), the charges C_{Q+} and C_{Q-} are separated from each other, and an electrical voltage is measurable on the electrodes due to the charge displacements. A piezoelectric crystal can convert an electrical input to a mechanical output and vice versa. Conversion from the mechanical to the electrical domain is named the direct piezoelectric effect, while the conversion from the electrical to the mechanical domain is referred to as the inverse piezoelectric effect [44].

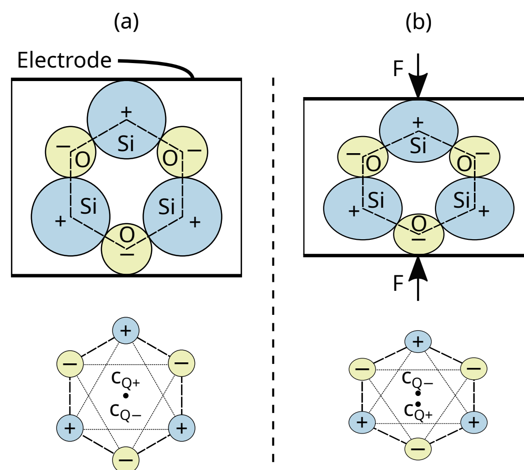


Figure 4.1.: Inner structure of a piezoelectric crystal consisting of silicon and oxygen. The left side (a) shows the crystal with no external mechanical force applied, while on the right side (b) a mechanical force is applied at the electrical contacts [44].

4.1. Equivalent Circuit

To model the behavior of a piezoelectric crystal in an electrical circuit, an equivalent circuit is required. In 1928, K. S. Van Dyke proposed the equivalent circuit shown in Figure 4.2. It consists of only four circuit elements, a parallel capacitor C_0 and a damped series resonant circuit $R_1L_1C_1$ [45]. Therefore, it only models the first and second resonance of a piezoelectric crystal, namely the series resonance of the series $R_1L_1C_1$ branch and a parallel resonance consisting of C_0 and $R_1L_1C_1$.

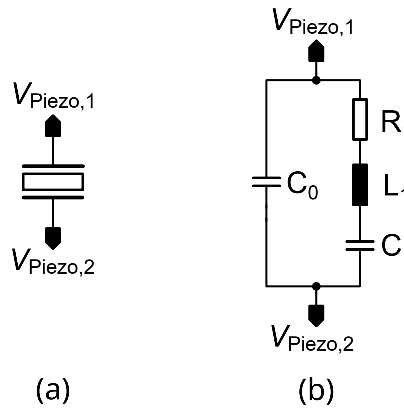


Figure 4.2.: Electrical equivalent circuit for a piezoelectric crystal.

A typical piezoelectric crystal impedance curve is shown in Figure 4.3. The basis is the Van Dyke equivalent circuit and it shows a series resonance f_s at about $600\,\mathrm{kHz}$ and a parallel resonance f_p at $840\,\mathrm{kHz}$. Resonances of higher orders are possible to model, by adding additional RLC resonance circuits in parallel to the existing circuit. The series resonance frequency enables a high power transmission with a piezoelectric crystal at low driving voltages due to the minimum impedance of the piezoelectric crystal at that frequency. Whereas the parallel resonance frequency has a maximum impedance at that frequency, making it ideal for receiving weak signals with a high voltage output.

4.2. Calculation of the Resonance Frequencies

The resonance frequency of a piezoelectric crystal is the preferred frequency for energy and data transmission. For a piezoelectric crystal disc in thickness extensional mode, where the diameter is d is at least ten times higher than the thickness of the piezoelectric crystal disc τ_x, it can be assumed that the resonance frequency is proportional to its thickness [44]. With the following equation, the resonance frequency f_r of a piezoelectric crystal disc can be calculated to

$$f_r = \frac{N_r}{\tau_x} \tag{4.1}$$

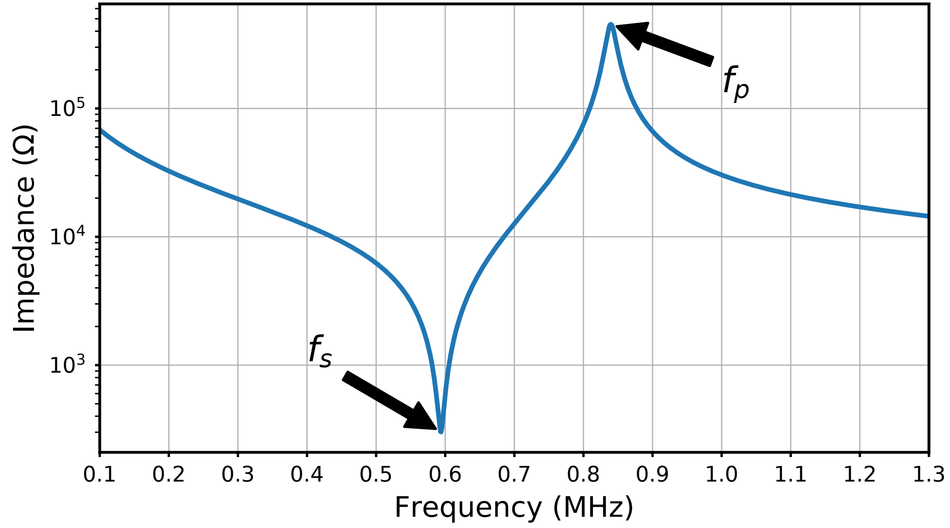


Figure 4.3.: Plot of a piezoelectric crystal impedance based on the Van Dyke equivalent circuit.

with N_r being the frequency constant of the piezoelectric crystal material in $\mathrm{Hz\,m}$. For the PZT-5A piezoelectric material, N_r ranges from $1900\,\mathrm{Hz\,m}$ to $2100\,\mathrm{Hz\,m}$, depending on the exact material type and manufacturer [46]. For piezoelectric crystals, where the diameter d is less than ten times the thickness τ_x, the assumption that the resonance frequency is proportional to its thickness is not valid anymore. For small systems where the piezoelectric crystal limits the miniaturization of the system, a cubical piezoelectric crystal is an often used geometry. R. Holland describes a model for the calculation of the resonance frequency for cubical piezoelectric crystals [47]. With the following approximation, the size of the cubical piezoelectric crystal can be calculated for a given resonance frequency:

$$\tau_x = \frac{\Omega^v}{2 \cdot f_p^v} \cdot \sqrt{\frac{c_{3333}^E}{\rho}} \tag{4.2}$$

τ_x now represents the edge length of the piezoelectric crystal cube, Ω^v the dimensionless eigenfrequency dependent on the oscillation mode, f_p^v the parallel resonance frequency, c_{3333}^E the electroelastic coefficient and ρ the material density of the PZT-5A crystal. v describes different oscillation modes of the piezoelectric crystal. Mode 1 is the correct mode for a parallel resonance and results in 0.629 for $\Omega^{(1)}$. With the electroelastic coefficient c_{3333}^E of $11.1 \times 10^{10}\,\mathrm{N\,m^{-2}}$ and the density of PZT-5A of $7550\,\mathrm{kg\,m^{-3}}$ inserted into Equation 4.2, the edge length of the piezoelectric crystal can be calculated to

$$\tau_x = \frac{0.824}{2 \cdot f_p^{(1)}} \cdot \sqrt{\frac{11.1 \times 10^{10}\,\mathrm{N\,m^{-2}}}{7550\,\mathrm{kg\,m^{-3}}}} = \frac{1579.74\,\mathrm{m\,s^{-1}}}{f_p^{(1)}}. \tag{4.3}$$

The equation demonstrates that the resulting edge length τ_x of the piezoelectric crystal cube is inversely proportional to the resonance frequency $f_p^{(1)}$.

4.3. Measuring Piezoelectric Crystal Parameters

A $50\,\Omega$ matched **V**ector **N**etwork **A**nalyzer (VNA) is used to measure the resonance frequencies of a piezoelectric crystal. Figure 4.4(a) shows the reflection technique which is especially suitable for small impedances around $50\,\Omega$, while the series-through technique is preferred for impedances over $50\,\Omega$, as shown in Figure 4.4(b) [48]. Both techniques require different wiring of the piezoelectric crystal and a different calculation of the resulting impedance since a VNA only calculates the **S**cattering-**p**arameter (S-parameter).

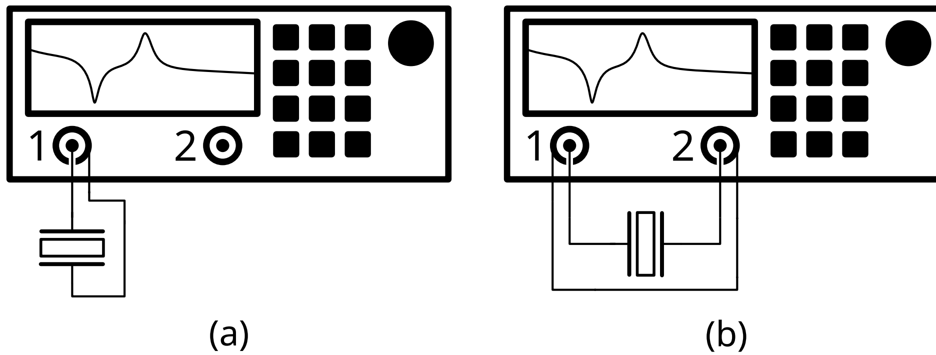


Figure 4.4.: Set up for measuring the impedance of a piezoelectric crystal with a VNA. (a) shows the reflection technique for low-impedance piezoelectric crystals while (b) shows the series-through method for high-impedance piezoelectric crystals.

For measuring the impedance with the reflection technique, the piezoelectric crystal is connected as shown in Figure 4.4(a), and the S_{11} parameter is measured. The result can then be converted to the piezoelectric crystal impedance $Z_{Piezo,Reflection}$ using

$$Z_{Piezo,Reflection} = 50\,\Omega \cdot \frac{1 + S_{11}}{1 - S_{11}}. \tag{4.4}$$

For calculating the resulting impedance of the piezoelectric crystal with the series-through technique, the piezoelectric crystal is connected as shown in Figure 4.4(b). By measuring the S_{21} parameter, $Z_{Piezo,Series-through}$ calculates to [49]

$$Z_{Piezo,Series-through} = 100\,\Omega \cdot \frac{1 - S_{21}}{S_{21}}. \tag{4.5}$$

Part III.

Implemented and Fabricated Autonomous System-on-Chips with Wireless Energy and Data Transmission

5. Ultrasonic Powered ASIC for Sensor Integrated Machine Elements

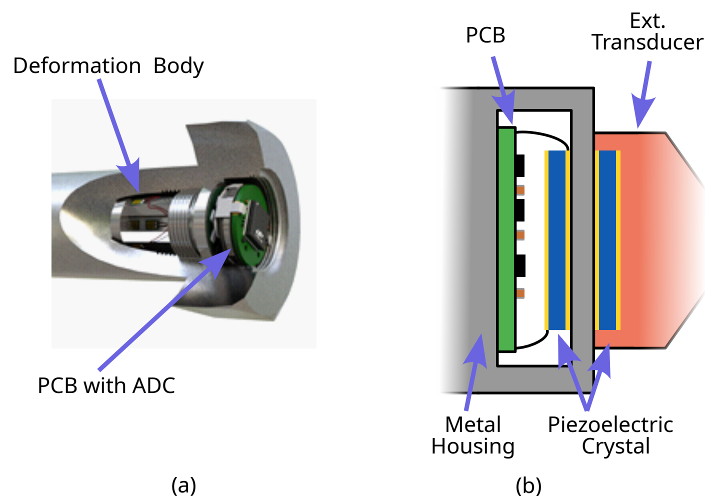


Figure 5.1.: (a) 3D rendering of the sensor integrated bolt [95], (b) Sectional view of the bolts' head with attached ultrasonic transducer.

Forecasting the remaining lifetime of critical machine elements can prevent production downtimes and reduce operating costs. By monitoring individual parts of the machine, the maintenance schedule can be extended, while detecting imminent failures in advance. The monitoring of individual devices can be achieved by a SiMe, embedded directly in the machine element [50, 51]. Usually, a commercially available sensor element is attached to the machine, while an external **A**nalog-to-**D**igital **C**onverter (ADC) reads out the analog signal. An external sensor and evaluation circuit requires a modification of the machine element and routing of cables inside the machine [52]. To avoid a modification of the machine element, a solution with a standardized component is preferred. An example of this can be a standardized bolt developed by Herbst et al. [9]. The developed bolt has an internal multi-axis force sensor for measuring the bolting torque. Three strain gauges are glued on a deformation body inside a cavity in the bolt. The cavity weakens the strength of the bolt by approximately one strength class. The cavity has a size of $12\,\mathrm{mm} \times 20\,\mathrm{mm}$ for the force sensor and $16.4\,\mathrm{mm} \times 6.4\,\mathrm{mm}$ reserved for the electronics [95]. The cavity's cap closes with a metal sheet, forming a Faraday cage. Since the strain gauge's

ADC must measure voltage differences in the range of microvolts, the cavity provides an ideal low-noise environment. Additionally, the metal closed cavity makes the bolt resistant to chemicals or environmental influences. Figure 5.1(a) shows a rendering of the sensor integrated bolt with the integrated strain gauge and the electronic, protected by the closed metal housing. Since the screw is completely encapsulated by metal, wireless energy and data transfer is hardly possible with an RF transmission. Instead, ultrasonic communication and energy transfer are suitable to penetrate the metal housing [53, 54]. Figure 5.1(b) shows a sectional view of the bolt's head. It has an external removable ultrasonic transducer on the outer side and an internal piezoelectric crystal as a receiver. An ASIC for the energy transfer and communication keeps the internal electronic as small as possible.

The focus of this chapter is on the development of the ASIC and on ultrasonic energy and data transmission. The first section covers an ultrasonic bidirectional communication protocol. In the following sections, the ASIC implementation is shown, followed by measurement results and a brief summary. This project is motivated by the DFG priority program 2305 [55], in which different energy harvesting and communication systems for machine elements are evaluated.

5.1. Bidirectional Ultrasonic Communication

The sensor-integrated bolt measures the tightening torque and bending of the bolt and saves it to the internal memory. Additional sensors like temperature and acceleration can be used to detect vibration in the machine. All recorded data are transmitted to the external transducer via ultrasound. The energy required for the transmission and the measurements must first transmitted to the bolt. Therefore, a bidirectional communication for sending commands to the ASIC and receiving the recorded data with an energy transfer is necessary.

5.1.1. Receive Protocol

Figure 5.2 shows the protocol for receiving energy and data with the ASIC. The transmission starts with a charging phase to receive power. The length of this phase depends on how much power can be received and the size of the used energy storage. A typical charging time for a $30\,\mathrm{mF}$ capacitor through a $1\,\mathrm{mm}$ brass sheet is around $3\,\mathrm{s}$. For larger capacitors or batteries, the charging times have to be increased. After the charging phase, a unique start bit is received. The start bit consists of a period t_{chg} without received ultrasound. To create a unique start bit, the period without ultrasound has to be longer than the dead time t_{dt} between single bits. The standard value is 5000 ASIC clock cycles, resulting in around $9\,\mathrm{ms}$. Followed by the start bit, the first data bit is received. The number of ultrasonic pulses encodes the value of each data bit. The standard value is 200 ultrasonic pulses for a zero and 800 ultrasonic pulses for a one. After eight received bits, the transmission is complete. The digital controller will check the correctness of the received data by setting internal boundaries for minimal and maximal length for the start bit as well as dead time and data bits. When all boundaries are met, the digital controller will send a wake-up interrupt to the microcontroller to signal that new data has arrived. The microcontroller wakes up

and can catch data over an integrated **S**erial **P**eripheral **I**nterface (SPI) interface from the ASIC.

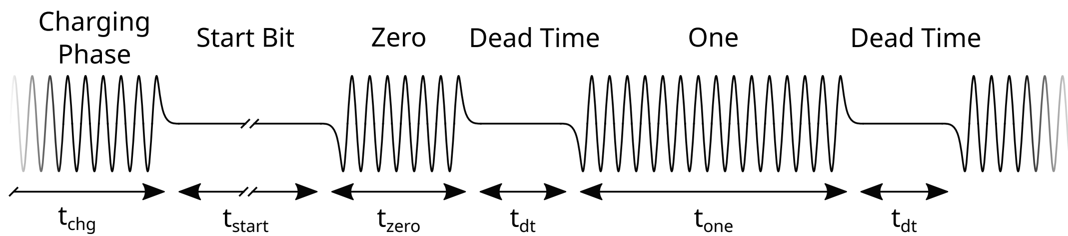


Figure 5.2.: Communication protocol for transmitting energy and data to the ASIC. The exact timing can be adjusted and is dependent on the transmission path as well as the size of the energy storage.

5.1.2. Transmit Protocols

The ASIC implements four different transmission modulations for transmitting data to the external transducer. They are based on backscatter, frequency, amplitude, and resonance modulation. The backscatter protocol does not require an active transmitter circuit and can transmit data passively. The other three protocols, namely frequency, amplitude, and resonance modulation require an active transmission circuit for sending the data.

Backscatter Modulation

Figure 5.3 shows the backscatter protocol implementation. It employs a change in the reflection coefficient of the piezoelectric crystal connected to the ASIC. A switchable load impedance attached to the piezoelectric crystal will change the reflection coefficient and thereby the amplitude of the reflected signal. The length of the transmitted bit t_{zero} or t_{one} decodes the value of a data bit. Between each bit, a dead time t_{dt} separates each data bit. The parameters t_{zero}, t_{dt} and t_{one} are adjustable in length with a 16-bit register from $0\,\mathrm{ms}$ to $119\,\mathrm{ms}$.

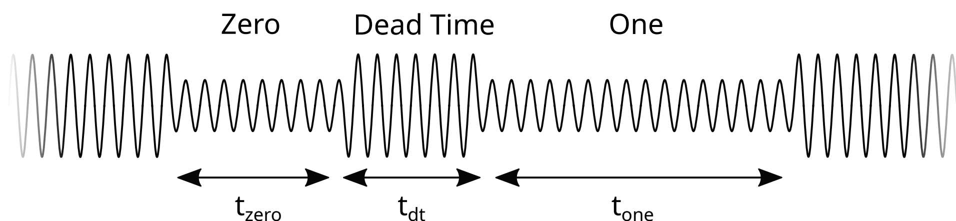


Figure 5.3.: Backscatter communication protocol for transmitting data from the ASIC to an external transducer. The amplitude of the reflected signal is modulated by changing the impedance connected to the piezoelectric crystal.

AM and FM Modulation

The active transmission protocols utilize an on-chip active transmitter. This requires an internal adjustable oscillator for transmitting the data to be calibrated to the piezoelectric crystal resonance frequency. During the receive phase, the microcontroller can start a calibration scheme that calibrates the adjustable oscillator to the ultrasonic frequency. Figure 5.4(a) shows the FM modulation scheme. A one and zero are encoded with the different frequencies f_{zero} and f_{one}, which are programmable in a wide range. The same is valid for the **A**mplitude **M**odulation (AM) modulation scheme, shown in Figure 5.4(b), which uses an OOK modulation. The length of each bit t_{bl} can be user-programmed and range from zero to $119\,\mathrm{ms}$ with a resolution of 16-bit.

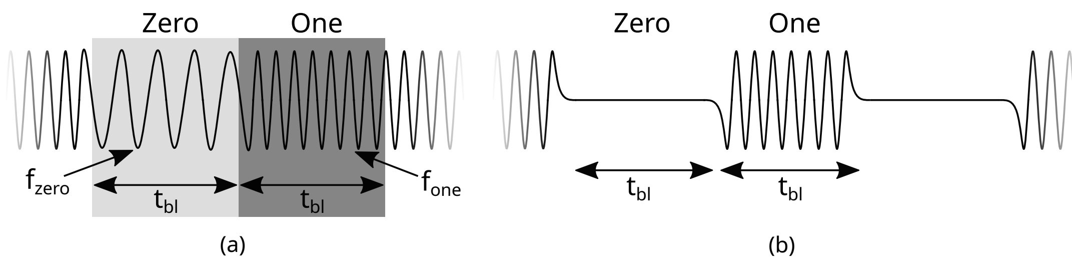


Figure 5.4.: Communication protocol for transmitting data with the ASIC. (a) shows FM communication, and (b) shows AM communication.

Resonance Modulation

The fourth active transmission protocol is the resonance modulation method. When a piezoelectric crystal oscillates free, it resonates at its specific resonance frequency. By actively driving it with a slightly higher or lower frequency, it is forced to oscillate at a different frequency. When active driving is stopped, the piezoelectric crystal starts immediately oscillating in its resonance frequency again. This behavior can be employed for communication. The internal adjustable oscillator is configured slightly below or above the piezoelectric crystal resonance frequency and drives the piezoelectric crystal actively with a frequency offset. Then, the internal adjustable oscillator turns off, and the piezoelectric crystals' oscillation frequency shifts to its resonance frequency. This behavior can be detected by the transducer. Figure 5.5 shows the implemented protocol using a Manchester coding. An active actuated piezoelectric crystal and then free running piezoelectric crystal decodes a one, and a free running piezoelectric crystal followed by an active actuated piezoelectric crystal decodes a zero. The timings for active actuation and free-running oscillation of the piezoelectric crystal can be adjusted from zero to $119\,\mathrm{ms}$ with a resolution of 16-bit. The same applies to the frequency, which can be adjusted with a fine setting of 4-bit and a coarse setting of 5-bit. Section 5.2.1 explains the active transmitter circuit in detail.

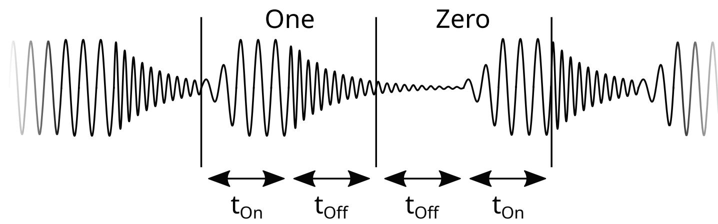


Figure 5.5.: Resonance modulation for receiving data from the ASIC. The piezoelectric crystal is forced to a slightly higher or lower frequency than the resonance frequency during the on period and oscillates freely during the off period.

5.2. Implemented SoC for Sensor Integrated Machine Elements

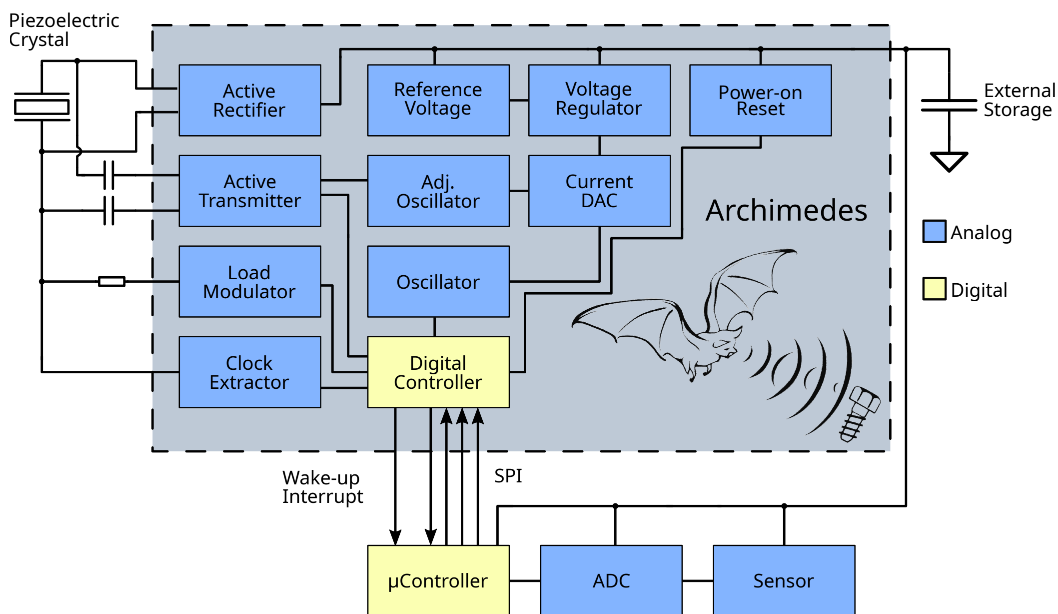


Figure 5.6.: Block diagram overview for the integrated ASIC and optional external ADC and sensors. The external microcontroller for ultrasonic communication is always required.

Figure 5.6 shows the block diagram of the manufactured ASIC. It implements all necessary hardware to enable energy harvesting and communication over ultrasound. The ASIC needs an external microcontroller for controlling the communication interface. ADC and sensors are optional and connected to the microcontroller. The ASIC provides with its active rectifier a DC voltage generated from the AC voltage of the piezoelectric crystal. An external energy storage stabilizes the internal supply voltage. Since the space for the energy storage inside the bolt is

limited to about $200\,\mathrm{mm}^3$, only small-sized components can be used. Depending on the duration without ultrasound and the power consumption of the sensor activity an electrolytic capacitor, a supercapacitor, or a rechargeable battery can be connected. Electrolytic capacitors can supply the electronics for a few seconds, while supercapacitors are a suitable power source for up to one month, limited by the high self-discharge rate of a supercapacitor. A rechargeable battery, however, could allow runtimes for over a year. As an experimental platform, the ASIC provides the hardware for four different transmit protocols, namely three active transmission protocols for amplitude, frequency, and resonance modulation and a load modulation scheme using backscatter. A low data rate is sufficient for sending data to the ASIC since only commands are sent to the ASIC. Therefore, the receive protocol is based on counting ultrasonic pulses, which provides an easy and area-efficient implementation into the ASIC. The ASIC provides an internal voltage reference to generate a reference voltage and current. The LDO creates a constant supply voltage for all internal digital circuits. An adjustable oscillator provides a precise clock signal for the connected piezoelectric crystals' resonance frequency. The digital controller implements an SPI interface for communication with the microcontroller and provides programmable registers for the configuration and control of the ASIC.

5.2.1. Schematic Implementation

Bandgap Voltage Reference

Figure 5.7 shows the implemented schematic of the bandgap voltage reference. It generates the reference voltage for the linear voltage regulator and for the oscillators. M_1 to M_6 form the start-up circuit of the bandgap voltage reference. M_1 and M_5 are zero voltage threshold devices, generating a constant current of $180\,\mathrm{nA}$. At the start-up of the bandgap voltage reference, transistor M_4 is turned on through transistors M_1 and M_2. This will pull the gate of the current mirror M_6 to M_{10} down, starting the bandgap voltage reference. Once it is started, transistor M_6 pulls the input of the inverter formed of M_2 and M_3 high, disabling the start-up circuit. The bandgap voltage reference is based on a standard reference circuit and provides a constant voltage to the internal circuitry [24]. It consists of a current mirror including the operational amplifier and the two bipolar transistors Q_1 and Q_2 with a size ratio of 1:8. Resistor R_4 and transistor Q_3 convert the generated **P**roportional **t**o **A**bsolute **T**emperature (PTAT) current into a temperature-independent voltage. The output voltage is tuned to $1.24\,\mathrm{V}$ at a supply voltage range of $1.4\,\mathrm{V}$ to $3.6\,\mathrm{V}$ at the nominal corner. The current consumption is $3.9\,\mathrm{\mu A}$.

LDO Voltage Regulator

The digital controller requires a constant voltage of typical $1.8\,\mathrm{V}$. Since the voltage generated by the piezoelectric crystal can reach up to $3.6\,\mathrm{V}$, an LDO voltage regulator is implemented. The internal bandgap voltage reference provides a constant voltage of $1.24\,\mathrm{V}$ to the LDO regulator as reference. Therefore, the digital controller operates at a lower voltage, reducing the overall power consumption. The schematic of the LDO voltage regulator is shown in Figure 5.8 and is

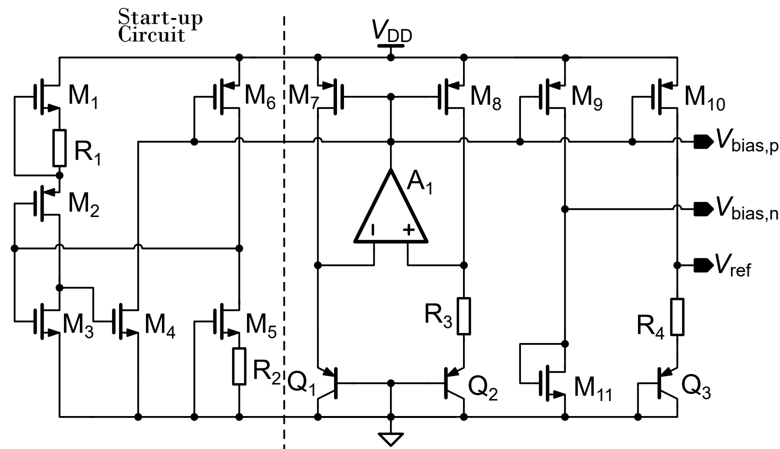


Figure 5.7.: Schematic of the low power bandgap voltage reference including a start-up circuit. It provides a current reference for the oscillator circuit.

based on an LDO regulator with a push-pull output stage [56]. The core of the LDO is built of a push-pull operational amplifier, providing a fast response to counteract load transients as well as a low quiescent current of $1.25\,\mu\mathrm{A}$. The compensation capacitor C_1 ensures stability over an operating range from zero to $1\,\mathrm{mA}$ load current. M_{17} is the p-channel pass transistor. It has the advantage of eliminating the typical voltage drop of n-channel transistor-based LDOs. However, the control loop needs a more careful design to avoid instabilities. It achieves a drop-out voltage of $110\,\mathrm{mV}$ at the maximum output current of $1\,\mathrm{mA}$.

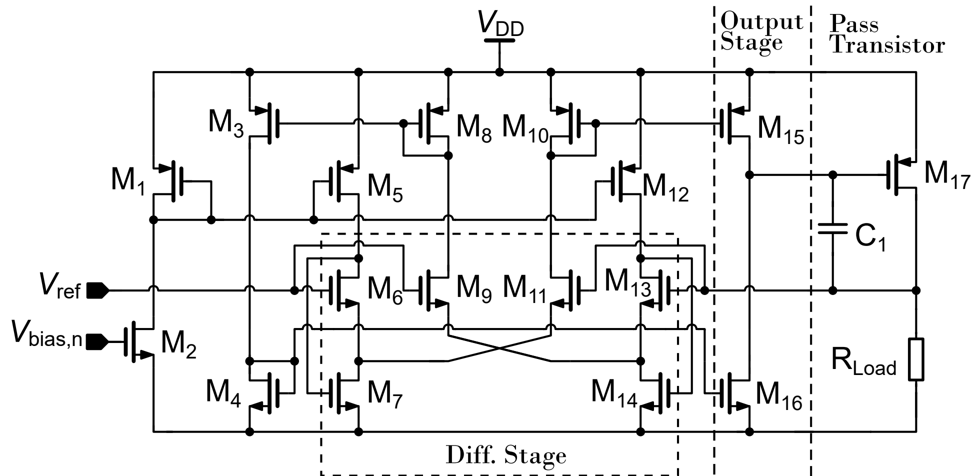


Figure 5.8.: Low-dropout voltage regulator which generates the digital power supply.

Power-on Reset

The power-on reset holds the SiMe in a defined reset state while the supply voltage is below $1.35\,\mathrm{V}$. This assures a proper initialization of the digital controller after the power-up sequence. Figure 5.9 shows the schematic of the power-on reset circuit. V_{LDO} is the $1.24\,\mathrm{V}$ generated by the LDO, whereas V_{DD} is the supply voltage generated by the active rectifier. While V_{DD} is lower than V_{LDO} plus the threshold voltage of transistor M_1, capacitor C_1 is discharged through transistor M_2. This transistor is a zero voltage threshold device, providing a pull-down current of $390\,\mathrm{nA}$, leading to a low reset signal output. During the start-up phase, V_{DD} rises slowly to a voltage between $2\,\mathrm{V}$ to $3\,\mathrm{V}$, while V_{LDO} stabilizes at a voltage of $1.24\,\mathrm{V}$. Once V_{DD} is approximately $100\,\mathrm{mV}$ higher than V_{LDO}, transistor M_1 turns on, charging the capacitor C_1. This will turn transistor M_3 off, allowing capacitor C_2 to discharge through transistor M_4. The discharge current is $10\,\mathrm{nA}$, provided by a bias voltage from the bandgap voltage reference. Discharging of C_2 adds a delay of $75\,\mathrm{\mu s}$ before executing the reset signal through the remaining three inverters and ensures that small spikes in the supply voltage cannot activate the reset signal. Once the reset signal is executed, transistors M_3 and M_5 are both turned off. Therefore, no current flows through transistors M_4 and M_6, disabling the bias currents in these transistors and leading to a current consumption of $390\,\mathrm{nA}$.

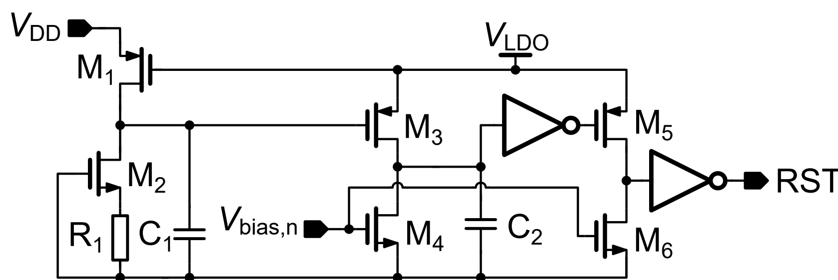


Figure 5.9.: Schematic of the power-on reset circuit. It generates the reset signal for the digital controller.

Active Rectifier

The amount of energy and voltage generated by the piezoelectric crystal is limited. Therefore, an efficient rectification of the generated AC piezoelectric crystal voltage is mandatory. A full bridge diode rectifier consisting of four diodes has a voltage drop of two forward-direction diode voltages. Since a typical CMOS process does not include Schottky diodes, silicon diodes or the body diode of a MOSFET could be used. This leads to an unacceptable high voltage drop of approximately $1.4\,\mathrm{V}$ for the rectifier. To solve this problem, transistors replace the diodes in an active rectifier. Figure 5.10 shows the schematic of the active rectifier implemented in the ASIC. M_7, M_8, M_9, and M_{10} are the rectifying transistors, which connect to the piezoelectric crystal. The p-channel transistors M_7 and M_8 form a cross-coupled connection, which is directly controlled by the piezoelectric crystal. M_9 and M_{10} are the input n-channel transistors with a width of $800\,\mathrm{\mu m}$, whereas the

p-channel input transistor has double its size due to the lower charge carrier mobility. The control circuits input stage consists of transistors M_1, M_2, M_3, and M_4, forming a comparator. If the input voltage generated by the piezoelectric crystals is higher than the current supply voltage V_{DD}, the comparator switches the corresponding transistor M_9 or M_{10} on. The inverters one and two act as an output stage for the comparator. The active rectifier can rectify currents up to $30\,\mathrm{mA}$, enough to charge a supercapacitor or a lithium-ion battery.

By pulling the Dis pin high, the active rectifier enters a low power state and deactivates itself. In this mode, the current consumption enters a low power mode by turning the input n-channel transistors M_9 and M_{10} off. Compared to the active mode with $43\,\mu\mathrm{A}$ quiescent current consumption, the low power mode has only $1.5\,\mu\mathrm{A}$ quiescent current consumption. In the low power mode, a rectification is still possible. The p-channel input transistors are controlled by the piezoelectric crystal, while the n-channel input transistors use the body diode for rectification instead, causing a higher drop voltage.

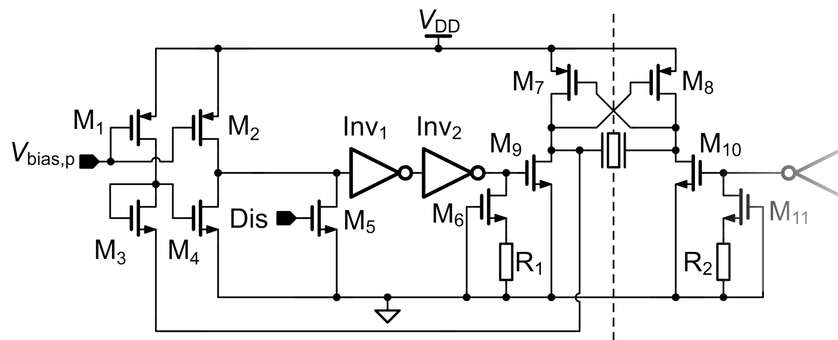


Figure 5.10.: Schematic of the active rectifier for rectifying the AC voltage of the piezoelectric crystal. Compared to a diode full bridge rectifier, it eliminates the diode voltage drop.

RC Oscillator

The on-chip RC oscillator provides a clock for the digital controller, which also samples the piezoelectric crystal clock signal. The minimal clock frequency is $150\,\mathrm{kHz}$, which has to be maintained under all **P**rocess, **V**oltage, **T**emperature (PVT) variations. Therefore, the nominal frequency is set to $570\,\mathrm{kHz}$, leaving a wide margin. The oscillator is based on an RC oscillator architecture, shown in Figure 5.11, where the charging current of the capacitor is provided by a constant current generated by the bandgap voltage reference. Capacitors C_1 and C_2 are **M**etal-**O**xide-**S**emiconductor (MOS) capacitors, providing a higher capacitance per area than **M**etal-**I**nsulator-**M**etal (MIM) capacitors. The two comparators A_1 and A_2 compare the capacitor voltage a the reference voltage of $900\,\mathrm{mV}$. Once the voltage is higher than V_{ref}, the subsequent RS-flipflop composed of two nand gates, sets or resets the output Clk. The power consumption is $4.7\,\mu\mathrm{A}$ in the nominal case.

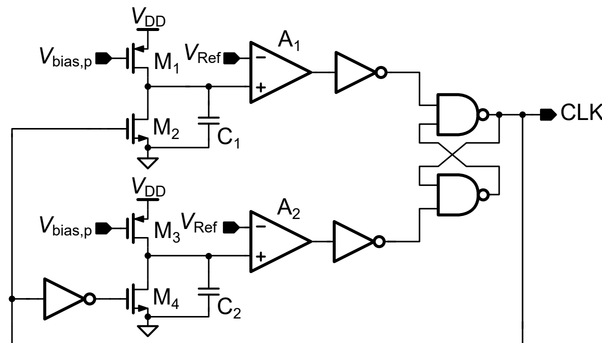


Figure 5.11.: Schematic of the RC oscillator providing $570\,\mathrm{kHz}$ for the digital controller.

Clock Extractor

The rising edges of the piezoelectric crystal are counted for receiving data in the ASIC. Figure 5.12 shows the schematic of the clock extractor circuit. The comparator detects the crossing of the piezoelectric crystal voltage and the reference voltage of $1.24\,\mathrm{V}$. Transistors M_1 and M_2 form a current-starved inverter to decrease the rise- and fall time of the comparator. This reduces the power consumption in the following inverters. Since the clock frequency of the digital controller is lower than the piezoelectric crystal frequency, the input is divided by 8 with three flip flops. It allows the digital controller to count the ultrasonic pulses with a lower clock frequency and hereby saves power.

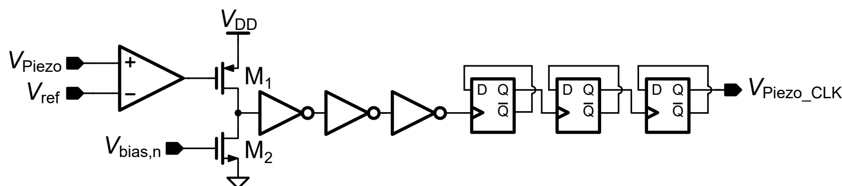


Figure 5.12.: Schematic of the clock extractor circuit. It counts the clock edges of the piezoelectric crystal for receiving data.

Active Transmitter

There are two general transmission types to transmit data from the ASIC to an external receiver: Passive and active transmission. The passive transmission uses a backscatter modulation, while active transmission enables amplitude and frequency modulation. Backscatter has the advantage of requiring only one transistor and a resistor for impedance matching. It will modulate the reflected signal by changing the impedance connected to the piezoelectric crystal. An active transmission can be advantageous, depending on the transmission path or the required data rate. The exact resonance frequency has to be replicated by the ASIC since piezoelectric crystals

have an impedance highly dependent on the frequency and, therefore a small frequency range for transmitting data. An on-chip crystal oscillator for highly accurate clocks is not integrable, therefore an on-chip digital adjustable RC oscillator is implemented. It consists of two components: The RC oscillator and a digital controllable current **D**igital-to-**A**nalog **C**onverter (DAC). The digital adjustment is necessary because of PVT variations on the ASIC and to adapt to different resonance frequencies for different piezoelectric crystals. Figure 5.13(a) shows an excerpt of the implemented current DAC. V_{bias} is a bias voltage generated by the internal bandgap voltage reference, providing a constant current. Transistors M_1 and M_2 mirror the bias current of the voltage reference. Transistors M_3 to M_5 represent the output current mirror, which feeds the RC oscillator. The gates of the transistor M_4 and M_5 can be switched between Vdd or the gate voltage of transistor M_3, turning them off or on with transistors M_6 and M_7. This circuit is replicated multiple times with binary weighted transistors M_5 and M_6 to achieve a digitally controllable current through the $Data$ port. To cover a higher current range, the current DAC consists of two binary weighted current mirrors with the same architecture but with different V_{bias} voltages for a fine and a coarse adjustment. The coarse adjustment has a range of 4-bit and the fine adjustment of 5-bit. The current generated by the current mirror directly supplies the RC oscillator input, shown in Figure 5.13(b). $Current_1$ and $Current_2$ charge the internal capacitors C_1 and C_2 alternately to generate a duty cycle of 50%. To compensate for PVT variations and adapt to different piezoelectric crystals, the tuning range is between $30\,\text{kHz}$ and $2.3\,\text{MHz}$.

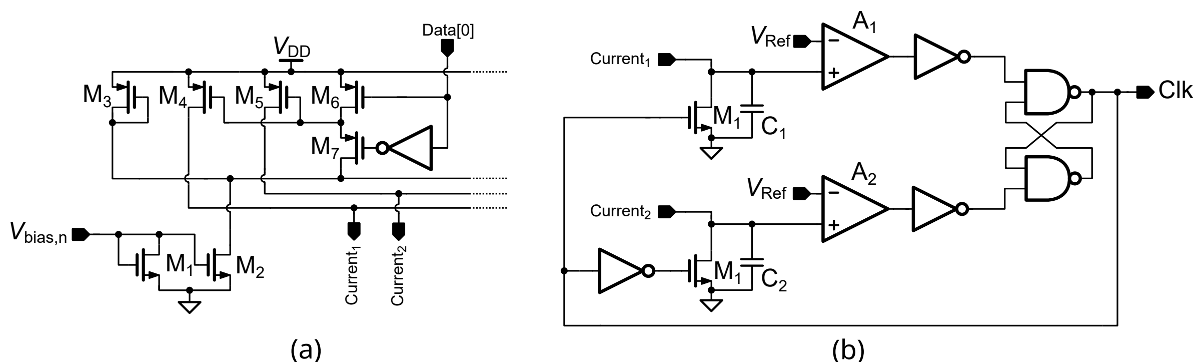


Figure 5.13.: Schematic of the digital controlled adjustable oscillator. (a) shows the current DAC. (b) shows the implemented RC oscillator with a 50% duty cycle.

The internal adjustable oscillator has to be calibrated to the current resonance frequency of the piezoelectric crystal to enable an ultrasonic transmission. Therefore, the external microcontroller has to set a “calibrate start” bit in a register in the ASIC. During the calibration process, a constant frequency over ultrasound is provided to the ASIC to allow a comparison of the piezoelectric crystal frequency and the internal adjustable oscillator. Figure 5.14 shows the simulated implemented algorithm of the calibration for the internal adjustable oscillator. It starts with the lowest possible coarse value of 0 and a fine adjustment of 31. Two 8-bit counters start counting the ultrasonic pulses and the oscillator pulses. After the adjustable oscillator counter has reached

the programmed counter value, both counters are compared. As long as the internal oscillator frequency is smaller than the piezoelectric crystal frequency, the coarse register is incremented by one and the counters are started at zero again. Once the internal oscillator has a higher frequency, the coarse register value stays constant, and the fine register decreases by one. The algorithm stops and takes the last register value as the final result if the oscillator frequency is smaller than the piezoelectric crystal frequency. Both registers, which contain the fine and coarse measurement results, are then read back by the microcontroller.

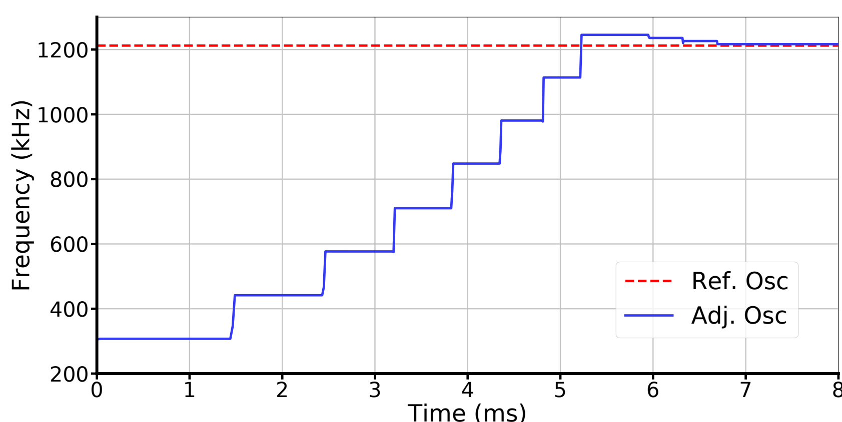


Figure 5.14.: Cadence Virtuoso simulation of the automatic oscillator calibration to the piezoelectric crystal frequency.

Directly connected to the output of the internal adjustable oscillator is the output stage, shown in Figure 5.15. It consists of two half bridges with two complementary transistors each and is controlled directly by the digital controller. The two internal transistor drivers control each one half bridge. They include a level shifter to drive the output transistors, a dead time generation circuit to prevent a shoot-through condition, and an enable signal input. When the transistor driver is disabled, both output transistors M_1 and M_2 are turned off, representing a high impedance mode. This mode is important during the receiving phase and assures that no additional load for the piezoelectric crystal is created. During the transmit phase, the capacitors C_1 and C_2 will increase the impedance from the transmitter to the piezoelectric crystal, consequently, the transmit power will decrease allowing to send data with a lower power level. The resistors R_1, R_2, R_3, and R_4 with a resistance of $500\,\Omega$ act as a current limit with a limit of $2.3\,\text{mA}$.

5.2.2. Fabricated ASIC and Demonstrator

The ASIC was fabricated in a $180\,\text{nm}$ technology and is shown in Figure 5.16. On the right-hand side, the analog circuit is embedded under a power distribution net, which reduces the IR drop. The digital controller on the left-hand side hides under the fill structures of the metal layer and, hence, is not visible on the die shot. The size of the complete die is $1523\,\mu\text{m} \times 1522\,\mu\text{m}$, which

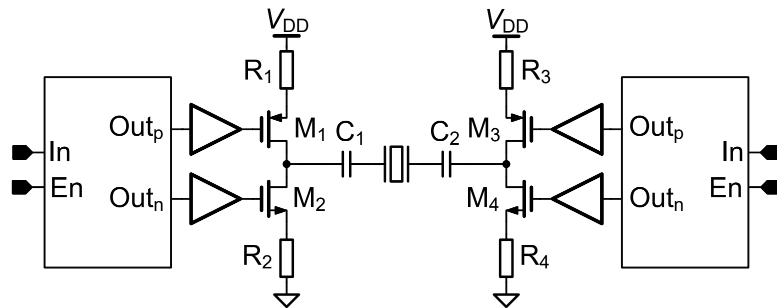


Figure 5.15.: Schematic of the output stage for the active transmitter.

sums up to an area of $2.318\,\mathrm{mm}^2$. The digital controller and the analog circuitry, except the active rectifier, consume $0.1\,\mathrm{mm}^2$ area, respectively. The active rectifier has an area of $0.059\,\mathrm{mm}^2$ because of the big rectification transistors required to carry the current of up to $60\,\mathrm{mA}$. An additional $1.139\,\mathrm{mm}^2$ is required for the IO ring, including the 28 bond pads. The high number of bond pads allows probing signals for testing purposes. An artwork on the upper left side occupies another $0.249\,\mathrm{mm}^2$ while $0.633\,\mathrm{mm}^2$ remains unused. In a future production run, the chip area can be significantly reduced by reducing the number of test bond pads and omitting the artwork.

An experimental test setup was built to test the communication and energy transfer between an external transducer and the ASIC. Figure 5.17 shows a schematic drawing of the experimental setup. The left-hand side shows the external components, while the right-hand side shows the SiMe. A computer controls the custom-designed PCB which contains an **F**ield **P**rogrammable **G**ate **A**rray (FPGA), piezoelectric crystal driver, ADC, and a **L**ow **N**oise **A**mplifier (LNA). The CMOD S7 FPGA module powered by a Spartan-7 offers a serial data connection via **U**niversal **S**erial **B**us (USB). Directly connected to the FPGA is the piezoelectric crystal driver. It consists of two transistors forming a half-bridge with a subsequent low pass filter, removing the harmonic frequencies of the rectangle. The output of the piezoelectric crystal driver connects directly to the piezoelectric crystal, mounted on a $1\,\mathrm{mm}$ thick brass sheet. The small signal amplitude for receiving data from the ASIC gets amplified by an LNA to up to $2\,\mathrm{V}$. This signal is then digitized by a 10-bit ADC, the MAX1426. The result is stored in the FPGA for further processing and transmitted to the computer after the transmission is completed. On the internal side, the ASIC receives the ultrasonic signals. On successful reception of the data, the received data are transmitted to the microcontroller. If data from a sensor are available, these can be sent back to the external side through the ASIC. Figure 5.18 shows the designed external PCB. It requires two supply voltages, one for digital and analog circuits, and one for the piezoelectric crystal driver. The piezoelectric crystal can be supplied with up to $85\,\mathrm{V}$, which is only necessary for a highly dampened ultrasonic transmission path.

Figure 5.19(a) shows the brass tube used for encapsulation of the ASIC. A metal shielding between the transducer and the ASIC is necessary for good shielding since the used piezoelectric crystal works at a frequency of $1.1\,\mathrm{MHz}$. This prevents electric coupling between the piezoelectric crystals and guarantees that the energy and data transfer only take place through ultrasound.

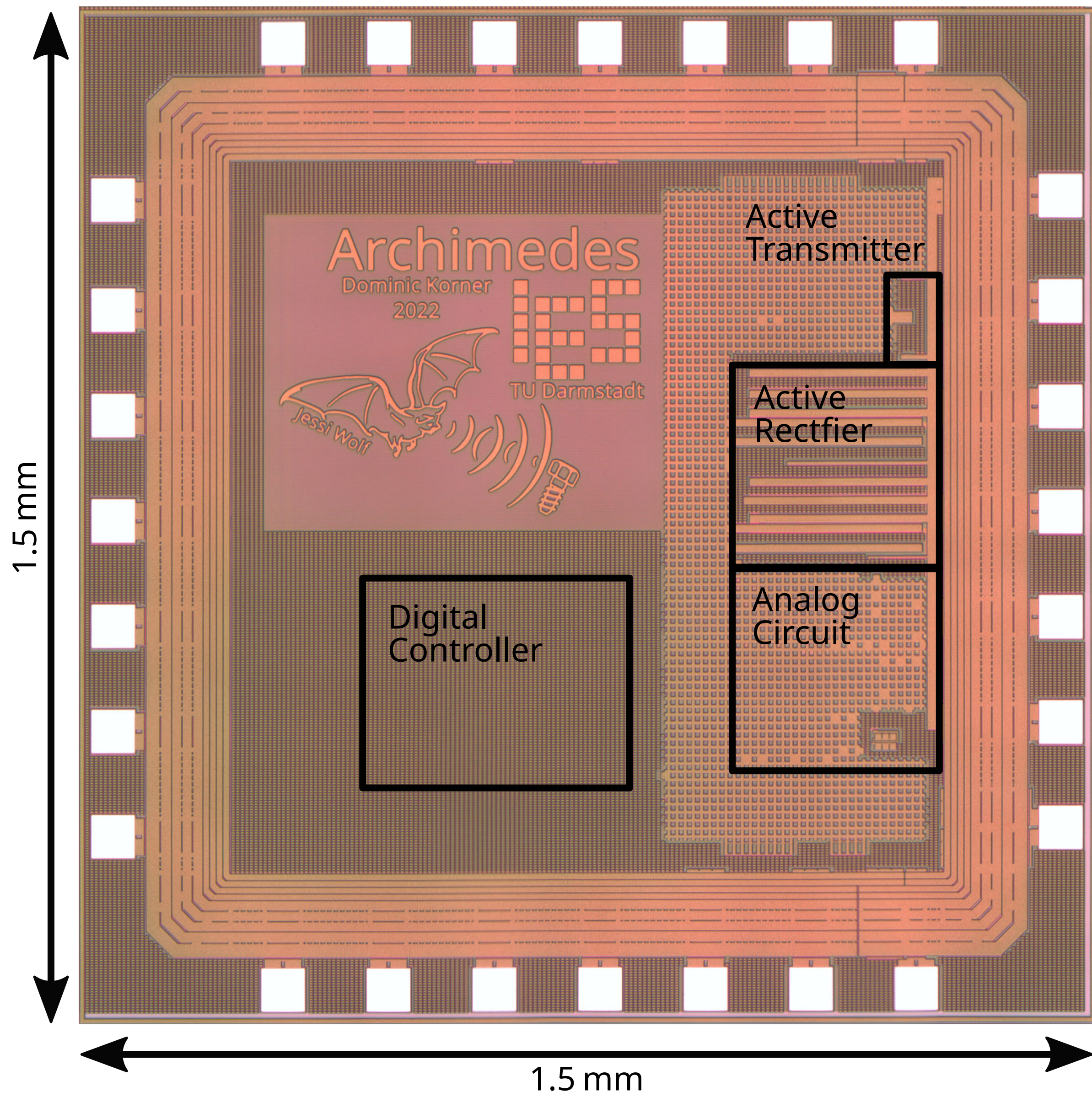


Figure 5.16.: Dieshot of the fabricated SiME ASIC. The small chip area of only $2.318\,\mathrm{mm}^2$ makes it ideal for integration into standard-sized bolts.

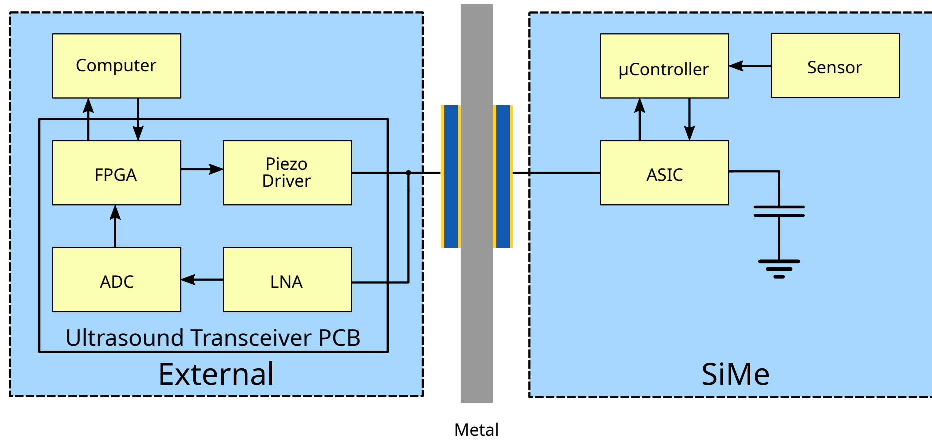


Figure 5.17.: Schematic drawing of the experimental setup for data and energy transfer between a computer and the microcontroller through a closed metal barrier.

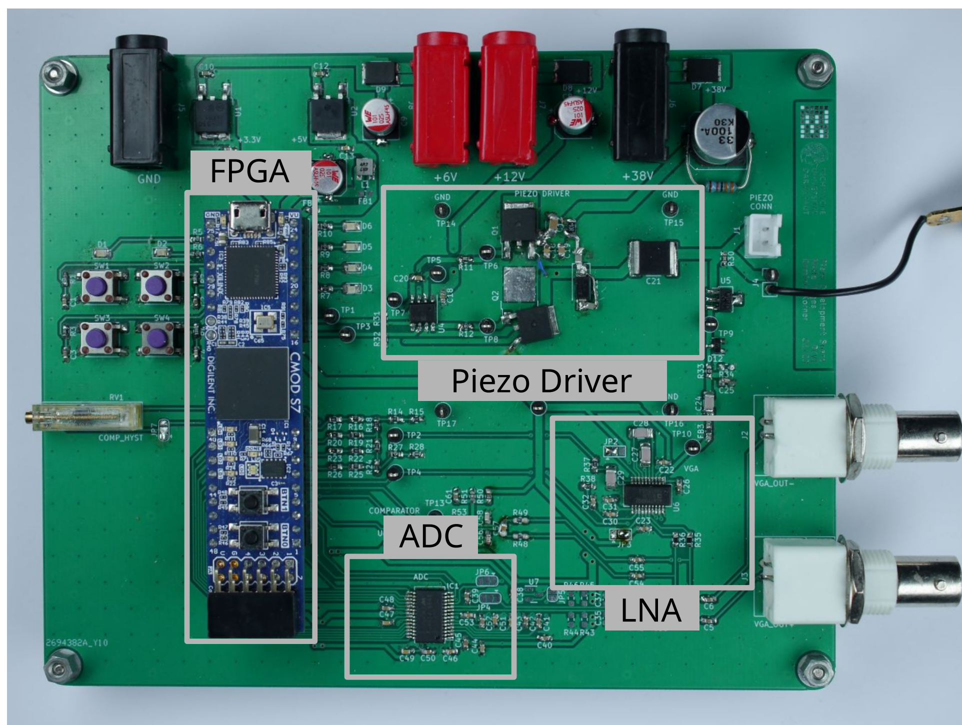
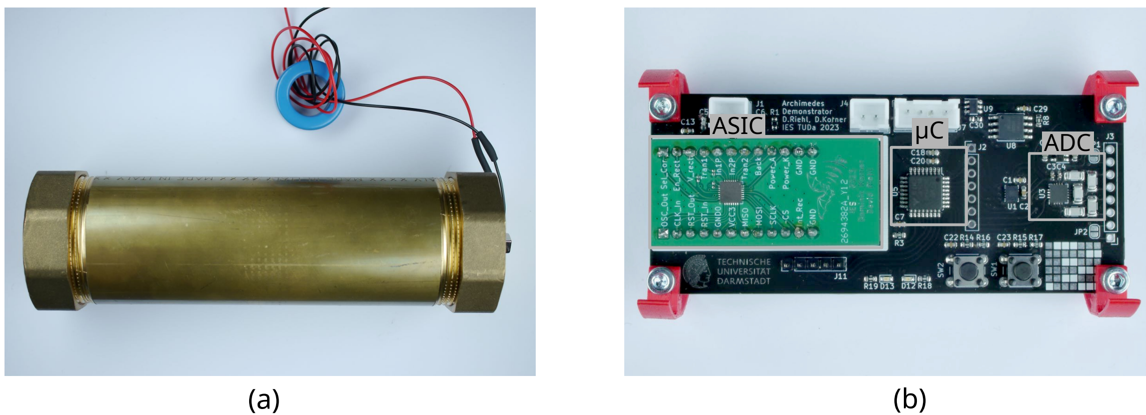


Figure 5.18.: Ultrasonic transmission PCB for generating the ultrasonic waveform for energy transfer and communication. An onboard LNA and ADC allow an evaluation of the received data and send it through the FPGA to a computer.

Therefore, the brass tube encapsulates the complete PCB containing the ASIC. The screw top is machined to a thickness of $1\,\mathrm{mm}$, which is equal to one-quarter of a wavelength for this ultrasonic frequency and brass material. It assures that most of the energy induced in the metal is coupled out to the other side [57]. Figure 5.19(b) shows the PCB carrying the ASIC, microcontroller, energy storage, ADC, and additional sensors. Since the ASIC mounts on a separate PCB, different ASICs can be tested without soldering. An 8-bit microcontroller handles the communication between the ASIC and the sensors. The PCB has an ADC for the evaluation of strain gauges, an accelerometer, and a gyroscope built-in. The energy storage are three $11\,\mathrm{mF}$ supercapacitors. The whole PCB can mounted inside the brass tube for an ideal electrical isolation.



(a) (b)

Figure 5.19.: (a) Brass tube with internal PCB for the designed ASIC. It provides an isolation for radio signals, only ultrasound can pass the brass barrier. (b) Designed PCB carrying the ASIC, microcontroller, and supercapacitor.

5.3. ASIC Measurements

At first, the piezoelectric crystal and the transmission path are measured with a $50\,\Omega$ system impedance network analyzer E5062A. Therefore the piezoelectric crystal, with a diameter of $16\,\mathrm{mm}$ and a thickness of $2\,\mathrm{mm}$ is applied to the brass tube with two magnets. A drop of paraffin oil between the brass tube and the piezoelectric crystal ensures good acoustic coupling. The resulting measurement is shown in Figure 5.20. The piezoelectric crystal has a resonance frequency of about $1.022\,\mathrm{MHz}$. At this frequency, the impedance drops to $78.5\,\Omega$. The same frequency offers the best transmission S_{21} parameter over the complete transmission path of 0.49, resulting in an energy efficiency of $24\,\%$. This shows the high energy efficiency of the system.

For testing the ASICs' energy and data transmission, the voltage of the supercapacitors inside the brass tube is read out, showing the ability to transfer power and communicate through a closed brass sheet inside the brass tube. Electromagnetic waves are shielded and can be assumed not to contribute to the communication or energy transfer since the ASIC and all connected electronics

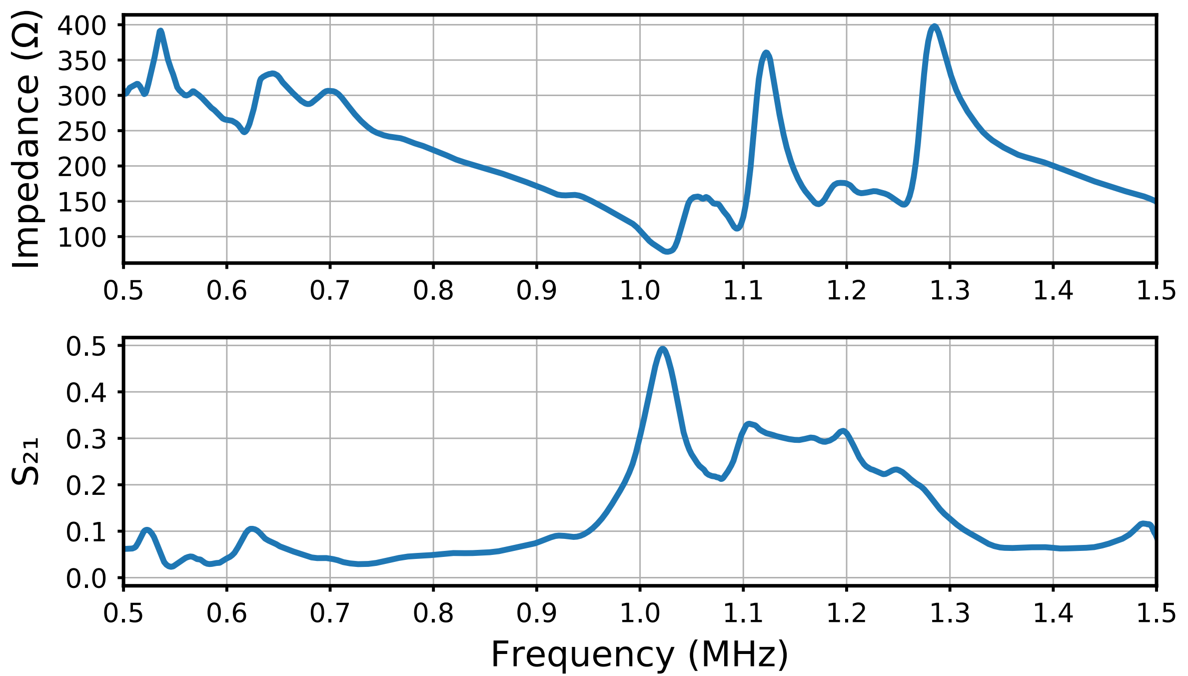


Figure 5.20.: Network analyzer measured piezoelectric crystal impedance and S_{21} parameter. The S_{21} parameter shows the transmission through brass with two piezoelectric crystals over frequency. At $1.022\,\mathrm{MHz}$ the piezoelectric crystal has its resonance frequency and the maximum transmission amplitude is reached.

are enclosed in the brass tube. Figure 5.21 shows the transmit sequence for sending data to the ASIC inside the brass tube generated by the ultrasonic transceiver board. The piezo is actuated with a voltage of $10\,\mathrm{V}$ and a frequency of $1.022\,\mathrm{MHz}$, reaching a transmit power of $280\,\mathrm{mW}$. The transmission starts with a $5\,\mathrm{s}$ charging phase. In this phase the internal supercapacitors with a capacity of $33\,\mathrm{mF}$ are charged to a voltage of $3.3\,\mathrm{V}$. During that phase, the internal adjustable oscillator calibrates its frequency to the piezoelectric crystal resonance frequency. After the supercapacitors are charged, a start bit, consisting of a $9.1\,\mathrm{ms}$ break, signals the ASIC a starting communication. One command has a size of 8-bit. A digital one is encoded as 1600 ultrasonic pulses, whereas a digital zero has 400 ultrasonic pulses. Between every bit a dead time with a length of $1.1\,\mathrm{ms}$ separates each bit. After eight transmitted bits, the ultrasound stops, and the transmitter PCB waits for an answer from the ASIC. After a successful transmission, the ASIC generates an interrupt waking the microcontroller up. The microcontroller then reads the received data and frequency calibration bits from the ASIC and starts the ADC for measuring the supercapacitor voltage. After the conversion, the data is sent via the SPI interface to the TX register of the ASIC and a start transmit command is given. The ASIC transmits the data in an amplitude-modulated ultrasonic signal. The ultrasonic transceiver board records the amplified ultrasonic pattern with the 10-bit ADC and transfers it to the computer, where a Python script interprets the data.

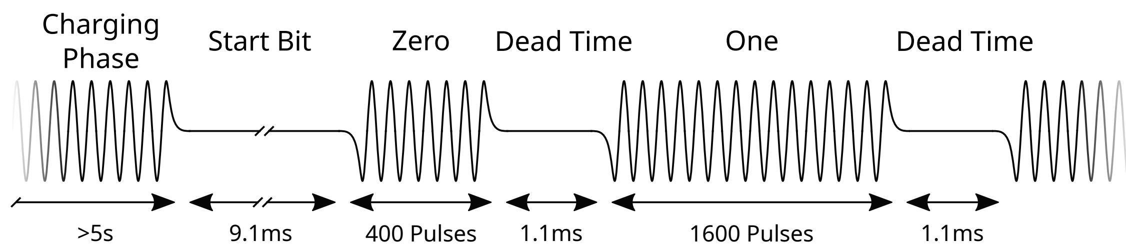


Figure 5.21.: Ultrasonic transmit sequence for testing the ASIC inside the brass tube.

The received signal for an amplitude modulation is shown in Figure 5.22. At $0\,\mathrm{ms}$, the transmission to the ASIC has just finished and the remaining oscillation dies. Then the microcontroller starts the ADC and reads out the received data from the ASIC. After approximately $3\,\mathrm{ms}$, the ASIC starts to send the first bit. The current setting is 100 clock cycles of the ASIC per transmitted bit. Since the internal clock of the ASIC operates at $550\,\mathrm{kHz}$, 100 clock cycles correspond to $180\,\mathrm{\mu s}$, resulting in $180\,\mathrm{\mu s}$ per transmitted bit. The setting of 100 clock cycles can be adjusted for a higher data rate or better robustness. The transmission starts with a one and is followed by a zero as indicated in the picture. The ultrasonic signal is amplified by an LNA and converted with the 10-bit ADC to the digital domain.

Measurements show that the active rectifier can deliver a tested output power of $60\,\mathrm{mW}$ at an output voltage of $2\,\mathrm{V}$. Since special attention was given to the size of the rectifier, it is only $0.059\,\mathrm{mm}^2$ in size. Table 5.1 shows a comparison of different publicized active rectifier implementations. The here-introduced active rectifier yields the highest power density of $1016\,\mathrm{mW\,mm}^{-2}$, making this implementation the most area-efficient design.

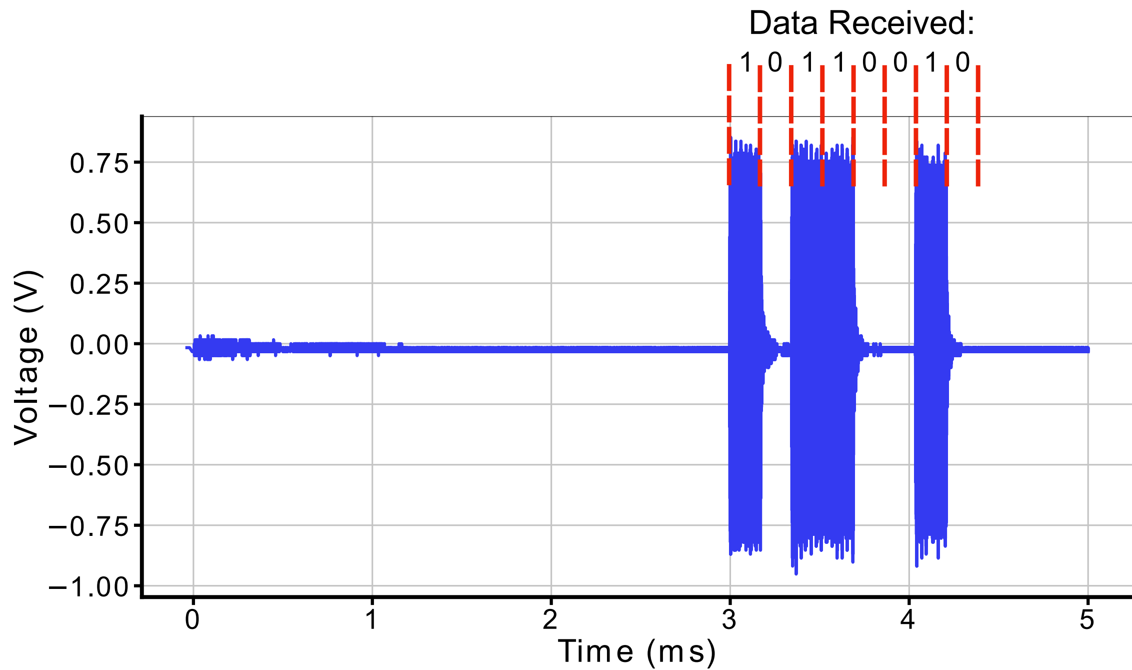


Figure 5.22.: Received ultrasonic data from the ASIC. The ultrasonic signal is amplified with an LNA to get a sufficient amplitude for the ADC.

Parameters	JSSC'15 [58]	TBCAS'19 [59]	TBCAS'20 [60]	LSSC'23 [61]	Access'24 [22]	**This Work**
Tech. (nm)	65	180	180	180	28	180
Freq. (MHz)	1.0	2.7	1.38	**5.0**	2.15	1.025
Distance (mm)	**30**	n.d.	n.d.	n.d.	10	1.2
Area (mm^2)	0.2	0.09	**0.0025**	0.0026	0.0045	0.059
$V_{in,max}$ (V)	0.8	3.0	3.3	n.d.	2.5	**3.6**
P_{out} (mW)	0.1	2.27	2.29	2.405	1.0	**Tested up to 60 mW @ 2V**
Power Dens. (mW/mm^2)	0.5	25.2	904	925	222.2	**1016**

Table 5.1.: Comparison of the implemented active rectifier with recent publications. The active rectifier presented in this work yields the highest energy and highest power density.

5.4. Summary

The implemented ASIC shows a working proof of concept for the sensor-integrated machine element by enabling ultrasonic energy and data transmission through a metal barrier. The ASIC, manufactured in a $180\,\mathrm{nm}$ technology, acts as an ultrasound to SPI bridge, handling the energy harvesting and data transmission over ultrasound. It provides an SPI interface for an external microcontroller to process the received data, which is beside an energy storage the only additional required component, except for optional additional sensors.

Due to the short ultrasonic transmission path, high power can be transmitted over ultrasound, allowing a fast charging of the energy storage of the SiMe. The results show that the internal rectifier can provide a power of $60\,\mathrm{mW}$ at an output voltage of $2\,\mathrm{V}$ over the ultrasonic transmission path. With the area of the active rectifier of only $0.059\,\mathrm{mm}^2$, it achieves a high power density of $1016\,\mathrm{mW\,mm}^{-2}$. Compared to other recent publications, this work presents the highest energy density to date. The internal adjustable oscillator and the active transmitter enable four different communication protocols, namely backscatter, AM, FM, and resonance modulation. With the external microcontroller, the ASIC is configurable for a variety of different applications.

In summary, the fabricated ASIC with different analog and digital building blocks has proven its functional capabilities. Energy harvesting and communication over ultrasound are successfully shown in the lab. Integrating the ultrasonic transceiver and active rectifier into one single ASIC enables a more compact design in contrast to previous approaches with discrete components.

6. Ultrasonic Powered ASIC for Medical Smart Implants

Implants for the human body enable the monitoring of vital health parameters, for example, oxygen monitoring or brain-machine interfaces [8, 62]. Additional areas of application are active nerve stimulators [17, 63, 64]. All these applications make it vital that the implant is as compact as possible. Internal batteries are almost impossible to integrate for a long operation period because of the compactness and required longevity of the implant. Therefore, the implant requires a wireless energy transfer, including a bidirectional data transfer. The implant presented here focuses on implants in deep tissue $10\,\mathrm{mm}$ below the skin. There, ultrasound has multiple advantages over an RF transmission of energy and data: Ultrasound has a much lower attenuation in the tissue of only $1\,\mathrm{dB\,cm^{-1}}$ [65] compared to RF transmission of $2\,\mathrm{dB\,cm^{-1}}$ to $10\,\mathrm{dB\,cm^{-1}}$, depending on the RF transmission frequency of $1\,\mathrm{MHz}$ to $1\,\mathrm{GHz}$ [66]. Second, the size of the receiving ultrasound element can be smaller due to the smaller wavelength of ultrasound compared to the RF signal in human tissue. A typical RF frequency will possess a wavelength in the range of meters, compared to an ultrasonic wavelength of $1.44\,\mathrm{mm}$ at a speed of sound of $1440\,\mathrm{m\,s^{-1}}$ and an ultrasonic frequency of $1\,\mathrm{MHz}$. The lower speed of sound also allows a more accurate location of the device. Thirdly, the FDA limit for ultrasound is $720\,\mathrm{mW\,cm^{-2}}$ compared to $10\,\mathrm{mW\,cm^{-2}}$ for RF signals, allowing much higher energy density in the tissue [67, 68, 62].

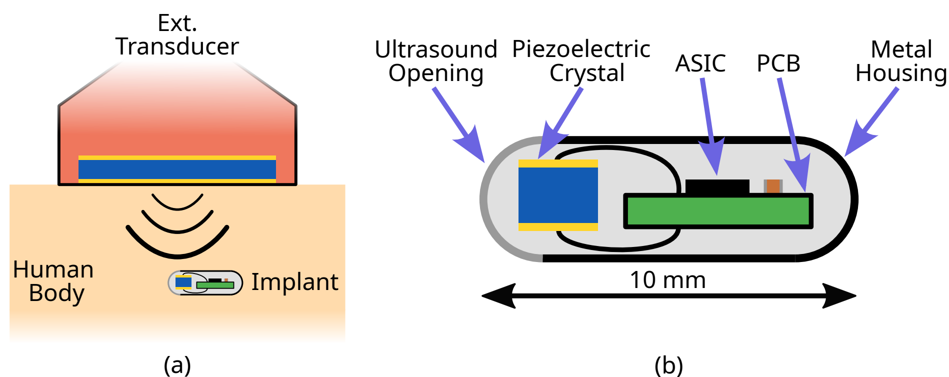


Figure 6.1.: (a) Application example for the developed ASIC, implanted into the human body, powered with an external transducer. (b) Detailed internal view of the implant with an ultrasonic opening to allow ultrasound to penetrate the metal housing.

Figure 6.1 (a) shows the device implanted below the human skin. For energy and data transfer, an external transducer transmits ultrasound and receives the resulting echo for a distance calculation between the transducer and implant. Additionally, the implant modulates the echo to the transducer for communication. Figure 6.1 (b) shows the implant's internal components with the ultrasonic opening on the left side. The piezoelectric crystal inside the metal housing supplies the ASIC with energy and data. ASIC and a capacitor for energy storage are mounted on a PCB. The complete length of the implant is specified to be a maximum of $10\,\mathrm{mm}$, which limits the size of the internal components.

This chapter presents an ASIC for implantation in the human body. The first section presents the communication protocol, followed by the schematic implementation and fabricated ASIC in the second section. The chapter concludes with a brief summary.

6.1. Bidirectional Ultrasonic Communication and Location of the implant

The communication interface has to provide a communication link, ensure a constant energy transfer, and detect the location of the implant in the human body. Counting ultrasonic pulses represents a simple and area-efficient method for receiving data via ultrasound. Only a comparator and a counter are necessary for decoding the received data in the ASIC. Figure 6.2 shows the resulting communication protocol. At the beginning of the transmission, the capacitor connected to the ASIC is charged, which usually takes less than $1\,\mathrm{s}$, but depends on the orientation and distance between the ASIC and transducer. After the charging phase, a start bit is transmitted by pausing the ultrasonic signal. The standard length start bit is $9.25\,\mathrm{ms}$ and can be adjusted from zero to $120\,\mathrm{ms}$ through the SPI interface. The actual data is decoded by the number of ultrasonic pulses. A zero value decodes by 100 ultrasonic pulses, while a one decodes by 400 ultrasonic pulses. Both parameters are adjustable from zero to 4095 pulses over the SPI interface. Each bit is separated by an ultrasonic break with a length of $925\,\mathrm{\mu s}$, which is also adjustable between zero and $120\,\mathrm{ms}$. After four transmitted bits, the transmission is complete.

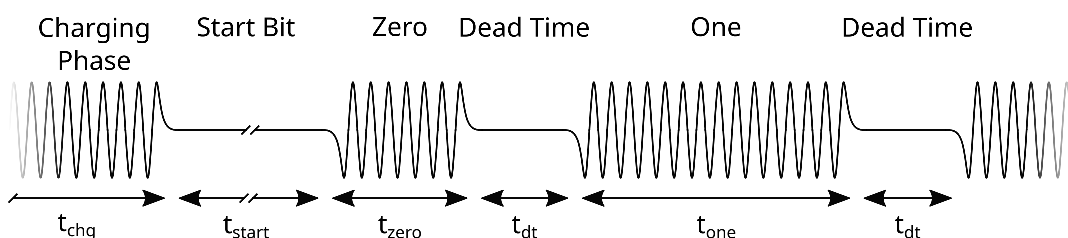


Figure 6.2.: Communication protocol for transmitting data to the ASIC.

The ASIC uses a backscatter modulation for receiving data, as shown in Figure 6.3. In contrast to an active transmitter, a backscatter transmission requires no power for transmitting data, only a modulation of the load impedance connected to the piezoelectric crystal. The transmission is

accomplished by applying a load impedance in parallel to the piezoelectric crystal, which lowers the reflection coefficient of the piezoelectric crystal. The result is a lower amplitude of the reflected echo. A zero is decoded with a time of $46\,\mu s$, a one with $185\,\mu s$, and the dead time between the data bits again with $46\,\mu s$. All values for the four-bit transmission are adjustable in a range of 16-bit from zero to $120\,ms$. The current setup transmits the same data back after the ASIC successfully receives the four data bits and allows testing of the transmission in both directions.

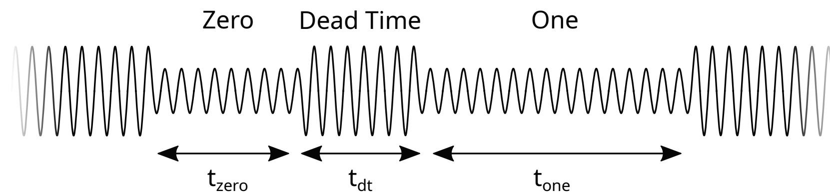


Figure 6.3.: Communication protocol for receiving data from the ASIC.

After receiving the modulated echo from the ASIC, a precise estimate of the distance between the ASIC and the transducer is possible because of the known velocity of sound in the human body and the time the echo takes to arrive at the transmitter. To make the implant better visible in a medical ultrasonography, the implant will modulate the reflected echo periodically, as shown in Figure 6.4. The location beacon has a length t_{loc} of $4.6\,ms$, and the dead time between the two beacons t_{dt} has a length of $46\,ms$. Each length can be adjusted independently between zero and $120\,ms$. The location beacon is only active if no data is transmitted. Once the ASIC detects a start bit, the location beacon stops and the ASIC waits for new data.

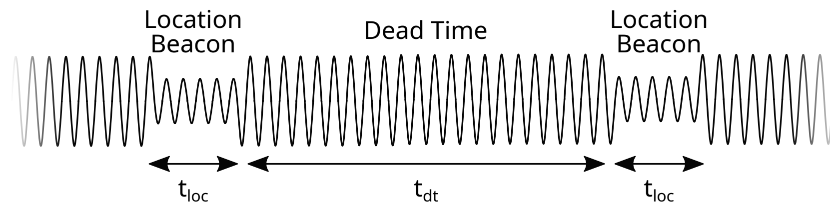


Figure 6.4.: Location beacon periodically generated by the ASIC allowing a location of the implant in the human body.

6.2. Implemented ASIC for Medical Smart Implants

The specified size of the implant must be below $2\,mm \times 2\,mm \times 10\,mm$, including the internal electronics with piezoelectric crystal and capacitors. Therefore, the external elements have to be as small as possible. As piezoelectric crystal, a cube with an edge length of $1.6\,mm$, resulting in a resonance frequency of $950\,kHz$, is used. The external capacitor has a 0402 **S**urface-**M**ounted **D**evice (SMD) package, which translates to a size of $1\,mm \times 0.5\,mm \times 0.55\,mm$ and offers capacities of up to $1\,\mu F$. Figure 6.5 shows the complete implemented system in detail. The ASIC of the implant

is manufactured in a 180 nm technology, providing a low power consumption and small size. It offers an active rectifier for efficient energy harvesting from the piezoelectric crystal. The over-voltage protection limits the input voltage of the ASIC to around 3.6 V, protecting it at low distances between the transducer and the implant. A reference voltage generates the required voltage and current to control a voltage regulator and the oscillator. For the backscatter communication, a load modulator and a clock extractor for counting ultrasonic pulses are integrated. An integrated power-on reset circuit holds the digital controller in a reset state until the external capacitor is sufficiently charged. The digital controller receives and transmits data and generates the location beacon. The SPI interface is not mandatory for operation, but offers the possibility to adjust the communication interface parameters and read status information from the ASIC for debugging purposes. It provides access to the internal received data and allows the adjustment of the receive, transmit, and location beacon parameters in a wide range.

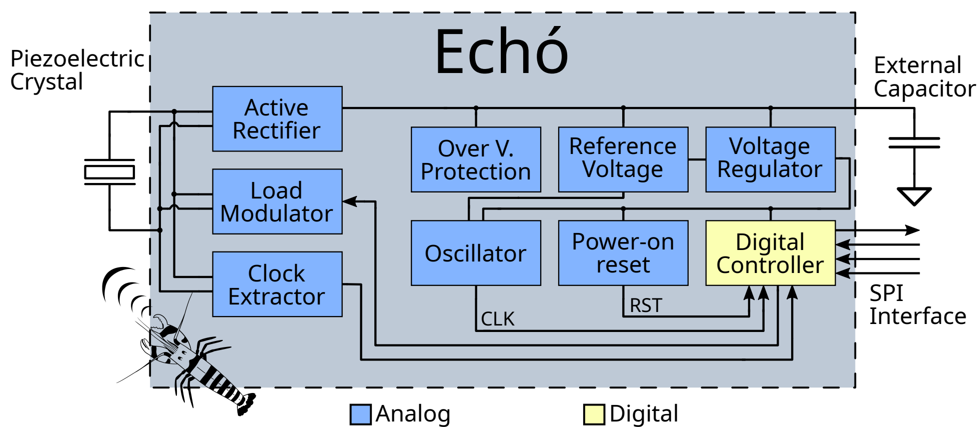


Figure 6.5.: Block diagram overview of the integrated ASIC for the implant. It is a standalone component and only requires the external piezoelectric crystal and an external capacitor for energy storage.

6.2.1. Schematic Implementation

Voltage Reference

To supply the internal oscillator, power-on reset, and digital controller, a stable low power voltage reference is required. Figure 6.6 shows the implemented low power voltage and current reference. It is based on a current mirror with an added start-up circuit and output stage [23]. The start-up circuit pulls down the gates of the current mirror M_4, M_5, M_9, and M_{10} if the circuit does not start correctly. Therefore, the zero voltage threshold transistor M_1 generates a current of 20 nA. The subsequent inverter consisting of M_2 and M_3 switches transistor M_6 on and pulls down the current mirror that starts the voltage reference. Once the voltage reference is started, the inverter turns transistor M_6 off. The first reference voltage $V_{ref,1}$ provides a voltage of 0.588 V used for

the oscillator and the reset circuit. The output stage generates a second reference voltage $V_{ref,2}$ of $1.022\,\mathrm{V}$ at $3\,\mathrm{V}$ input voltage over the bipolar transistor Q_1 and resistor R_4. At this input voltage, the complete reference circuit consumes $605\,\mathrm{nA}$ plus the reference current provided by transistor M_{10} of $200\,\mathrm{nA}$. The minimal operating voltage is $1.1\,\mathrm{V}$.

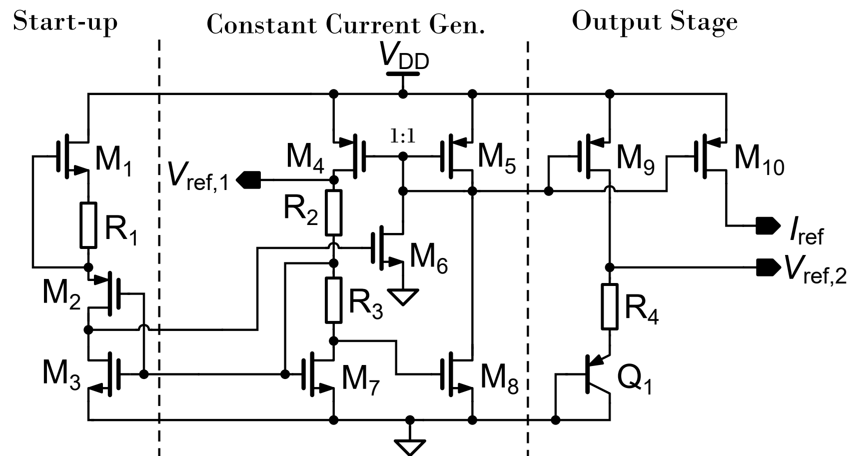


Figure 6.6.: Schematic of the low power voltage and current reference including a start-up circuit.

LDO Voltage Regulator

The LDO is the same as used in the SiMe and is shown in Figure 5.8. Since the reference voltage is smaller than for the SiMe, it supplies the oscillator and the digital controller with a regulated voltage of $1.022\,\mathrm{V}$. The lower output voltage, compared to the SiMe, reduces the power consumption of the connected circuitry further.

Over Voltage Protection

Depending on the distance between the transducer and the implant, the voltage generated from the piezoelectric crystal can be higher than the maximum allowed $3.6\,\mathrm{V}$ operating voltage. To protect the implant from an overvoltage condition, an overvoltage protection circuit guards the electronics on the ASIC. Figure 6.7 shows the integrated circuit. It consists of three serially connected transistors, starting to conduct at about $2\,\mathrm{V}$. This leaves enough voltage headroom at the input of the active rectifier. The additional resistor linearizes the current at an overvoltage condition.

Power-on Reset

The power-on reset generates a reset signal for initializing the digital controller at the start-up of the implant. The schematic is shown in Figure 6.8. Transistors M_2 and M_4 are supplied by the

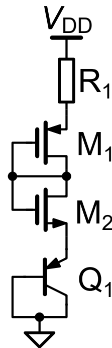


Figure 6.7.: Schematic of the overvoltage protection circuit integrated in the ASIC.

constant current of the voltage reference and generate a current of $70\,\mathrm{nA}$. Transistor pairs M_1, M_2, and M_3, M_4 form a variation of a current-starved inverter, decreasing the power consumption. The voltage reference supplies V_{ref} with a voltage of approximately $0.5\,\mathrm{V}$. If the supply voltage V_{dd} rises above $1.35\,\mathrm{V}$, transistor M_1 begins to conduct and charges capacitor C_1. Once the capacitor is charged to $300\,\mathrm{mV}$, the output RST switches to high and enables herewith the digital controller. After a generated reset, the circuit consumes only $70\,\mathrm{nA}$.

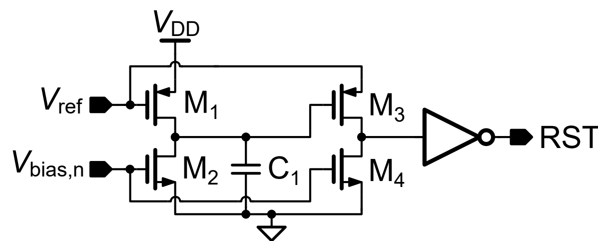


Figure 6.8.: Schematic of the power-on reset circuit for the digital controller.

Active Rectifier

Due to the low amplitude of the voltage received by the piezoelectric crystal, an energy-efficient rectification of the generated AC voltage is necessary. A standard full bridge rectifier, consisting of silicon diodes, has a nominal drop voltage equivalent to two diode voltages, resulting in a voltage drop of about $1.4\,\mathrm{V}$. To reduce the drop voltage, an active rectifier rectifies the incoming voltage. Figure 6.9 shows the implemented active rectifier, consisting of four transistors forming an H-bridge. The H-bridge is controlled by two comparators, controlling the transistors M_3 and M_4. Transistors M_1 and M_2 are connected as a cross-coupled pair, eliminating an active control of these transistors. A peak-to-peak voltage of the piezoelectric crystal of $1.4\,\mathrm{V}$ generates a DC voltage of $760\,\mathrm{mV}$ at an output current of $15\,\mathrm{\mu A}$. Compared to a full bridge rectifier, it nearly halves the drop voltage.

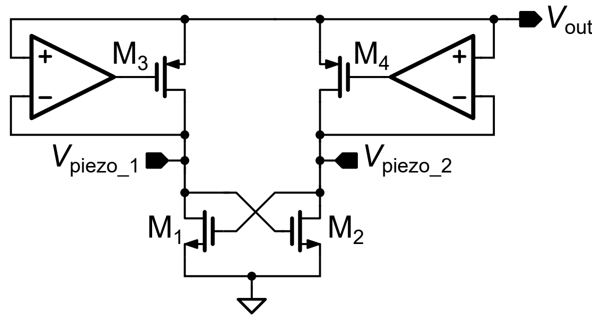


Figure 6.9.: Schematic of the active rectifier, rectifying the piezoelectric crystal voltage.

RC Oscillator

The RC oscillator uses the same architecture as in the SiMe and is shown in Figure 5.11. Since a different voltage reference is used and the sizes of transistors are optimized for lower frequencies, the power consumption is lower. In nominal case, the current consumption is $1.022\,\mu\text{A}$ at an output frequency of $539\,\text{kHz}$. The lower current consumption also results from the lower supply voltage of only $1.1\,\text{V}$ compared to the SiMe with an internal supply voltage of $1.24\,\text{V}$.

Clock Extractor

The clock extractor generates a rectangle signal from the received ultrasound. Figure 6.10 shows the schematic with a connected frequency divider. The comparator extracts the clock signal of the piezoelectric crystal, followed by a current-starved inverter. The following two inverters increase the slope of the generated rectangle to meet the timing requirements of the frequency divider. The frequency divider divides the clock signal by 4 and allows the sampling of the $950\,\text{kHz}$ piezoelectric crystal resonance frequency with the digital controller which operates at a frequency of $539\,\text{kHz}$. A division by four leaves enough headroom for PVT variations of the implemented ASIC.

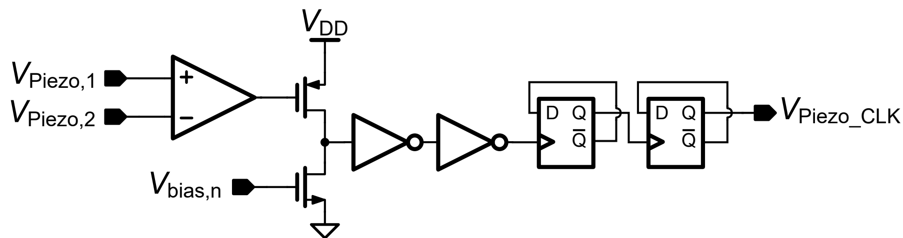


Figure 6.10.: Schematic of the clock extractor for the implant. Generates a by 4 divided clock signal from the piezoelectric crystal frequency for communication.

Load Modulator

The load modulator modulates the echo from the implant to enable a communication link from the implant to the transducer. Figure 6.11 shows the schematic of the modulator. It consists of a transistor connected in series with a resistor in parallel to the piezoelectric crystal. This allows changing the load impedance of the piezoelectric crystal by turning transistor M_1 on or off. The transistor directly connects to the digital controller. The piezoelectric crystal determines the resistance of R_1 and depends on the impedance of the receiving piezoelectric crystal at the resonance frequency. This will result in the smallest reflected amplitude and enable the distinction between the two different amplitudes for the transducer.

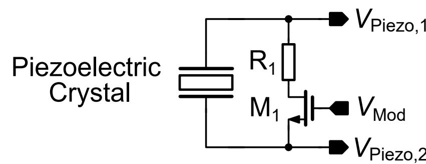


Figure 6.11.: Schematic of the load modulator for enabling a communication link from the implant to the transducer.

The piezoelectric crystal with an edge length of $1.6\,\mathrm{mm}$ results in a transmission link frequency of $950\,\mathrm{kHz}$. At that frequency, the piezoelectric crystal oscillates in the parallel resonance. To determine the required resistance R_1, the series resonance has to be measured. Therefore, the network analyzer E5062A records the impedance over the frequency curve. Figure 6.12 shows the resulting impedance with the real and imaginary parts of the impedance. At $730\,\mathrm{kHz}$, the real value of the impedance reaches its lowest value of $827\,\Omega$, the series resonance of the piezoelectric crystal. This is the ideal resistance for R_1 and achieves the lowest reflection coefficient for the piezoelectric crystal.

6.2.2. Fabricated ASIC and Experimental Setup

A test setup for transmitting and receiving ultrasound was constructed to test the designed and manufactured ASIC. Figure 6.13 shows a block diagram of the experimental setup, consisting of the implant connected to the piezoelectric crystal and an external control PCB for transmitting and receiving ultrasound. The communication with the ASIC is initiated by sending a command to the custom-made ultrasonic PCB from a connected computer. The FPGA of the PCB generates the required waveforms for the transducer. Additionally, the PCB includes an on-board piezoelectric crystal driver and an LNA for amplifying the received signal. The transducer itself consists of a single piezoelectric crystal, submerged in water, and is connected directly to the PCB. Water has a similar speed of sound as the human body which makes it ideal for tests in the lab [69]. The implants' piezoelectric crystal, also submerged in water, receives the ultrasonic wave and converts it to electrical signals, evaluated by the ASIC. A microcontroller in the implant is not required and is only optional.

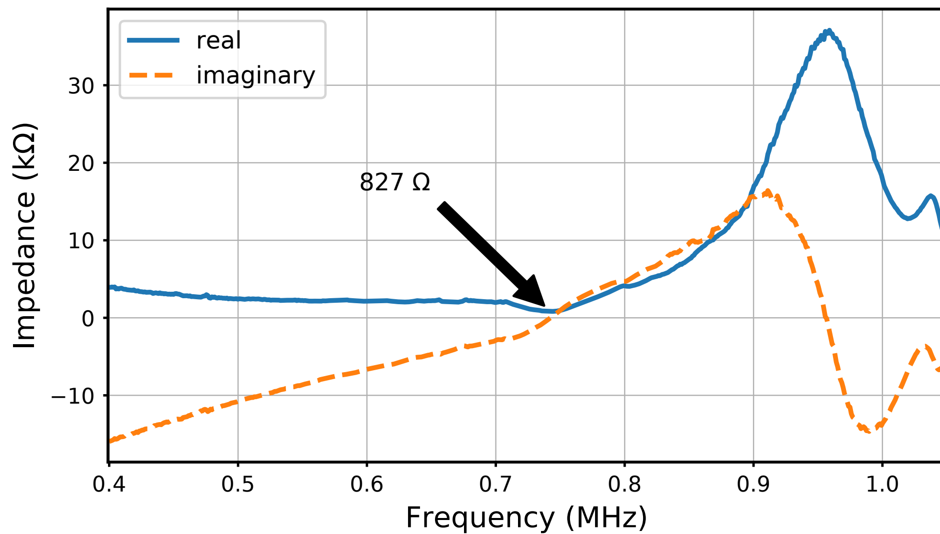


Figure 6.12.: The measured impedance of the implants' piezoelectric crystal. At $730\,\mathrm{kHz}$ the series resonance shows that the ideal terminating resistance is $827\,\Omega$.

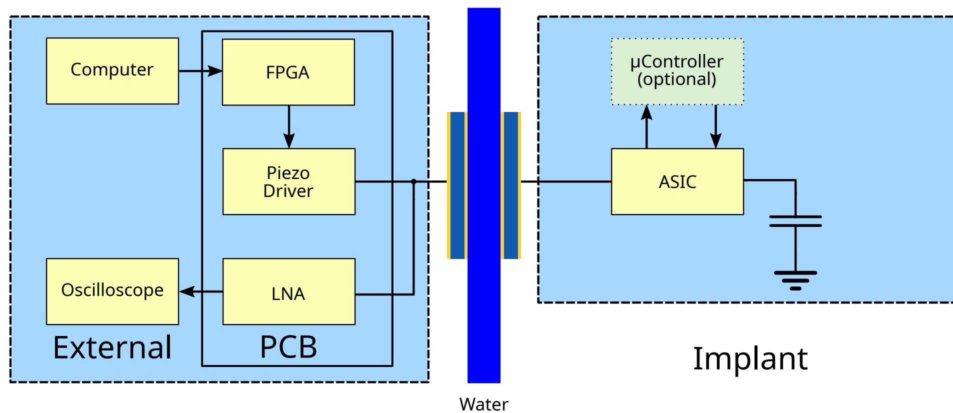


Figure 6.13.: Block diagram of the experimental setup for testing the manufactured ASIC. Between the transducer and the implant, water serves as a transmission medium and provides similar properties as the human body with respect to ultrasonic propagation.

Figure 6.14 shows the custom-made PCB for transmitting data to and receiving data from the implant. A computer connected to a CMOD S7 FPGA board controls the PCB. It generates the required signal for driving the piezoelectric crystal and controls the LNA for receiving ultrasound. The onboard piezoelectric crystal driver can amplify the voltage to a maximum of $100\,\mathrm{V}$ for high power outputs. It consists of a transistor half-bridge, generating a rectangle signal. The echo of the transmitted ultrasound is amplified by the LNA, capable of an amplification of $55.5\,\mathrm{dB}$. This is sufficient to observe the echo on an external oscilloscope.

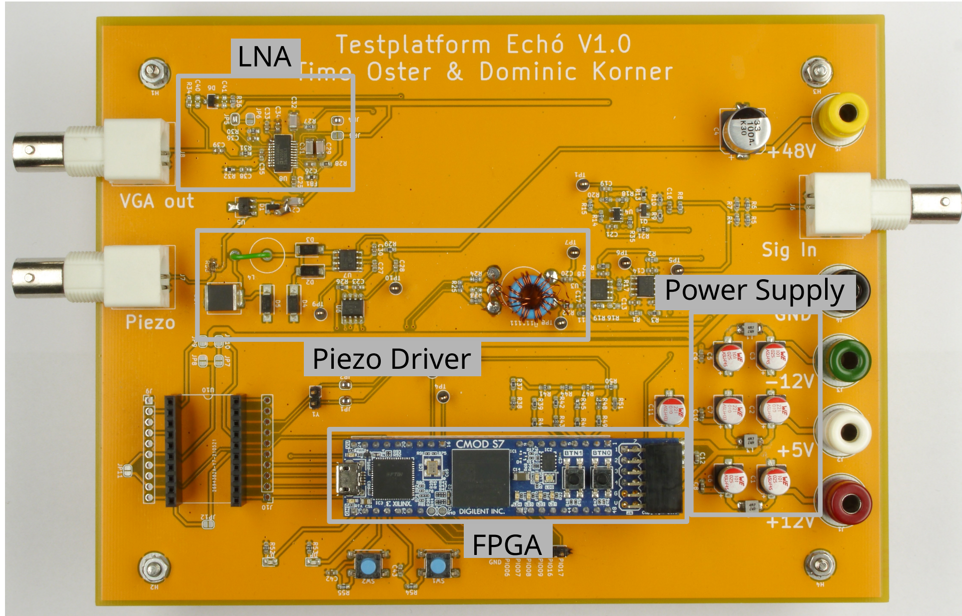


Figure 6.14.: Custom-made PCB for transmitting and receiving ultrasound for communication and energy transfer with the implant.

The transducer for transmitting the ultrasound to the implant as well as receiving the echo has a diameter of $25\,\mathrm{mm}$ at a resonance frequency of $1\,\mathrm{MHz}$. Since the implant size is limited, the implant's piezoelectric crystal has to be as small as possible. A cubic form of the piezoelectric crystal makes it ideal for integration into the implant. The edge length of the cubic can be calculated with the following equation [47]:

$$\tau_x = \frac{\Omega^v}{2 \cdot f_p^v} \cdot \sqrt{\frac{c_{3333}^E}{\rho}} \tag{6.1}$$

τ_x represents the edge length of the piezoelectric crystal cube, Ω^v the dimensionless eigenfrequency, f_p^v the parallel resonance frequency, c_{3333}^E the electroelastic coefficient and ρ the density of the PZT-5A material. The parallel resonance of the equivalent circuit of the piezoelectric crystal results in the highest impedance at that frequency. At high impedances, the voltage output of the piezoelectric crystal reaches its peak and allows operating the implant at low ultrasonic levels. For

an ultrasonic frequency of $1\,\mathrm{MHz}$, the PZT-5A material should have an edge length of $1.58\,\mathrm{mm}$. For practical reasons, the fabricated piezoelectric crystal cube has an edge length of $1.6\,\mathrm{mm}$, which can be manufactured from standard materials. The resulting measured parallel resonance frequency is $950\,\mathrm{kHz}$, which is close enough to the intended frequency of $1\,\mathrm{MHz}$. The deviation from the calculated frequency of $987.3\,\mathrm{kHz}$ at an edge length of $1.6\,\mathrm{mm}$ can be explained through production variances in size and material, and the additional mass for electrical connection on the piezoelectric crystal. Figure 6.15 shows a size comparison of the transducer and the receiving piezoelectric crystal cube. Additionally, the fabricated ASIC is shown which has a comparable size to the piezoelectric crystal cube.

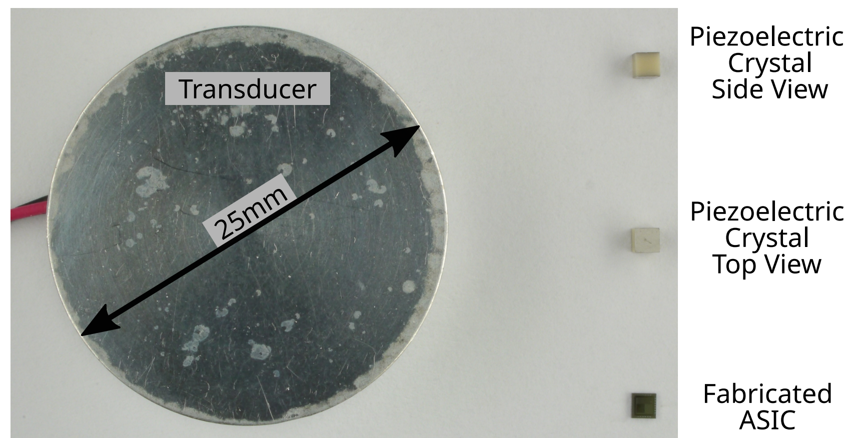


Figure 6.15.: Piezoelectric crystal size comparison of the transducer and the receiving piezoelectric crystal of the implant. As a reference, the fabricated ASIC is shown with a comparable size to the piezoelectric crystal.

The experimental setup for transmitting energy and data in water is shown in Figure 6.16. The transducer and the receiving piezoelectric crystal are submerged in water, which emulates a similar behavior as in the human body. The water tank has a size of $10\,\mathrm{cm} \times 15\,\mathrm{cm}$ for testing various distances and angles of the ultrasonic transmission. Therefore, an XY coordinate table allows a precise displacement between the transducer and the piezoelectric crystal. The ASIC and a capacitor as energy storage are connected to the receiving piezoelectric crystal. For this test, a $220\,\mathrm{nF}$ X7R 0603 SMD capacitor stores enough energy to allow the system to operate. The maximum communication distance is up to $30\,\mathrm{mm}$, at longer distances the energy received over ultrasound is insufficient to charge the capacitor and power the ASIC. The ASIC starts fully operating at a supply voltage of $1.3\,\mathrm{V}$, consuming a current of $18.5\,\mathrm{\mu A}$. At this voltage, the oscillator operates at a frequency of $465\,\mathrm{kHz}$. At a supply voltage of $0.8\,\mathrm{V}$, the on-chip oscillator starts with a current consumption for the complete chip of only $8.5\,\mathrm{\mu A}$.

Figure 6.17 shows the charging curve for energy transmission over ultrasound with a distance between the transducer and piezoelectric crystal of $30\,\mathrm{mm}$. Beginning at $0\,\mathrm{ms}$, ultrasound is received by the ASIC and charging the capacitor. At about $10\,\mathrm{ms}$, a voltage of $1.4\,\mathrm{V}$ is reached.

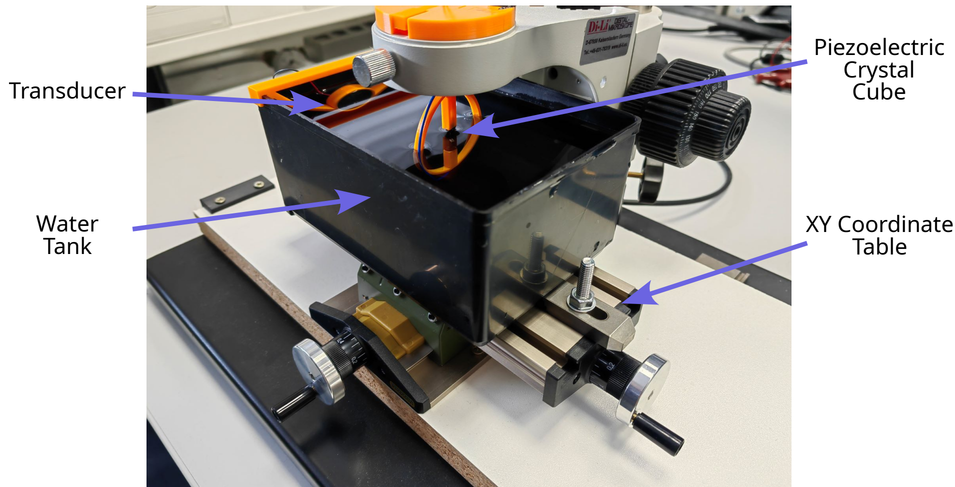


Figure 6.16.: Experimental setup for transmitting ultrasound from the transducer to the piezoelectric crystal receiver in water.

The operation of the complete ASIC starts at about $1.3\,\mathrm{V}$, which is $7\,\mathrm{ms}$ after the ultrasound is switched on. At this voltage, the reset circuit enables the digital circuit. Faster charging times and higher voltages are possible with an increased ultrasonic amplitude or a smaller distance between the transmitting and receiving piezoelectric crystal.

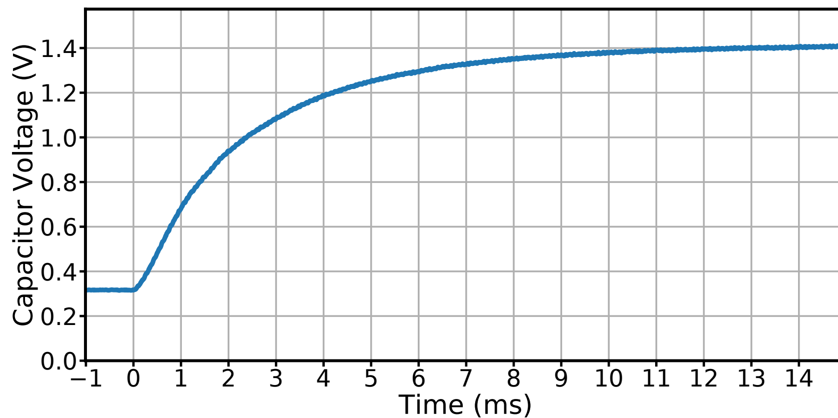


Figure 6.17.: Charging curve of the $220\,\mathrm{nF}$ capacitor over ultrasound with the ASIC.

Figure 6.18 shows the location pulse generated by the ASIC. Unfortunately, the altered echo from the implant cannot be measured with this ASIC. Due to a late change of the receiving piezoelectric crystal, the load modulator resistor does not have the correct resistance for the currently used piezoelectric crystal of $827\,\Omega$. Instead, an integrated fixed internal load modulator

resistor with $250\,\Omega$ is implemented in the ASIC, making a change after fabrication impossible. Therefore, data can only be transmitted to the ASIC, but not received with the present ultrasonic transmission path. However, to observe the location pulse on the ASIC, it is powered with a laboratory power supply at a constant voltage of $1.4\,\mathrm{V}$. One piezoelectric crystal input of the ASIC is pulled down to ground with a $100\,\mathrm{k\Omega}$ resistor, whereas the other input has a pull-up resistor attached to the supply voltage. Once the load modulator turns on, the voltage of the piezoelectric crystal input rises due to the load modulator. This behavior can be observed every $56.5\,\mathrm{ms}$.

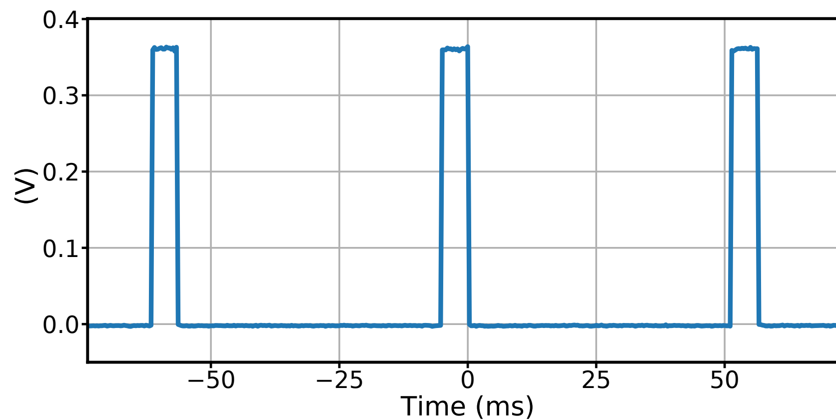


Figure 6.18.: Location pulses generated by the ASIC. Every $56.5\,\mathrm{ms}$ the impedance is adapted to transmit a location pulse.

The fabricated ASIC in a $180\,\mathrm{nm}$ technology is shown in Figure 6.19. The area of the complete ASIC is $2.25\,\mathrm{mm}^2$, whereas active circuitry uses only $0.13\,\mathrm{mm}^2$. The remaining area is occupied by bond pads, an IO ring, and an ASIC artwork. Only 4 of the 24 bond pads are necessary for operation. The rest of the implemented bond pads are for test purposes and the optional SPI interface. Therefore, the size of the complete ASIC can be significantly reduced for a future ASIC.

6.3. Summary

An ASIC in a $180\,\mathrm{nm}$ technology was fabricated, showing a working concept for ultrasonic-powered ASICs in smart implants with a projected size of $2\,\mathrm{mm} \times 2\,\mathrm{mm} \times 10\,\mathrm{mm}$. A bidirectional communication protocol was developed with the fabricated ASIC. To locate the implant inside the human body, the ASIC generates a location beacon periodically. Finally, a test platform for transmitting ultrasonic energy and data was developed which demonstrates energy and data transmission for distances of up to $30\,\mathrm{mm}$ to the ASIC and shows the successful operation of the system.

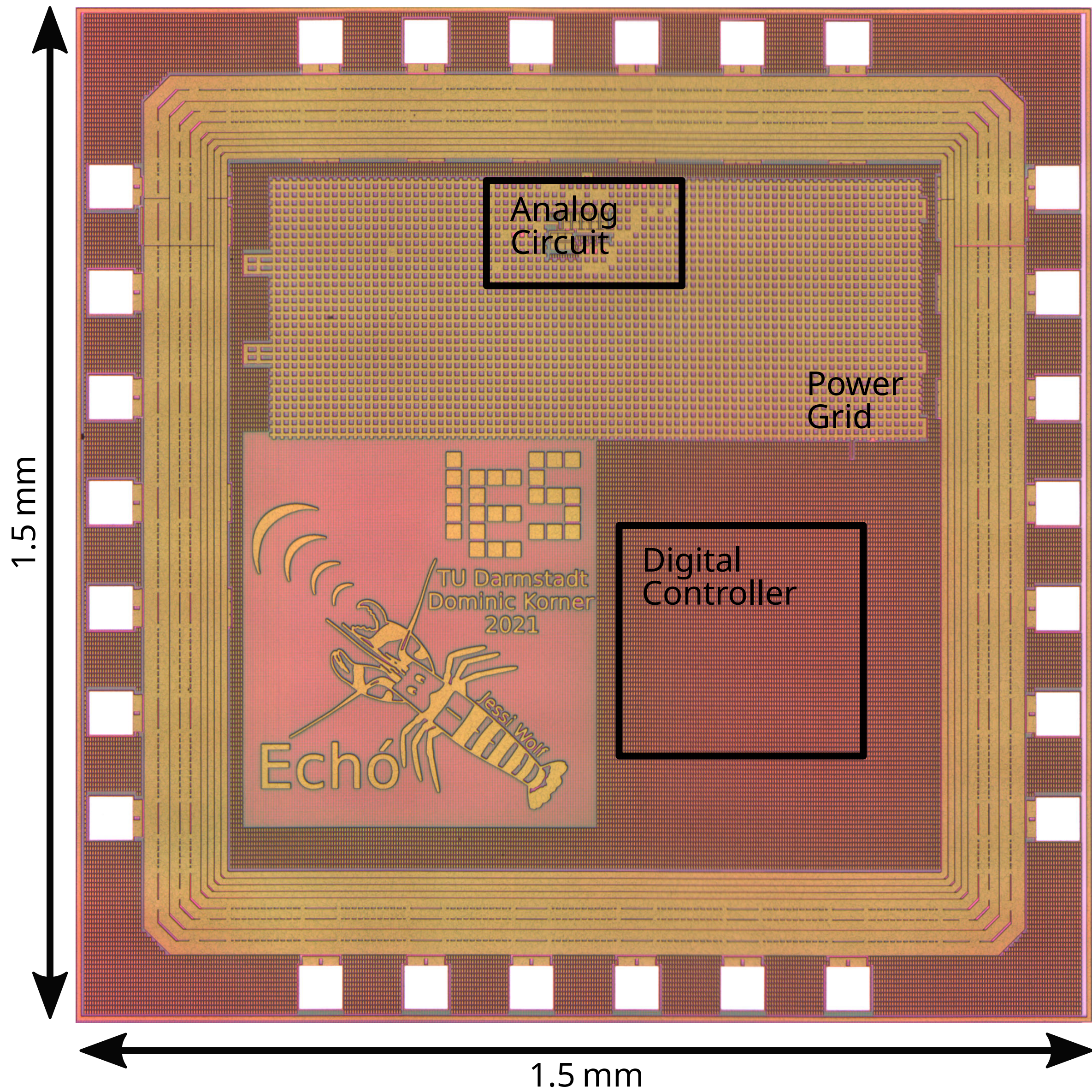


Figure 6.19.: Dieshot of the fabricated ASIC in a $180\,\mathrm{nm}$ technology with an area of $2.25\,\mathrm{mm}^2$.

7. Light Powered ASIC Tag for Discovery of Novel Drug Candidates

Identification of novel drug candidates requires large libraries of created compounds [70]. Combinatorial chemistry, invented by Árpád Furka in 1982, can generate vast numbers of different compounds in a single split and pool process [71, 72]. A programmable ASIC particle is developed to track the formation of the compounds and speed up the tracking process of the formed compounds. This method requires thousands of individual particles to accomplish a good coverage during the experiment, making the programmable particle very cost-sensitive. Each ASIC particle gets coated with a different compound during the split and pool synthesis, therefore it needs to be mechanically and chemically robust. Additionally, the simultaneous programming of many ASIC particles has to be possible. Due to the cost sensitivity and the required mechanical and chemical robustness, an ASIC particle without any external components is preferred. Integrated solar cells allow an ASIC particle without the need for any external components for energy and data transmission. Many similar systems have been developed, but none of them feature an at run-time programmable NVM, which imposes additional requirements on the system [73, 74, 75, 76, 77].

This chapter presents a programmable ASIC particle powered over light. Therefore, the first section explains the split and pool synthesis, followed by the implemented and fabricated ASIC in Section 7.4. It also includes measurements of the integrated solar cells in Section 7.4.4.

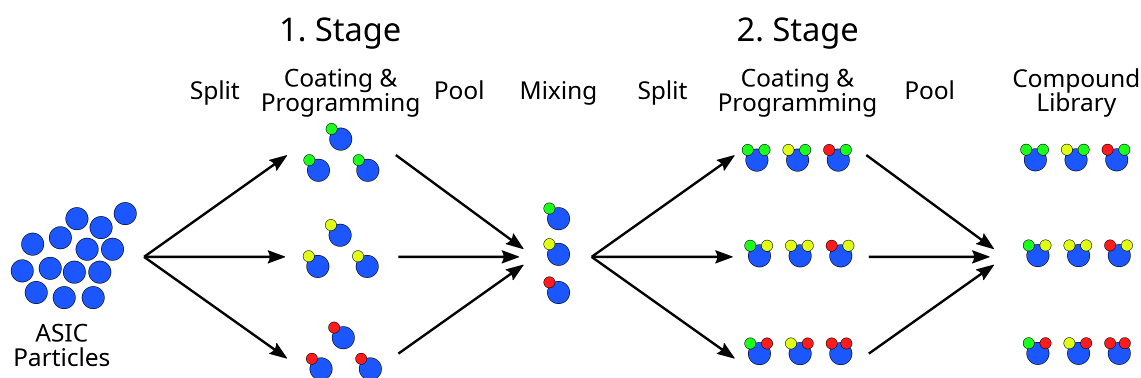


Figure 7.1.: Split and pool synthesis using three different building blocks and two stages. This will result in 9 different generated compounds in the resulting library.

7.1. Split and Pool Synthesis

Figure 7.1 shows a two-stage split and pool synthesis with three different **B**uilding **B**locks (BBs), displayed in green, yellow, and red. In general, the number of stages and compounds is not limited, making the generation of large amounts of different compounds in one single split and pool process possible. The first step divides all ASICs into three portions (split). Every portion is coated with a different BB, resulting in three differently coated ASIC particles. The information on which BB is coated to the particle is written to every group of particles by using an optical link. It is saved permanently by writing the information to an internal NVM. In the next step, all particles are combined and mixed, forming a mass of three different coated particles (pool). In the second stage, the particles are split again, forming three portions. Every portion contains particles with all three different kinds of coatings, namely green, yellow, and red. Now, the first portion is coated with the green BB, the second with the yellow BB, and the third with the red BB. Again, the respective information is written to every group of particles. Every portion now contains three different combinations. The resulting compound library is constructed by pooling the three portions, resulting in nine compound combinations. The promising formed compounds can be identified chemically, but the exact way to reproduce the compound is lost in the process during a conventional split and pool synthesis. However, in this case, the compound can be identified by reading the information stored in the ASIC particle.

The complete split and pool synthesis is based on a combinatorial process, therefore it cannot guaranteed that every possible compound is present in the resulting compound library. In any case, more particles than possible formed compounds are required. The maximal number of formed compounds N per experiment is expressed in the following equation, where s is the different BBs and m is the number of stages:

$$N = s^m \tag{7.1}$$

The probability P that a certain compound forms during the split and pool synthesis can be calculated to

$$P = 1 - \left(\frac{N-1}{N}\right)^k \tag{7.2}$$

where k is the number of used ASIC particles. The probability P is equal to the coverage of the whole experiment. As an example, a split and pool synthesis, which uses 4 different BBs and 6 stages, results in 4096 different generated compounds. If 10000 particles are available, the coverage of particles coated with a compound compared to all possible formed compounds can be calculated to

$$P = 1 - \left(\frac{N-1}{N}\right)^k = 1 - \left(\frac{4096-1}{4096}\right)^{10000} = 91.3\%. \tag{7.3}$$

Subsequently, a successful split and pool synthesis requires a large number of individual particles and hence the cost of the individual particle is an important factor. The particle should only

consist of a single ASIC without any external components to reduce the cost. Therefore, it has to contain all necessary components integrated into a single ASIC containing a power source, data receiver, NVM, and control logic. Additionally, the cost is dominated by the size of the ASIC, so an area-efficient design is important. A suitable technology has to be selected, which offers solar cells for the energy supply and an NVM as shown in Figure 7.2.

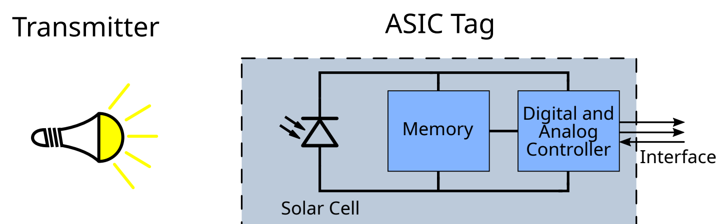


Figure 7.2.: The ASIC particle has to contain an on-chip solar cell, NVM, digital, and analog circuits to track the deposited BBs during a split and pool synthesis.

7.2. Technology Selection

A suitable technology that is applicable in a split and pool synthesis has to offer an integrated NVM, solar cells, and the possibility to include analog and digital circuitry. Implementation of analog and digital circuitry is possible in nearly all modern CMOS technologies. An NVM, on the other hand, requires additional process layers and is therefore only available in a few technology variants. There are different NVM types suitable for integration in this application: OTP which can be programmed only once, and EEPROM which is multiple times programmable. Both variants are viable options for this use case since the available storage is sufficient to save all data of a split and pool synthesis. An EEPROM would have the advantage of deleting and rewriting the memory and therefore use it in multiple split and pool synthesis thereby reducing the cost.

An OTP, consisting of polysilicon, usually needs a high current to burn the fuse link. The current required to save data and hence burn the fuse link is in the range of $20\,\mathrm{mA}$ to $100\,\mathrm{mA}$ for several milliseconds [78]. Hence, using this kind of fuse requires a lot of power, making this type of storage unsuitable for the ASIC tag since the internal capacitors cannot store enough energy. An internal EEPROM, on the other hand, requires a high voltage of about $10\,\mathrm{V}$ to $20\,\mathrm{V}$ and has a write and erase time of about $1\,\mathrm{ms}$ to $5\,\mathrm{ms}$ [79]. The current needed for Fowler-Nordheim tunneling, and hereby programming the EEPROM, is negligibly small compared to the power consumption of a polysilicon fuse. An on-chip charge pump or a serialization of solar cells is necessary for generating such high voltages on the ASIC.

A serialization of solar cells would save the area required for a charge pump to generate the supply voltage of the analog building blocks and the integrated EEPROM. However, standard CMOS processes do not allow serialization of solar cells because they cannot be electrically isolated from each other. An **S**ilicon-**o**n-**I**nsulator (SOI) technology on the other hand, can provide a galvanic

isolation for each solar cell, and hence a serialization of multiple solar cells is possible. It allows solar cells, with a single voltage of around $0.5\,\mathrm{V}$ to $0.7\,\mathrm{V}$, to generate the supply voltage for any part of the ASIC without using a charge pump, which would cost additional energy and chip area.

Every p-n junction is sensitive to incident light on the ASIC and generates leakage currents when exposed. Therefore, the sensitive circuitry needs protection from the light of the light source. Protection can be formed by a closed metal layer that covers all circuitry except the solar cells on the ASIC. Since the metallization layer needs to be closed, it cannot be used for routing electrical signals anymore. When using two metal layers for electrical signal routing, at least a third metal layer is required to form the light protection layer.

Table 7.1 gives an overview of typical mixed signal CMOS processes. As previously noted, a suitable process would need an EEPROM as a non-volatile memory, on-chip solar cells, and an SOI process. Only the process XT06 from X-Fab fulfills all these requirements [80, 81]. To save costs, the fabricated ASICs in this thesis are based on the process XC06 from X-Fab, which is the same process with regard to electrical and optical properties, but without the SOI option. Since this process does not allow serialization of solar cells, the fabricated solar cells are measured in a single configuration, while the rest of the circuit is fabricated and measured normally. Measurements from single solar cells allow the calculation of the required area and amount of solar cells, as well as enabling the construction of a simulation model.

Manufacturer	Node	Technology	Photodiodes	OTP	EEPROM/Flash	Reference
X-FAB XC06	$600\,\mathrm{nm}$	Bulk	Yes	Yes	Yes	[82]
X-FAB XT06	$600\,\mathrm{nm}$	SOI	Yes	Yes	Yes	[82]
X-FAB XH035	$350\,\mathrm{nm}$	Bulk	Yes	Yes	Yes	[82]
AMS C35 Opto	$350\,\mathrm{nm}$	Bulk	Yes	No	No	[83]
X-FAB XT018	$180\,\mathrm{nm}$	SOI	No	Yes	Yes	[82]
UMC L65N	$65\,\mathrm{nm}$	Bulk	No	No	No	[84]

Table 7.1.: Selection of different technologies available for prototyping. The process XT06 from X-Fab offers all required devices and is hereby selected for the ASICs.

7.3. Communication Protocol

The communication protocol ensures a constant energy transfer during the active phase of the ASIC since no internal or external energy storage is possible. Therefore, the ASIC uses an amplitude-modulated signal as shown in Figure 7.3. An AC signal is modulated onto a DC carrier with an amplitude of roughly 10%. A $100\,\mathrm{\mu s}$ period represents a digital one, while a $20\,\mathrm{\mu s}$ signal period represents a digital zero. At the beginning of a transmission, a power-up sequence charges the internal capacities and lets the internal reset circuit and bandgap reference stabilize. The power-up sequence consists of transmitted zeros, allowing the receiver to adapt to the current illumination intensity. After the power-up sequence, the start transmission signal consisting of 13 ones is transmitted, followed by the actual payload consisting of a 5-bit address and 8-bit data. After the

payload is transmitted, the same data is transmitted again, but bitwise inverted to the ASIC to make sure that the correct data has been received. A decoder reconstructs the address and data in the digital controller. After a successful transmission, the ASIC will need roughly $10\,\mathrm{ms}$ time to write the received information to the EEPROM. Hence, the last phase of the communication sends energy by transmitting zeros to the ASIC, like in the power-up phase.

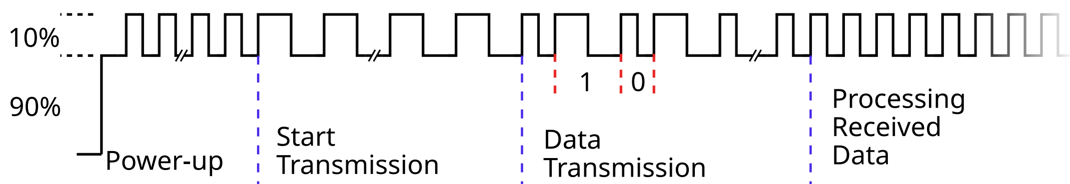
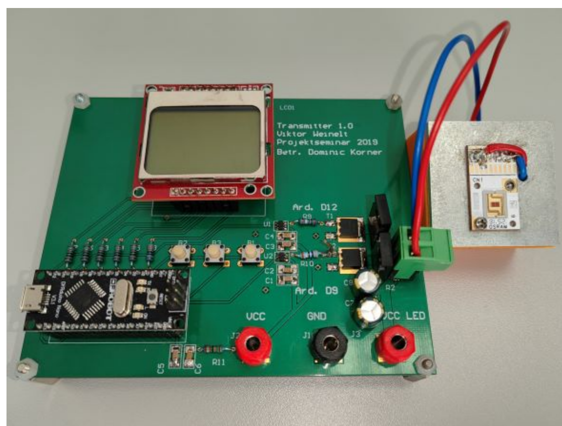
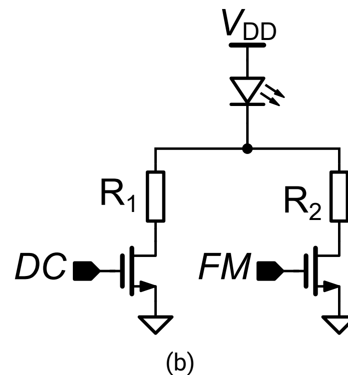


Figure 7.3.: Optical communication protocol scheme for transmitting data to the ASIC.

The optical transmitter generates the required waveform for powering the ASIC and transmitting the data. Figure 7.4 shows the transmitter PCB and the circuit for controlling the red high power **L**ight-**E**mitting **D**iode (LED), here an Osram LE A P1W. A MOSFET in series with a resistor controls the current through the LED. R_1 has a resistance of $2\,\Omega$, while R_2 has a resistance of $22\,\Omega$, achieving a signal amplitude of approximately 10% with a DC offset of 90% at an LED current of $10\,\mathrm{A}$. The heat generated by the resistors is negligible due to the short length of the complete communication and storage phase of the ASIC of less than $20\,\mathrm{ms}$. This approach is capable of transmitting data with a bandwidth of over $4\,\mathrm{MHz}$, measured with a discrete-build photodiode transimpedance amplifier. Therefore it qualifies for generating a rectangle signal of $50\,\mathrm{kHz}$ for the communication protocol.



(a)



(b)

Figure 7.4.: (a) Optical transmitter for sending data with a red high power LED to the ASIC. (b) Schematic for optical transmitter.

7.4. Implemented Solar Powered ASIC Tag

Figure 7.5 shows a block diagram of the complete implemented SoC for the split and pool synthesis. It consists of one single ASIC with all required components monolithically integrated. It includes a power-on reset circuit, bandgap voltage reference, optical receiver, RC oscillator, digital controller, and test circuitry. The test circuitry implements a large closed metal plane with solar cells below it. This enables a measurement of the light gradient below a closed metal plane and therefore evidence on how to design an effective metal plane shield. These measurements are presented in Chapter 8.3.3 in detail. For this prototype, the XC06 process is used instead of the XT06 process from X-Fab, which does not offer the SOI process option. This affects the EEPROM and the solar cell array. The EEPROM is not available in this process, therefore the EEPROM itself is not integrated into this version, but the interface for controlling the EEPROM is simulated and tested on the fabricated ASIC. Due to the missing SOI option, the solar cell array could not be fabricated in the XC06 process. Instead, a variety of solar cell structures and sizes are fabricated, allowing an estimation of the required solar cell area and number of in series connected solar cells. Additionally, it enables the generation of a simulation model for a solar cell array.

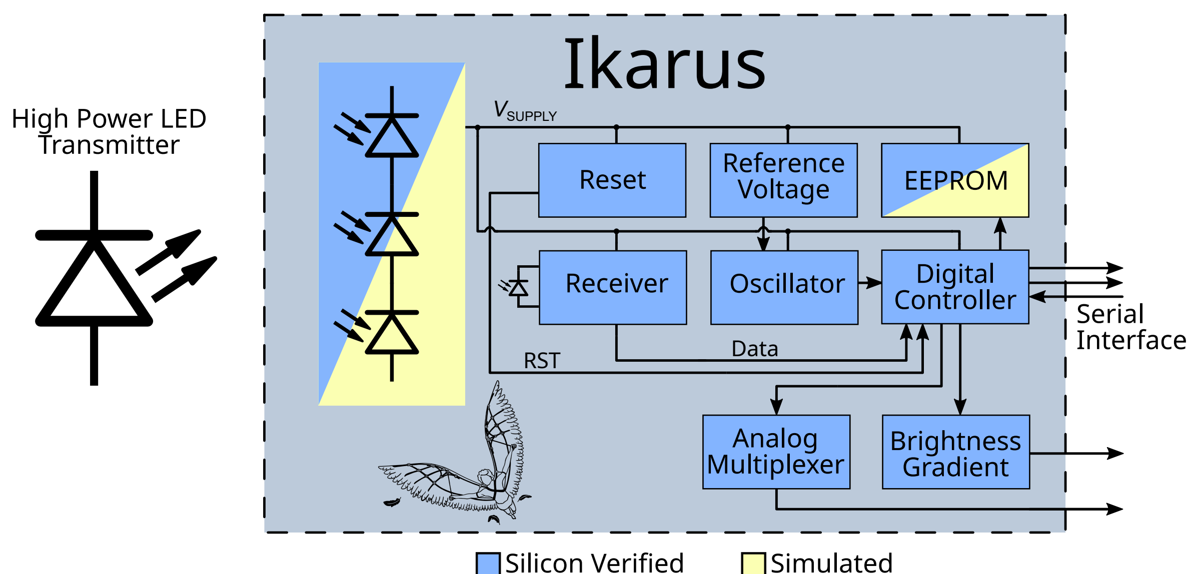


Figure 7.5.: Overview of the implemented ASIC. The blue system blocks are implemented and verified. The yellow blocks are simulated, but not yet implemented in the current ASIC. Different solar cells were implemented to characterize the performance and estimate the required chip area.

7.4.1. Analog Schematic Implementation

The internal analog circuitry of the SoC consists of a power-on reset circuitry, a bandgap voltage reference, the optical receiver, and an RC oscillator. This section provides a detailed schematic and description of each component.

Power-on Reset

Figure 7.6 shows the implemented power-on reset generator. Compared to a standard reset circuit, it generates a reset if sufficient voltage is present and additionally monitors the light intensity by loading the solar cells. Therefore, it prevents an inadvertent activation of the system without a sufficient light intensity present. The on-chip solar cells generate the supply voltage V_{dd} for the power-on reset circuit. Since the open circuit voltage of a solar cell at low light conditions is not distinguishable from a solar cell at high light conditions, the four resistors R_1 to R_4 form a reference voltage and a resistive load. The comparator $Comp_1$ switches the output to a high level once the voltage over R_4 is higher than V_{ref}. This is only the case if the solar cells provide a voltage of $3.8\,\mathrm{V}$ or more and thereby a current over $110\,\mu\mathrm{A}$. A short light burst will not activate the system since capacitor C_1 adds a delay of $400\,\mu\mathrm{s}$ to the output. The reset generator only unlocks the system if the high light condition persists until the capacitor C_1 is charged.

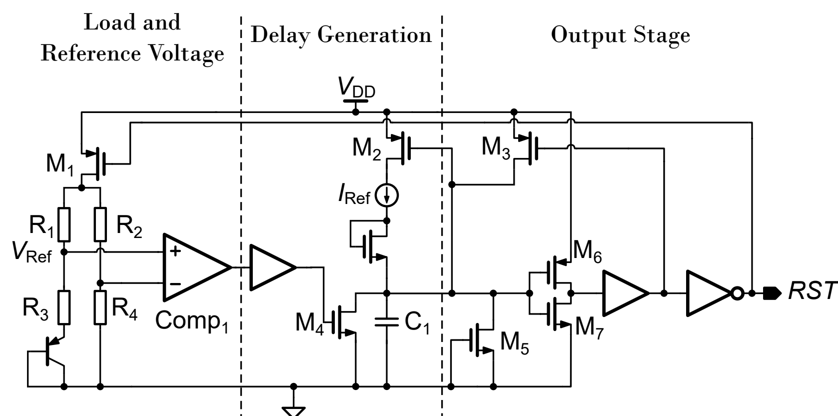


Figure 7.6.: Schematic of the reset generator including a resistive load to prevent inadvertent activation of the system.

Bandgap Voltage Reference

The bandgap reference circuit shown in Figure 7.7 is based on the proposed design of the book "Design of Analog CMOS Integrated Circuits" [24]. Instead of a passive current mirror, this bandgap reference uses an active-controlled current mirror consisting of the transistors M_1 to M_4 and the operational amplifier A_1. It improves the power supply rejection ratio and requires a lower supply voltage compared to a cascode reference. Schottky diode D_1 raises the input voltage

of A_1 about $300\,\mathrm{mV}$, allowing the n-channel input stage of A_1 to work properly. Due to PVT variations, the bandgap reference has a specified output voltage range of $1.15\,\mathrm{V}$ to $1.27\,\mathrm{V}$ and supplies the EEPROM and the internal oscillator. Monte Carlo simulation and measurements on the fabricated ASIC confirm compliance with the required specifications. The simulated nominal power consumption is $8.4\,\mu\mathrm{A}$.

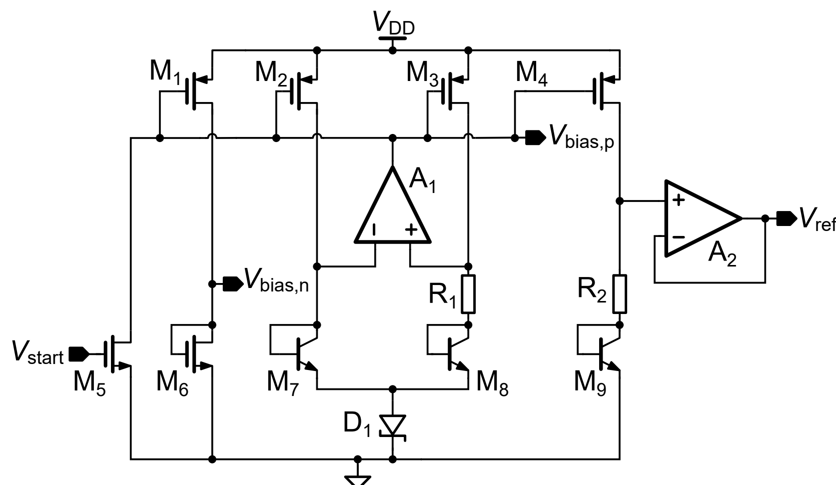


Figure 7.7.: Schematic of the low power bandgap reference providing robust output voltage and current against PVT variations.

RC Oscillator

The internal oscillator is based on an RC oscillator architecture, as shown in Figure 7.8. Internally, the oscillator runs at a frequency of $78\,\mathrm{kHz}$ and has a power consumption of $3.7\,\mu\mathrm{A}$. Since the EEPROM requires a frequency of around $100\,\mathrm{Hz}$ to $200\,\mathrm{Hz}$, the clock is divided by 9 flip-flops to $152\,\mathrm{Hz}$.

Optical Receiver

Figure 7.9 shows the implemented optical receiver. It is based on a paper from Mahowald [85]. A brightness adaption circuit consisting of amplifier A_1, transistor M_1, and low pass filter LP_1 controls the optical receiver diode D_1. A_1 amplifies the voltage over the photodiode. The elements M_1, LP_1, and A_1 form a control loop to adapt to different light intensities. Since a digital one and zero are distinguished by the length of each data bit, the time between each bit is measured. Therefore, capacitor C_1 charges with a constant current, and comparator $Comp_2$ sets the flip-flop to one if capacitor C_1 is charged above the threshold V_{ref}. The charging curve of capacitor C_1 is designed in a way, that despite PVT variations, the receiver can reliably distinguish between a zero and a one. At the start-up of the ASIC, the receiver is active while the EEPROM is inactive.

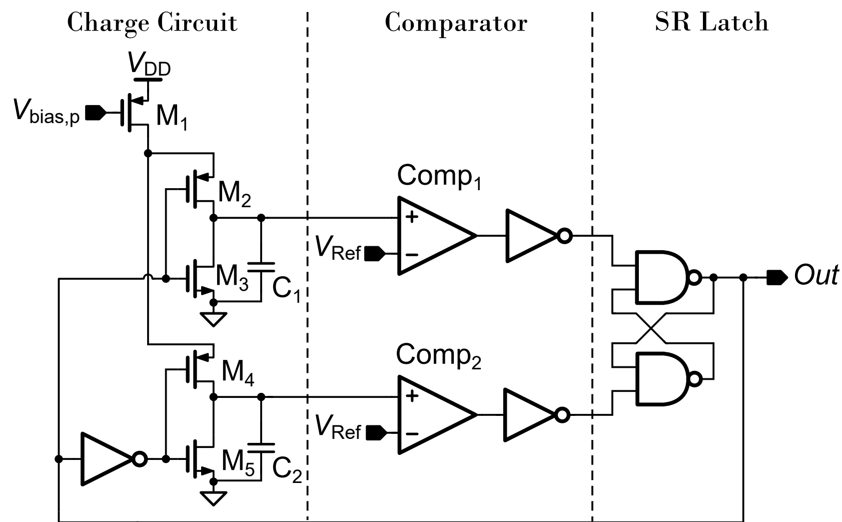


Figure 7.8.: Schematic of the low power RC oscillator with an output frequency of $78\,\mathrm{kHz}$.

After a successful reception of data, the receiver will be shut down, and the EEPROM can store the information on its NVM. Since the EEPROM consumes much more power than the receiver, the circuit is tuned towards a low bit error rate and small layout area instead of power consumption. The current consumption of the receiver is $56.52\,\mu\mathrm{A}$.

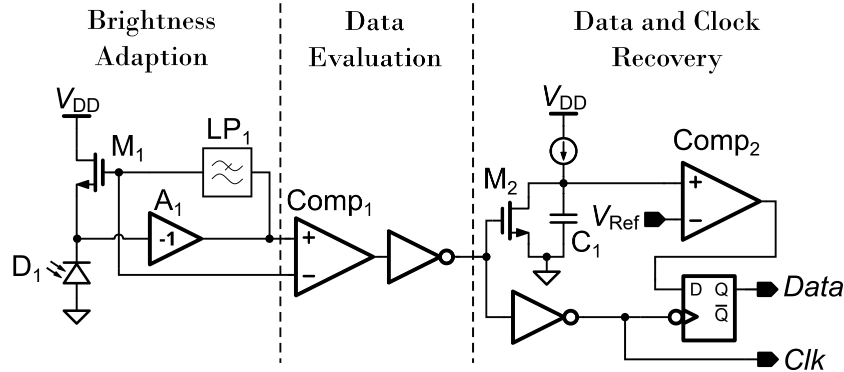


Figure 7.9.: Optical receiver schematic including clock and data recovery circuit.

7.4.2. Digital Controller

Figure 7.10 shows the digital controller of the ASIC. It is divided into two circuit blocks consisting of a circuit for normal operation (blue underlined blocks) and a circuit for test purposes only (yellow underlined blocks). During regular operation, the decoder decodes the received 26-bit

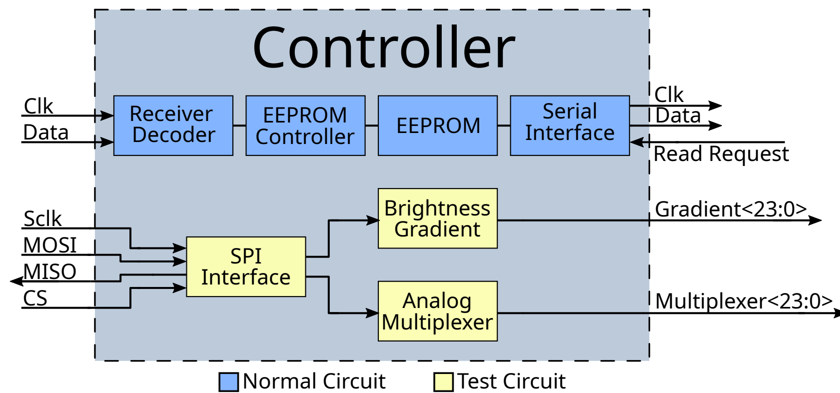


Figure 7.10.: The digital controller includes the decoder for the optical receiver as well as an EEPROM controller and the serial interface for reading out the EEPROM. Additionally, an SPI interface for test purposes is integrated.

data and checks if the first 13-bit data matches with the subsequent received inverted 13-bit data. If this is the case, the EEPROM stores the data at the received address. After a split and pool synthesis, a serializer module can read the complete EEPROM to track individual ASIC particles. At a rising edge of the $ReadRequest$ signal, the data and the corresponding clock start to output the complete EEPROM content.

The test circuit consists of an SPI interface controlling a digital interface for the brightness gradient test circuit and the analog multiplexer. The brightness gradient module controls the solar cells under the shading metal plane. The analog multiplexer connects different analog signals on the ASIC to one bond pad. This allows the readout of multiple independent analog signals with only one physical bond pad.

7.4.3. Fabricated ASIC

Two ASICs were fabricated with a chip area of $8.16\,\mathrm{mm}^2$ each. Figure 7.11 shows the initial version of the light programmable tag. It possesses all the necessary functionality for programming the tag, except the in series connected solar cells and the EEPROM. During testing, it was revealed that the implemented light-protecting shield, consisting of the third metal layer, was insufficient to block the light in the sensitive circuit areas. This is caused by a too-small overlap over the circuit area and the metal slots engraved in the top layers. These metal slots are required for stress relief by the design rules.

The final fabricated ASIC, shown in Figure 7.12, reduces the energy consumption of the circuit and hereby reduces the area of the required solar cells. Compared to the first version, the actual size of the circuit for receiving and decoding the signal is much smaller, with only $1.35\,\mathrm{mm}^2$. The remaining chip area is occupied by test structures and IO pads. Also, the complete ASIC accomplishes higher precision analog circuitry and better reliability. The solid shading metal

Parameters	JSAC'09 [73]	TVLSI'11 [74]	p-Chip [75]	TED'12 [76]	TBioCAS'17 [77]	**This Work**
Tech. (nm)	180	350	-	350	180	600
Light Source	Laser	Laser	Laser	LED	Halogen Lamp	LED
Wavelength (nm)	830	532	658	White	White	617
Light Intensity	$80\,\mu W\,mm^{-2}$	-	$5\,mW$ to $60\,mW$	$31\,klx$	$1.13\,mW\,mm^{-2}$	$10\,Mlx \approx 36.6\,mW\,mm^{-2}$
Programmable NVM	No	No	No	No	No	Yes
Voltage boosting	Stacked	-	-	Stacked	Charge Pump	Series Connection
Area (mm^2)	25	0.338	0.36	1.38	1.54	1.921

Table 7.2.: Comparison of the implemented smart dust system with other state-of-the-art systems.

plane is fabricated without metal slots for reduced leakage currents in the circuitry and accurate measurements of leakage current under the metal plane. With these measurements and silicon-verified circuits, a final ASIC on the basis of an SOI process with in-series connected solar cells can be fabricated. The presented and fabricated ASICs prove the possibility of integrating all functionality on one single die since the closely related SOI process.

Table 7.2 shows a comparison of recent publications in the field of smart dust. The proposed ASIC is the only one of the compared smart dust ASICs that offers an NVM. Additionally, the NVM is writable, while the smart dust ASIC is powered solely with light. The here proposed ASIC uses the highest light intensity of $36.6\,mW\,mm^{-2}$ to supply the NVM, leading to a decreased required solar cell area. Compared to the other smart dust implementations, which use a light intensity up to $1.13\,mW\,mm^{-2}$, this implementation increases the light intensity by a factor of over 30.

7.4.4. Fabricated Solar Cells

All three fabricable solar cell types are tested on a manufactured ASIC to verify their efficiency. The measurements are carried out with the X-Fab XC06 process and a red high power LED LE A P1W from Osram [86]. It generates a light intensity of $10\,Mlx$ at a wavelength of $617\,nm$ on the ASIC. To achieve such a high light intensity, the high power LED is driven with a current of $10\,A$ and is mounted with a distance of $8\,mm$ between the ASIC and the high power LED. Since the LED consumes up to $36\,W$, it radiates a high amount of heat. During the measurement, the high power LED operates for only $150\,ms$ while taking a measurement point and then letting the LED and ASIC cool down. Since different structures of solar cells are possible, all three are tested for the highest efficiency in conjunction with the red high power LED. Figure 3.5 in Chapter 3.3 provides an overview of the possible solar cells in CMOS technologies. Figure 7.13 shows the load line of the three solar cell architectures, all with a size of $100\,\mu m$ x $100\,\mu m$. The Nwell/P+ solar

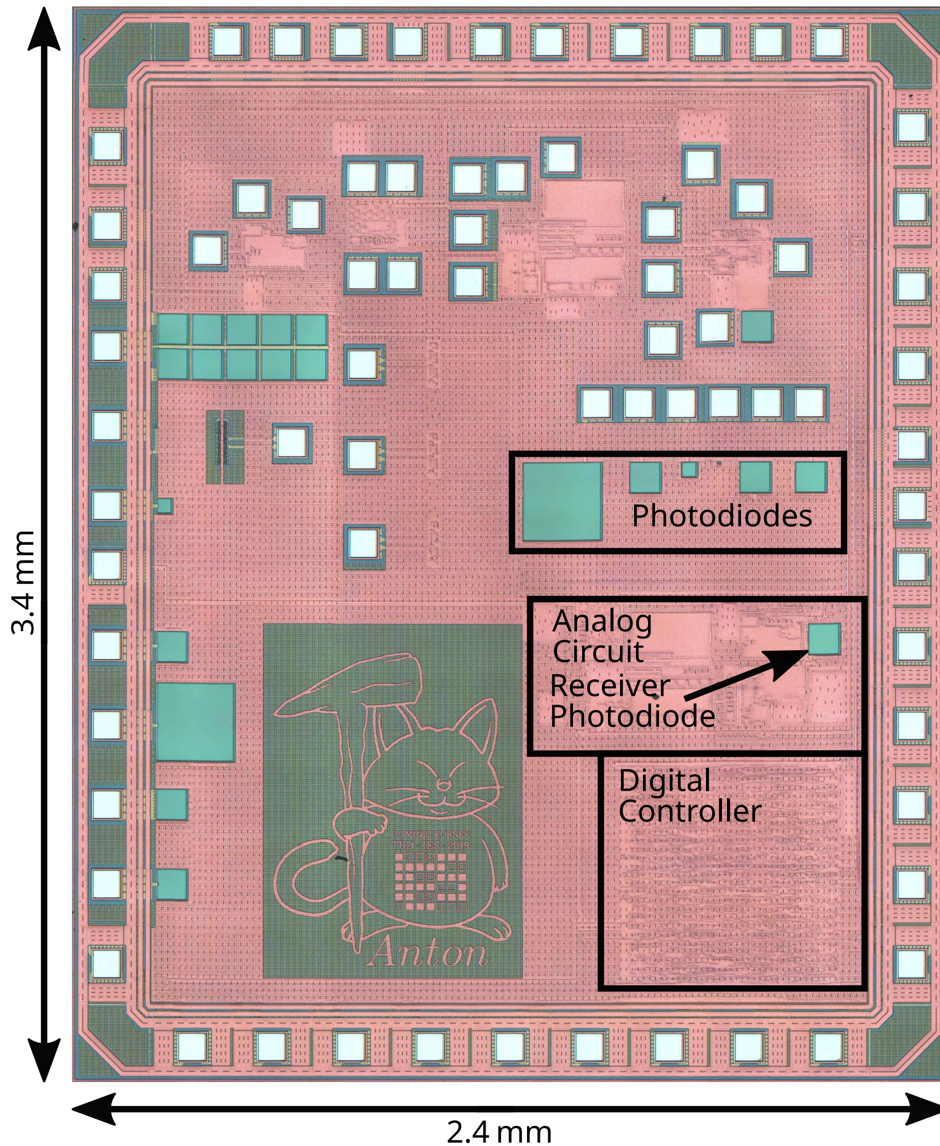


Figure 7.11.: Die photograph of the first fabricated version of the light programmable tag. The photodiodes have an edge length from left to right of $250\,\mu m$, $100\,\mu m$, $50\,\mu m$ and $8\,\mu m$.

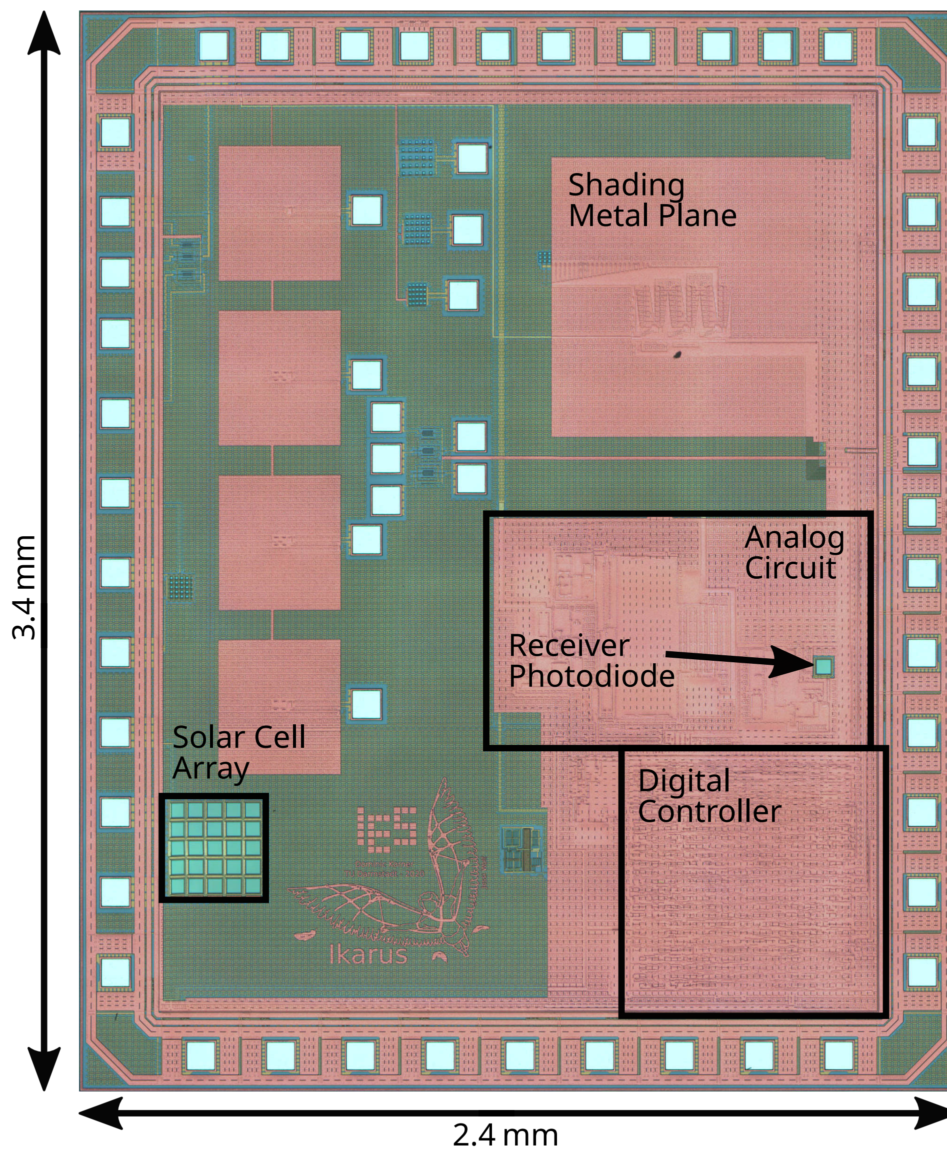


Figure 7.12.: Die photograph of the second fabricated version of the light programmable tag with improved power consumption and light-induced leakage current tests.

cell has the highest energy efficiency. It can generate up to 86 µW at an illuminance of 10 Mlx. At this power, it provides a voltage of 0.56 V and a current of 156 µA.

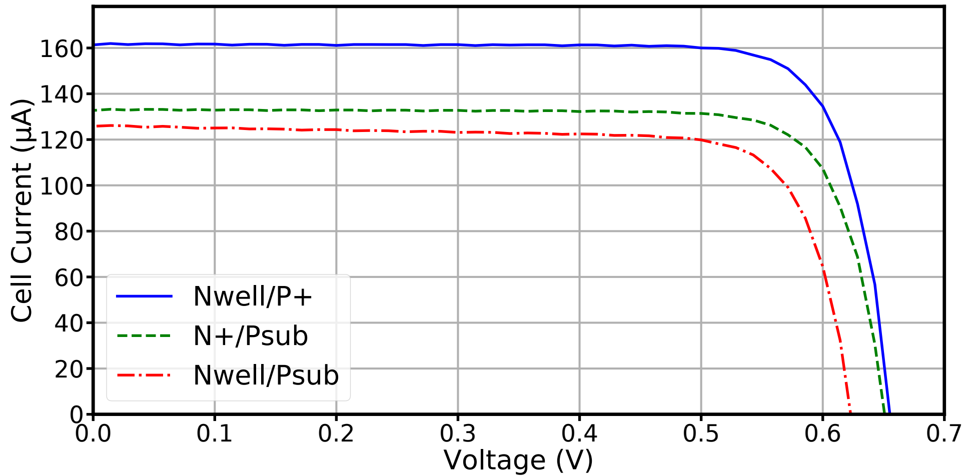


Figure 7.13.: Three different solar cell structures were measured with a size of 100 µm x 100 µm. The Nwell/P+ solar cell has the highest energy efficiency.

Since the power generated by one 100 µm x 100 µm solar cell is not enough to power the complete ASIC, a bigger solar cell size has to be used. The solar cell generates a current proportional to the incident light, which encounters the active p-n region. By using a bigger solar cell, the ratio between the outer edge and the inner active area of the solar cell changes. Hence, the power generated per area will decrease for bigger solar cells. Figure 7.14 shows the measurement results of an N+/Psub solar cell with 8 µm, 50 µm, 100 µm, and 250 µm edge lengths. It allows an estimation of the required solar cell area for the future fabricated ASIC. For solar cell areas over 62 500 μm^2, an extrapolation is required.

With the previous data, the required solar cell area can be calculated to 0.2 mm^2 at a light intensity of 10 Mlx or 36.6 $mW\,mm^{-2}$. The light intensity is approximately 30 times higher than other publications for smart dust powered by light. In theory, a lot higher intensities are possible, virtually only limited by the heat on the ASIC [21]. The drawback of this high light intensity is an increased leakage current in p-n junctions on the ASIC. Therefore, the additional metal shield layer is necessary to protect the ASIC.

7.5. Summary

For the novel approach of a light-powered ASIC tag, two ASICs were fabricated in a 600 nm process. The first iteration focuses on measuring the solar cells and testing the initially designed analog and digital circuits. In the second iteration, the analog circuit is improved in terms of area and power consumption and the light-induced leakage currents are investigated with a custom test

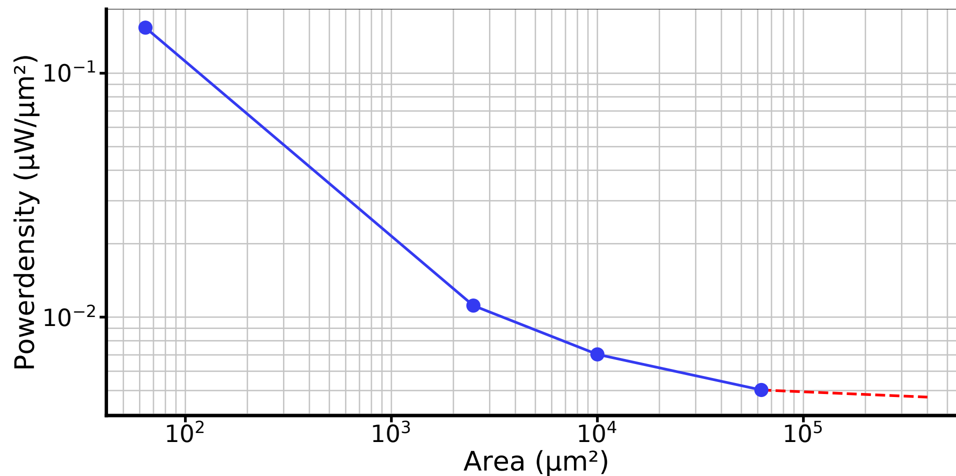


Figure 7.14.: Four different sizes of the N+/Psub solar cell are compared in terms of power over area. The blue line is measured on the fabricated ASIC. The red line extrapolates the results to larger solar cells.

structure.

In comparison to other publications, the application for identifying new drug candidates requires an NVM, which is programmable while the ASIC is powered solely over light. Due to the high power demand of the existing EEPROM solution, caused by the internal charge pump, the solar cells require a lot of chip area on the ASIC. To reduce the required area, the light intensity is raised to $10\,\mathrm{Mlx}$, which is 30 times higher than other implementations. This reduces the required chip area for supplying the ASIC to approximately $0.2\,\mathrm{mm}^2$.

Light shielding for the active circuitry is important to reduce leakage currents. Due to the high light intensity used in this thesis, the light shield becomes even more important. Therefore, a unique circuit for measuring the light intensity under a metal plane is implemented and explained in Section 8.3.3. To the author's knowledge, this is the only publication that measures the light intensity under a solid metal plane. It shows that a solid metal plane must extend at least $100\,\mathrm{\mu m}$ over leakage-sensitive circuits to reduce the generated leakage current significantly.

In summary, the second fabricated ASIC implements all necessary building blocks for carrying out a split and pool synthesis. The individual systems are fabricated and tested. It shows how to mitigate the light-induced leakage current on the ASIC. A future revision with an SOI process enables the serialization of solar cells and thus allows the full integration of the complete system into one single ASIC.

Part IV.

Results and Conclusion

8. Design of Autonomous System-on-Chips

This chapter deals with the major design considerations for implementing an autonomous SoC with wireless energy and data transmission. The first section dives into the importance of the correlation between the system design and the transmission technique and shows approaches to decrease the system size. The second and third sections focus on the transmission of energy and data over ultrasound as well as visible light, while the fourth section concludes these design considerations with a brief summary. At the end of each section, a box summarizes the most important findings.

8.1. System Size vs. Wavelength

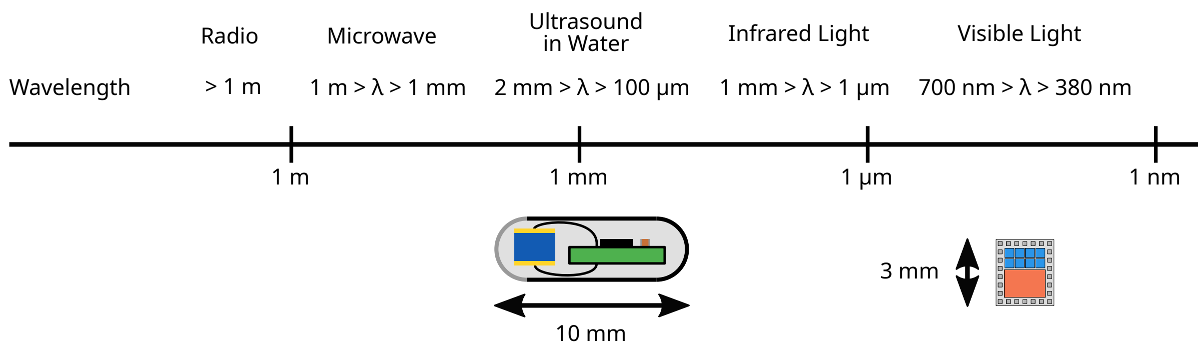


Figure 8.1.: Comparison of the wavelength for different power transmission methods.

The wavelength of the used wireless power transmission method has a direct influence on the overall system size due to the required antenna for energy and data transmission. For radio and microwave transmission, the length of a dipole antenna is proportional to the wavelength. Consequently, a smaller wavelength results in a smaller antenna [87]. This principle is valid for all kinds of antennas and not restricted to RF antennas and allows a first rule of thumb for selecting a proper operating frequency. Besides the size of the antenna, the dampening of the carrier wave in the transmission medium plays a major role for the energy transmission wavelength. It limits the maximum distance between the transmitter and receiver and represents an additional restriction in the selection of a suitable frequency. As a consequence, the most suitable wavelength for an application is to be carefully selected, depending on the transmission medium. Figure 8.1

shows a comparison chart of the different physical power transmission options. Besides light and microwave, ultrasound offers a wavelength within the range of a few millimeters in water, the human body, or metal, making the receiving element much smaller compared to an RF antenna. Therefore, this thesis focused on ultrasound and visible light for power transmission, which both offer a small wavelength and therefore promise a small overall system size. Ultrasound features a small wavelength in the human body and metal, resulting in the size of a few millimeters of the receiving piezoelectric crystal. In addition, ultrasonic waves can penetrate metal and have lower attenuation in human tissue in comparison to microwave transmissions. Compared to ultrasound, visible light additionally brings the potential of integrating solar cells as antennas on the same ASIC, allowing a single-chip energy autonomous communication platform without any external components and thereby making it extremely small.

As a result, the two major points for selecting a proper wavelength and transmission method are as follows:

Size vs. Wavelength

- **Antenna size scales proportionally with the wavelength: $\lambda \propto l$.** The size of the overall system is limited by the antenna size. Smaller wavelengths have a significant impact on the system size.
- **Dampening of the carrier wave restricts the maximum distance between transmitter and receiver.** A careful selection of a suitable wavelength and transmission method is necessary to avoid excessive dampening in the transmission medium. Additional restrictions on the maximum allowable transmission intensity may apply.

8.2. Systems with External Components

The ASIC for integrated machine elements in Chapter 5 and the medical smart implant in Chapter 6 both use ultrasound for energy and data transmission. Ultrasound is a technique used for many years in medicine, making it safe for operating implants below the maximum energy limits determined by the FDA in the human body. However, ultrasound is also suitable for machine elements, transmitting energy and data through a closed metal barrier. In both cases, a precise matching of the transmitting and receiving piezoelectric crystal is necessary for an efficient transmission. These systems always require at least one external element since piezoelectric crystals are not fabricable in a CMOS process.

8.2.1. Ultrasonic Energy Transfer

For a high-efficiency energy transfer, a good coupling between the transmitter and receiver piezoelectric crystal is essential. In the case of a SiMe, two piezoelectric crystal discs are in direct contact with a metal surface and the transmitter and receiver are only a few millimeters separated from each other. An additional layer of paraffin oil provides an airless contact to increase the energy

transfer efficiency. Two identical piezoelectric crystals with the same resonance frequency are used for transmitting and receiving ultrasound. In the SiMe, a further optimization of the resonance frequencies for the piezoelectric crystals is not required, since no limitation of the ultrasound intensity exists and the close distance of transmitter and receiver. For medical implants, the situation is quite different. Here, the FDA limits the ultrasound power and the distance between the piezoelectric crystal is much higher compared to the SiMe. The piezoelectric crystal of the implant also needs to be as small as possible to fit inside the housing. These constraints decrease the received voltage amplitude and therefore the usable power. To maximize the received voltage amplitude, the receiving piezoelectric crystal has to operate in the parallel resonance frequency for the ultrasound transmission. At this resonance, the impedance of the piezoelectric crystal has a local maximum, increasing the output voltage. A cubical form of the piezoelectric crystal is compact and allows the reception of ultrasound from almost any angle. As a reminder, the edge length τ_x of the cubical piezoelectric crystal for a given resonance frequency $f_p^{(1)}$ calculates to

$$\tau_x = \frac{1579.74\,\mathrm{m\,s^{-1}}}{f_p^{(1)}} \tag{8.1}$$

where $f_p^{(1)}$ is the parallel resonance frequency [47]. The opposite is valid for the transmitting piezoelectric crystal. At the series resonance frequency, the impedance has a local minimum, which allows the transmission of the highest power at a given input voltage. A standard piezoelectric crystal disc can be used to generate the ultrasonic wave since here no size constraints exist. Once the ultrasound energy is received, it requires a rectification on the ASIC. An integrated active rectifier increases the efficiency by avoiding the drop voltage of a standard diode rectifier. The following points summarize the measures taken for an efficient energy transmission:

Ultrasonic Energy Transfer

- **An efficient ultrasound transmission requires a good coupling between the piezoelectric crystals.** In liquids like water, an additional coupling layer is not necessary, but for transmission through metal, an adaption layer is necessary for a good coupling between the piezoelectric crystal and the metal surface.
- **Parallel resonance frequency of the piezoelectric crystal for receiving ultrasound.** In the parallel resonance frequency, the piezoelectric crystal operates with the maximum impedance, leading to the highest output voltage.
- **Series resonance frequency of the piezoelectric crystal for transmitting ultrasound.** In the series resonance frequency, the piezoelectric crystal operates with the lowest impedance, leading to the highest transmit power.
- **Active rectifier for efficient energy conversion from AC to DC.** An active rectifier eliminates the voltage drop compared to a diode bridge rectifier, increasing the efficiency of the overall system.

8.2.2. Ultrasonic Data Transfer

Both fabricated ultrasonic ASICs offer a bidirectional communication. Data transmitted to the ASIC is preferably based on counting pulses to decrease the required chip area. Therefore, the number of pulses encodes the data. This method requires only a comparator on the receiver side and therefore offers a small implementation size and low energy consumption at the expense of a low data rate compared to other modulation schemes. For receiving data from the ASIC, a backscatter amplitude modulation is preferably used for energy-efficient and small implementation sizes, only consisting of a resistor and transistor. The transmission option can be extended to an active scheme for transmitting data at higher speeds. An active transmission offers a higher data rate compared to a backscatter transmission at the expense of added energy consumption caused by the transmitter and more required chip area. Three active modulation types are integrated in this thesis, namely frequency, amplitude, and resonance modulation. For an ultrasonic data transfer, the following major design choices should be considered:

Ultrasonic Data Transfer

- **Counting pulses for data transmission to ASIC.** Counting pulses represents an energy- and area-efficient method for the implementation of a communication interface in an ASIC, at the expense of data rate.
- **Backscatter modulation for receiving data from the ASIC.** Backscatter data transmission from the ASIC is an energy- and area-efficient method for the implementation of a communication interface in an ASIC, at the expense of data rate.
- **Active transmission scheme for receiving data from the ASIC.** If higher data rates are required for receiving data from the ASIC, an active transmission scheme can exceed a backscatter communication, at the expense of higher energy consumption and higher area consumption on the ASIC.

8.3. Systems without External Components

Energy autonomous systems, fully integrated into one single ASIC reduce the overall system size and thus offer new application areas. A standard CMOS process enables two ways to replace the former external antenna for receiving energy and data: radio waves, microwaves, and light. Light offers a higher energy density and a higher range compared to an RF approach on ASICs, especially for small ASICs. Therefore, the focus of this section is on visible light to receive energy and data with on-chip solar cells.

8.3.1. Solar Cell-based Energy Transfer

On-chip solar cells provide a way to integrate an electrical energy source directly into the ASIC to receive the necessary power. A typical silicon solar cell generates a voltage of about $0.6\,\mathrm{V}$ to

$0.7\,\mathrm{V}$ per cell [21]. The supply voltage required to operate a typical CMOS process is between $1\,\mathrm{V}$ and $5\,\mathrm{V}$. Therefore, the voltage generated by a single solar cell is insufficient to operate a mixed-signal ASIC. The voltage needs to be increased either by a voltage converter or serialized solar cells. Two voltage converter topologies are implementable: A boost converter or charge pumps. Both require a large area integrated into an ASIC. Charge pumps, which do not require an integrated inductor, still use large on-chip capacitors and have an efficiency of around $50\,\%$, especially at these low input voltages [88]. Therefore, the most practical solution to increase the voltage generated by solar cells is to serialize them.

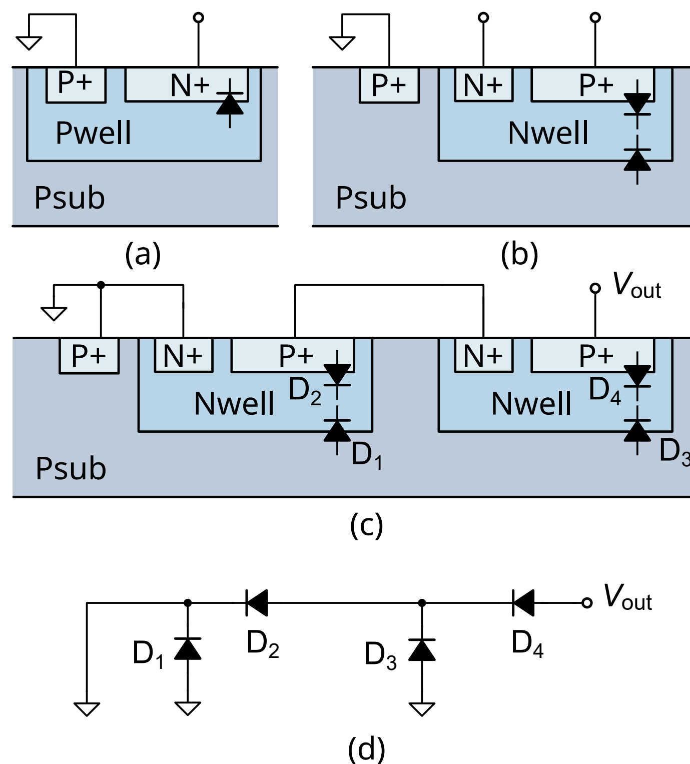


Figure 8.2.: (a) N+/Psub solar cell. (b) Nwell/Psub and Nwell/P+ solar cell. (c) Series connection of two Nwell/P+ solar cells. (d) Equivalent circuit of two in series connected Nwell/P+ solar cells [89].

Figure 8.2 shows a possible implementation to serialize solar cells in a standard CMOS process by using two different types of solar cells [89]. In Figure 8.2(a), the solar cell design consisting of an N+ implanted well on a p-doped substrate is shown. These solar cells cannot be serialized since the p-doped substrate would be shorted to the N+ implant. A viable solution is to use the solar cell structure shown in Figure 8.2(b). It consists of one solar cell from the p-doped substrate to an n-well and a solar cell from the n-well to a P+ implanted area. This allows a serialization of solar cells, as shown in Figure 8.2(c). The equivalent circuit of two solar cells in series is

shown in Figure 8.2(d). While solar cell D_1 is disabled by a short circuit and hence does not affect the circuit, solar cell D_3 is operated in the reverse direction, causing unwanted reverse currents. Unfortunately, light increases the leakage current of that solar cell, and part of the generated power of solar cell D_2 is drained to ground through solar cell D_3. This problem increases with the number of stages of in series connected diodes. As shown by Law et al., no more than three stages are realistically possible without increasing the size of the first stage massively, limiting the achievable voltage to $1.34\,\mathrm{V}$ [89].

Another approach to generate high voltages is shown by Horiguchi, by serializing an N+/Psub and Nwell/P+ solar cell [76]. Figure 8.3(a) shows the layout of this circuit, while Figure 8.3(b) shows the resulting equivalent circuit. In this configuration, a positive and negative voltage is generated by using a triple well process. The maximum voltage difference achievable with this configuration is boosted to $1.4\,\mathrm{V}$.

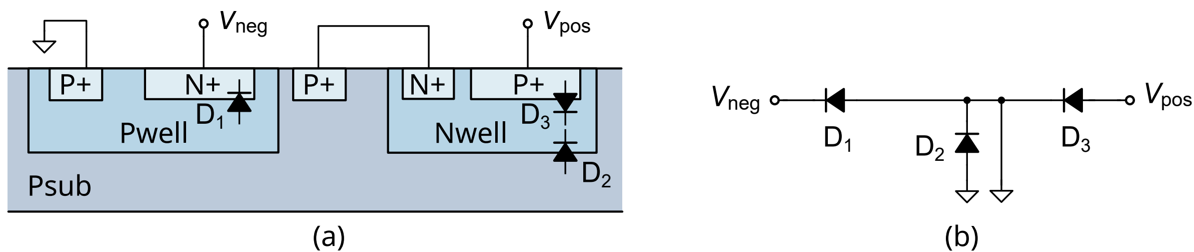


Figure 8.3.: (a) Series connection of a N+/Psub solar cell and a Nwell/P+ solar cell. (b) Equivalent circuit of two in series connected Nwell/P+ solar cells [76].

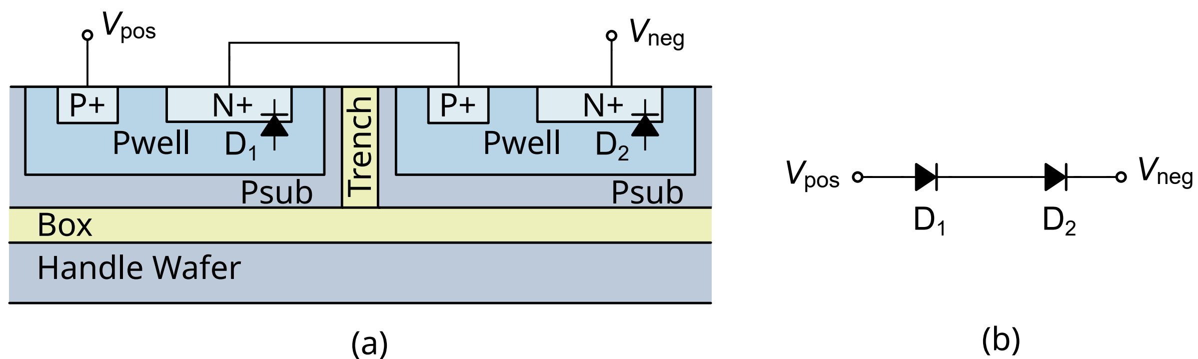


Figure 8.4.: (a) Series connection of two N+/Psub solar cells in an SOI process. (b) Equivalent circuit of two in series connected Nwell/Psub solar cells. No parasitic components are present, due to the galvanic isolation of the SOI process [90].

If a voltage above $1.4\,\mathrm{V}$ is required, there is no other way than using an SOI technology. With this technology, solar cells can be serialized practically infinitely on a single ASIC, depending only on the maximum trench and box isolation voltages [91, 92]. The SOI wafer contains an

additional **B**uried **ox**ide (Box) layer enabling a galvanic isolation between the handle wafer and the substrate in which the active devices are embedded. During the fabrication, a trench can be added separating the individual devices substrate. Figure 8.4(a) shows two solar cells connected in series in an SOI process. The trench between both solar cells provides a galvanic isolation between the two devices, preventing leakage current from parasitic diodes. In Figure 8.4(b) the equivalent circuit shows the two solar cells. Due to the isolation between the solar cells, no parasitic diodes are present, providing an ideal series connection.

Three solar cell topologies were presented in this section. A brief summary is given in the following box:

Solar Cell Topologies

- **A CMOS process limits the serialization of solar cells to 3 solar cells in series.** It results in a maximum output voltage of $1.34\,\mathrm{V}$. More than 3 solar cells in series would result in a high area consumption and low energy efficiency of the solar cells.
- **A positive and negative supply voltage can be generated by two different solar cell architectures.** With this approach, a voltage of $1.4\,\mathrm{V}$ has been demonstrated in a CMOS process.
- **Higher voltages than $1.4\,\mathrm{V}$ are only possible by using an SOI process.** An SOI process allows the almost unlimited serialization of solar cells and can hereby generate practically any required voltage directly on the ASIC with high efficiency.

8.3.2. Solar Cell-based Data Transfer

Solar cells can also be used for receiving data over light. By operating solar cells in the reverse direction as photodiodes, the receiving bandwidth is much higher compared to operating solar cells in the forward region. The transmitter uses a frequency modulation for transmitting data, with a continuously glowing LED. This ensures a constant energy transfer to the ASIC, which is required because of the lack of energy storage in the system. Measurements show that a commercially available high power LED can generate signals with a bandwidth of over $4\,\mathrm{MHz}$ [117]. Back communication with light is theoretically possible with an integrated LED on a CMOS process, but not available in standard CMOS processes. Due to the indirect bandgap of the silicon, no efficient silicon-based LEDs are fabricable at this time [93]. An external LED or an integrated **R**adio **F**requency **Id**entification (RFID) coil could enable a return channel, but external elements are not possible nor a return channel is needed in the described application in Chapter 7. The following box summarizes the most important findings in this section:

Solar Cell-based Data Transfer

- **A Solar cell operating in the reverse direction is used as a receiving element.** In reverse polarity, the receiving bandwidth of a solar cell is higher compared to forward operation.
- **A commercially available high power LED is fast enough as a transmitter LED.** An off-the-shelf LED provides a bandwidth of over 4 MHz and can generate a high illumination intensity to power multiple ASICs at once.
- **A constant on LED is required since no internal energy storage devices exist.** The constant on LED can supply the ASIC continuously with energy during active operation. On-chip capacitors are too small to cover short periods without light and would result in a restart of the ASIC.
- **For a bidirectional communication an integrated LED, or other communication methods than light are required.** To transmit data from the ASIC, an integrated LED or an internal coil is imaginable.

8.3.3. Light-Induced Leakage of Solar Cell-based ASICs

Increasing the light intensity in solar cell-based systems reduces the required chip area of the implemented solar cells. However, it also increases the generated leakage currents on the ASIC. Every p-n junction operated in the reverse direction on the ASIC can generate a leakage current if a photon hits the p-n junction. To counteract the increased power consumption, the ASIC needs light protection over the light-sensitive areas. Therefore, a metal layer acts as a light protection layer. Unfortunately, light can penetrate the space between the metal plane and the silicon. Usually, no exact process details are known to the IC designer, making the calculation of the size of the metal plane impossible. In addition, the design rules allow only a limited maximum size of metal planes without slots in the metal plane for mechanical stress relief. Since the specific process parameters are unknown, the exact penetration depth between the metal and silicon of the light cannot be calculated. Instead, the light gradient is measured on a fabricated ASIC by using photodiodes equally spaced under a closed metal plane. Figure 8.5(a) shows the complete metal plane, and Figure 8.5(b) the upper boundary of the shading metal plane in more detail, including the photodiodes. The measurement unit consists of a 3x24 photodiode array. Three photodiodes with a size $9.6\,\mu m \times 11.5\,\mu m$ are connected in parallel to increase the sensitivity. The pitch of the arranged photodiodes is $14.5\,\mu m$, accumulating to a total length of $348\,\mu m$. Every row is connected to a transmission gate, which is digitally controlled over an SPI interface to read out the array with a single bond pad. The transmission gates are placed in the middle of the shading metal plane, decreasing light-induced leakage as much as possible. The output is internally connected to a bond pad without any **E**lectro**s**tatic **D**ischarge (ESD) structure, avoiding additional leakage.

Figure 8.6 shows the measured photodiode current below the shading metal plane. The current

is proportional to the light intensity and decays exponentially under the metal plane. After 12 photodiode rows, the current saturates at about 3 µA, which translates to a distance of 174 µm. A future light shading metal plane has to extend at least this far to protect the underlying circuit from the high illumination intensity.

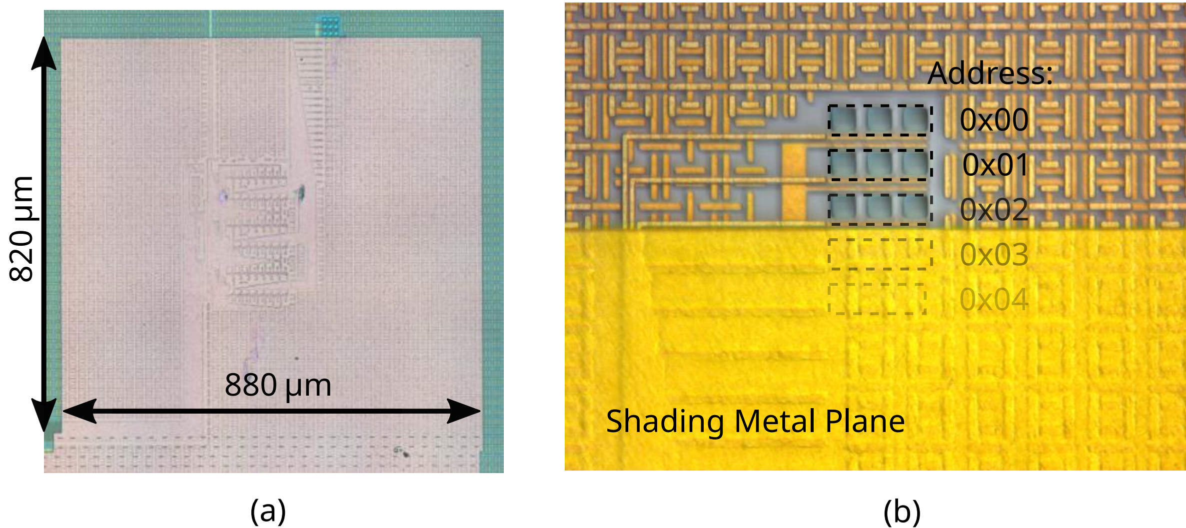


Figure 8.5.: Photograph of the fabricated shading metal plane. (a) The complete metal plane. (b) A cutout with three photodiode rows on the top.

The following recommended actions can be derived for shielding light from sensitive circuitry on the ASIC:

Light-Induced Leakage Current

- **Light generates leakage currents in p-n junctions across the ASIC.** Light on the ASIC generates significant leakage currents in the circuitry. A light-blocking metal layer can shield the majority of the light, therefore preventing the majority of generated leakage currents.
- **The metal layer has to extend** 100 µm **to** 200 µm **over the sensitive circuitry.** By following that rule, the light, and therefore the leakage current reduces over 90 %.
- **Any opening of the shielding metal layer must be avoided.** Although many technologies specify metal slots in their design rules, these must be omitted in critical areas over sensitive devices.
- **Use the lowest possible metal layer as a shield.** By using a lower metal layer, less light can penetrate the ASIC between the metal layer and semiconductor.

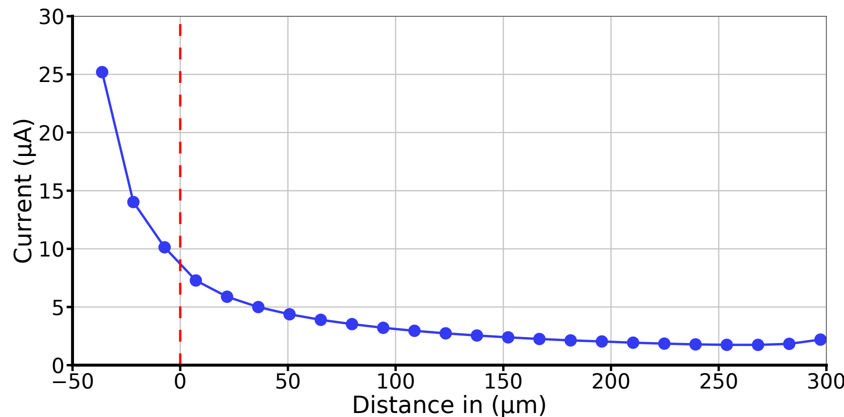


Figure 8.6.: Measured photodiode current below the shading metal plane under intense illumination generated by a high power LED current of $5\,\mathrm{A}$.

8.4. Summary

This chapter presents the most important design considerations for energy autonomous systems with regard to system size and how to supply an autonomous system with energy and data. It was shown, that the selected wavelength for transmitting data and energy, has a large effect on the overall system size, mainly caused by the required antenna. It proportionally scales with the wavelength, making smaller wavelengths better suited for smaller systems. Ultrasound with its small wavelength, is therefore beneficial for integration with system sizes with a length of minimal $10\,\mathrm{mm}$. For smaller systems, the required piezoelectric crystal limits the minimal size. On-chip solar cells can be used for these applications. They enable the integration of a complete system on a single die. Higher voltages than a single solar cell voltage of $0.7\,\mathrm{V}$ can be generated efficiently on the ASIC by using an SOI process. A high illumination intensity helps to decrease the required area for energy generation. However, the high illumination intensity leads to significant leakage currents in p-n junctions. Therefore, a metal plane should protect sensitive areas on the ASIC. Since light can crawl under the metal shield, it is suggested that the metal shield should extend at least $100\,\mathrm{\mu m}$ beyond the sensitive circuit area to shield a majority of the light.

9. Conclusion and Outlook

This thesis investigated the major design considerations and challenges for integrated autonomous SoCs with wireless energy and data transmission. After a brief introduction to the general architecture of autonomous systems and the wireless transmission methods, the most promising transmission methods were selected to demonstrate the theoretical findings with fabricated compact autonomous ASICs. Two ASICs using ultrasound for autonomous energy and bidirectional data transmission were fabricated in a $180\,\mathrm{nm}$ technology, showing an energy transmission power of $60\,\mathrm{mW}$. Two more autonomous ASICs utilizing light as a transmission medium were fabricated to reduce the system size further. These ASICs demonstrate the ability to transmit power and data to the system without any additional external components. General design considerations for autonomous SoCs were derived from the results of these four ASICs, which enable new application areas.

9.1. Conclusion

Several applications require extremely small energy autonomous systems without any wired connections. This work investigated different approaches using ASICs in standard CMOS technologies for the creation of such small autonomous systems. Two approaches that can provide energy and data to autonomous systems have been investigated. It was found, that applications allowing larger system sizes can be implemented using ultrasound. They require at least an external piezoelectric crystal, which cannot be integrated into a standard CMOS process. In contrast to ultrasound, visible light can provide energy to the ASIC and enable communication, while the system can be reduced to the ASIC only. For this purpose, solar cells can be integrated alongside the analog and digital circuitry and thus enable fully integrated autonomous SoCs, without any external components required.

The implemented ultrasonic SoCs demonstrate bidirectional communication and energy transmission to the system through different media like water and metal. By encoding the transmitted data with the number of transmitted ultrasound pulses, the size of the receiver circuitry can be minimized. The implemented active rectifier achieves a power density of $1016\,\mathrm{mW\,mm^{-2}}$. Using this technology, the longest dimension of the system can be reduced to $10\,\mathrm{mm}$. However, the energy-receiving element consumes most of the space, not the ASIC itself. In the case of ultrasound, this is the piezoelectric crystal, for electromagnetic waves, this would be usually a dipole or patch antenna.

Using electromagnetic waves to transmit power and data limits the reduction of system sizes

due to the antenna size. Integrating the antenna into an ASIC with a die size below $2\,\mathrm{mm}^2$ would result in a system that cannot receive enough power to carry out any energy-demanding tasks. This includes applications like writing on-chip memories or running compute-intensive tasks. Thus, to further reduce the system size, only light offers the possibility to additionally integrate the receiving element, in the form of solar cells, together with the digital and analog circuitry on a single die. On-chip solar cells can harvest higher power at a smaller system size. A series connection of solar cells can provide high voltages efficiently on the ASIC. This high voltage can be used to power the ASIC and directly write EEPROMs or OTP cells. It avoids therefore a low-efficient charge pump implementation, which would require additional chip area.

In contrast to the advantage of full system integration into a single ASIC, light generates leakage currents in p-n junctions of the surrounding circuitry. Therefore, a metal shield is proposed to block light from sensitive areas. Unique measurements show that light-induced leakage currents can be neglected when the light-protecting metal shield extends more than $100\,\mu\mathrm{m}$ over the sensitive circuitry. An area estimation of the required solar cell area can be made based on measurements for the harvested energy of the solar cells. Both findings show how to counteract the most severe problems of on-chip solar cells and are beneficial for the future implementation of fully integrated autonomous systems.

The results of this thesis lead to major design recommendations for prospective fully integrated SoCs with wireless energy and data transmission. Technology-specific and fundamental challenges of such SoCs are identified, and counteracting steps are provided. By taking these aspects into account, single-die, energy autonomous systems with integrated solar cells and integrated non-volatile memory in standard, cost-effective, CMOS processes enable a range of new applications.

9.2. Outlook

Based on the findings of this work, a new generation of fully integrated autonomous SoCs can be developed. The measurements for the light-blocking metal shield and the integrated solar cells allow an area-efficient implementation. The results are also adaptable to other, smaller process nodes for implementing an ASIC tag or other light-powered systems on a single die with an SOI process. The series connection of solar cells, shown in this work, offers the possibility to efficiently generate high voltages directly on the ASIC and would allow omitting charge pumps for high voltage generation. This would be advantageous for on-chip EEPROMs or OTP memories and can decrease the required chip area. A bidirectional communication interface would open new application fields for light-powered systems. A light source is currently not available in a standard CMOS process, but an integrated coil on the ASIC could offer a possible transmission link with electromagnetic waves.

Part V.

Appendix

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[95] David Riehl et al. "Flexible Modular Electronic Platform for Sensor-Integrating Bolts". In: *12. GMM/DVS-Fachtagung: Elektronische Baugruppen Und Leiterplatten - Nachhaltigkeit Und Energieeffizienz Mit Smarter Elektronik (EBL2024)*. Vol. 107. Fellbach, Germany: VDE-Verlag, Mar. 2024, pp. 313–316. ISBN: 978-3-8007-6265-1.

[96] Dominic Korner, David Riehl, and Klaus Hofmann. "Ultrasonic Energy Harvesting and Communication ASIC for Sensor-Integrated Machine Elements". In: *10. MikroSystemTechnik Kongress 2023*. Dresden, Germany, 2023.

[97] Dominic Korner et al. "Standalone Area Optimized ASIC Tag Powered and Programmable by Light for Identification of Novel Drug Candidates". In: *2023 26th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS)*. Tallinn, Estonia: IEEE, May 2023, pp. 150–154. ISBN: 9798350332773. DOI: 10.1109/DDECS57882.2023.10139720. Nominated for best paper award.

[98] Dominic Korner and Klaus Hofmann. "An ASIC-based Ultrasonic Beacon Sensor Platform with Energy Self-Sustaining Communication for Medical Implants". In: *EASS 2022; 11th GMM-Symposium*. 2022, pp. 1–3.

[99] Katrin Hirmer, Dominic Korner, and Klaus Hofmann. "Improving the Efficiency of a Multistage Boost Converter with Parallel Inductor Charging". In: *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*. IEEE, June 2018. DOI: 10.1109/compel.2018.8459928.

[100] Muhammad Bilal Saif, Dominic Korner, and Klaus Hofmann. "Apparatus and Method for Voltage Conversion". DE 10 2016 120 221 A1. June 2017.

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Supervised Theses

[102] Huanzheng Zhu. “Optimization of an Integrated Time-to-Digital-Converter for Resistive Strain Gauges”. Master Thesis, TU Darmstadt. 2024.

[103] K. Ding. “Design of a Time-to-Digital-Converter for Resistive Strain Gauges in a 180nm Technology”. Master Thesis, TU Darmstadt. 2023.

[104] M. Naneder. “Adaptive Threshold Estimation for Automatic Calibration of a Cellular Detector on SDR Basis”. Master Thesis, TU Darmstadt. 2023.

[105] M. Nilges. “Design and Development of a Custom ASIC Test PCB for Ultrasonic Communication”. Projektseminar, TU Darmstadt. 2023.

[106] L. Chen. “Evaluation and Implementation of Ultra Low Power Oscillator Circuits”. Master Thesis, TU Darmstadt. 2022.

[107] Q. Zheng. “Evaluation and Implementation of Ultra Low Power Voltage Reference Circuits”. Master Thesis, TU Darmstadt. 2022.

[108] Q. Zheng. “Low-Power-Consumption Optimization of the Clock Extractor”. Master Seminar, TU Darmstadt. 2022.

[109] H. Ahrens. “Design und Implementierung eines integrierten Transceivers für piezoelektrische Kommunikation mittels Ultraschall”. Bachelor Thesis, TU Darmstadt. 2021.

[110] H. Ahrens. “Quarzoszillatoren – der Pierce-Gate Oszillator”. Proseminar, TU Darmstadt. 2021.

[111] W. Lo. “Development of a Test Platform for High Resolution DC Current Transformer”. Master Seminar, TU Darmstadt. 2021.

[112] P. R. Valipe. “Low Power Oscillator Design in UMC 180nm”. Master Seminar, TU Darmstadt. 2021.

[113] T. Fuhrmann. “Implementation of an Active Rectifier in 180nm Technology”. Bachelor Thesis, TU Darmstadt. 2020.

[114] K. Münch. “Non Volatile Memory Cell Simulation in Synopsys Sentaurus TCAD”. Projektseminar, TU Darmstadt. 2020.

[115] J. Strobl. “Entwicklung eines diskreten Klasse-D-Verstärkers”. Master Seminar, TU Darmstadt. 2020.

[116] P. R. Valipe and S. Nagaraj. “Bandgap Reference Design Using UMC-180nm Technology”. Master Seminar, TU Darmstadt. 2020.

[117] V. Weinelt. “Aufbau und Evaluation einer Schaltung zur optischen Datenübertragung mittels LEDs”. Projektseminar, TU Darmstadt. 2019.

[118] V. Weinelt. “Design and Implementation of a Low Power Oscillator and Bandgap Voltage Reference in a 600 Nm SOI Technology”. Bachelor Thesis, TU Darmstadt. 2019.

[119] V. Weinelt. “Schaltung zur Datenübertragung mittels einer blauen high power LED”. Proseminar, TU Darmstadt. 2019.

Verilog-A Solar Cell Model

```
'include "constants.vams"
'include "disciplines.vams"

module Photodiode_Fwd_Temp(a,c);

  inout a,c;
  electrical a,c;

  parameter IL = 132.7265e-6;
  parameter I0 = 9.6e-11;
  parameter Rs = 0.01;
  parameter Rsh = 500000000;
  parameter N = 1.78;
  parameter Parallel = 1; // Solar cells in parallel
  parameter Series = 1; // Solar cells in series

  integer x = 0;
  real kq = 0.00008617342301;
  real Is, EG;

  analog begin
    // Bandgap
    EG = 1.17-0.000473*(pow($temperature,2)/($temperature+636));

    // reverse current
    Is = I0*exp(($temperature/300-1)*EG/(N*kq*$temperature))*
      ↪ pow($temperature/300,3);


    if(x == 1) I(c,a) <+ Parallel*(IL-Is*(exp((V(a,c)/
      ↪ Series+I(c,a)*Parallel*Rs)/(N*kq*$temperature))-1)-
      ↪ (V(a,c)/Series+I(c,a)*Parallel*Rs)/Rsh);
    else I(c,a) <+ ($abstime/0.0001)*Parallel*
      ↪ (IL-Is*(exp((V(a,c)/Series+I(c,a)* Parallel*Rs)/
      ↪ (N*kq*$temperature))-1)-(V(a,c)/Series+I(c,a)*Parallel*Rs)/Rsh);
        //ramp up current of solar cell
  end
```

```
  // Start current at zero, ramp it up at 100us
  analog begin
    @(timer(0.0001))
    x = 1;
  end
endmodule
```