

Automated Design of Robust Genetic Circuits: Structural Variants and Parameter Uncertainty

Supporting Information

Tobias Schladt,^{†,¶} Nicolai Engelmann,^{†,¶} Erik Kubaczka,^{†,¶} Christian
Hochberger,[†] and Heinz Koepl^{*,†,‡}

*†Department of Electrical Engineering and Information Technology, TU Darmstadt,
Darmstadt, 64283, Germany*

‡Centre for Synthetic Biology, TU Darmstadt, Darmstadt, 64283, Germany

¶The authors contributed equally to this research.

E-mail: heinz.koepl@bcs.tu-darmstadt.de

A Algorithms

A.1 Enumeration of Structural Circuit Variants

The following pseudo codes depict the enumeration and pruning procedure for synthesizing structural circuit variants and its recursive enumeration kernel.

```

input : A gate library  $\mathcal{L}$  containing gate types  $\mathcal{S}$ , a Boolean function specification
          $\phi$ , maximum circuit weight  $\omega$  and depth  $\delta$ 
output: A set  $C_\phi$  of circuits implementing  $\phi$  covered by  $\mathcal{L}$ 

                                                                 Initialization
1 new  $C \leftarrow \emptyset$ ;  $C_\phi \leftarrow \emptyset$ ;
2 new  $\gamma \leftarrow \emptyset$ ;  $\gamma_m \leftarrow \emptyset$ ;      Circuits are arrays of rows of gates and terminal
   elements
3 new  $b \in \mathbb{B}$ ;

                                                                 Enumerate with online pruning
4 enumerate( $\gamma, \mathcal{S}, \omega, \delta, n(\phi), C$ );       $n()$  returns the support size of a Boolean
   function

   Wire combinations of primary inputs  $\mathcal{P}$  and circuit inputs  $I$ 
5 foreach  $\gamma \in C, m \in \mathcal{M} \subset \mathcal{P} \times I$  do
6    $\gamma_m \leftarrow \text{wire\_inputs}(\gamma, m)$ ;
   Match circuit and target function
7   if  $\neg(\gamma_m \equiv \phi)$  then
8     continue;
9   end if

   Remove redundancies
10  foreach  $v \in V(\gamma_m)$  do
11    foreach  $u \in V(\gamma_m)$  do
    $f()$  returns the function of a gate with respect to  $\mathcal{P}$ 
12      if  $v \neq u \wedge f(v) = f(u)$  then
13        substitute\_gate( $v, u$ );      Replaces  $u$  by a fan out of  $v$ 
14      end if
15    end foreach
16  end foreach

   Final check of library constraints
17   $b \leftarrow \text{true}$ ;
18  foreach  $s \in \mathcal{S}$  do
19    if  $|v \in V(\gamma_m) : s_v = s| > |g \in \mathcal{L} : s_g = s|$  then
20       $b \leftarrow \text{false}$ ;
21      break;
22    end if
23  end foreach

   If circuit is implementable with  $\mathcal{L}$ , add to output set
24  if  $b$  then
25     $C_\phi \leftarrow C_\phi \cup \gamma_m$ ;
26  end if
27 end foreach
28 return  $C_\phi$ ;

```

```

input: A circuit  $\gamma$ , gate types  $\mathcal{S}$ , maximum circuit weight  $\omega$  and depth  $\delta$ , the
         minimum number of inputs  $n$ 
inout: A a set of fan-out free circuits  $C$ 
1 Function enumerate( $\gamma, \mathcal{S}, \omega, \delta, n, C$ )
2   new  $l \leftarrow \text{length}(\gamma)$ ;            $l$ : depth of the circuit  $\gamma$ 
3   new  $I_\gamma \leftarrow \text{get\_unconnected\_inputs}(\gamma)$ ;    $I_\gamma$ : set of unconnected gate
         inputs of  $\gamma$ 
                                     Abort criterion
4   if  $l \geq \delta$  then
5     | return;
6   end if
       Iterate permutations of gates that match the number of unconnected
       inputs
7   foreach  $r \in R \subset \{\mathcal{S}, \emptyset\}! : |R| = \max(|I_\gamma|, 1)$  do
8     new  $\gamma' \leftarrow \gamma$ ;           Copy  $\gamma$  and add new row of gates
9     new  $I_{\gamma'} \leftarrow \text{get\_unconnected\_inputs}(\gamma')$ ;
10     $\gamma'[l] \leftarrow r$ ;
                                     Prune circuits that are too big
11    if  $\omega_{\gamma'} > \omega$  then
12      | return;
13    end if
                                     Check, if  $\gamma'$  supports  $\phi$  and prune isomorph circuits
14    if  $|I_{\gamma'}| \geq n \wedge \neg \exists \gamma \in C : \gamma' \simeq \gamma$  then
15      |  $C \leftarrow C \cup \gamma'$ ;
16    end if
17    enumerate( $\gamma', \mathcal{S}, \omega, \delta, n, C$ );           Recurse
18 end foreach

```

A.2 Generation of an Equivalent Envelope-Free Circuit

The equivalent envelope-free circuit is just a 'common' circuit C^* , which is capable of carrying out the propagation of intervals through an original circuit C . Exploiting the monotonicity of all gate transfer functions in an extended gate library \mathcal{L}_e , which contains tuples $(g, \bar{g}, \underline{g}) \in \mathcal{L}_e$ for each $g \in \mathcal{L}$, the circuit C^* contains twice as many gates, only twice as many edges and its result is valid on the whole input domain.

For details on envelopes and the interval-based scoring, please refer to the Methods section from the original manuscript.

input : A circuit $C \equiv (\gamma, a)$, a gate library \mathcal{L}_e with additional envelope specifications

output: A circuit $C^* \equiv (\gamma^*, a^*)$ propagating the intervals of C

Initialization

1 new $V^* \leftarrow \emptyset$; $E^* \leftarrow \emptyset$; $a^* \leftarrow \emptyset$;

Build new circuit

2 new $D \leftarrow \emptyset$;

Helper D associates $v^* \in V^*$ with $v \in V$

$\gamma \equiv (V, E)$ consists of vertices V and edges $E \subset V \times V$

3 **foreach** $v \in V$ **do**

4 new v_h^*, v_l^* ;

5 $V^* \leftarrow V^* \cup \{v_h^*, v_l^*\}$;

Associate new nodes with old ones to connect correctly later

6 $D \leftarrow D \cup \{v, \{v_h^*, v_l^*\}\}$;

Elements $(v, g) \in a$ consist of a $v \in V$ and a $g \in \{g, g_h, g_l\} \in \mathcal{L}_e$

7 $a^* \leftarrow a^* \cup (v_h^*, g_h)$;

8 $a^* \leftarrow a^* \cup (v_l^*, g_l)$;

9 **end foreach**

10 **foreach** $v \in V$ **do**

Add crossed incoming edges between corresponding node pairs in V^*

11 **foreach** $e \in E$ **where** $e = (w, v)$, $w \in V$ **do**

12 $\{v_h^*, v_l^*\} \leftarrow \text{get_associated}(v, D)$;

13 $\{w_h^*, w_l^*\} \leftarrow \text{get_associated}(w, D)$;

14 $E^* \leftarrow E^* \cup (w_h^*, v_l^*)$;

15 $E^* \leftarrow E^* \cup (w_l^*, v_h^*)$;

16 **end foreach**

17 **end foreach**

Done. Return new circuit

18 new $\gamma^* \leftarrow (V^*, E^*)$;

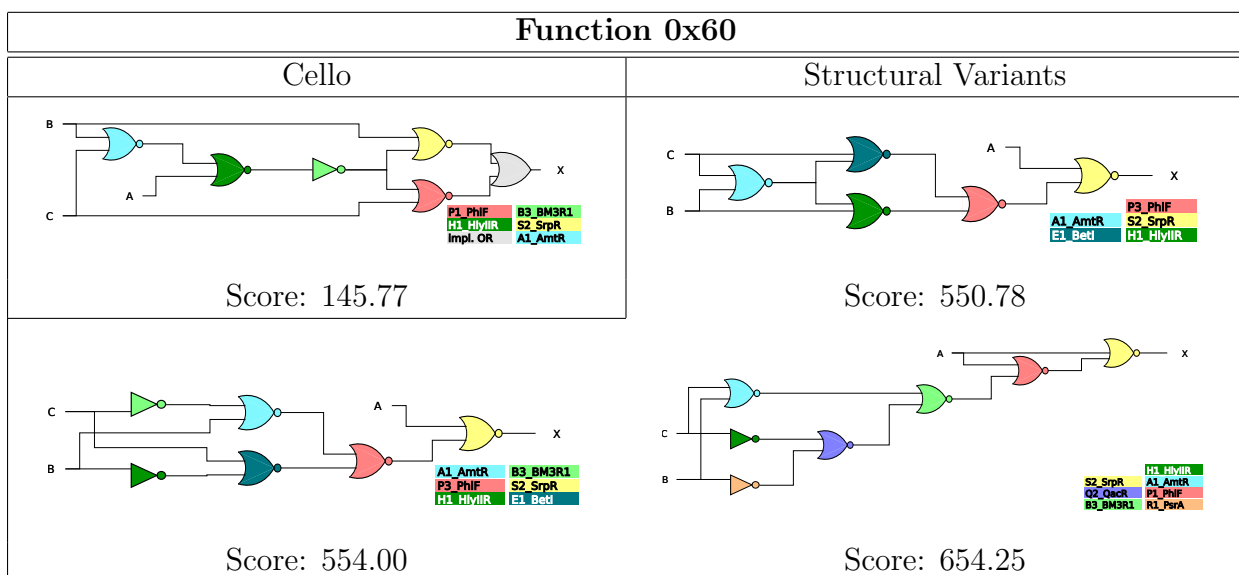
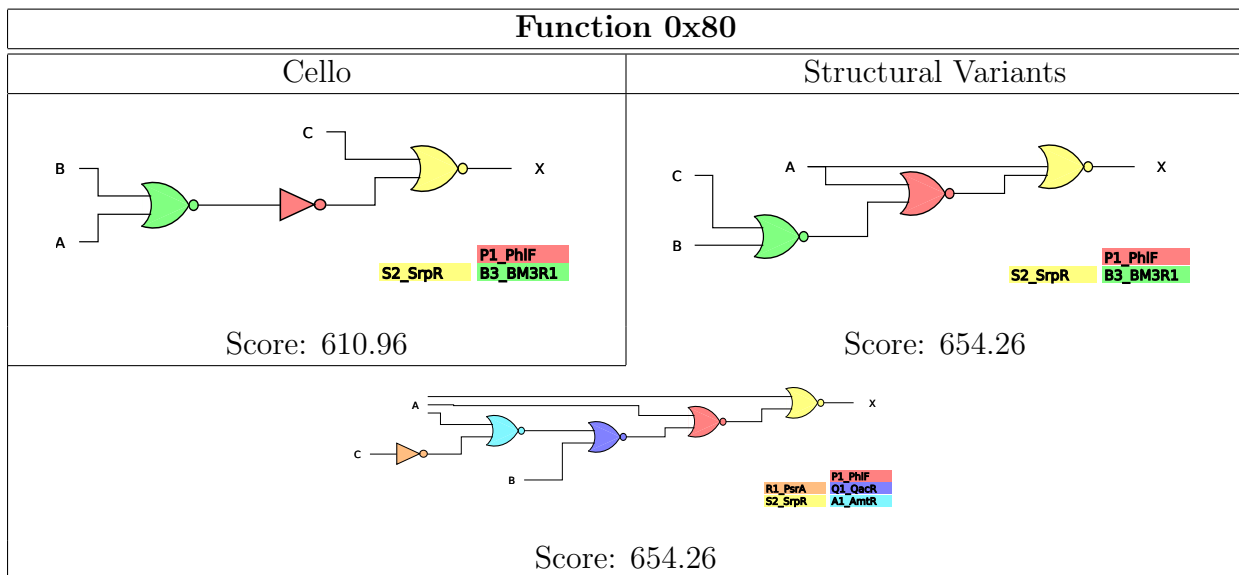
19 new $C^* \leftarrow (\gamma^*, a^*)$;

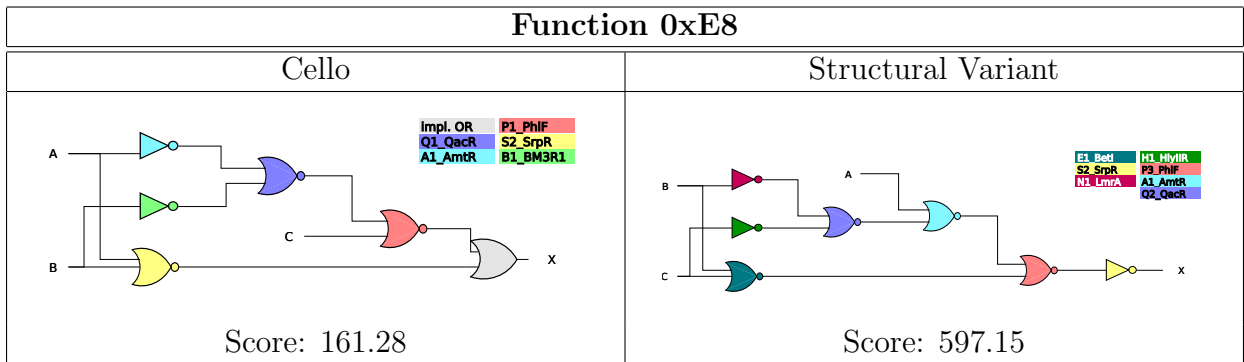
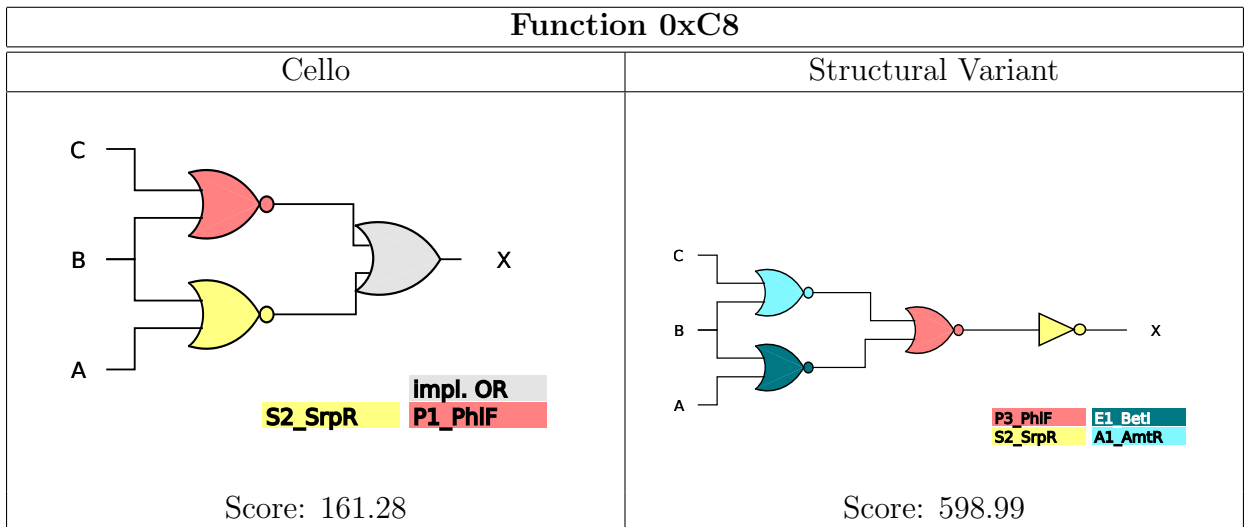
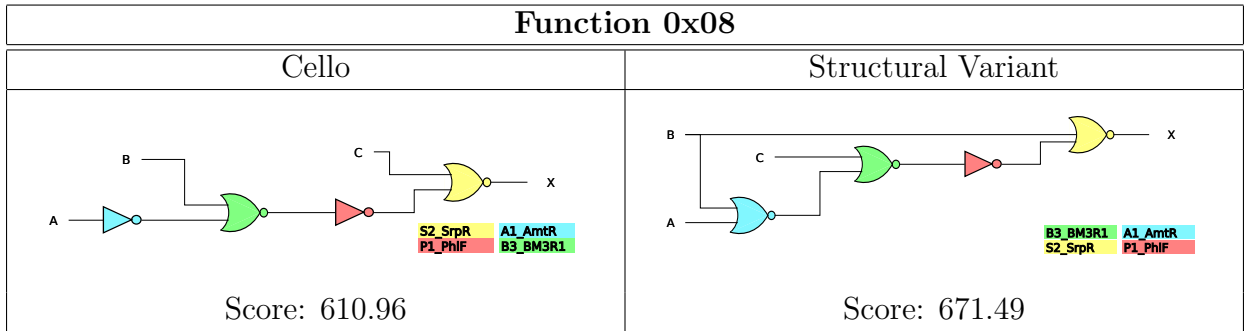
20 **return** C^*

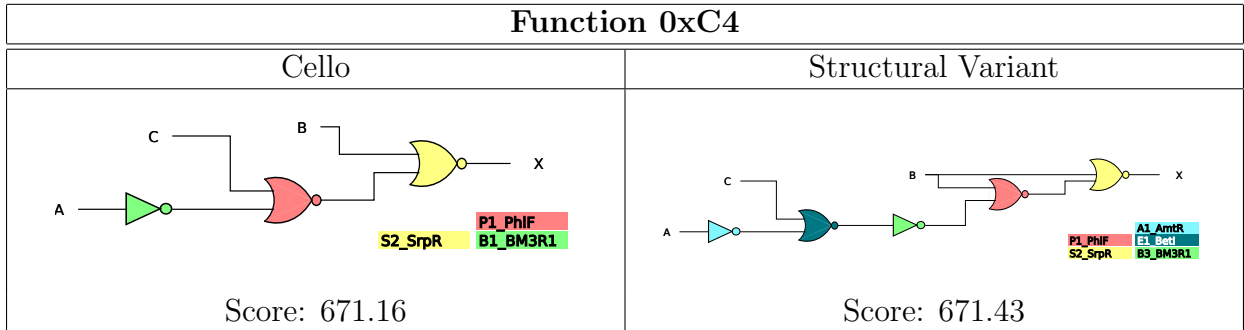
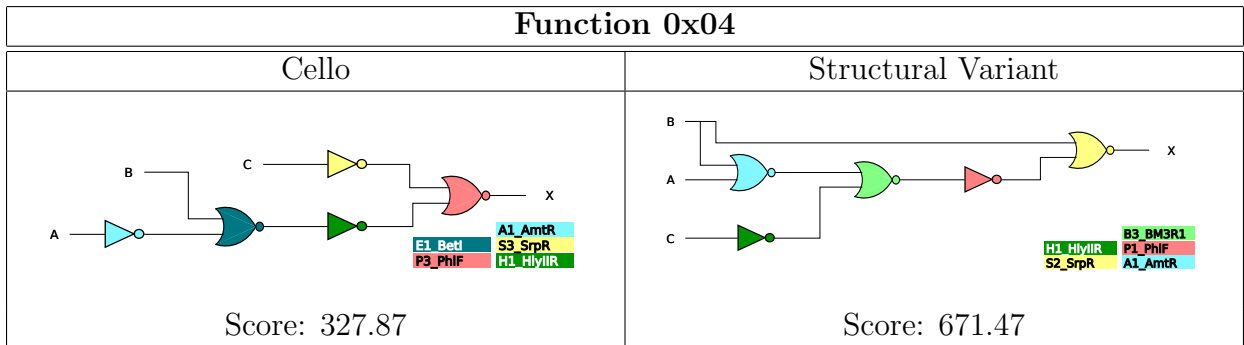
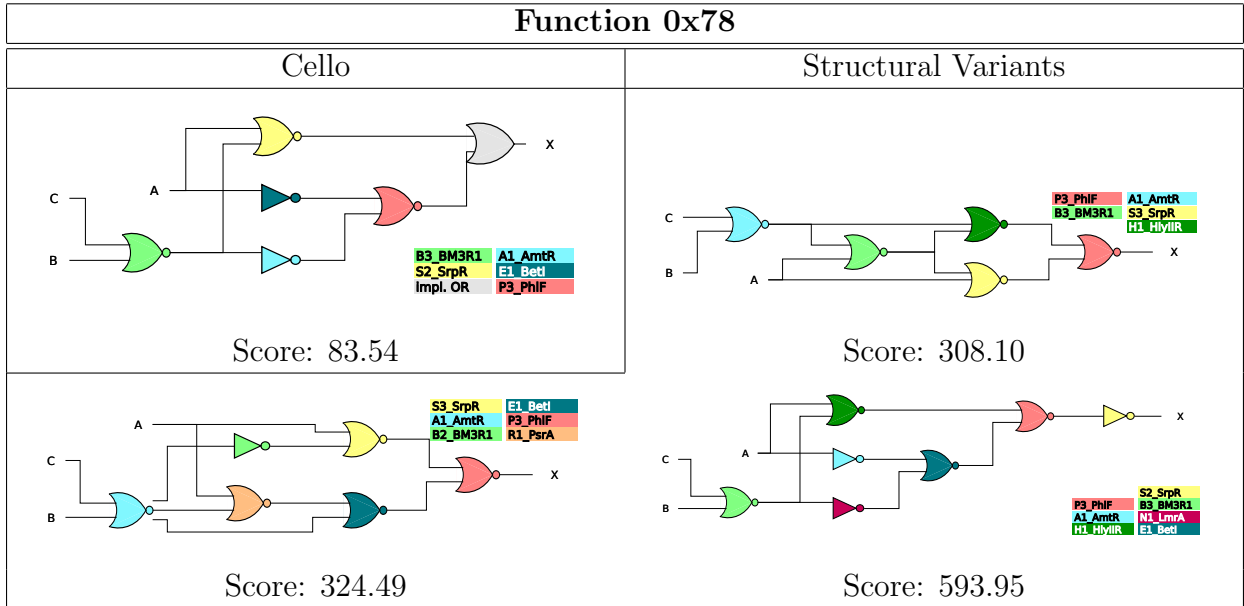
B Synthesized Circuit Designs

B.1 Structural Variants, Classical Assignment Optimization

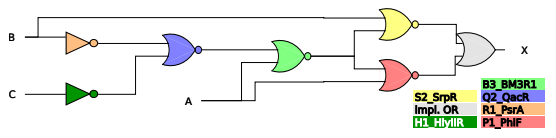
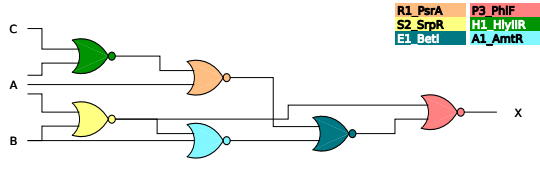
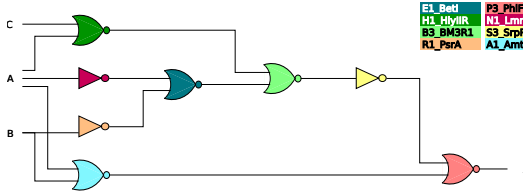
In the following, circuits synthesized by Cello and their structural variants synthesized by the proposed method are depicted, together with the optimal gate assignment found using the Cello score. Their corresponding final Cello scores are written below each. The diagrams have been automatically generated from the synthesis results.



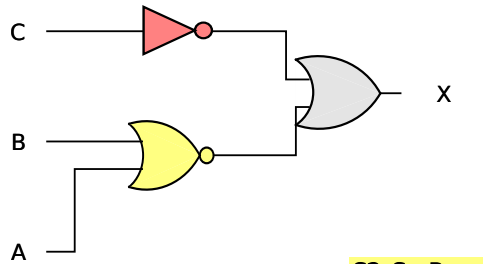
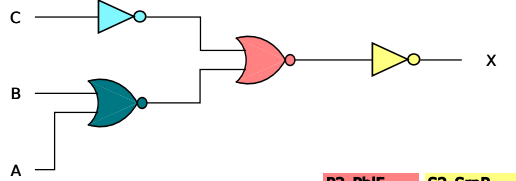


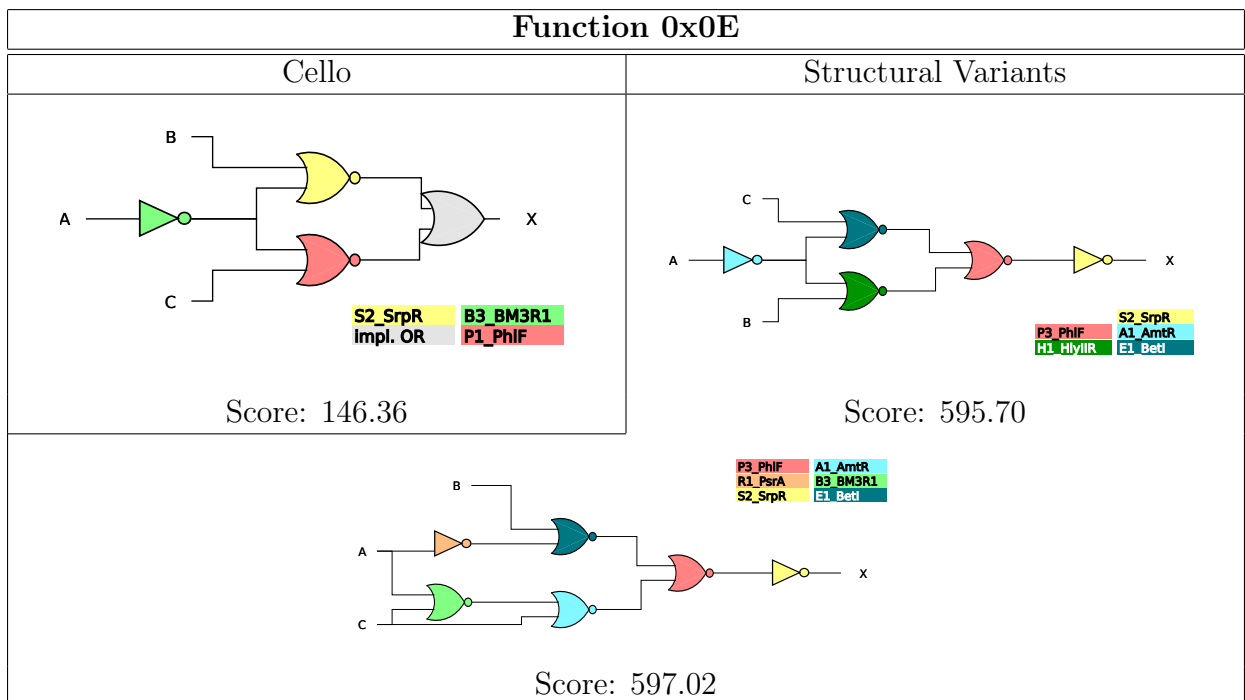
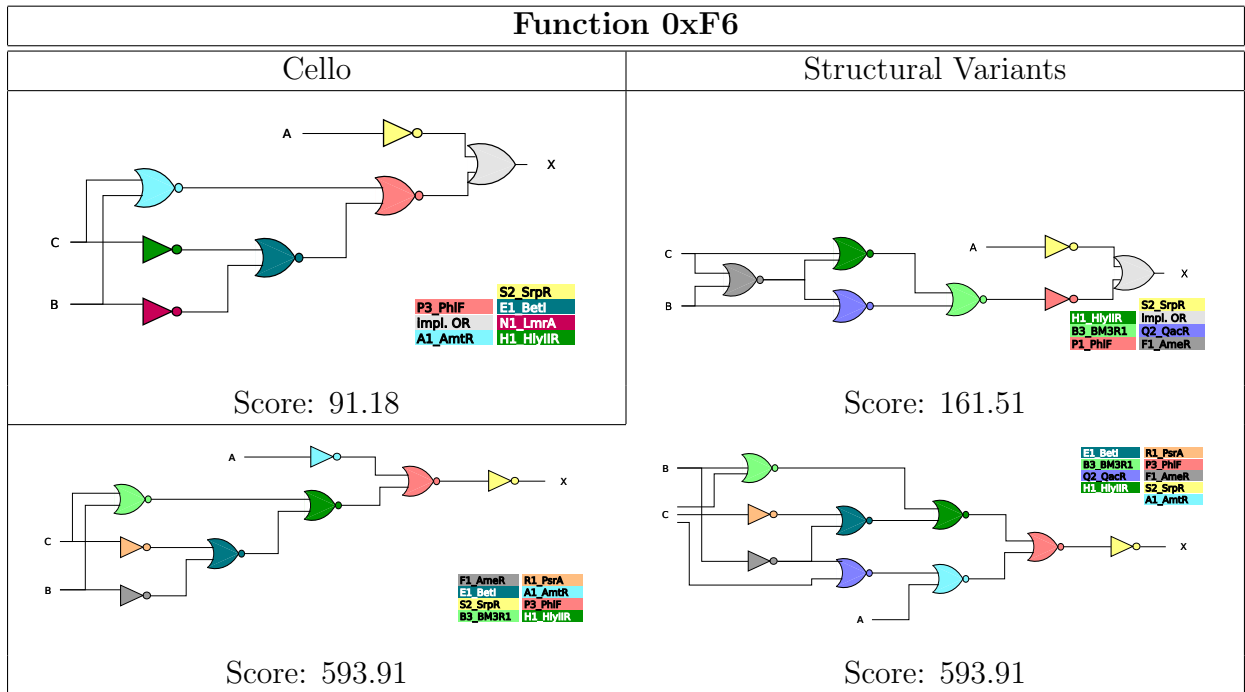


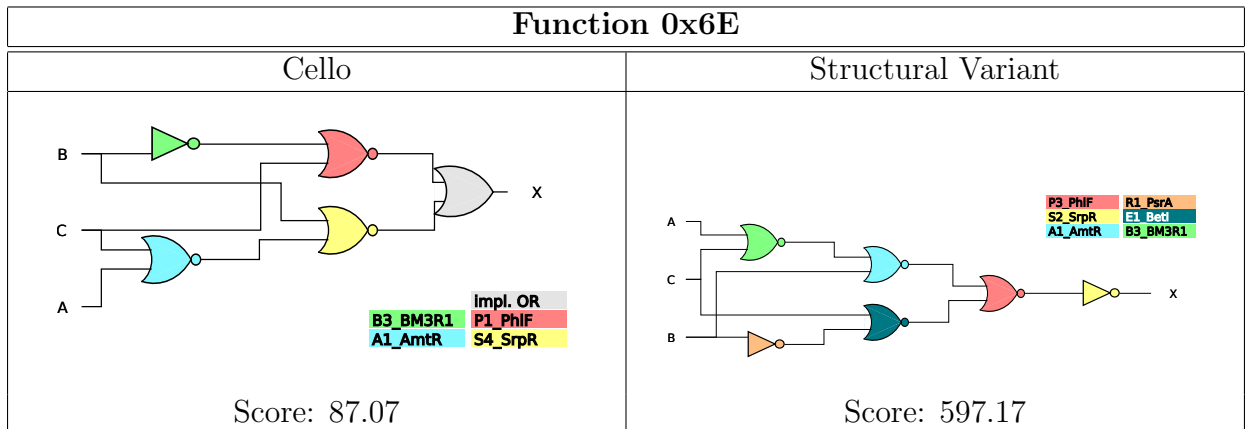
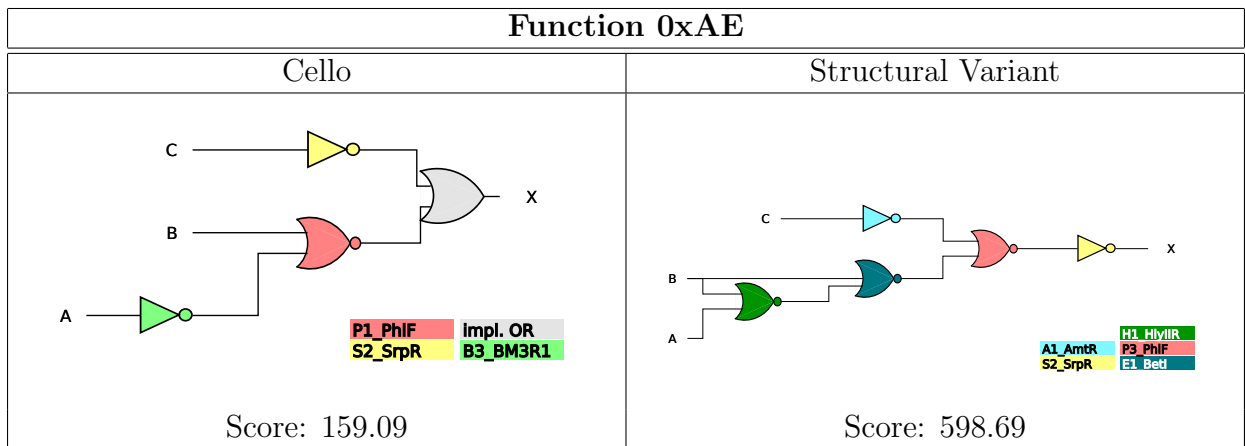
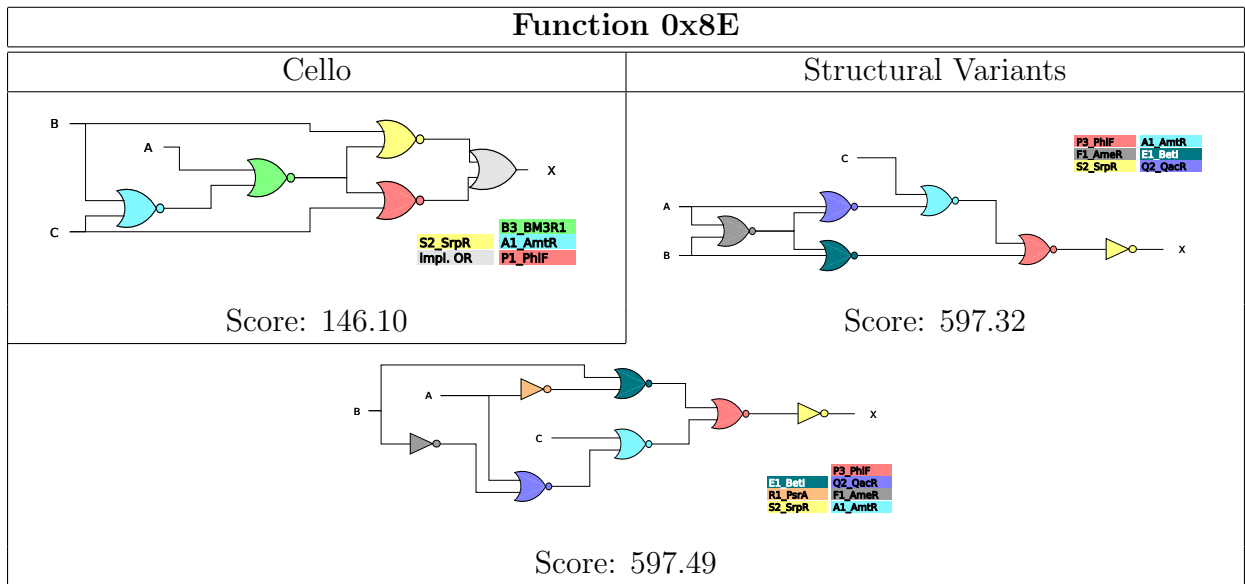
Function 0x1C

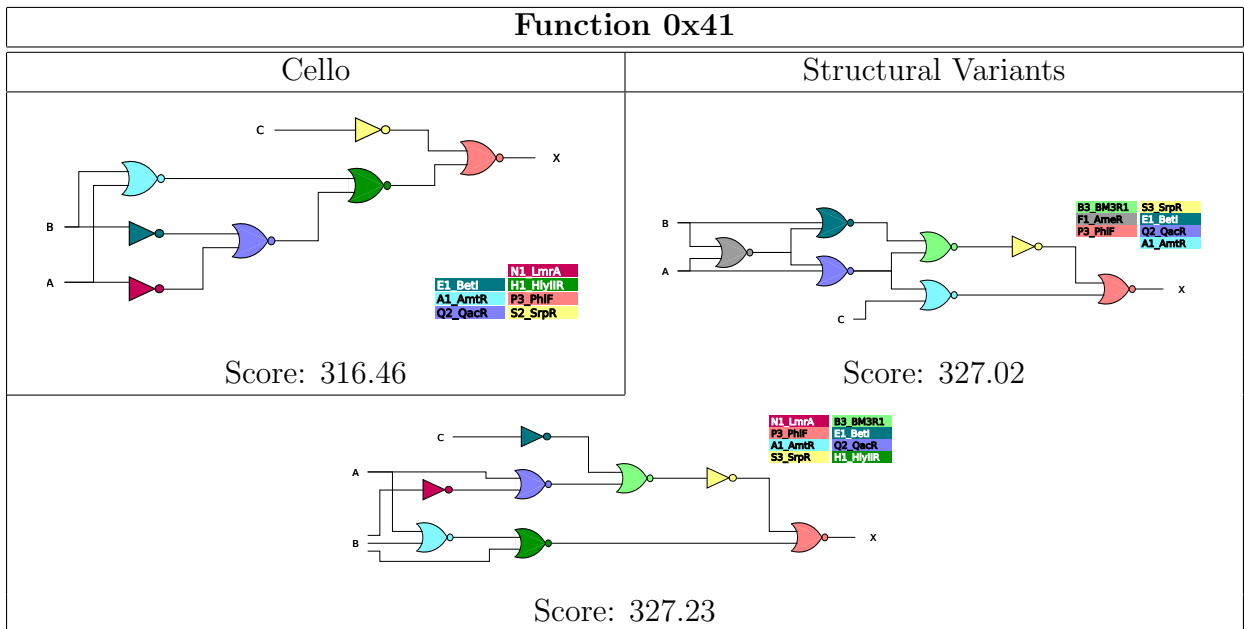
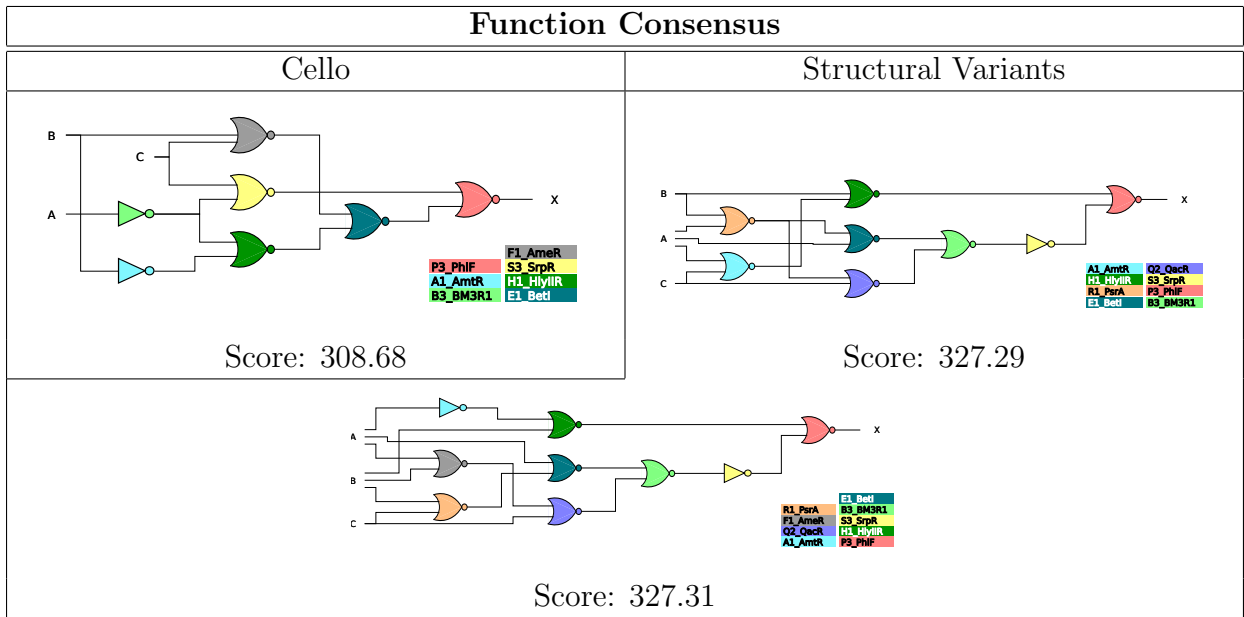
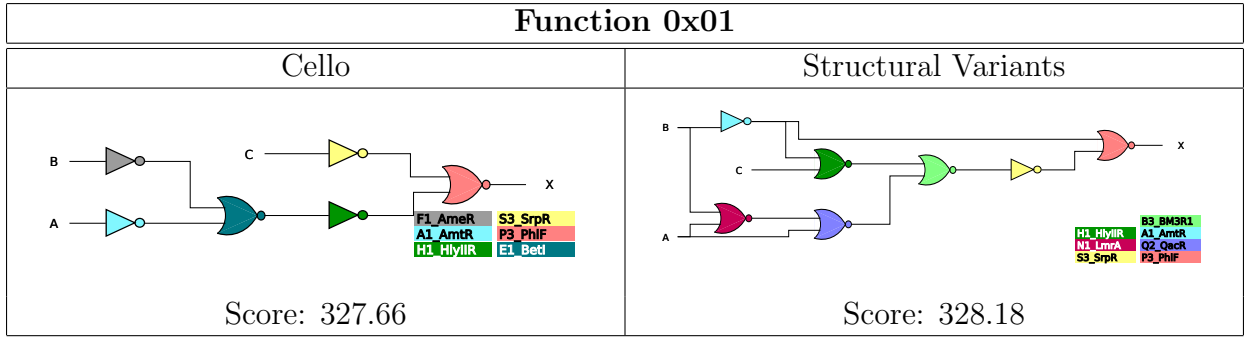
Cello	Structural Variants
 <p>Score: 146.34</p>	 <p>Score: 325.05</p>
 <p>Score: 327.34</p>	

Function 0xEA

Cello	Structural Variant
 <p>Score: 161.28</p>	 <p>Score: 598.99</p>





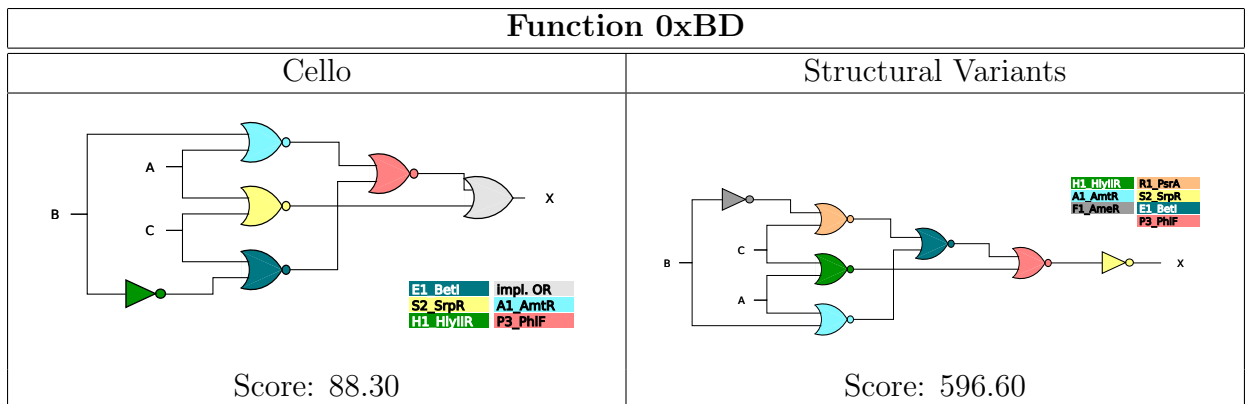
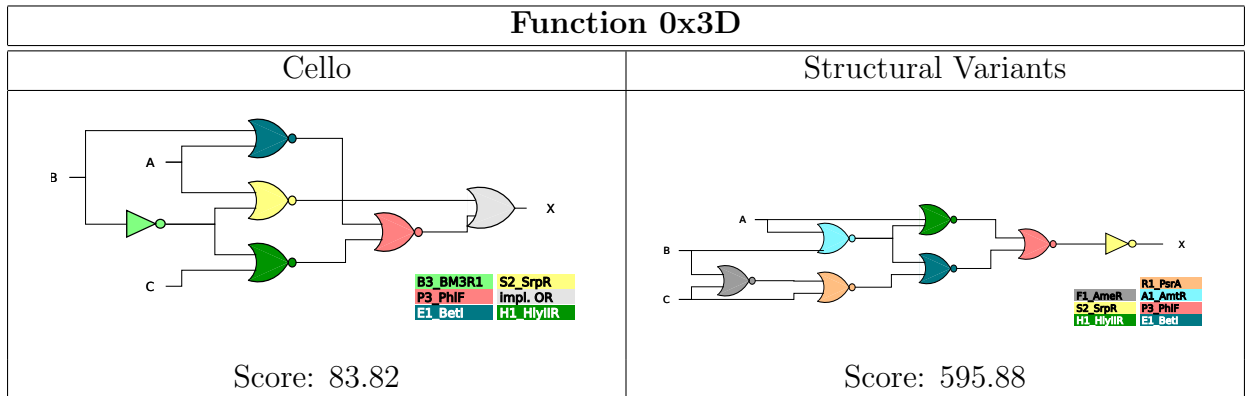
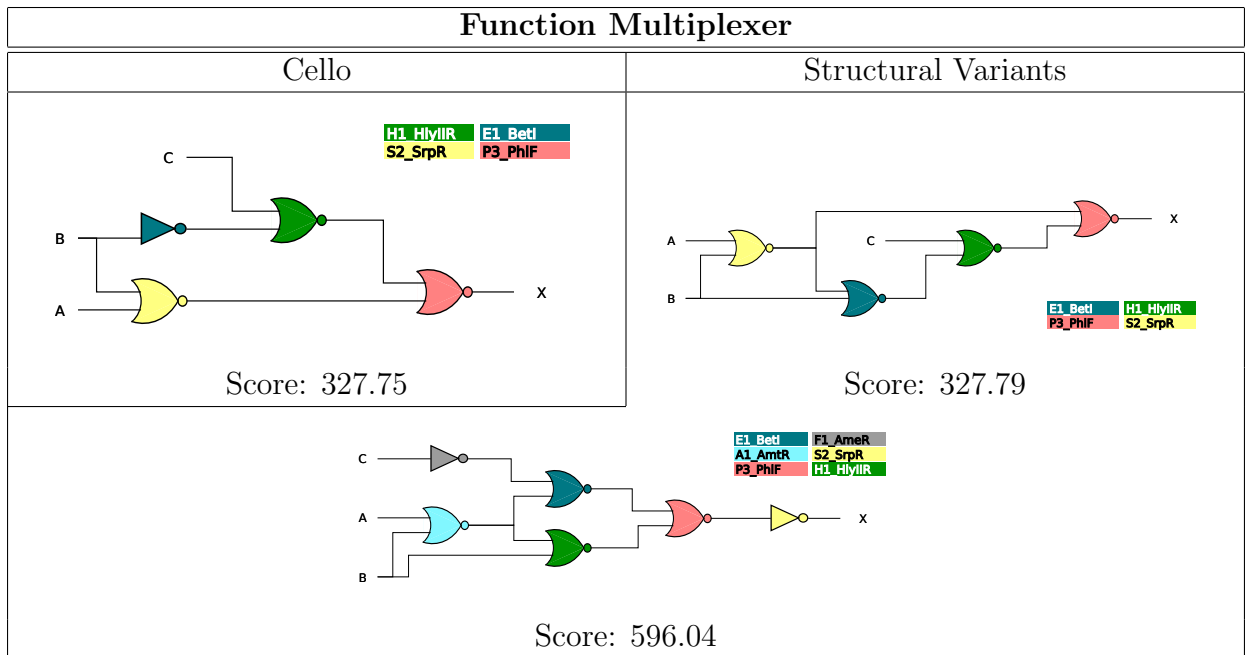


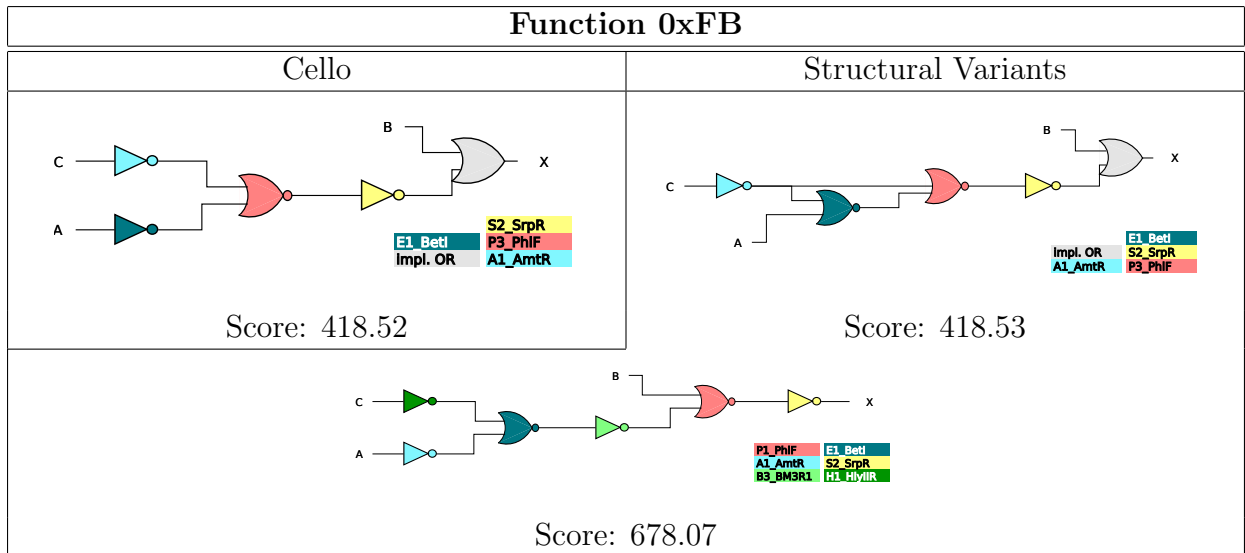
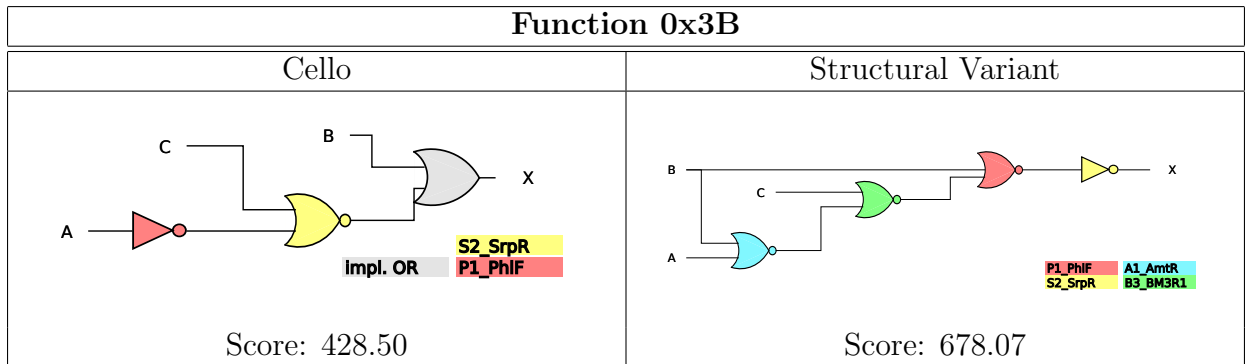
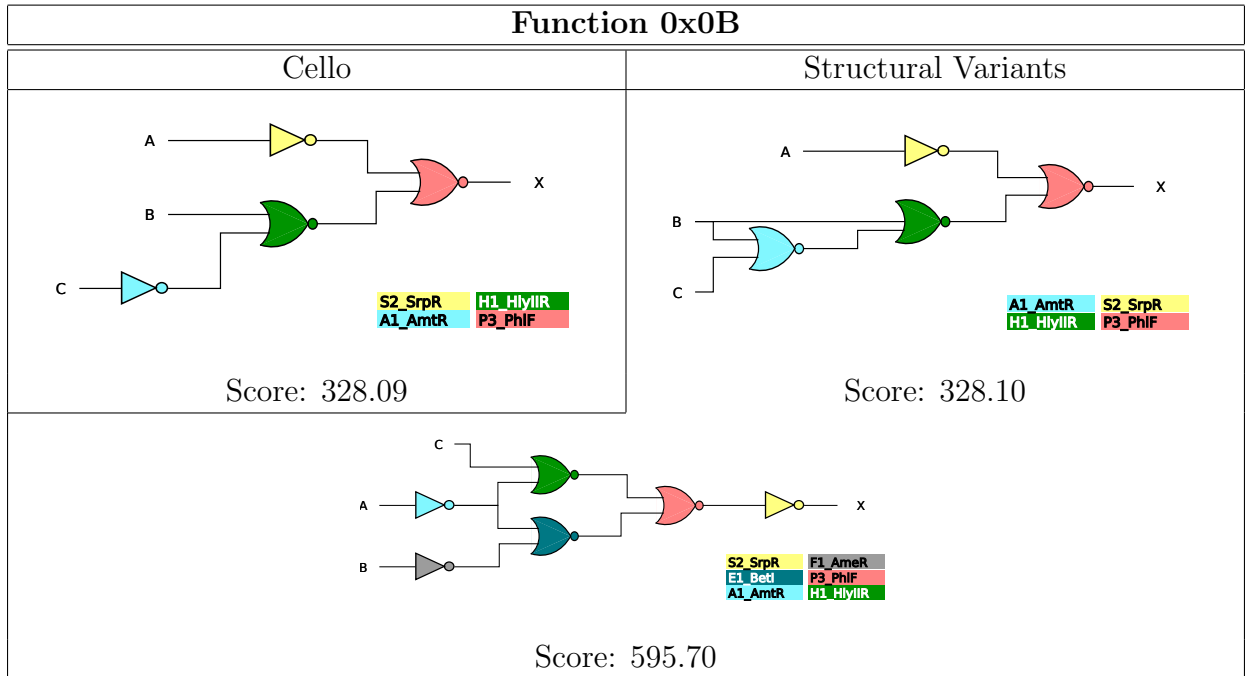
Function 0x4D

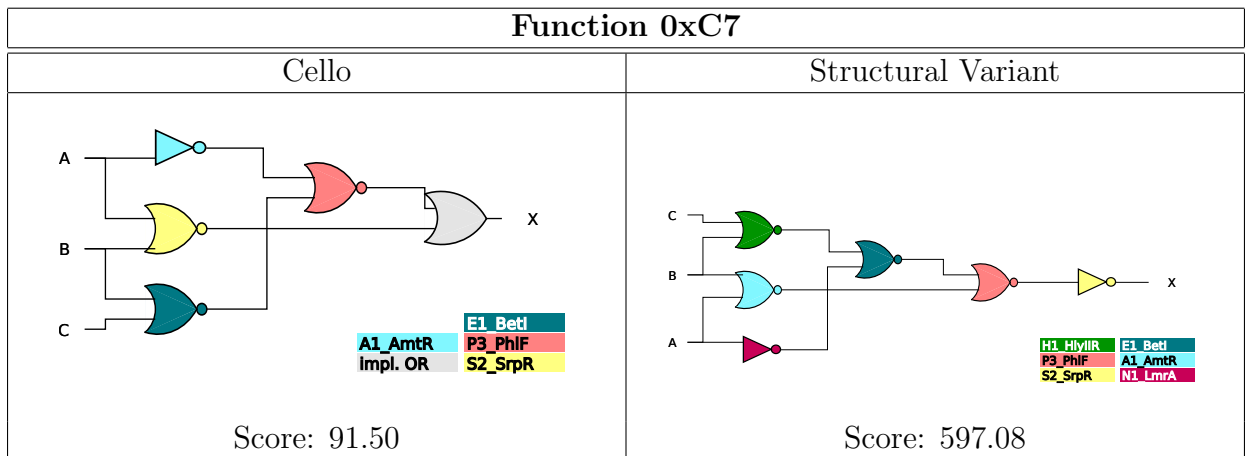
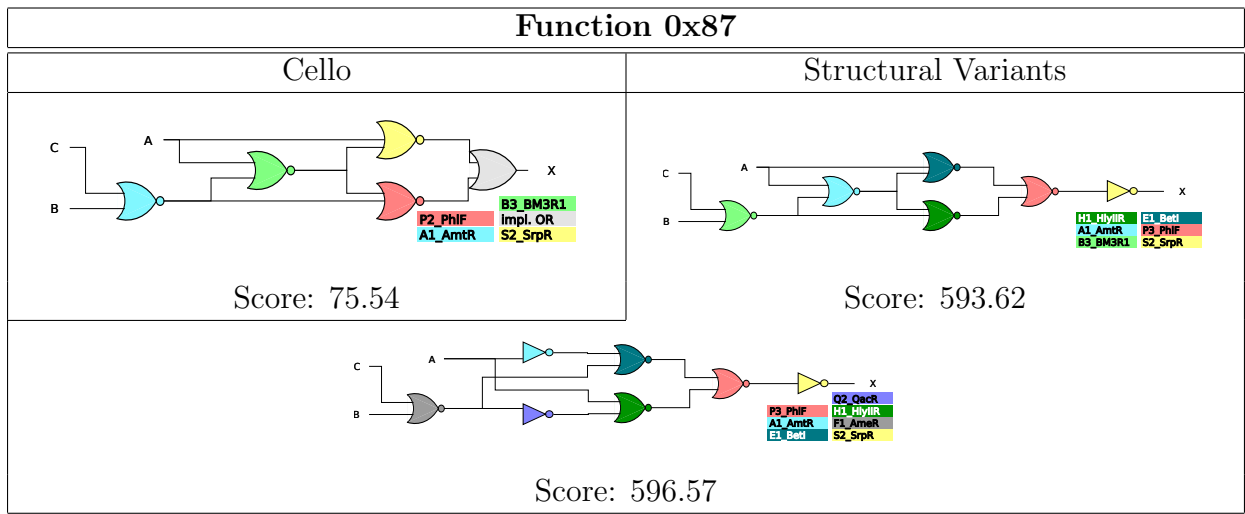
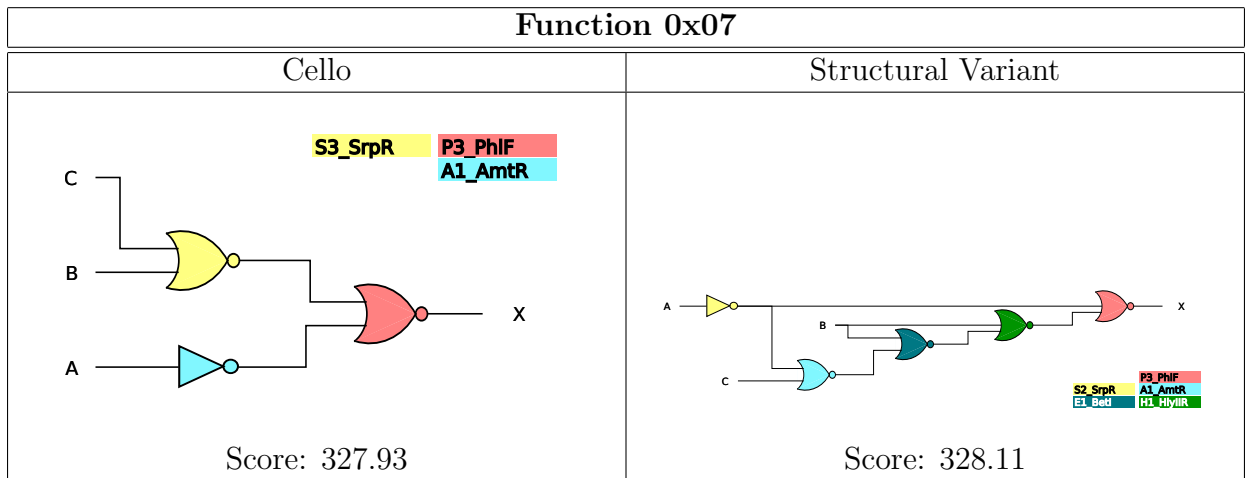
Cello	Structural Variants
<p>Score: 85.40</p>	<p>Score: 326.25</p>
<p>Score: 327.39</p>	<p>Score: 595.79</p>

Function 0xCD

Cello	Structural Variants
<p>Score: 91.93</p>	<p>Score: 308.48</p>
<p>Score: 327.29</p>	<p>Score: 597.10</p>







Function 0x37	
Cello	Structural Variants
<p>Score: 207.04</p>	<p>Score: 327.93</p>
<p>Score: 678.05</p>	

Function 0xF7	
Cello	Structural Variants
<p>Score: 161.53</p>	<p>Score: 473.93</p>
<p>Score: 678.07</p>	

Function 0x7F	
Cello	Structural Variant
<p>Score: 183.04</p> <p>Impl. OR P1_PhIF S2_SrpR</p>	<p>Score: 677.91</p> <p>B3_BM3R1 S2_SrpR A1_AmTR P1_PhIF</p>

B.2 Classical Structure, Uncertainty-Aware Assignment Optimization

In the following, the three circuits mentioned in the main text 0x1c, 0x81 and 0x41 synthesized by Cello (so the non-modified original circuit structure) are depicted together with the optimal gate assignment found using the Cello score and the expectation-based score. The least separated on and off output histograms and their resulting final Cello and expectation-based scores are written below each.

Like explained in the main text, since the median gate outputs obtained via sampling are of improved accuracy with respect to the true medians compared to those calculated by Cello in the context of a circuit, the toxicity constraints for our assignment for function 0x41 are met using the E-score but not when using Cello's score. Thus, we obtain an assignment with high E-score, which would also exhibit a higher Cello score when calculating the toxicity constraints using the improved accuracy from sampling.

Function 0x1C

Assignment by Cello score	Assignment by expectation-based score
<p>Cello-score: 146.34 E-score: 2.95</p>	<p>Cello-score: 129.98 E-score: 77.15</p>

Function 0x81

Assignment by Cello score	Assignment by expectation-based score
<p>Cello-score: 308.68 E-score: 52.48</p>	<p>Cello-score: 143.68 E-score: 57.8</p>

Function 0x41

Assignment by Cello score	Assignment by expectation-based score
<p>Cello-score: 316.46 E-score: 35.96</p>	<p>Cello-score: 317.65 (see above) E-score: 81.10</p>