Supercapacitors-based Pulsed Power Supply for the ASDEX Upgrade Toroidal Field Coil

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A. Magnanimo

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Kurzfassung

ASDEX Upgrade ist ein experimenteller Tokamak, in dem die Physik kernfusionsrelevanter Plasmen untersucht wird. Seine elektrische Energie liefern drei Schwungradgeneratoren, die vor Beginn jedes Experiments für einige Minuten mit bis zu 15 MW aufgeladen werden. Die gespeicherte Energie wird dann verwendet, um den hohen Leistungsbedarf während eines Experiments – Plasmapuls genannt – von bis zu 450 MVA zu decken. Der größte der drei Schwungradgeneratoren könnte im Falle eines größeren Schadens nicht ersetzt werden, da derzeit keine vergleichbaren Geräte auf dem freien Markt erhältlich sind. Daher ist die Entwicklung eines alternativen Stromversorgungssystems mit hoher Leistung und Energie und voll regelbarer Leistung geplant. Superkondensatoren sind bekannt für ihre sehr hohe spezifische Leistung. Durch die Kombination dieser Technologie mit einer geeigneten Stromrichtertopologie wie dem modularen Multilevel-Umrichter wäre es möglich, die Spulen zukünftiger Tokamaks mit höherer Leistung und Zuverlässigkeit zu speisen. Diese Topologie ermöglicht in der Tat eine diskret geregelte Ausgangsspannung und kann dank ihrer hohen Modulanzahl auch im Fehlerfall einiger von ihnen kontinuierlich weiter arbeiten, während ein Schwungrad-generator dies nicht kann. Diese Dissertation zeigt das Konzept der genannten Stromversorgung, zeigt Vorteile und Herausforderungen gegenüber bestehenden Technologien auf, konzentriert sich auf Zuverlässigkeit, Skalierbarkeit und Flexibilität mit der Idee, diese Lösung auch für andere Anwendungen in der Zukunft anzupassen. Darüber hinaus wurde ein kleiner Demonstrator aus vier identischen Modulen gebaut und in drei verschiedenen Konfigurationen getestet: seriell, parallel und kombiniert seriell/parallel. Die serielle Konfiguration wurde getestet, um die entwickelte Strategie zur Ansteuerung zu validieren, die parallele ist grundlegend für die Skalierbarkeit des Systems und die letzte Konfiguration validiert ihre Kombination. Die experimentellen Ergebnisse werden gezeigt und mit Simulationen verglichen, um abschließend ein klareres Bild über die Skalierbarkeit des Systems zu entwickeln.

Abstract

ASDEX Upgrade is an experimental tokamak where the physics of nuclear fusion relevant plasmas is studied. Its electrical power is provided by three flywheel generators that are charged up before the start of each experiment with up to 15 MW for several minutes. The stored energy is then used to satisfy the high power needs during an experiment - called plasma pulse - of up to 450 MVA. The largest one of the three flywheel generators could not be replaced in case of a major fault because currently there are no comparable devices available on the free market. Therefore, the development of an alternative power supply system with high power and energy and fully controllable output is planned. Supercapacitors are well known for their very high specific power. Combining this technology with a proper power converter topology such as the modular multilevel converter, it would be possible to feed the coils of future tokamaks with higher performance and reliability. This topology, indeed, allows a discrete-leveled output voltage and, thanks to its high modules number, it can operate continuously even in case of fault of some of them, while a flywheel generator could not. This dissertation shows the concept of the mentioned power supply, highlighting advantages and challenges compared to existing technologies, focusing on reliability, scalability and flexibility with the idea of adapting this solution even for different applications in the future. Furthermore, a small-scale demonstrator composed by four identical modules has been built, and it has been tested in three different configurations: serial, parallel and combined serial/parallel. The serial configuration has been tested to validate the developed control strategy, the parallel one is fundamental for the scalability of the system and the last configuration validated their combination. The experimental results are shown and compared with simulations, and finally a clearer picture about the scalability of the system was developed.

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List of Symbols

Symbol	*Unit*	*Description*
A	m^2	Area
B	T	Magnetic field
B_{Tor}	T	Toroidal magnetic field
C	F	Capacitance
c	m/s	Speed of light
C_c	F	Submodule's capacitor capacitance
C_{Filter}	F	Filter capacitance
C_{SC}	F	Supercapacitor capacitance
D		Duty cycle
d	m	Electrodes distance
E	J	Energy
e		Error
E_S	J	Stored energy
E_{SC}	J	Supercapacitor energy
ESL	H	Equivalent series inductance
ESR	Ω	Equivalent series resistance
E_{ss}	J	Short circuit energy
E_{TF}	J	TF coil's stored energy
E_u	J	Unused energy
E_w	J	Dissipated energy
f	Hz	Frequency
f_c	Hz	Control frequency
f_{co}	Hz	Cut-off frequency
f_{cr}	Hz	Maximum operating frequency
f_N	Hz	Nominal frequency
f_{sw}	Hz	Switching frequency
G_0		Open-loop transfer function
G_c		Converter transfer function
G_{Load}		Load transfer function
G_{PI}		PI transfer function

Symbol	*Unit*	*Description*
G_{W}		Closed-loop transfer function
H_{s}		Current sensors transfer function
I_{ch}	A	Charger current (rms)
i_{epr}	A	Leakage current
I_{TF}	A	TF coil current (rms)
i_{Load}	A	Load current
i'_{Load}	A	Measured load current
I_{P}	A	Plasma current (rms)
i_{pc}	A	Pre-charging current
i_{ref}	A	Reference current
i_{rs}	A	Short circuit current
i_{SC}	A	Supercapacitor current
i_{SM}	A	Submodule current
i_{ss}	A	Submodule short circuit current
I_{ssth}	A	Thereshold short circuit current (rms)
J	$\mathrm{A/m^2}$	Current density
k_{p}, k_{ps}		PI proportional contants
k_{i}, k_{is}		PI integral contants
L	H	Inductance
l	m	Length
L_{arm}	H	Arm inductance
L_{c}	H	Busbars inductance
L_{ch}	H	Charger inductance
L_{Filter}	H	Filter inductance
L_{i}	H	Internal inductance
L_{s}	H	Stray inductance
M	kg	Mass
m		Number of parallel submodules
M_{SC}	kg	Supercapacitor mass
M_{SCtot}	kg	Total supercapacitor mass
M_{tot}	kg	Total mass
n		Number of submodules in series
n_{c}		Number of cells
N_{SM}		Number of submodules
p_{c}	W	Conduction losses
p_{filter}	W	Filter losses
P_{N}	W	Nominal power (rms)
p_{SC}	W	Supercapacitor losses

Symbol	*Unit*	*Description*
p_{SM}	W	Submodule losses
p_{sw}	W	Switching losses
p_{Ω}	W	Ohmic losses
q	C	Charge
r	m	Radius
R_{arm}	Ω	Arm resistance
R_{c}	Ω	Busbars resistance
R_{CE}	Ω	Collector-emitter resistance
R_{Chopper}	Ω	Chopper resistance
R_{eq}	Ω	Equivalent resistance
R_{Load}	Ω	Load resistance
R_{thCH}	Ω	Case to heat sink resistance
R_{thJC}	Ω	Junction to case resistance
S		Switch
S_{N}	W	Nominal complex power
s_{n}		Switching commands
T_{IGBT}	°C	IGBT temperature
T_{FT}	s	Flat-top time
T_{op}	°C	IGBT operating temperature
t_{pulse}	s	Pulse time
T_{p}	°C	Plasma temperature
T_{s}	s	Sampling period
T_{sw}	s	Switching period
T_{thr}, T_{thr}	s	Short circuit detection time via gate drivers
T_{thSM}	s	Short circuit detection time via current sensors
U_{N}	V	Nominal voltage
v_{c}	V	Capacitor voltage
$v_{\mathrm{CE,ON}}$	V	Collector-emitter ON voltage
v_{cf}	V	Filter capacitor voltage
v_{ESL}	V	ESL voltage
v_{ESR}	V	ESR voltage
v_{GES}	V	Gate voltage
v_{Lch}	V	Charger inductor voltage
v_{Lf}	V	Filter inductor voltage
v_{Load}	V	Load voltage
v_{out}	V	Output voltage
v_{r}	V	PI output signal
v_{rl}	V	Load resistive voltage

Symbol	*Unit*	*Description*
v_{rn}	V	Normalized PI output signal
v_{SC}	V	Superapacitor voltage
v_{SCeop}	V	Supercapacitor voltage at the end of a pulse
v_{SM}	V	Submodule voltage
v_{SCmin}	V	Minimum sapacitor voltage
v_{th}	V	Thereshold voltage
w_i, w_p		Integral and proportional contants
Z	Ω	Impedance
Z_c	Ω	Busbars impedance
α		Helium nucleus
ϵ	F/m	Permittivity
ϵ_o	F/m	Permittivity in the free space
ϵ_r	F/m	Relative permittivity
η		Particle density
η_c		Converter efficiency
Θ	kg·m^2	Moment of inertia
ν	m/s	Speed of a particle
π		Pi
ρ	Ω·m	Resistivity
τ_c	s	Busbars time constant
τ_m	s	Time constant of parallel submodules
τ_{Load}	s	Load time constant
τ_s	s	Busbars time constant
τ_{SM}	s	Sensors time constant
ϕ_m	Deg	Phase margin
ϕ_{SC}	Deg	Supercapacitor impedance phase angle
ω	rad/s	Angular speed
ω_c	rad/s	Control angular frequency

List of Abbreviations

AC	Alternating current
ASDEX	Axially symmetric divertor experiment
BCP	Boost-charging phase
BOL	Beginning of operational life
CAES	Compressed air energy storage
CS	Central solenoid
D	Deuterium
DC	Direct current
DEMO	Demonstration power plant
DTT	Divertor tokamak test
ECRH	Electron cyclotron resonance heating
EES	Energy storage system
EOL	End of operational life
EPR	Equivalent parallel resistance
ESC	EtherCAT slave controller
EtherCAT	Ethernet for control automation technology
EZ2	Energiezentrale 2
FDU	Fast discharge unit
FPGA	Field programmable gate array
HEV	Hybrid electric vehicles
HVDC	High-voltage direct current
ICRH	Ion cyclotron resonance heating
IGBT	Insulated-gate bipolar transistor
IPP	Max-Planck-Institute for Plasma Physics
ITER	International thermonuclear experimental reactor
MB	Modulation and balancing block
MMC	Modular multilevel converter
NBI	Neutral beam injector
NTC	Negative temperature coefficient
PCB	Printed circuit board

PCP	Pre-charging pahse
PF	Poloidal field
PI	Proportional-integral
PLC	Programmable logic controller
PPS	Pulsed power supply
RFH	Radio-frequency heating
SC	Supercapacitor
SNU	Switching network unit
SM	Submodule
SMES	Superconductive magnetic energy storage
STATCOM	Static synchronous compensator
T	Tritium
TF	Toroidal field
UPS	Uninterruptible power supply

1 Introduction

1.1 Motivation of the dissertation

ASDEX Upgrade is a mid-size tokamak operated at the Max-Planck-Institute for Plasma Physics (IPP) since 1991 [1]. This experimental reactor allows to study the plasma physics in a reactor-like environment, which means that most of the systems studied there are similar (but scaled-down) to the ones that will be used in a future fusion reactor that could generate net energy out of it. Among those systems, the power supply is one of the most challenging ones. ASDEX Upgrade electrical power is provided by three independent flywheel generators which have been built only for this experiment more than 30 years ago. Since the flywheel generators market has changed in the last decades, there exist no present company able to produce nowadays a flywheel generator with a size as large as the largest one ('EZ2') used at IPP. For this reason IPP scientists started to search for alternative power supply systems that could replace one or more of the flywheel generators in case of permanent faults. The first idea consisted in conducting a feasibility study on the adoption of several smaller flywheel generators in parallel to reach the same power required by EZ2, but the outcome of this research was not successful due to synchronization problems [2]. Since modern flywheel generators seem to be not an option, IPP decided to search for a different technology with similar energy and power density: common batteries have higher energy density but too low power density, leading to a huge excess of (unused) energy in order to reach the required power; capacitors on the other hand have a very high power density, but a low energy density. For these reasons it has been decided to investigate on the upcoming technology of supercapacitors, which fits with flywheel generators in terms of both energy and power density. In order to deliver the required power to ASDEX Upgrade coils however supercapacitors are not enough, and a proper power converter is necessary. As it will be shown along the dissertation there exist already some supercapacitors-based power supplies for fusion applications, but all those systems use supercapacitors as a single passive bank and a single powerful converter controls them. This would be the equivalent supercapacitor-based solution of a flywheel generator which would solve the current problem of replacing EZ2, but on the other hand it would present its main concern: any major failure in the supercapacitors bank or in the output converter would affect the whole system and therefore the operation of ASDEX Upgrade would be affected. This concern led to the search of a modular system and

from here the idea of combining together supercapacitors with the modular multilevel converter was born: this converter has several identical small-scale power converter modules (submodules) that can control individually the supercapacitor modules; in this way in case of failure of a single supercapacitor module or submodule, the whole converter would not be affected or it could even continue the operation with a proper fault management. Right now there exists no similar solution as the one described in this dissertation, and for this reason it has been decided to keep the design as much flexible as possible, so that in case of need it can be adapted for different applications.

1.2 Organization of the dissertation

The dissertation starts with a brief introduction of the nuclear fusion reaction and how it could generate electricity in future. Some general information about tokamaks are also provided, with the focus on ASDEX Upgrade - the experimental reactor operated at IPP - to provide the context and better understand why the idea of this PhD came out. Chapter 3 provides first an overview on the existing technologies in the field of pulsed power in general, than flywheel generators and supercapacitors are explained and compared, while the chapter ends with the introduction of the modulal multilevel converter which is the topology used as reference to build the developed converter. Chapter 4 describes the proposed converter, providing all the relevant information about its design in order to be able to adapt it in case of different applications. The following chapter instead describes the stepwise developed prototype, from the single module to the demonstrator together with the experimental results. All the main components have been described and information about why they have been chosen are provided. The last chapter finally shows first the validated results and then the main challanges to be faced to eventually scale up the prototype.

1.3 Software used for the dissertation

This dissertation has be written with the help of LaTeX [3]. The model of the proposed converter (see Ch. 4.2.3) has been developed on PLECS [4], while all the plots - both simulated and measured - have been adapted on Matlab [5] to keep a uniform style. EAGLE [6] finally has been used to design and print all the printed circuit boards of the prototype.

2 The nuclear fusion as an energy source

2.1 What is fusion?

Nuclear fusion is the process that powers the sun and the stars, making life on earth possible. It is named 'fusion' because the energy is produced by combining light atomic nuclei, such as hydrogen isotopes, at extremely high temperatures [7], [8]. In this process part of the mass of the reactants is converted into kinetic energy of the reaction products, which in turn can be used to produce electrical energy in a standard steam turbine cycle. Nuclear fusion is considered an essential element of a sustainable and CO2-free basket of electrical energy sources, which will be used to meet the quick growth of the global energy demand. Global energy demand is indeed expected to be more than doubled by 2050 due to the combined effect of the increase of population and energy need per person in developed countries [9]. The most advantageous features of the future fusion devices can be therefore summarized as follows:

- *Environment-friendly:* the products of the most promising fusion reactions (deuterium and tritium) are only helium and neutrons. No long-term radioactive wastes are generated and with a proper choice of materials for the reaction chamber, induced radioactivity in structural components decays in a relatively short time (tens of years) if compared with the values of conventional nuclear power plants (hundreds of thousands of years).
- *Intrinsically safe:* no chain-reaction is possible, since a very small amount of fuel is needed; in case of damage, accident, or loss of control, fusion reactions and heat generation decay in a few ms and inherently switch off.
- *Sustainable:* the fuel - deuterium and lithium (tritium can be produced from lithium in the reactor) - are widely available and virtually unlimited (deuterium is abundant in sea water and lithium can be extracted from rocks and ocean water).
- *CO_2-free:* there is no direct production of greenhouse gases involved [10].

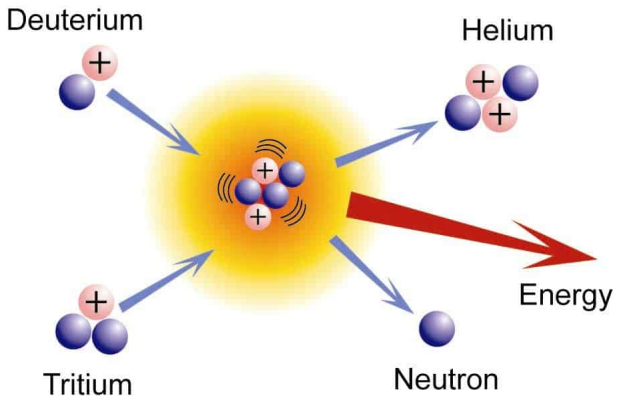

Figure 2.1: D-T reaction: this is the most favourable reaction among all the possible ones on the Earth. The fusion of a D and a T nuclei generates a nucleus of helium and a neutron, releasing 17 MeV of energy [8].

2.1.1 The reaction

An atom consists of a nucleus around which electrons gyrate. It has a null total charge, because of the equal number of positive charges (protons) and negative charges (electrons). The nucleus consists of two kinds of particles, neutrons and protons, linked to each other thanks to intense nuclear forces. Nuclear fusion is the nuclear reaction in which two or more atomic nuclei collide at very high energy and fuse together into a new nucleus. If light nuclei are forced together, they will fuse while releasing energy because the mass of the combination will be less than the sum of the masses of the individual nuclei. Therefore according to the Einstein equation $\Delta E = \Delta M \cdot c^2$ (where c=3 $\cdot 10^8$ m/s is the speed of the light), the amount of released energy ΔE directly depends on the difference of mass among products and reactans of the reaction (ΔM).

The Deuterium - Tritium (D-T) fusion reaction is the most favourable one that can be reproduced in fusion devices. As shown in Fig. 2.1 and stated below, the fusion of a D and T nuclei generates a helium nucleus (also known as α particle) and a neutron releasing 17600 keV.

$$D + T \longrightarrow \alpha + n + 17.6\,\text{MeV}$$

Together with the D-T reaction there are many other possible fusion reactions, but studies of the nuclear properties of light elements indicate that three of such reactions may be attractive for the production of energy. These are, besides the D-T reaction, the deuterium-deuterium (D-D) and the deuterium-helium-3 (D-3He) reactions. One would think that the D-D reaction is the most convenient one since it does not involve tritium, but only deuterium which is not radioactive and largely abundant in nature. However, the D-D reaction requires about 10 times higher temperatures than the D-T reaction,

which poses already several challenges to be achieved.

2.1.2 The plasma state

Due to the very specific conditions required - e.g. very high temperatures - fusion can occur only if the fuel is in the plasma state. In physics the term plasma is used to identify an ionized gas consisting of a collection of electrons and ions that is globally neutral (its total electrical charge density is zero) and presents collective behaviours. It is considered as the fourth state of matter, which is therefore different from solid, liquid and gaseous states. "Ionized" in this case means that a significant fraction of electrons has been ripped out from the atoms; the free electrical charges ensure that the plasma is a good conductor of electricity, and that it responds strongly to electromagnetic fields [11]. The most famous example of plasma present in the nature is the sun: there, the gravity is so strong to trap the hydrogen of the athmosphere and fuel sun's fusion reactions. In its core - at 15 million degrees - hydrogen gas becomes plasma and the positively charged atomic nuclei move furiously and collide at high speeds overcoming the natural electrostatics repulsion that exists between the positive charges: thus the hydrogen nuclei fuse forming heavier helium nuclei [12]. Since the gravity on the earth is much weaker than the one on the Sun, the plasma has to be confined in a forced way in order to make fusion possible: among all the different methods, the magnetic confinement is the technically most advanced and promising method.

2.1.3 Magnetic confinement

In a plasma - without any external magnetic field - particles would be free to move in any direction (see Fig. 2.2), reaching the walls of the container in which they are contained, cooling the plasma and inhibiting the fusion reactions. An appropriate configuration of the external magnetic fields can force the particles to follow spiral trajectories around the field lines, preventing their contact with the walls.

In particular, charged particles in a magnetic field follow an helical path around the field lines according to the Larmor equation, which defines precisely the Larmor radius:

$$r = \frac{M\upsilon}{qB} \tag{2.1}$$

where M is the mass of the particle, q is its charge, υ is the speed of the particle perpendicular to the magnetic field and B is the intensity of the magnetic field [13], [14]. The Larmor radius expression shows that a particle follows a trajectory with a distance r from the magnetic field line. The magnetic confinement that can be obtained in a reactor however is not as efficient as the one in the sun for technological limitations (lower density, smaller size). This means that in order to obtain fusion on earth, the

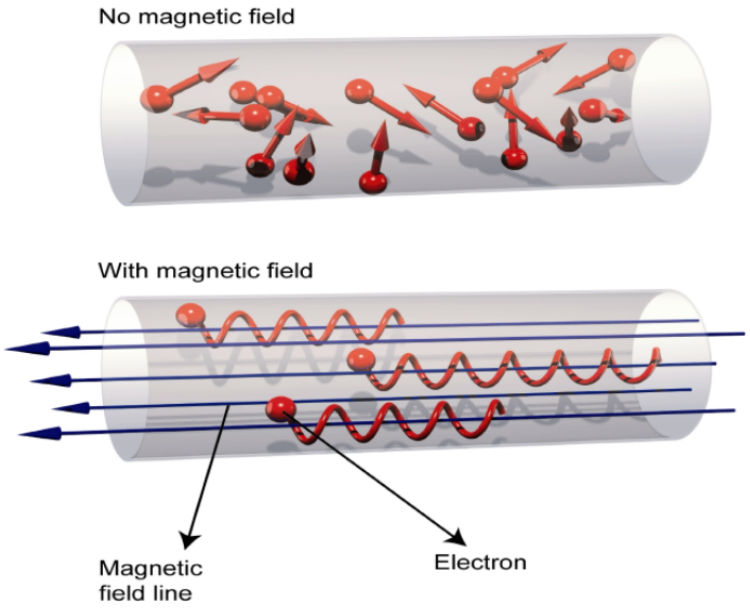

Figure 2.2: Magnetic confinement: without any induced external magnetic field in a plasma, electrons are free to move in any directions. By applying a magnetic field instead, they are forced to move in the direction of the magnetic field lines and gyrate around them: this is the principle on which is based the magnetic confinement of fusion devices [7].

temperature of the plasma must be much higher, approximately in the range of 150-200 million degrees - about 10 times the sun's core temperature.

2.2 The tokamak

The tokamak is a toroidal shaped device which is based on the magnetic confinement. "Tokamak" is a transliteration of the Russian words "TOroidalnaya KAmera" and "MAgnitnaya Katushka", which stands for toroidal chamber and magnetic coil [15]. This type of machine has been the most studied in the field of magnetic confinement and is currently considered to be the most promising solution for building a fusion power plant in the future. Tokamaks' magnets system usually mainly consists of three kind of coils: Toroidal Field coils (TF), Poloidal Field coils (PF) and Central Solenoid (CS, or inner poloidal field) coils. TF coils generate a toroidal field that combines with the poloidal field provided by the plasma itself. In the combined field, the field lines run helicoidally around the torus centre and thus the so-called magnetic cage is formed. Apart from the toroidal field generated by the external field coils and the field generated by the plasma, the tokamak requires a third vertical field (generated by the PF coils), fixing the position and the shape

of the plasma. The CS forms a transformer together with the plasma, and it has the main function of inducing a magnetic flux variation into it, providing an effective initial ohmic heating of the plasma and ramping up the plasma current (I_P). Plasma ignition can be realized by pre-charging the CS coils before the operation, and rapidly discharging it at the beginning of the experiments to provide a loop voltage of some tens of V, high enough to reach the breakdown. Since the CS coils can not be continously discharged, the tokamak can work only in pulsed operation.

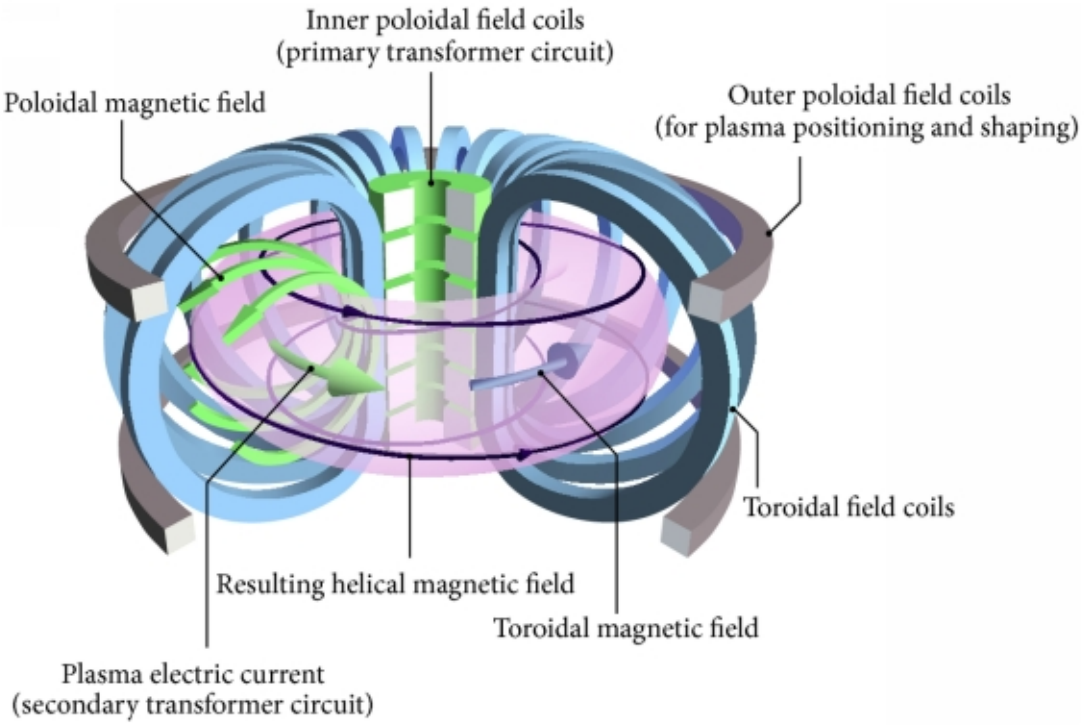

Figure 2.3: Main tokamak's coils: the CS coils, I_P, and the poloidal magnetic field are indicated in green; the TF coils and the toroidal magnetic field are shown in blue; the outer poloidal field (or PF) coils are displayed in gray. The confined plasma is represented by the magenta torus [7].

The ohmic heating anyway can not heat up alone the plasma at the required temperature, especially in large tokamaks, where several keV are typically targeted. This energy, expressed for convenience in terms of dissipated power density, is given by:

$$p_\Omega = \rho j^2 \tag{2.2}$$

where ρ is the resistivity of the plasma and j is the current density. However, as the temperature increases, the frequency of collisions and the resistivity decrease. Consequently,

at the temperatures required for the ignition, the ohmic heating is very low. Therefore, the need of one or more additional heating systems is evident. The Neutral Beam Injection (NBI) and Radio Frequency Heating (RFH) are indeed the most famous additional heating systems used in fusion devices. The NBI injects highly energetic neutral particles, which have to be neutral because otherwise they would be reflected by the magnetic field of the tokamak, and would not be able to reach the plasma core region. By crossing the plasma, the neutral particles collide with the plasma particles while transfering their kinetic energy, which is equal to heat transfer. The RFH instead transfers energy to the plasma mixture through high frequency electromagnetic waves. Since plasma ions and electrons rotate around the magnetic field lines with specific frequency (depending on their mass and magnetic field amplitude), electromagnetic waves can resonate with them if they have the same frequency, transferring their energy to the plasma particles and heating them up. Depending on the target particles, the RFH can be divided in Electron Cyclotron Resonance Heating (ECRH) for electrons heating and Ion Cyclotron Resonance Heating (ICRH) for ions heating: ECRH generates electromagnetic waves with frequencies in the range of 100-200 GHz, while ICRH's fequencies are in the range of tens of MHz.

2.2.1 Lawson criterion

The Lawson criterion has been formulated by the English engineer and physicist John D. Lawson in 1955 to characterize the set of parameters allowing a fusion reactor to produce more energy than it absorbs. Plasma has to be heated at very high temperatures and the quality of the heat confinement allows to keep the plasma in favourable conditions for the reactions. The capacity of conserving the heat defines the "Energetic Confinement" and apart from it a certain density of the particles is required for a specific time. The Lawson Criterion therefore defines the parameters to reach the condition by which the energy produced from the fusion reactions equals the energy supplied to the plasma, the so called Breakeven condition:

$$\eta \tau_{\mathrm{E}} T_{\mathrm{p}} \geq 3 \cdot 10^{21} \mathrm{m}^{-3}\ \mathrm{keVs} \tag{2.3}$$

where η is the density of particles, τ_{E} is the confinement time and T_{p} is the temperature. In future fusion reactors the product $\eta \tau_{\mathrm{E}} T_{\mathrm{p}}$ has to satisfy the breakeven condition, reaching the ignition, which means that the plasma becomes self-sustaining [15]. The Lawson criterion has become a fundamental relationship over the years that must be satisfied by fusion reactors: it essentially indicates that the so-called "triple product" has to be greater than the value of Eq. 2.3. Even if significant values of one of the three parameters can be relatively easily obtained in modern laboratories, getting all three at the same time is a difficult task and it is one of the main challenges of the actual and future fusion reactors.

2.2.2 Energy production in a thermonuclear power plant

Once the ignition has been reached, each fusion reaction generates 17 MeV of energy of which only a fraction can be extracted: most of the α particles are trapped into the magnetic cage and their thermal energy helps to sustain the high temperature of the plasma, while the neutrons can escape the magnetic fields and collide with the first wall of the reactor. The kinetic energy of the neutrons is thus converted into thermal energy and thanks to a proper refrigerant, it can be extracted and converted into electrical energy through one of the conventional methods used in present thermonuclear power plants (i.e. steam-turbine-generator system). Furthermore, future fusion reactors will have lithium present in their first wall (called breeding blanked in that case), which will react with the neutrons producing tritium, helium and additional neutrons according to the following reactions:

$$Li^6 + n \longrightarrow T + He^4 + 4.8\ MeV$$

$$Li^7 + n \longrightarrow T + He^4 + n - 2.5\ MeV$$

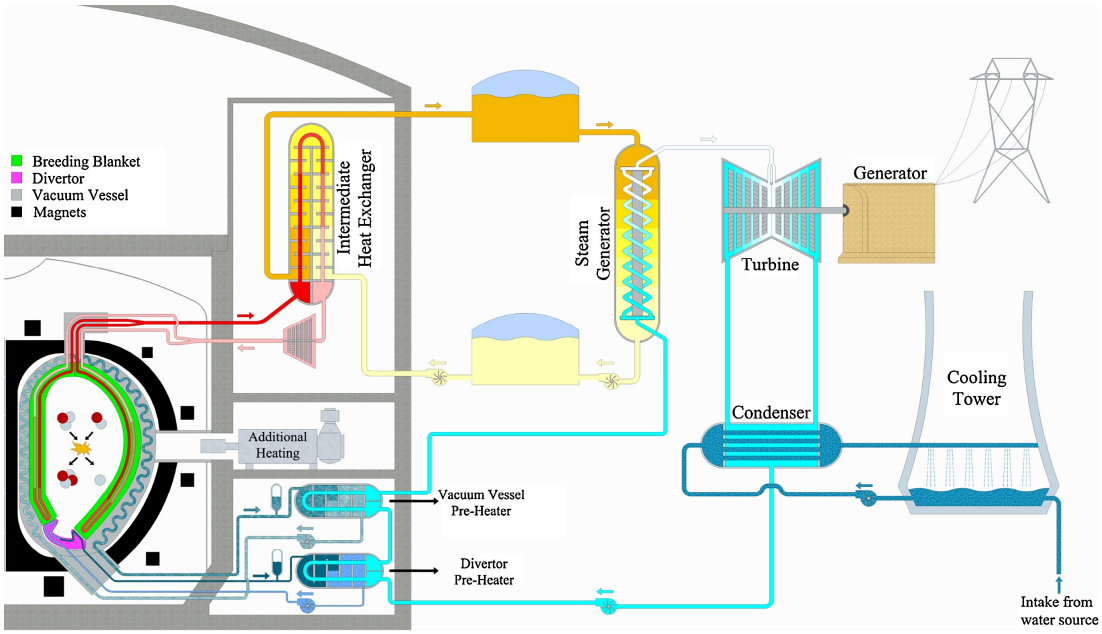

Figure 2.4: Demo heat transfer chain: most of the thermal energy produced by the fusion in the reactor is extracted from the breeding blanket and it passes through an intermediate heat exchanger that acts as buffer between the tokamak and the turbine-generator system, in order to mitigate the pulsed operation of the reactor in terms of electrical energy generation [16].

The produced tritium can therefore be extracted and re-injected into the reactor to fuel it, avoiding the need of any external tritium supply [17]. In Fig. 2.4 a scheme of

the future DEMO power plant is shown, which is foreseen to be the first demonstrator fusion power plant to be operative within the first half of this century. The first wall of the reactor will have to extract about 85% of the power generated by the tokamak and its conceptual design foresees four concepts that rely on different cooling systems, such as water or helium based ones. With the aim of mitigating the potential negative impact of the plasma pulsing on the turbine for the DEMO plant a heat transfer chain has been investigated, which foresees the use of an intermediate heat transfer system that should act as bridge between the reactor and the turbine. Such intermediate system is equipped with an energy storage system that, during the pulsed operation, collects a portion of the thermal energy transferred by the tokamak in order to give it to the turbine-generator system during the resting time of the reactor; this device should therefore limit sharp changes in turbine load and let it to work in pseudo steady-state condition both during pulse and resting time [16].

2.2.3 ASDEX Upgrade

ASDEX Upgrade is a medium-sized metallic-wall divertor tokamak located at the Max-Planck-Institute for Plasma Physics in Garching (Germany). The machine entered into operation in 1991, and it is the follow-up experiment of the ASDEX (Axial Symmetric Divertor EXperiment) tokamak, which was operated from 1980 to 1990. This tokamak has currently the highest ratio of the heating power to the size of the machine, which makes it particularly suited for exhaust studies and plasma scenario development for future reactors. The main objective of the ASDEX Upgrade project is to develop integrated scenarios for long-pulse operation of burning plasmas in future fusion reactors which include solutions for plasma shaping, confinement and stability, divertor and power exhaust, as well as the choice of appropriate wall materials. This effort includes advancing the physical understanding of related fundamental problems in order to create reliable predicting capabilities and to discover new paths to advanced plasma operation [18].

ASDEX Upgrade has 16 TF coils generating a constant toroidal field during the whole experiment duration, even though it can be varied during the discharge if the physical requirements ask for it. 12 vertical field coils - including the CS - are used to control the plasma shape (elliptical with an X-point in the lower region) and two additional ones are close to the plasma (PSL) for a faster shape control. The described set of coils is controlled in real-time by the discharge control system (DCS), which estimates plasma shape and position in real-time mainly thanks to a high number of magnetic probes placed close to the plasma and corrects the currents in the field coils in order to achieve the desired values. In the Tab. 2.1 the typical values for a plasma experiment are shown. The available heating systems consist of 8 NBI sources, providing up to 2.5 MW each for a total of 20 MW of heating power, 8 ECRH gyrotrons, each delivering about 0.7 MW of heating power for a total 6 MW, and 4 ICRH generators, heating the plasma with 1.5

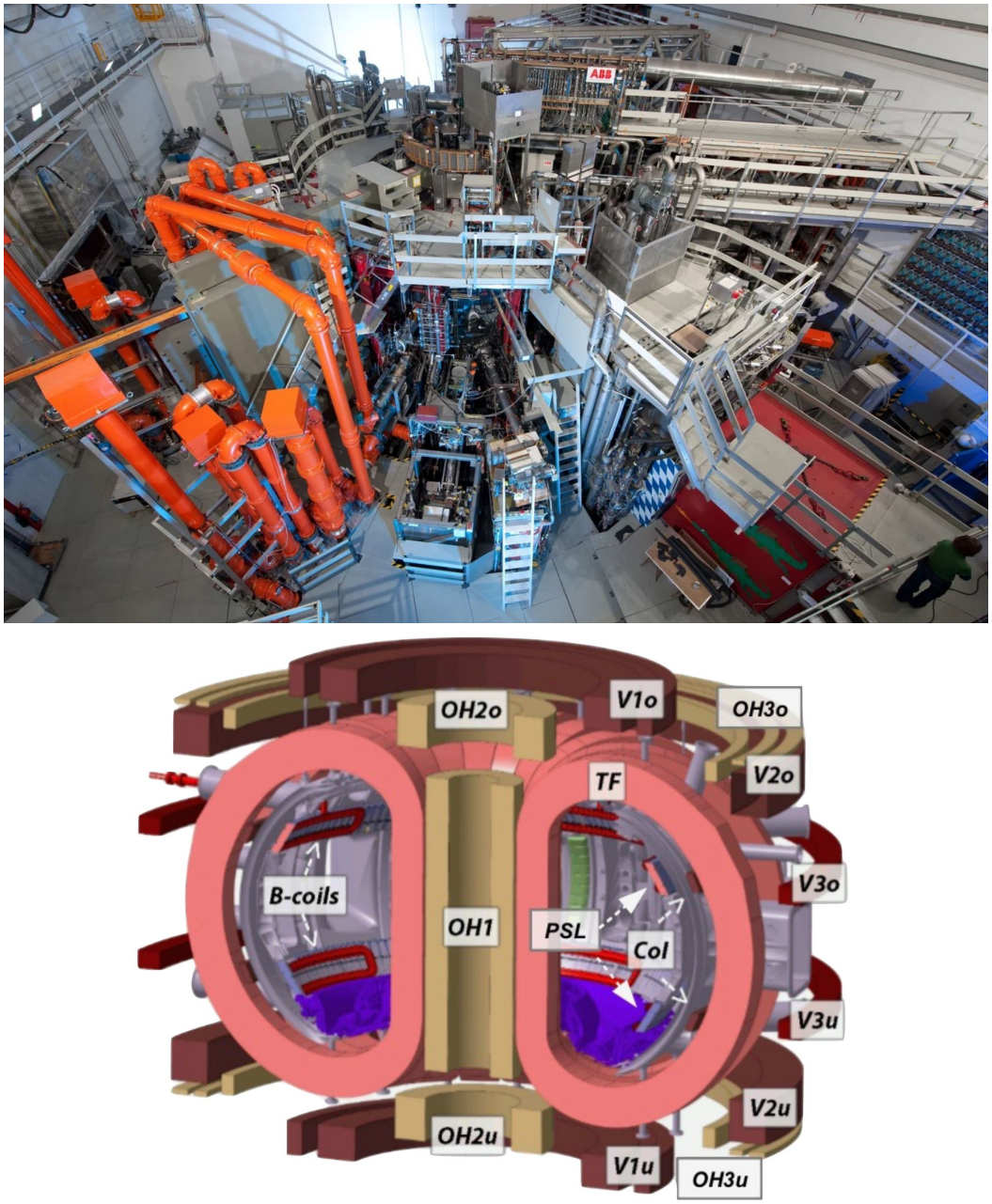

Figure 2.5: Panoramic view of the ASDEX Upgrade torus hall (top) and machine coils' configuration (bottom) [19].

MW each for a total of 6 MW. The NBI sources have different orientations, leading to a deposition of the power which can be more central or more peripheric (4 beams are more aligned to the magnetic axis while the other 4 are pointing more off-axis). The ECRH system makes use of metallic mirrors which can be tilted to deflect the beam at the desired angle and change the heating position or even to drive the plasma current.

Parameter	Value
Total height of the experiment	9 m
Weight of the experiment	800 t
Material of the first wall	Tungsten
Number of TF coils	16
Number of PF coils	12
Plasma current I_P	0.6-1.6 MA
Toroidal magnetic field B_{tor}	1.5-3.2 T
Pulse duration	$<$ 10 s
Time between pulses	15...20 min
Maximum NBI power	20 MW
Maximum ECRH power	6 MW
Maximum ICRH power	6 MW

Table 2.1: Main ASDEX Upgrade' s machine parameters.

The position of the ICRH antennas is fixed so it is not possible to change the location of the heating power by means of mechanical movements of the system. The power supply system of ASDEX Upgrade is described in the next chapter.

3 Energy storage systems for pulsed power supplies

3.1 Pulsed power supplies

3.1.1 Definition and typical scenario

Pulsed Power Supplies (PPS) are systems where stored energy is discharged as electrical energy into a load in a single or multiple pulses with a controllable repetition rate. They are usually based on an energy storage system that is slowly charged with a relatively low charging power and then rapidly discharged. Thanks to this procedure a large power multiplication can be obtained and the process can be repeated several times if necessary. The energy can be stored either chemically, mechanically or electrically. Mechanical and electrical storage systems, being part of the core of this thesis, are described in the next subsections of the chapter. Typical power and energy ratings of PPS are around 10^6...10^9 W and 10^3 J, with voltage and current in the ranges of 1 kV...1 MV and 1 kA...10 MA, respectively. In addition to its electrical parameters, a pulse is characterised by a specific shape divided into three main phases: ramp-up, flat-top and ramp-down phases, as shown in Fig. 3.1. Ramp-up (and ramp-down) are usually defined by time that the load current takes to rise from 10% to 90% (and vice versa) of its flat-top average value, while the overall duration of high-power pulses can range between some nanoseconds and a few seconds. Flatness of the flat-top phase is an important requirement and the current ripple during this phase can have a maximum thereshold depending on the application [20]. The specific case of ASDEX Upgrade TF coil requires a current profile similar to the one shown in Fig. 3.1 with main costraints of flat-top current (54 kA to be kept constant), energy (800 MJ of net energy per experiment required) and time (flat-top time of at least 10 s). The constraints used as a reference are the minimal requirements for a typical 2.5 T pulse, but the TF coils are rated to operate with up to 4 T. In the next section the actual current profile is described in detail and existing pulsed power systems able to produce it are shown, highlighting their limitations before introducing the proposed MMC-like solution.

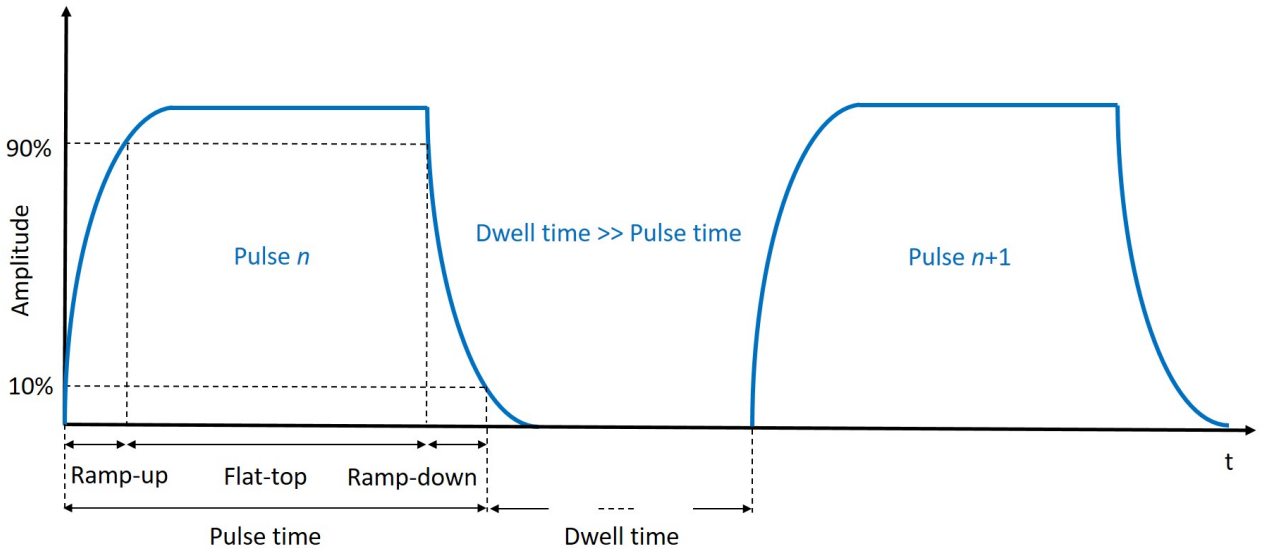

Figure 3.1: Typical current shape of a pulsed powered load. The time between consecutive pulses (dwell time) is typically several orders of magnitude longer than the pulse time [20].

3.1.2 The Ragone plot

The so-called "Ragone plot" (Fig. 3.2) compares the main energy storage systems used for pulsed power supplies in terms of energy and power density: technologies such as Compressed Air Energy Storage (CAES) and batteries can store large amount of energy (high energy density) but can not deliver it in a powerful way (low power density); on the other hand standard capacitors, for example, can be very powerful but have a very limited amount of stored energy. According to energy and power density of the current power supply system of the ASDEX Upgrade TF coil ('EZ2' in Fig. 3.2), only supercapacitors can be considered as potential candidates to replace it. Supercapacitors can reach a power density of up 5-10 kW/kg (similarly to standard capacitors) while they are similar to flywheels in terms of energy density (up to 10-20 Wh/kg) [21]. While batteries and standard capacitors have charging/discharging times in the range of minutes/hours and up to a few ms, respectively, supercapacitors can be considered as a hybrid solution between these two technolgies, considering their charging time of up to some tens of seconds. Therefore due to their position in the Ragone plot supercapacitors and flywheels technologies are used in many fusion-related experiments as it will be shown in the next sections. The Superconductive Magnetic Energy Storage (SMES) has also a well-fitting energy-power ratio for fusion applications and it is object of current research activities [23]. However, even though this technology is currently used in non-fusion applications [24], its application requires complex conditions (i.e. cryogenic systems...) and at the moment there exists no working SMES supplying fusion systems as for the case of flywheels and supercapacitors.

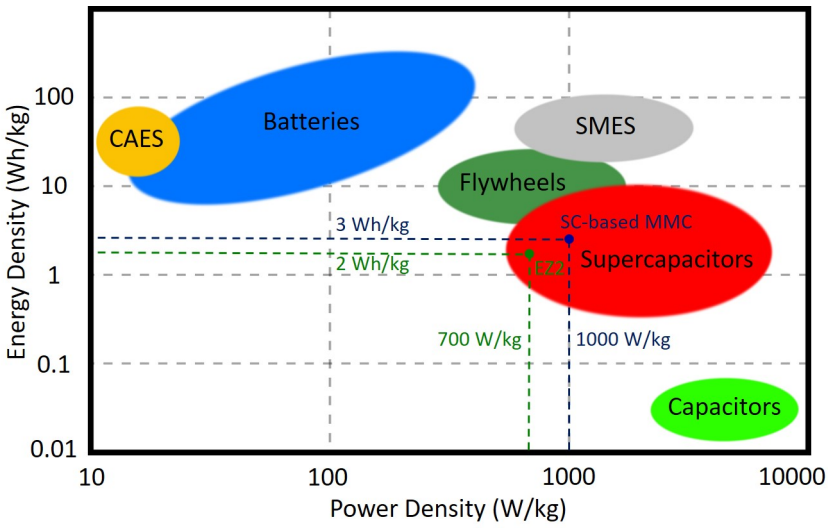

Figure 3.2: Comparison among different energy storage systems in terms of energy and power density; CAES and SMES stand for compressed air energy storage and superconducting magnetic energy system, respectively [21]-[22]. The colored zones are only indicative of a family of devices, and further curves could be inserted for a more specific type of device (for instance, type of battery or capacitor) but they are not shown for simplicity.

Most of the mentioned storage systems, however, require additional systems - such as motors/generators or power converters - to drive their energy in a proper manner to the respective loads. Therefore, the operating point of a power supply containing one of those technolgies can be outside from the operating area of the energy storage itself. In Fig. 3.2 indeed EZ2 is pointed out and compared with the solution proposed in this dissertation. The data used to place EZ2 in the figure are described in Ch. 3.2.2, while a detailed size estimation of the proposed power supply system is shown in Ch. 6.2.

3.2 Flywheel generators

3.2.1 Flywheel storage systems

The first known utilization of flywheels specifically for energy storage applications was to homogenize the energy supplied to a potter wheel, and several types of flywheel energy storage systems exist [25]. However, in fusion experiments only flywheel generators have been used so far. A flywheel generator is composed by a motor, a flywheel and a generator: the motor is usually one or more orders of magnitude smaller than the generator and it accelerates the flywheel with a relatively low power up to a specific speed, depending on the required energy; the generator then can convert the kinetic energy of the flywheel to elecrical energy again when required. Power and size difference

of motor and generator defines the input/output power multiplication, however in many cases a single machine is used both as motor and generator. The maximum amount of energy that can be stored depends on the moment of inertia (Θ) and on the angular speed (ω) of the flywheel, according to the formula:

$$E = \frac{1}{2}\Theta\omega^2. \tag{3.1}$$

Θ represents the resistance of the moving body to changes in its momentum. By approximating the flywheel as a solid rotating disk of mass M and radius r, the moment of inertia increases with the increase of M as well as with the increase in r around the axis of rotation ($\Theta = 1/2Mr^2$). In this inertia/applied force interaction lays the basic concept behind the utilization of flywheels for energy storage in any mechanism. With the obvious discharge limitations of other storage technologies, such as standard capacitors and batteries, flywheels have significant advantages for discharge times between 1 and 100 s and discharge powers above 20 kW. In terms of power and energy density this fits the requirements of most of the ASDEX Upgrade's electrical loads and for this reason this technology has been chosen for the mentioned experimental reactor power supply system.

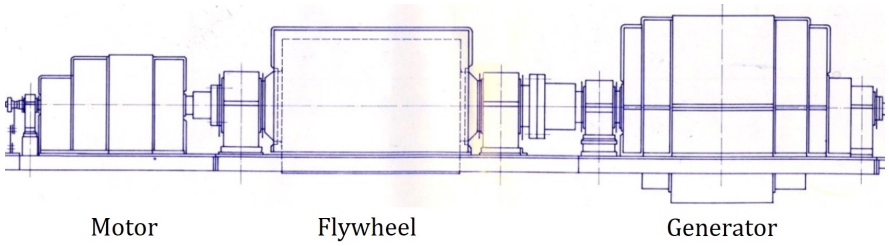

Figure 3.3: Typical structure of a flywheel generator: a motor accelerates a flywheel, converting electrical energy into kinetic energy. Once the amount of required energy has been stored within the flywheel, the generator can convert it back into electrical energy again powering the electrical load [19].

3.2.2 ASDEX Upgrade power supply system

The Max-Planck-Institute for Plasma Physics is connected to the external public grid by two 110 kV / 10 kV transformers. A 31.5 MVA transformer is dedicated to the standard network and base load supply. An SF6 substation with 36 switch panels distributes the power to the line transformers of IPP and nearby institutes. For surge load and large experimental consumers, a second 16 MVA transformer is reserved. Three connected air-insulated substations feed large drives and converter installations and about 150 smaller transformers are spread over the premises. The pulsed power needed for an ASDEX

Upgrade plasma discharge amounts up to 580 MVA for 10 s. To buffer this excessive peak load from the public grid, its operation relies on three large flywheel generators: "EZ2", "EZ3" and "EZ4". These generators feed the pulsed power supply system for the magnetic confinement (high current) and additional heating (high voltage) of the plasma with up to 2818 MJ of stored energy (see Fig. 3.4) [26].

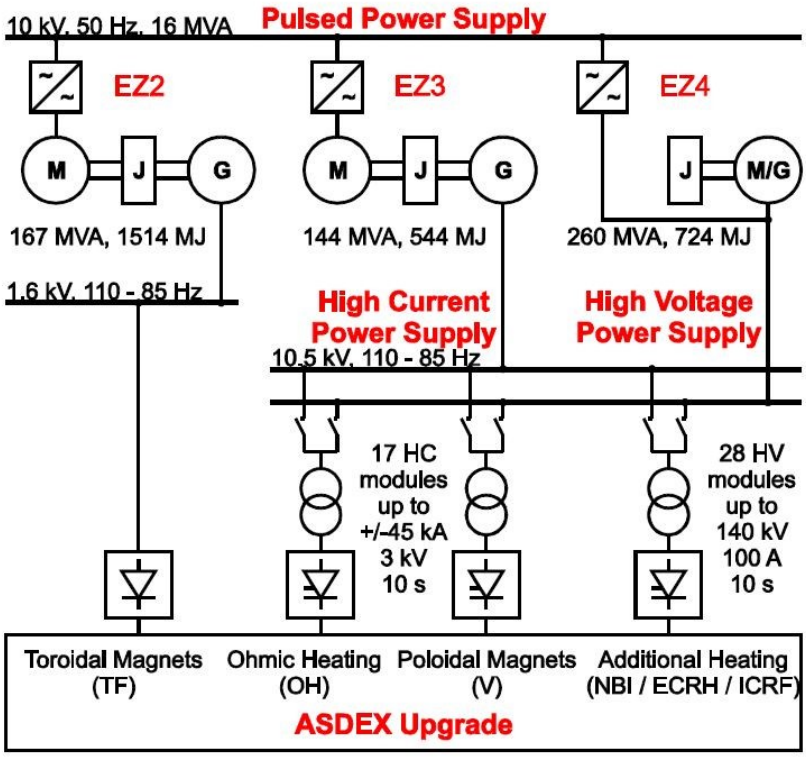

Figure 3.4: ASDEX Upgrade's pulsed power supply system. The schema shows the three flywheel generators, each of which supplying a different load: EZ2 provides power to the TF coil while EZ3 and EZ4 supply CS, PF coils and the additional heating systems. The output configurations of EZ3 and EZ4 can be changed and they can both power the mentioned loads [26].

The machine units have a horizontal shaft line assembly with oil lubricated bearings. The motor drives of EZ2 and EZ3 are a 5.7 MW and a 7.5 MW doubly-fed four pole induction machines respectively. The stator is fed from the 10 kV / 50 Hz network, the rotor is connected to a hydraulic rheostat for start-up and a drive converter takes over at neutral frequency. The converter output is controlled on slip frequency, and modifying this frequency between -7.5 and +5 Hz allows the setting of a generator speed in the range of 1275 to 1650 rpm. The three phase synchronous generators have eight salient-pole rotor windings connected to an excitation converter, while the stator is connected to the load feeder. The output line frequency varies between 110 and 85 Hz, proportional to the generator´s speed. The technical data of the three FGs are summarized in Tab. 3.1.

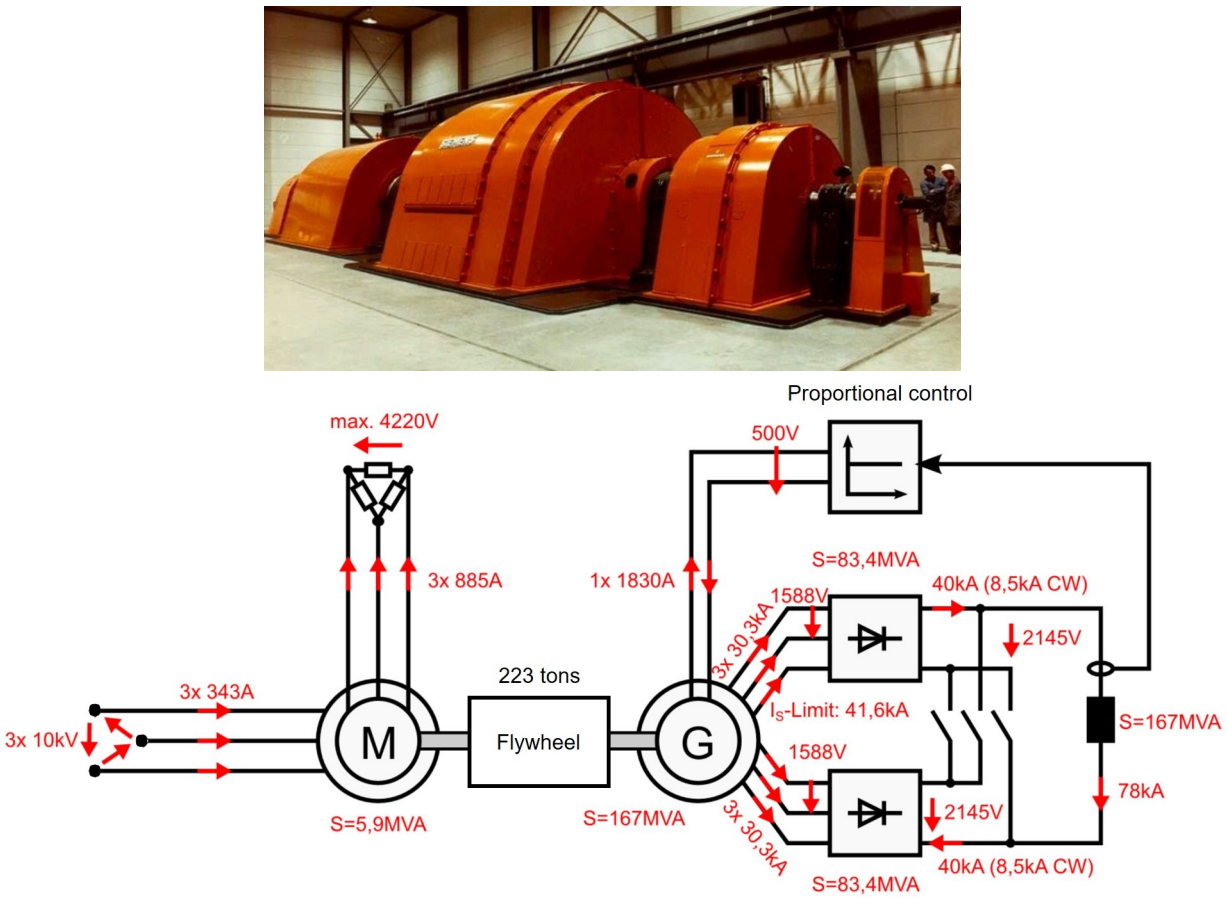

Figure 3.5: Flywheel generator EZ2 photo (top) and electrical simplified schema (bottom): the three-phase motor drive takes 5.7 MW from the 10 kV grid storing up to 2 GJ in the flywheel within 30 min; the 167 MVA generator thus can convert the kinetic energy of the flywheel into eletrical energy, generating up to 150 MW for 10 s. Its output power passes through an 80 kA diode rectifier directly powering the ASDEX Upgrade's TF coil [26].

The flywheel generator EZ2 is directly connected to an 80 kA diode rectifier feeding the ASDEX Upgrade main toroidal field. This toroidal field is proportional to the rectifier output current and controlled directly by the generator excitation. The maximum possible field is 3.7 T corresponding indeed to 80 kA (see Fig. 3.5). EZ3 and EZ4 supply two independent 10.5 kV busbars, feeding the high current converters for the plasma shape and position control coils and the high voltage controllers for the additional heating systems. The start-up time of EZ2 is about 30 min and in order to reduce friction losses, the generators run at an idle speed around 1380 rpm. Depending on the power and energy needed for the next plasma pulse, the tokamak remote control sets the individual operating speed for every generator and sends the command to start acceleration. The acceleration time is determined by EZ2 and is about 5 min. To optimize ramp-up with

Flywheel generator		**EZ2**	**EZ3**	**EZ4**
Date of manufacture		1973	1977	1987
Speed	ν [rpm]	1275-1650	1275-1650	1275-1650
Rotating mass	M [t]	323	117	142
Available energy	E [MJ]	1514	544	724
Motor				
Drive power	P_N [MW]	5.7	7.5	
Nominal voltage	U_N [kV]	10	10	
Generator				
Output frequency	f_N [Hz]	85-110	85-110	85-110
Output power	S_N [MVA]	167	144	260
Power factor	$\cos\phi_N$	0.93	0.86	0.49
Nominal voltage	U_N [kV]	1.6	10.5	10.5
Flywheel				
Diameter	d [m]	2.9	3.4	3.4
Length	l [m]	3.9	0.73	0.95
Mass	M [t]	223	59	76

Table 3.1: Main data of ASDEX Upgrade' s FG: EZ2 is the largest and oldest one.

respect to time, peak power and 15-min-demand limits, EZ3 and EZ4 are accelerated one after another, but in parallel with EZ2. During the pulse the generators convert the rotational kinetic energy of the flywheels into electrical energy and the generators' speed drops down from a maximum of 1650 rpm to a minimum of 1275 rpm. Since the available energy is proportional to the square of speed, 40 percent of the total energy stored within the generator shaft line can be used. After a discharge finally the flywheels return to idle speed, again. Fig. 3.6 shows the main electrical parameters required by the TF coil during a typical experiment, which is fully supplied by the flywheel generator EZ2. The 16 TF coils (they are connected in series and can be considered as a single equivalent coil) represent an inductance of 120 mH and a resistance of 14 mΩ, since they are not superconductive. The current is first ramped-up, than kept smooth and constant during the flat-top phase and finally ramped-down at the end of the pulse. The TF coil impedance is almost perfectly constant and decoupled from the other loads of the tokamak. The voltage needed during the ramp-up phase is higher (2.7 kV) than during the flat-top phase with approximately 800 V (to cover ohmic losses) for a current of approximately 54 kA to provide a typical TF magnetic field of 2.5 T in the tokamak vessel. The energy need during flat-top phase is in the range of 0.5 GJ. The main concerns about flywheel generators come from the fact that all the stored energy is concentrated within the flywheel, meaning that in case of any fault the whole machine has to stop.

Furthermore, there are no companies able to produce generators of such a large size

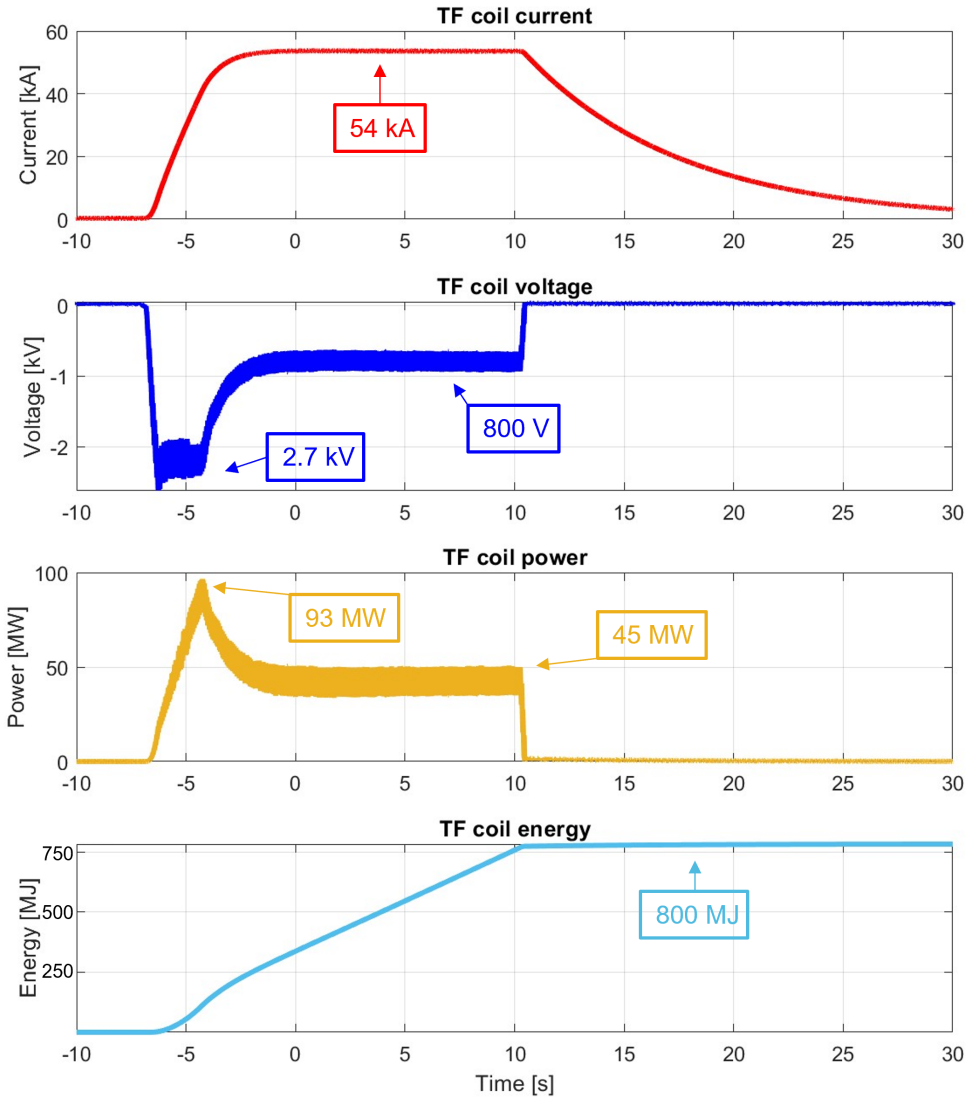

Figure 3.6: AUG's TF coil measured electrical scenario in a typical 2.5 T / 10 s experiment: the current (blue curve) is ramped-up at 54 kA and kept constant during the flat-top phase with a limited ripple (<0.1%); the voltage required is 2.7 kV during the ramp-up and 800 V during the flat-top, where only copper losses have to be covered. The whole experiment requires about 800 MJ of energy [27].

and in case of any permanent fault there would not be any available replacements for one or more of them. These are the main reasons why the idea of the project of this thesis was born, and - as described in the next chapters - the combination of two recent technologies such as the modular multilevel converter and supercapacitors seems to be a promising solution for pulsed power supply systems.

3.3 Supercapacitors

Supercapacitors are well known for their balanced ratio of energy and power density. Due to their material composition and design structure they have a lower equivalent series resistance (ESR) in comparison with other electrical energy storage (EES) systems, leading to higher efficiency, larger current charge and/or discharge capacity and relatively low heating losses. Thanks to their high power density, supercapacitors have several potential applications, but they are mainly used for Uninterruptible Power Systems (UPS) and Hybrid Electric Vehicles (HEV) [28].

3.3.1 Physical description

A cross-sectional view of a supercapacitors cell is shown in Fig. 3.7. Fundamentally, it consists of two metal plates separated by an insulator, just like an ordinary capacitor. The separator, however, is porous and is soaked in an electrolyte. Since the ions of the electrolyte can move freely through the separator, positive and negative ions move in opposite directions and cling to their respective electrodes. The important feature in supercapacitors is that the inner surface of each electrode is not a smooth surface but is rather padded with activated (porous) carbon. This results in a surface area that is up to 10^5 times as large as the surface area of an ordinary capacitor. The large surface area of a supercapacitor, however, is not the only novel feature of the device. Since charges are carried by ions attached to the inner surfaces of the electrodes, the distance between the positive and negative charges at each electrode is on the order of a few Angstrom, being provided from the molecules of the solvent (acting as dielectric). The capacitance of a parallel-plate capacitor is given by:

$$C = \frac{\varepsilon A}{d} \tag{3.2}$$

where $\varepsilon = \varepsilon_0 \varepsilon_r$ is the product of the dielectric constant of the insulator and the permittivity of free space, A is the area of the electrode, and d is the distance between the positive and the negative charge concentrations. By maximizing A and minimizing d, therefore, supercapacitors achieve extremely high values of capacitance [30]. Their main features can be therefore summarized as follows:

- High specific capacitance (more than 10000 F/kg);
- High specific power (more than 5 kW/kg);
- Up to 10 Wh/kg of specific energy;
- Low ESR, contributing to fast power release;
- Fast charging time (from some seconds to some minutes) and low leakage conductivity;

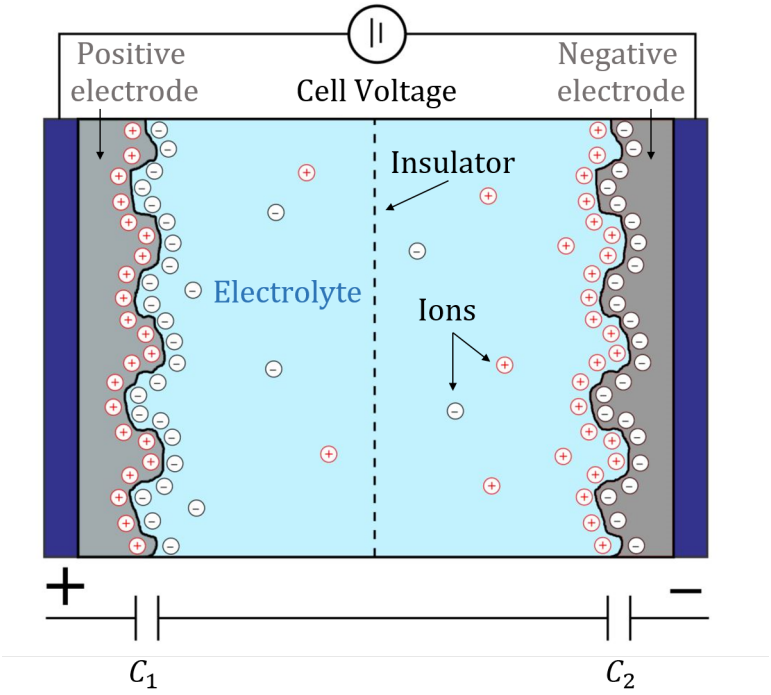

Figure 3.7: SC cell simplified inner structure: the cell capacitance C is the equivalent capacitance of the two charge-ion double layers (C_1 and C_2) at the interface between electrodes and electrolyte ($C = \frac{C_1 \cdot C_2}{C_1 + C_2}$) [29].

- Characteristics not significantly affected by the state of charge;
- Lifetime up to 1 million of charge/discharge cycles and up to 15 years, several orders of magnitude longer than batteries (up to 10000 cycles at low current) due to the negligible presence of chemical reactions;
- Stable performances over large temperature ranges (-40 to 80 °C).

The main limitation is the maximum voltage. Considering the minimized (double-layer) distance $d < 10$ nm, the operating voltage of a single supercapacitors cell is typically limited to 2.5 - 2.7 V (with peaks up to 4 V in some cases). The limited voltage V also affects the maximum energy E that can be stored in a cell, that is:

$$E = \frac{1}{2} C V^2. \tag{3.3}$$

The use of supercapacitors for higher voltages is possible only by making use of supercapacitors modules, composed by several cells connected in series. However, due to the capacitance and ESR unbalancing, it is usually necessary to introduce active or passive components to balance evenly the modules internal voltages, thus increasing the global costs and

complexity. In order to mitigate these inconveniences, manufactures provide assembled modules reaching hundreds of V and F.

3.3.2 Electrical simplified model

Several authors propose electrical models that describe the behaviour of a supercapacitor with a more or less good approximation [31]-[32] depending on the application. However, one of the simplest approximations is a series RLC circuit (see Fig. 3.8) composed by the module's capacitance C, its ESR and an equivalent series inductance (ESL). The equivalent circuit of a module thus depends on the number of cells in series and/or parallel composing the module itself. Furthermore, all the parameters of the equivalent RLC circuit composing a module are frequency-dependent. In particular C drastically decreases with a frequency increase, while ESR and ESL are proportional (not linearly) to it.

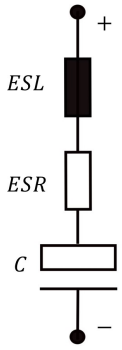

Figure 3.8: Supercapacitors module simplified equivalent circuit: the ESR is the equivalent resistance on the circuit while the ESL depends on shape and area of the current path. Both the parameters are minimixzed by manufacturers.

A decrease of capacitance means less available stored energy, while higher values of ESR and ESL mean higher losses (and heating) and higher voltage spikes during switching events. The supercapaciors module voltage v_{SC} can indeed be expressed as:

$$v_{\mathrm{SC}} = v_{\mathrm{C}} + v_{\mathrm{ESR}} + v_{\mathrm{ESL}} \tag{3.4}$$

where v_{C} is the voltage over C and v_{ESR} is the voltage drop over the ESR. v_{ESL} is:

$$v_{\mathrm{ESL}} = ESL \cdot \frac{\mathrm{d}i_{\mathrm{SC}}}{\mathrm{d}t} \tag{3.5}$$

where i_{SC} is the current flowing into the supercapacitors module. As shown from the previous formula, a rapid change of i_{SC} and/or a large ESL can cause an overvoltage and damage the module. Internal losses can be expressed as:

$$p_{SC} = ESR \cdot i_{SC}^2 \tag{3.6}$$

Power losses therefore directly depend on ESR. These are the main reasons why supercapacitors are mainly designed for DC operation and when operating them in switched environment with a frequency higher than a few tens of Hz, proper filtering is required to guarantee the full lifetime. Frequent overheating of the supercapacitors can cause permanent increase of the ESR and once it permanently doubles its datasheet value, a supercapacitors is said to be at the end of its lifetime.

3.3.3 Existing Supercapacitors-based power supplies for fusion experiments

PROTO-SPHERA power supply

One of the first fusion applications where supercapacitors have been used is PROTO-SPHERA, the first plasma experiment with a simple connected configuration and closed flux surfaces [33]. Its magnetic configuration provides an elongated spherical plasma with a minimal geometrical size (70 cm diameter). The toroidal plasma current and related magnetic field of this machine have anyway the same characteristics of those induced in a standard tokamak. The power supply of this experiment has been designed to provide up to 2 kA of continous current to the machine for 1-2 s every 600 s and its electrical simplified schema is shown in Fig. 3.9.

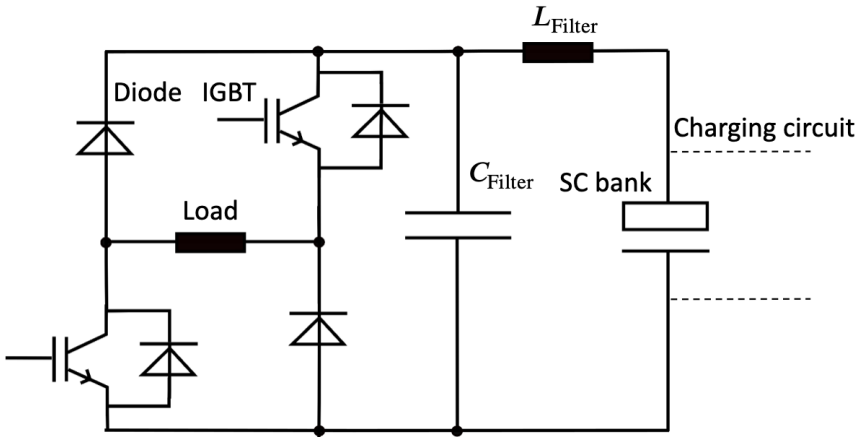

Figure 3.9: PROTO-SPHERA power supply simplified schema: the supercapacitors bank is composed by four modules which can be connected in several configurations; a filter ensures to limit the high frequency content of the supercapacitors current and a H-bridge converter is used to control the load current [34].

The supercapacitors bank is charged with a 10 A charging current provided by an external power supply which is disconnected after the charging phase. The amount of energy to be stored into the supercapacitors E_{SC} can be evaluated by considering that for a rectangular pulse it should cover at least the energy stored into the load inductance plus the dissipated energy during the pulse, which means:

$$E_{SC} > \frac{1}{2} L I_{FT}^2 + R_{eq} I_{FT}^2 T_{FT} \tag{3.7}$$

where I_{FT} and T_{FT} are the flat-top current and duration, while R_{eq} is the equivalent resistance in the power supply circuit. Considering the parameters of this experiment (I_{FT}=2 kA, I_{FT}=2 s, L= 500 μH and R_{eq}= 10 mΩ), the required minimum energy to be stored into the supercapacitors for a pulse is 160 kJ. Four supercapacitors modules (Maxwell BMOD0165P048C01) have been used to achieve up to 764 kJ of stored energy in order to perform even longer pulses (up to 10 s). The available configurations are either the parallel of four modules at 48 V or the parallel of the series of two modules at 96 V. The configuration can be selected by moving the internal bars connecting the supercapacitors, and the controller automatically recognizes the selected configuration. In the circuit an electrical filter is present in order to limit the high frequency content of current drawn by the superacapitors, which could affect their lifetime. The power stage is composed by an H-bridge containing two IGBT and two diodes able to produce the required output currents and voltages. The typical waveform necessary for the experiments consists in a trapezoidal pulse with fast rise/fall times and a long flat-top phase, as shown in Fig. 3.10 where the current has been kept contant at 2 kA for 10 s [34]. This kind of power supply could also be considered for applications such as the ASDEX Upgrade TF coil, but taking into account the high risk of failure of the device if scaled-up to large size. With a single fault of a supercapacitors module or a switch indeed, the experiment would fail.

DTT poloidal field power supply

The Divertor Tokamak Test (DTT) facility [10] is a large fusion experiment expected to provide relevant contributions to ITER and DEMO by investigating the problem of the power exhaust, namely of the elements produced by the plasma processes and directed outside the confinement region through the divertor [35]. DTT has six modules composing the central solenoid and six poloidal magnets, all superconductive and supplied by independent circuits via supercapacitors. Fig. 3.11 shows a typical power supply circuit connected to a poloidal field coil: an external charger charges the supercapacitors bank up to the required voltage (depending on the energy need), a chopper is used to protect them in case of overvoltage (induced by reverse energy flow from coil side) and a filter limits the high frequency content of the current; the power stage is composed by a IGBT full-bridge which controls the current injected into the coil. A crowbar is present to by-pass IGBT and load coil in case of fault, while a switching network unit (SNU) and

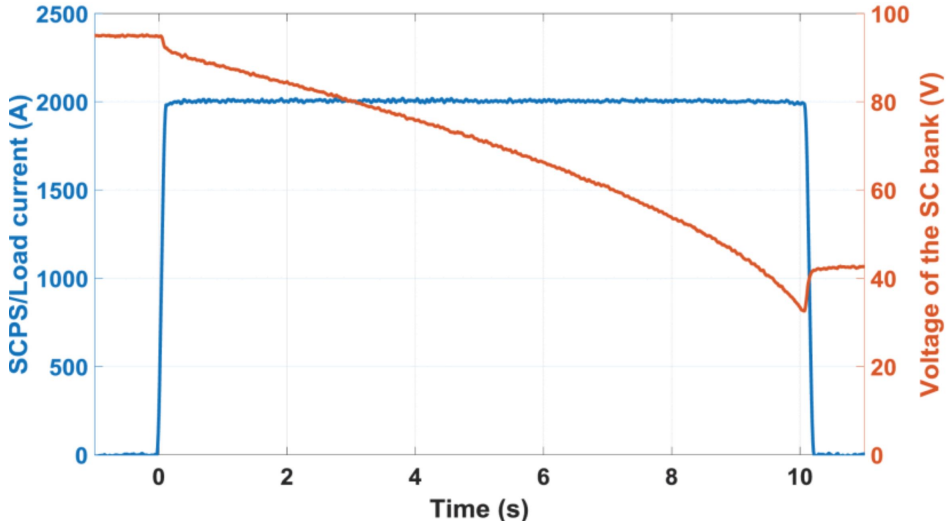

Figure 3.10: PROTO-SPHERA typical experiment: the current is ramped-up at 2 kA, kept constant for the flat-top phase (10 s in this case), and finally ramped-down again [34].

a fast discharge unit (FDU) are used to generate an overvoltage of about 3 kV at the plasma breakdown and to insert a resistor in the circuit if emergency discharge of the coil is necessary (e.g. quenching of the coil) [35].

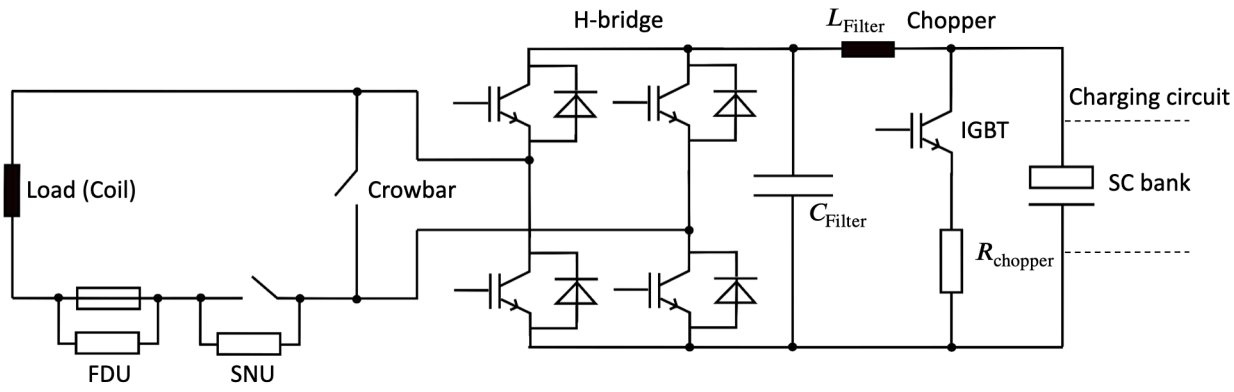

Figure 3.11: DTT poloidal filed coils typical power supply circuit: a charger is used to reach the required voltage level at the supercapacitors bank terminals; a chopper and a filter are present to preserve the lifetime of the supercapacitors, while the IGBT full-bridge controls their output current. A switching network and a fast discharge units finally ensure a proper voltage level during plasma breakdown and a safe discharge path for the inductive energy of the coils in case of fault. [35].

This topology allows to give back the power to the supercapacitors bank by recharging

them also during the operating period. The energy to be stored into the supercapacitors can be estimated in the same way of the previous example with the addition of the SNU losses to be taken into account. This topology as for the case of PRTO-SPHERA is a promising solution for future fusion applications, but it would not fit the requirements of ASDEX Upgrade TF coil: in this case the 16 toroidal field coils are in series and supplied by the same power supply, which means that it is not possible to supply them individually; furthermore, as for the previous example, in case of fault of any component of the circuit the experiment has to be aborted. A solution that could replace a flywheel generator at IPP has to be capable to continue the operation even in case of local small faults, due to the importance of the experiments conducted and the much higher involved stored energy. A single fault could have catastrophic consequences if the whole stored energy would be discharged into the fault within short time (e.g. short circuit of a cell).

3.4 The modular multilevel converter

The MMC has received considerable attention since the beginning of this century and it has become one of the most attractive converters for high-power applications such as high-voltage DC (HVDC) converters [36]-[37], STATCOM [38]-[39], railway power supplies [40]-[41], but also fusion devices' power supplies. This converter, thanks to the discrete-leveled output voltage and its identical submodules by which it is composed, represents a promising alternative to replace the flywheel generator EZ2 that actually provides electrical power to ASDEX Upgrade's TF coil.

3.4.1 The topology

The generalized circuit configuration of a three-phase MMC is shown in Fig. 3.12. The DC system of an MMC is usually called DC-bus or DC-link, and it is connected across the positive and negative bars of the converter legs (or phase units). The three-phase AC system is connected to the midpoint of each converter leg (a, b, and c). Each leg of the MMC is divided into two arms: the arms connected to the positive bars are called upper arms (u), while the arms connected to the negative bars are called lower arms (l). Each arm consists of a series connection of n submodules and an arm inductor (L_{arm}). The arm inductor helps to limit the inrush current caused by the instantaneous voltage difference between the arms and it decouples arm operations. The main advantages of the MMC are its modular structure with identical modules, the scalable output voltage and the distributed stored energy, while the main challenge of realizing this converter comes from the high number of semiconductor switches involved, which leads typically to a complex controller.

The MMC can be realized using different submodules among the several existing types

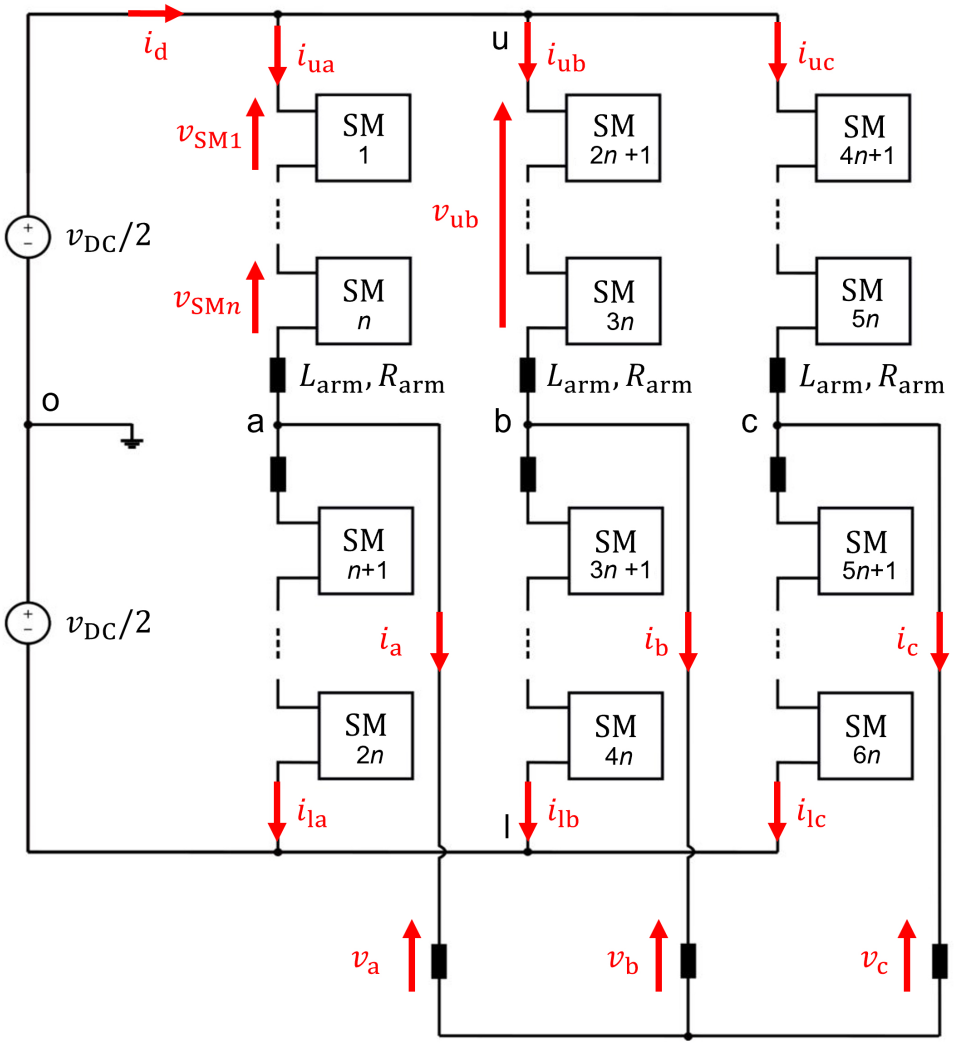

Figure 3.12: Conventional MMC topology for 3-phase loads [42].

to meet the application requirements, but the most popular and widely used submodule configurations are the half-bridge and the full-bridge ones, as shown in Fig. 3.13. The half-bridge submodule is composed of two IGBT and a submodule capacitor, and it is mainly used for the MMC-HVDC transmission lines. Its simple construction results in a simple control and design. During its normal operation, only one semiconductor device is in “ON” state. Hence, the half-bridge submodule has half conduction losses and thus higher efficiency. Its main drawback is that its output voltage can assume positive voltage levels (0 and v_C, see Tab. 3.2) solely and cannot support the bipolar operation. The full-bridge submodule is also known as H-bridge circuit and its configuration is shown in Fig.3.13. This configuration requires twice the number of semiconductor devices as

compared with the previous one for the same voltage rating but the control and design complexity are similar. Two devices carry the submodule current during the normal operation, resulting in a higher device power loss and lower efficiency, however this configuration can generate three voltage levels: 0, v_C and -v_C (see Tab. 3.3).

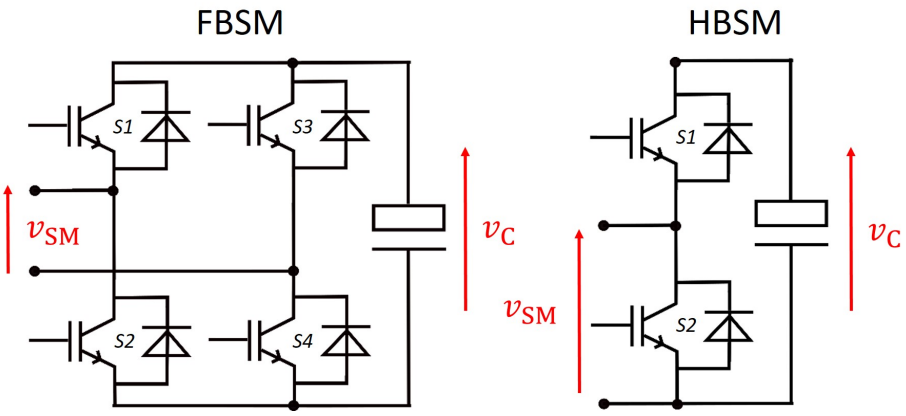

Figure 3.13: MMC most used submodule configurations: the full-bridge submodule (FBSM) has four IGBT (S1,...S4), a four-quadrant operation and it can handle an internal fault with its own switches but its semiconductor losses are double than the half-bridge submodule (HBSM) [42].

SM State	S1	S2	v_{SM}	S
State 1	1	0	v_C	1
State 2	0	1	0	0
State 0	0	0	-	-

Table 3.2: Half-bridge submodule states: this configuration can generate only positive (State 1) or zero (State 2) output voltage (2-quadrant operation).

Furthermore, the full-bridge submodule does not require any additional safety switch being provided with four switches; this is not the case for the half-bridge, where in case of fault of one of its two IGBT, it could not be disconnected from its arm. In order to keep the converter as simple as possible but at the same time safe and reliable, only the full-bridge configuration has been considered for the proposed converter for ASDEX Upgrade's TF coil.

3.4.2 Fundamental equations

The submodules of each phase can be grouped into two blocks with voltages v_{uk} (upper arm) and v_{lk} (lower arm), where k=a, b or c (see Fig. 3.12). The capacitor of each

SM State	S1	S2	S3	S4	v_{SM}	S
State 1	1	0	0	1	v_C	1
State 2	0	1	0	1	0	0
State 3	1	0	1	0	0	0
State 4	0	1	1	0	-v_C	-1
State 0	0	0	0	0	-	-

Table 3.3: Full-bridge submodule states: this configuration can generate positive (State 1), negative (State 4) or zero (State 2 and State 3) output voltage (4-quadrant operation); the capability to by-pass the submodule capacitor with two different states allows a well distributed power dissipation leading to a longer lifetime of the semicondutor devices.

submodule is kept charged with a voltage equal to $V_{DC}/2$ divided by the number of submodules per arm n:

$$v_C = \frac{V_{DC}}{2n} \tag{3.8}$$

The equation relating the AC output voltage can be obtained through both upper and lower arm equations:

$$v_k = \frac{V_{DC}}{2} - v_{uk} - L_{arm}\frac{di_{uk}}{dt} \tag{3.9}$$

$$v_k = -\frac{V_{DC}}{2} + v_{lk} + L_{arm}\frac{di_{lk}}{dt} \tag{3.10}$$

where v_k is the load voltage over the k^{th} phase. Resistances of the circuits have been neglected for simplicity. The arm voltages v_{uk} and v_{lk} depend on the conduction states S_{ukj} and S_{lkj} of their respective submodules and on their capacitor voltages v_{Ckj}:

$$v_{uk} = \sum_{j=1}^{n} S_{ukj} v_{Cukj} \tag{3.11}$$

$$v_{lk} = \sum_{j=n+1}^{2n} S_{lkj} v_{Clkj} \tag{3.12}$$

Arm currents (i_{uk} and i_{lk}) are equal to half of the respective phase current i_k plus a third of the DC current i_d and the so called circulating current i_{zk}:

$$i_{uk} = \frac{i_k}{2} + \frac{i_d}{3} + i_{zk} \tag{3.13}$$

$$i_{lk} = -\frac{i_k}{2} + \frac{i_d}{3} + i_{zk} \tag{3.14}$$

The circulating current can be therefore calculated as follows:

$$i_{zk} = \frac{i_{uk} + i_{lk}}{2} - \frac{i_d}{3} \tag{3.15}$$

and the sum of the three circulating currents is zero:

$$i_{za} + i_{zb} + i_{zc} = 0 \tag{3.16}$$

The output voltage of each AC phase can assume $4n + 1$ ($2n + 1$ in the case of the half-bridge submodule) different values, depending on the amount of enabled submodules [43].

3.4.3 Single-phase MMC

The single-phase MMC is a simplified version of the three-phase one and its structure is shown in Fig. 3.14. The main circuit consists of a phase leg and two DC side voltage sources. The phase leg consists of an upper and lower arm, where each arm comprises n series-connected submodules and one arm inductor. The middle point (o) of the DC side voltage sources is connected to the ground. Both the middle point of phase leg (a) and of DC side sources constitute the AC electrical interface, which can either be connected to an external grid or an AC load [44]. Assuming that the only phase is the phase 'a' of the three-phase version, $i_d = i_u$ with $i_u = i_{ua}$ (and $i_l = i_{la}$) and $i_a = i_{Load}$. The capacitors voltage is still $V_{DC}/2$ divided by the number of submodules per arm n:

$$v_C = \frac{V_{DC}}{2n} \tag{3.17}$$

while the load voltage can be obtained by upper and lower arms equations again:

$$v_{Load} = \frac{V_{DC}}{2} - v_u - L_{arm}\frac{di_d}{dt} \tag{3.18}$$

$$v_{Load} = -\frac{V_{DC}}{2} + v_l + L_{arm}\frac{di_l}{dt} \tag{3.19}$$

where v_{Load} is the load voltage.

The arm voltages v_u and v_l depend on the conduction states S_{uj} and S_{lj} of their respective submodules and on their capacitor voltages v_{Cj}:

$$v_u = \sum_{j=1}^{n} S_{uj} v_{Cuj} \tag{3.20}$$

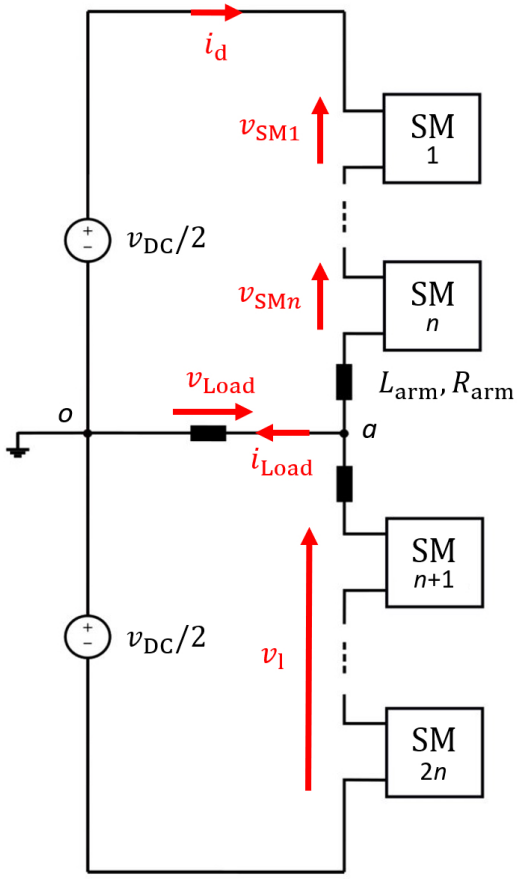

Figure 3.14: MMC simplified cicuit for a single-phase AC load [44].

$$v_l = \sum_{j=n+1}^{2n} S_{lj} v_{Clj} \tag{3.21}$$

The load current i_{Load} can be finally expressed as follows:

$$i_{Load} = i_u + i_l = i_d + i_l \tag{3.22}$$

and in this case no circulation current is present. The reason why a brief desciption of the single-phase MMC has been given is that the converter proposed in this dissertation is a revised version of it: in particular, as it will be shown in the next chapter, the main change consists in using several parallel arms to increase the amount of energy that can be stored into the submodules as well as the total output current. Another difference consists in avoiding the usage of any large DC-link system, while using the submodules capacitors as distributed energy storage systems.

4 The proposed MMC-like topology for ASDEX Upgrade TF coils

4.1 The concept

The converter proposed in this chapter is a revised version of the single-phase MMC shown in the previous one. It has to be fault-tolerant, which means that in case of fault of one or more submodules it has to be able to recognize the fault and isolate it from the other submodules in order to finish the experiment. On the other hand it has to be possible to scale the device to any size without changing control, communcation protocol and/or submodule design.

4.1.1 Topology description

Since the first prototype has been built for ASDEX Upgrade's TF coil – a DC constant load - the single-phase MMC has been further simplified as shown in Fig. 4.1. The converter consists of a n x m matrix of submodules, where n and m are the number of modules in series and in parallel, respectively. In particular the converter can be subdivided in m 'arms' ($SM_{1.1} - SM_{1.n}$, $SM_{2.1} - SM_{2.n}$...$SM_{m.1} - SM_{m.n}$) and n 'rows' ($SM_{1.1} - SM_{m.1}$, $SM_{1.2} - SM_{m.2}$...$SM_{1.n} - SM_{m.n}$). Submodules were initially intended to be half-bridge type - which would be theoretically sufficient for DC loads - but in order to increase the flexibility of the topology and make it suitable for AC loads, the full-bridge submodule configuration has been chosen. This choice is optimal also in terms of reliability: in case of any submodule internal fault (e.g. fault of an IGBT switching) it can still be by-passed thanks to the other available half-bridge without affecting the operation of the whole submodules matrix, which would not be possible with the half-bridge configuration. In this way the converter can safely operate and failed submodules can be replaced directly after the operation. The main objective of the converter is to generate a constant output current of 54 kA for about 10 s every 15-20 min (dwell time). The supercapacitor modules are charged at their nominal voltage with a low charging current within the dwell time, after which the matrix is ready for the next pulse. The charging process is described in detail in Ch. 4.1.3.

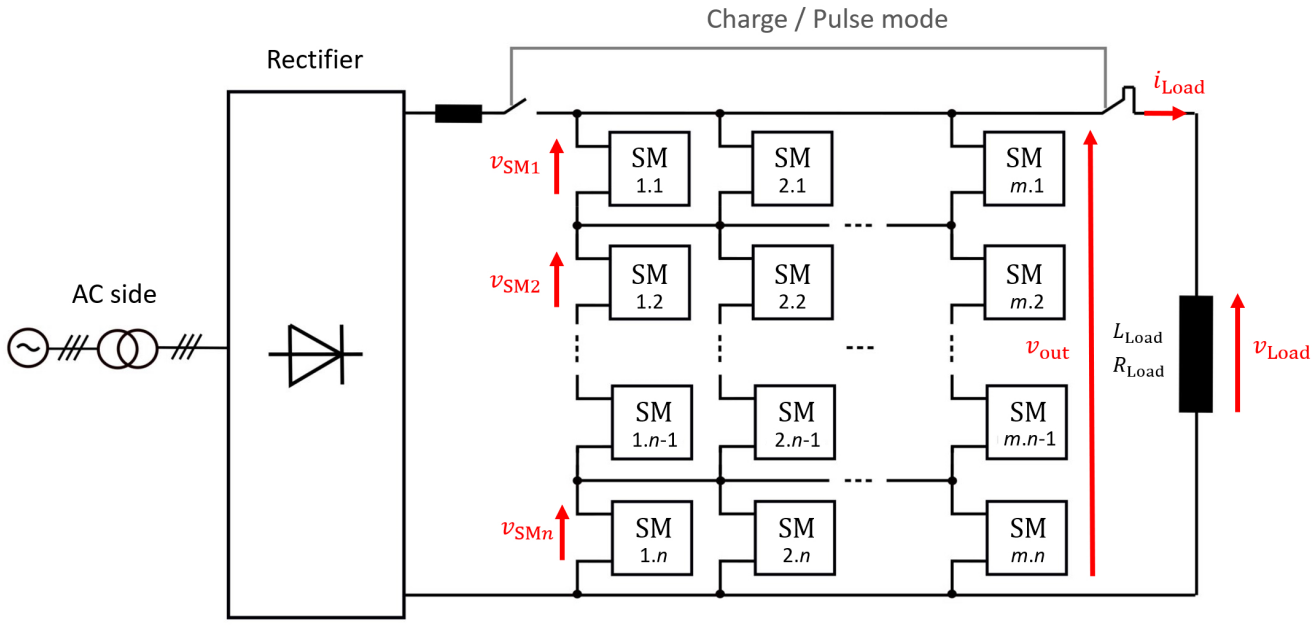

Figure 4.1: Revised MMC for the ASDEX Upgrade TF coil pulsed power supply system.

During a pulse ramp-up and ramp-down phases duration is limited to reduce losses by applying all the available voltage (about 3 kV when supercapacitors are charged), while during the 10 s of the flat-top phase the current may have a ripple that must not exceed the 0.1% of its nominal value (Δi_{max}=54 A) [27]. This value directly depends on the voltage difference (Δv) among converter' s output voltage v_{out} and load resistive voltage drop v_{rl} ($v_{Load} = v_{rl} + v_{ll}$), on the load inductance L_{Load} and on the switching frequency f_{sw} of the converter. Submodules belonging the same rows are synchronized in order to simplify the control (see next sections) and they have same output voltage, thus v_{out} can be expressed as:

$$v_{out} = \sum_{j=1}^{n} v_{SMj} = \sum_{j=1}^{n} S_j v_{SCj} \tag{4.1}$$

The current ripple can be therefore estimated as follows:

$$\Delta i_{Load} = \frac{\Delta v}{L_{Load} \cdot f_{sw}} = \frac{v_{out} - v_{rl}}{L_{Load} \cdot f_{sw}} = \frac{\sum_{j=1}^{n} S_j v_{SCj} - v_{rl}}{L_{Load} \cdot f_{sw}} \tag{4.2}$$

Eq. 4.2 overestmiates the load current ripple since the converter does not produce the same output voltage for a full period. However as a worst-case scenario the "ON-time" has been approximated with the switching period $T_{sw} = \frac{1}{f_{sw}}$ validating Eq. 4.2. Since L_{Load} is constant (120 mH) and Δv depends on the supercapacitors' modules voltage, the current

ripple can be reduced by increasing the switching frequency of the converter. Considering the maximum Δv as a worst case during the first milliseconds of the flat-top (during the operation it decreases due to the discharge of the supercapacitors) an output switching frequency of 50 Hz would ensure the current ripple to not exceed 50 A. The inductive energy stored into the TF coil during the pulse ($0.5 \cdot L_{\text{Load}} \cdot i^2_{\text{Load}}$) can be recovered by the supercapacitor modules thanks to the 4-quadrant operation of the full-bridge submodules. A preliminary estimation of the total amount of submodules required to fulfill the TF coil requirements in terms of energy, voltage and current leads to about 1500 submodules needed. However, for this calculation circuit losses have been neglected and it can not be considered realistic. Only after having designed roughly the main components (submodule superapacitors module, power stage filter...) a second estimation could be made including all relevant losses leading to about 2200 total modules required (n=23, m=96). n is limited by the maximum isolation voltage of the TF coil (3 kV), while m has been defined depending on energy and current contraints. The precise calculation is shown in Ch. 6.2 since the parameters required for it are described during the next two chapters.

4.1.2 Submodule configuration

As mentioned already, the chosen submodule configuration is the full-bridge one, introduced in Ch. 3.4.1. The adopted circuit is however slightly different from the ideal one and it is shown in Fig. 4.2. The submodule is mainly composed by four IGBT with integrated antiparallel diodes (S_1-S_4), a supercapacitor module and a power stage LC filter. Depending on the toggled IGBT, both v_{SM} and i_{SM} can be either positive, zero or negative (see Tab. 3.3). The supercapacitor module is represented as a RLC circuit and the LC filter has two main functions: the first one is to protect both IGBT and supercapacitors from overvoltages during transients, while the second purpose consists in reducing the high frequency content of i_{SC} which could reduce the module' s lifetime.

The power stage filter

In order to protect supercapacitors, the filter capacitance has to be large enough to compensate the energy stored into the inductances of the circuit (mainly ESL in this case). When a switching event occurs indeed, the energy stored into ESL has to discharge somewhere and if no filter capacitor is present this energy causes an overvoltage over power stage and supercapacitor module. By adding a filter capacitor this excess of energy can be overtaken by it limiting voltage spikes. C_{Filter} value can be therefore estimated by applying the energy equilibrium formula:

$$\frac{1}{2} \cdot C_{\text{Filter}} \cdot v^2_{\text{Cf}} = \frac{1}{2} \cdot ESL \cdot i^2_{\text{SC}} \tag{4.3}$$

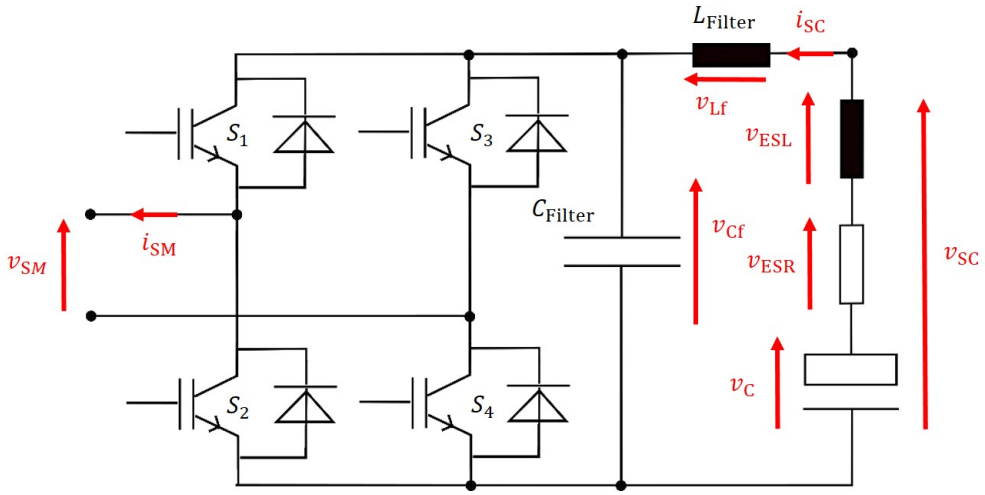

Figure 4.2: Proposed submodule simplified circuit: the power stage filter is required to protect IGBT and supercapacitors modules especially during transients.

where v_{Cf} is the voltage over the filter capacitor. This leads to:

$$C_{\text{Filter}} = \frac{ESL \cdot i_{\text{SC}}^2}{v_{\text{Cf}}^2} \tag{4.4}$$

which is the minimum value of capacitance needed. If C_{Filter} is so large to require many capacitors in parallel or electrolytic capacitors, additional stray inductances will be added (by the components) to the circuit and a second (or even more) capacitive filter stage closer to the IGBT may be required. In order to reduce as much as possible unwanted stray inductances during the design phase it is important to place phisically the capacitors as close as possible to the power stage, reducing therefore the area of the current path. The filter inductance L_{Filter} is used to decouple the supercapacitors module from the power stage. According to the circuit shown in Fig. 4.2, the following expressions can be derived:

$$v_{\text{Cf}} = v_{\text{Lf}} + v_{\text{ESL}} + v_{\text{ESR}} + v_{\text{c}} \tag{4.5}$$

$$v_{\text{Lf}} = L_{\text{Filter}} \cdot \frac{\mathrm{d}i_{\text{SC}}}{\mathrm{d}t} \tag{4.6}$$

Taking into account Eq. 3.4 and combining it with the equations above, v_{Cf} can be expressed as:

$$v_{\text{Cf}} = v_{\text{SC}} + L_{\text{Filter}} \cdot \frac{\mathrm{d}i_{\text{SC}}}{\mathrm{d}t}. \tag{4.7}$$

Eq. 4.16 shows that the introduction of L_{Filter} leads to an increase of v_{Cf} during switching events which is also seen at the terminals of IGBT. If this is taken into account during the design phase it will not cause any damage. On the other hand, the main reason why L_{Filter} has been introduced is that it slows down i_{SC} variation and, according to Eq. 3.5, it reduces v_{ESL} (and v_{SC}) during transients, decoupling power stage and the supercapacitor module. The formed *LC* circuit indeed is a low-pass filter and it filters out the supercapacitor module's harmonic content with a frequency higher than the cut-off frequency f_{co} defined as:

$$f_{\text{co}} = \frac{1}{2\pi\sqrt{L_{\text{Filter}}C_{\text{Filter}}}}. \tag{4.8}$$

Submodule internal losses

Another important aspect to take into account during the design of a submodules is the internal power loss p_{SM}. Most of the submodule losses are generated by the supercapacitor module, the filter inductor and the IGBT. Supercapacitors losses have been already described in Ch. 3.3.2 and they can be estimated via Eq. 3.6. The filter inductor has an equivalent series resistance R_{Filter} (not shown in the ideal circuit of Fig. 4.2, but represented in the realistic circuit of Fig. 5.4) and its losses directly depend on it:

$$p_{\text{Filter}} = R_{\text{Filter}} \cdot i_{\text{SC}}^2. \tag{4.9}$$

IGBT power losses are composed by the sum of two terms: the switching losses p_{sw} and the conduction losses p_{c}. The switching losses depend on the switching frequency f_{sw}, on the collector-emitter voltage of the IGBT V_{CE} ($=v_{\text{SC}}$), on the collector current I_{C} ($=i_{\text{SM}}$) and on the IGBT switching time t_{s} which is the sum of the times required by the IGBT for the ON-OFF transition and vice versa. Therefore, the term p_{sw} can be estimated as:

$$p_{\text{sw}} = \frac{1}{2} \cdot v_{\text{SC}} \cdot i_{\text{SM}} \cdot t_{\text{s}} \cdot f_{\text{sw}}. \tag{4.10}$$

The conduction losses depend on i_{SM}, on the IGBT collector-emitter ON voltage $V_{\text{CE,ON}}$ and on the duty cycle D of the single power switches. In this specific case, since the full-bridge is composed by four IGBT and at each time instant two of them are ON, the conduction losses can be estimated as:

$$p_{\text{c}} = 2 \cdot V_{\text{CE,ON}} \cdot i_{\text{SM}}, \tag{4.11}$$

where $V_{\text{CE,ON}} = V_{\text{CE,0}} + I_{\text{C}} \cdot R_{\text{CE}}$ is the collector-emitter ON voltage and it depends on the IGBT collector-emitter internal resistance (R_{CE}), current and operating temperature. V_{CE} does not need to be calculated since usually manufacturers provide on the component datasheet $I_{\text{C}} - V_{\text{CE}}$ curves for different operating temperatures.

Eq. 4.11 is valid for the full-bridge operation of the described submodule and it is the result of considering two switches always ON. Depending on the state of the submodule, the current can flow through two IGBT, one IGBT and one diode, or two diodes. Conduction losses of diodes are lower than the ones of IGBT (lower $V_{CE,ON}$). However - to be on the safe side in terms of losses estimation - for Eq. 4.11 two IGBT always ON have been considered. The total amount of power losses of a single submodoule can be therefore expressed as:

$$p_{SM} = p_{SC} + p_{Filter} + p_{sw} + p_c. \tag{4.12}$$

This parameter has to be kept into account during the design of the total amount of submodules required for the converter since p_{SM} consumes a certain amount of energy which has to be added on the top of total energy requirements. Since p_{SM} can significantly change depending on the lifetime of the supercapacitors (ESR) and temperature conditions, different losses scenarions have been analyzed and are shown in Ch. 6.1.

4.1.3 Charging process

The charging process is divided into two phases: the Pre-Charging Phase (PCP) and the Boost-Charging Phase (BCP). The first one is realized thanks to a low power step-down converter, used as pre-charger. The pre-charging can be achieved in different ways, depending on the available pre-charging time and on the charger power. If the rows are individually charged (see Fig. 4.3 (a)), each row is charged at the pre-charger voltage v_{PC} which has to be at least v_i/n, where v_i is the rectifier output voltage. On the other hand, if all the rows are charged simultaneously (see Fig. 4.3 (b)), the pre-charger voltage v_{PC} has to be at least as high as v_i. This method therefore would require a pre-charger with a higher power (assuming the same charging current i_{PC}). i_{PC} can be chosen as low as possible depending on the available time for the pre-charging phase. However an important constraint to take into account is the leakage current of the supercapacitor modules i_{epr}: this parameter depends on the equivalent parallel resistance (EPR) of the supercapacitor modules and it is the main cause of their self-discharging. If i_{PC} would have the same value of i_{epr}, the pre-charging time would be infinite, and for this reason i_{PC} should be at least one order of magnitude larger than i_{epr}. The chosen supercapacitor module has an average I_{epr}=1 mA, meaning that i_{PC} should never be lower than 10 mA.

v_i has an upper hard limit given by the minimum voltage level reached at the end of each pulse by the whole submodules matrix. This limit is the main constraint to take into account when rating the input rectifier and can be expressed as:

$$v_i < n \cdot v_{SCeop} \tag{4.13}$$

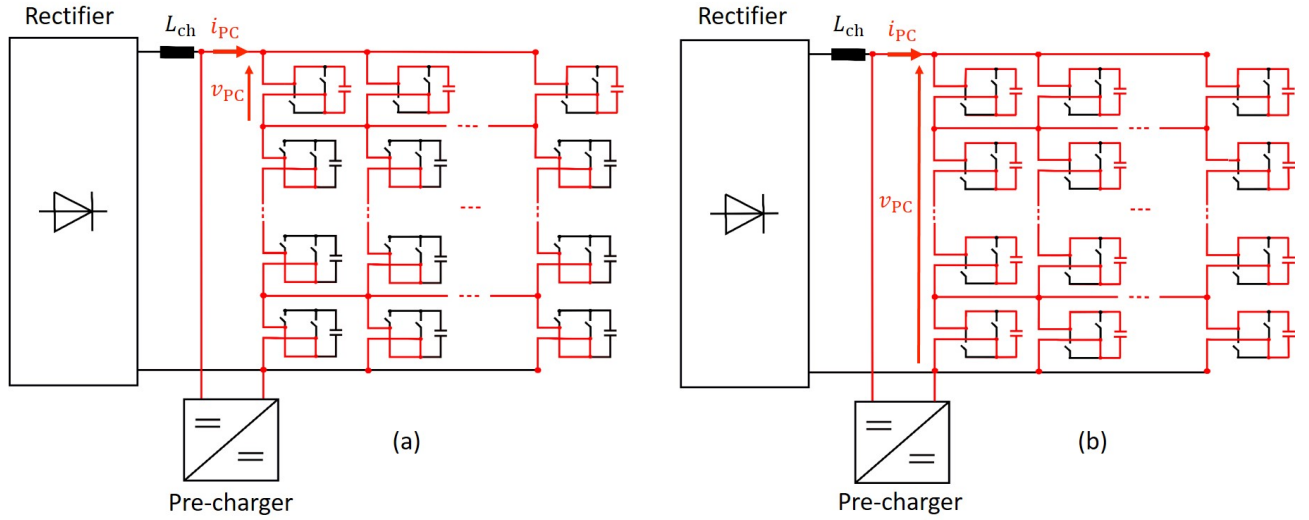

Figure 4.3: Pre-charging phase: this phase is required to charge the supercapacitor modules at the mimum voltage required by the boost-charging phase. Considering the rectifier output voltage v_i=800 V, the pre-charger should have an output voltage of 38 V (see Eq. 4.14) if each row is charged individually (a) or 800 V if all the supercapacitors are charged together (b). The charging current has to be at least one order of magnitude larger than the leakage current of the supercapacitors in order to avoid to end up in an infinite pre-charging time. In order to keep the schema clear IGBT and supercapacitor modules symbols used in this picture have been simplified to standard switches and capacitors, respectively.

where v_{SCeop} is the average voltage of the supercapacitor modules at the end of a pulse. In order to make the system as efficient as possible, $n \cdot v_{SCeop}$ has to be higher (but as close as possible) the load voltage drop, which is the minimum voltage required to control the load current. According to the resistive voltage drop of the TF coil of about v_{rl}=800 V, the minimum v_{SC} can be estimated as:

$$v_{SCmin} = \frac{v_{rl}}{n} = \frac{800\ \text{V}}{23} = 35\ \text{V} \tag{4.14}$$

In order to be able to control the load current however the converter should be able to provide at least one voltage level above 800 V. Furthermore an additional voltage level is required in case of failure of one row and during steady state operation the submodules can provide at the output only 90% of the supercapacitors voltage (due to internal losses, see Ch. 4.1.2 and 6.1). Therefore v_{SCmin} can be estimated as:

$$v_{SCmin} = \frac{v_{rl} + v_{SCmin} + 10\% v_{SCmin}}{n-1} = 38\ \text{V} \tag{4.15}$$

which means that v_i should never exceed $22 \cdot v_{SCmin}$=840 V. For this reason v_i=800 V

has been chosen, and it is also the minimum voltage required by the submodules matrix in order to start the boost-charging phase. However, considering the ASDEX Upgrade application, if the supercapacitor modules have to be pre-charged at the beginning of each operating day, a I_{PC}= 10 A would ensure to achieve the required v_i by charging the row individually in less than two hours.

During the boost-charging phase instead (see Fig. 4.4), supercapacitor modules are charged up at their full voltage with a step-up converter-based charger realized by the help of the submodule' s IGBT power stage: this means that apart from the (low power) pre-charger, the charging process, as for the pulse phase, is controlled via the single submodules in a distributed way, such that scalability is ensured without any need of hardware modifications. During the boost-charging phase indeed an inductor (which also limits the slope of the charging current) first stores energy and then uses it to charge supercapacitors. In order to transfer inductor's stored energy into supercapacitors, the current variation over the time must be negative. The voltage across the inductor is:

$$v_{Lch} = v_i - v_{out} \tag{4.16}$$

where v_{out} is the output voltage of the charger and it must be higher than the input voltage v_i . If v_{out} would be lower than v_i, i_{ch} would rise in a uncontrolled way. Therefore, when the boost-charging phase starts v_{out} must be already at a higher level than v_i and this is the reason why the pre-charging phase is required.

An example of pre-charger can be provided considering the voltage and current as constraints. I_{PC}=10 A is the lowest value that ensures to pre-charge the modules in less than two hours, while 38 V/row is the minimum value to achieve v_{out}=840 V (assuming a rectifier with v_i=800 V) for the boost-charging phase (with 23 rows). With the chosen values the total current required from the pre-charger is I_{PC}=61·10 A = 960 A, which multiplied with the voltage (38 V if rows are charged one by one) provides the minimum power required from the charger P_{PC}=36 kW. This is only an example of pre-charger design, but depending on the wanted charging current and rectifier voltage its size can significantly change. Once all the rows have reached the required v_{SCmin}, the pre-charger can be disconnected and the boost-charging phase can be initiated a few minutes before the first experiment. It is important to mention that even though the pre-charging phase can last about two hours, it is required only when supercapacitors have to be charged from a voltage lower than v_{SCmin}. As it will be shown later, during typical experiments supercapacitors modules are never discharged below v_{SCmin} between consecutive pulses, meaning that apart from the first charging only the boost-charging phase (a few minutes long) is usually required. The main constraints for the boost-charging phase are the available grid power and the charging time: the first one is limited at 5 MW (maximum available power from the IPP AC grid for EZ2) and the second one must fit within the dwell time of 15 min; setting the charing current to I_{ch}=5.9 kA (97 A per arm) and an input voltage of 840 V (38 V·23 rows) the total charging power for the boost-charging

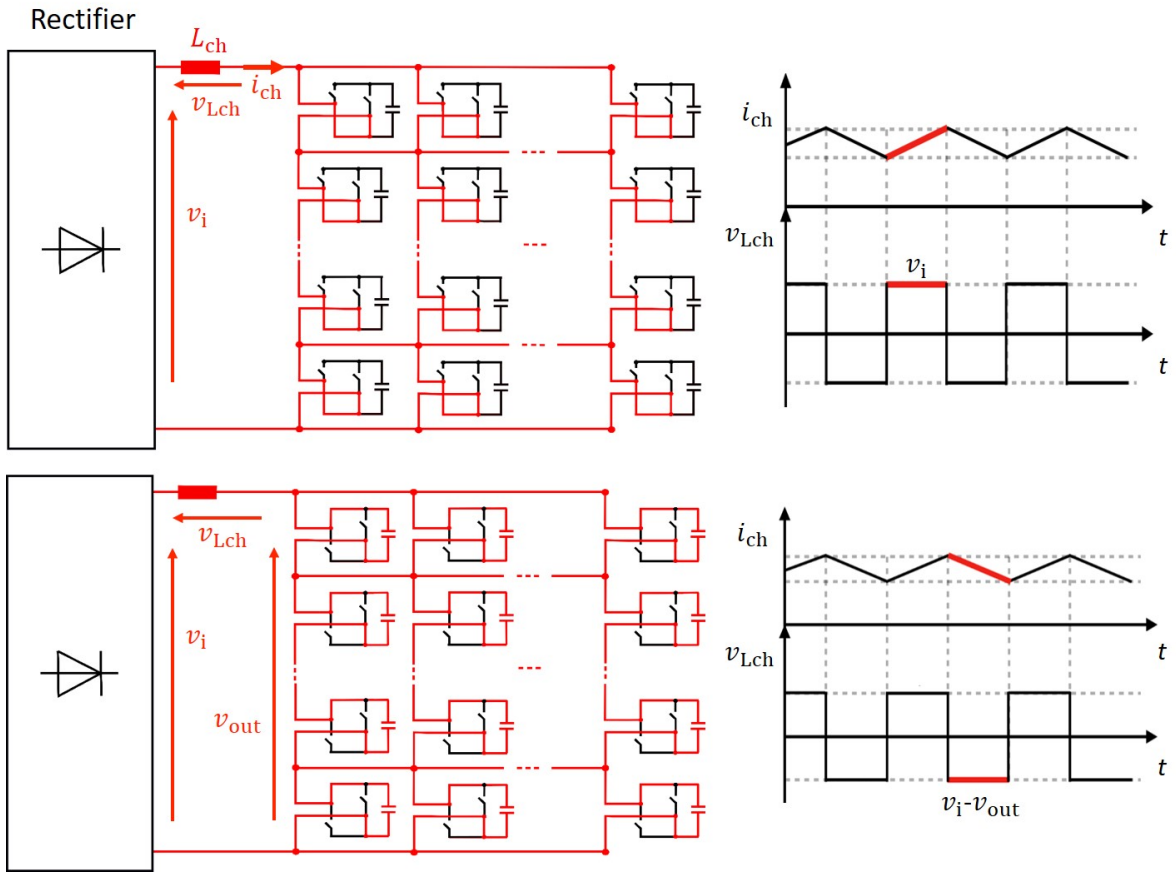

Figure 4.4: Boost-charging phase: the charger inductor first stores energy and uses it than to charge the supercapacitor modules, as in a step-up converter. During the second half of each period, the charging current decreases only if $v_i - v_{out}$ is negative, otherwise it would rise in an uncontrolled way. This is the main reason why this charging phase can start only if the supercapacitors have been charged at $v_{out} \geq v_i$ by the pre-charger.

phase would be exactly 5 MW. Some simulations have been performed in PLECS (shown in [27]) and demonstrated that less than 10 min are required for the boost-charging phase, which fits the actual requirements of ASDEX Upgrade's TF coil.

4.2 The control strategy

4.2.1 The current control

The adopted control strategy is based on a closed loop current control and it is represented in Fig. 4.5: the load current i_{Load} is measured and compared with a reference current i_{ref}, generating an error e. The error is then used as input for the main current controller

(proportional-integral or PI type [45]) which provides a normalized reference voltage v_{rn} that can be expressed as follows:

$$v_{\mathrm{rn}} = \frac{v_{\mathrm{r}}}{v_{\mathrm{SC}}} \tag{4.17}$$

where v_{r} is the reference output voltage of the converter and v_{SC} is the supercapacitors modules voltage measured in real time.

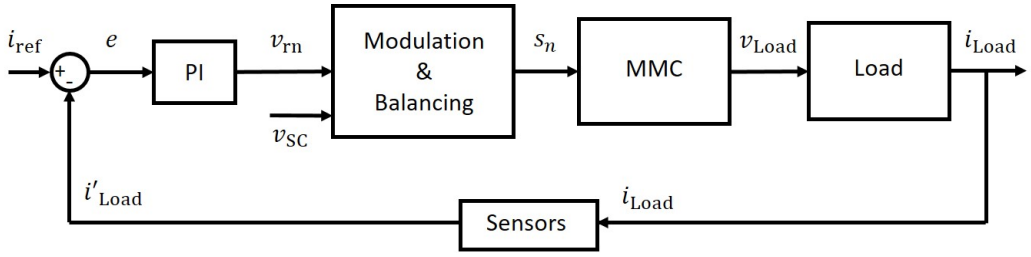

Figure 4.5: Closed-loop control scheme.

The signal v_{rn} is then used as input by the modulation and balancing (MB) control block. This block firstly rounds the signal v_{rn} to the closest integer value in order to define the number of voltage level required (modulation), and then it enables the needed number of submodules depending on their respective supercapacitors module voltages (balancing). According to the real time measurements of i_{Load} and v_{SC}, a Bubble Sort-based algorithm [46] arranges the submodules in ascending/descending order depending on the i_{Load} sign and on the rounded v_{rn}: in this way the first r submodules of the sorted list are selected to be enabled. On the top of this, power stages (IGBT) temperature and error signals are also checked to detect potential overheating or short circuits. Therefore the modulation and balancing control block generates n output signals forwarded to each row. The converter then generates the required output voltage v_{Load} for the load, which generates the requested i_{Load}. The load current is finally measured and a new control cycle takes place. In order to size properly the controller's parameters, it makes sense to switch from time to Laplace domain. The closed loop current control scheme thus can be updated as shown in Fig. 4.6. The transfer function of a PI controller in the Laplace domain can be expressed as:

$$G_{\mathrm{PI}}(s) = \frac{s \cdot k_{\mathrm{p}} + k_{\mathrm{i}}}{s} \tag{4.18}$$

where k_{p} and k_{i} are the proportional and integral constants. In order to estimate these parameters, the open-loop $G_0(s)$ and closed-loop $G_{\mathrm{W}}(s)$ transfer functions of the system are required [47].

$G_0(s)$ can be expressed as:

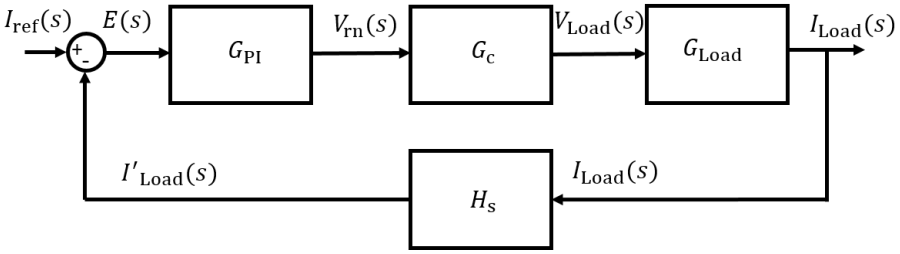

Figure 4.6: Closed-loop control scheme in the Laplace domain.

$$G_0(s) = G_{PI}(s) \cdot G_c(s) \cdot G_{Load}(s) \cdot H_s(s), \tag{4.19}$$

where $G_c(s) = v_{SC}$ includes the MB and MMC blocks (internal delays are neglected), while $G_{Load}(s)$ is the transfer function of the load and can be expressed as:

$$G_{Load}(s) = \frac{1}{R_{Load} + s \cdot L_{Load}}. \tag{4.20}$$

$H_s(s)$ is the current sensors transfer function and it can be modeled as a first order time delay depending on the sensors time constant τ_s:

$$H_s(s) = \frac{1}{1 + s \cdot \tau_s}. \tag{4.21}$$

Therefore $G_0(s)$ is:

$$G_0(s) = \frac{s \cdot k_p + k_i}{s(1 + s \cdot \tau_s)} \cdot \frac{v_{SC}}{(R_{Load} + s \cdot L_{Load})}. \tag{4.22}$$

Once $G_0(s)$ has been defined, $G_W(s)$ can be directly derived from it as follows:

$$G_W(s) = \frac{G_{PI}(s) \cdot G_c(s) \cdot G_{Load}(s)}{1 + G_0(s)} = \frac{\frac{s \cdot k_p + k_i}{s} \cdot \frac{v_{SC}}{(R_{Load} + s \cdot L_{Load})}}{1 + \frac{s \cdot k_p + k_i}{s(1 + s \cdot \tau_s)} \cdot \frac{v_{SC}}{(R_{Load} + s \cdot L_{Load})}}. \tag{4.23}$$

After deriving $G_0(s)$ and $G_W(s)$, k_p and k_i can be derived by imposing the required stability contraints according to Bode criterion which means that $|G_0(j\omega_c)|$ (with $\omega_c = 2\pi f_c$ and f_c as cut-off frequency) and ϕ_m have to be positive. ϕ_m can be expressed as [45]:

$$\phi_m = \arctan\left(\frac{\text{Im}}{\text{Re}}\right)_{Num} - \arctan\left(\frac{\text{Im}}{\text{Re}}\right)_{Den}, \tag{4.24}$$

where *Num* and *Den* are numerator and denominator of $G_0(j\omega_c)$, respectively. Eq. 4.24 allows to identify the k_p/k_i ratio as a function of the phase margin ϕ_m:

$$\frac{k_\mathrm{p}}{k_\mathrm{i}} = \frac{1}{\omega_\mathrm{c}} \cdot \tan\left[\frac{\phi_\mathrm{m} \cdot \pi}{180^\circ} + \arctan\left(-\frac{R_\mathrm{Load}}{\omega_\mathrm{c} \cdot L_\mathrm{Load}}\right)\right] \tag{4.25}$$

By imposing ϕ_m, $k_\mathrm{p}/k_\mathrm{i}$ can be obtained. The second stability constraint can be satisfied by imposing $|G_0(j\omega_\mathrm{c})|=1$, and if combined with result of the first constraint ($k_\mathrm{p}/k_\mathrm{i}$ ratio known) it allows to determine the two PI constants. The Bode plots (see Fig. 4.7) of open-loop and closed-loop transfer functions help to analyze the stability of the system. As it can be seen from the figure, the system is stable since both gain margin and phase margin are positive. The plots have been obtained by using the paramteres shown in Tabs. 4.1 and 4.2.

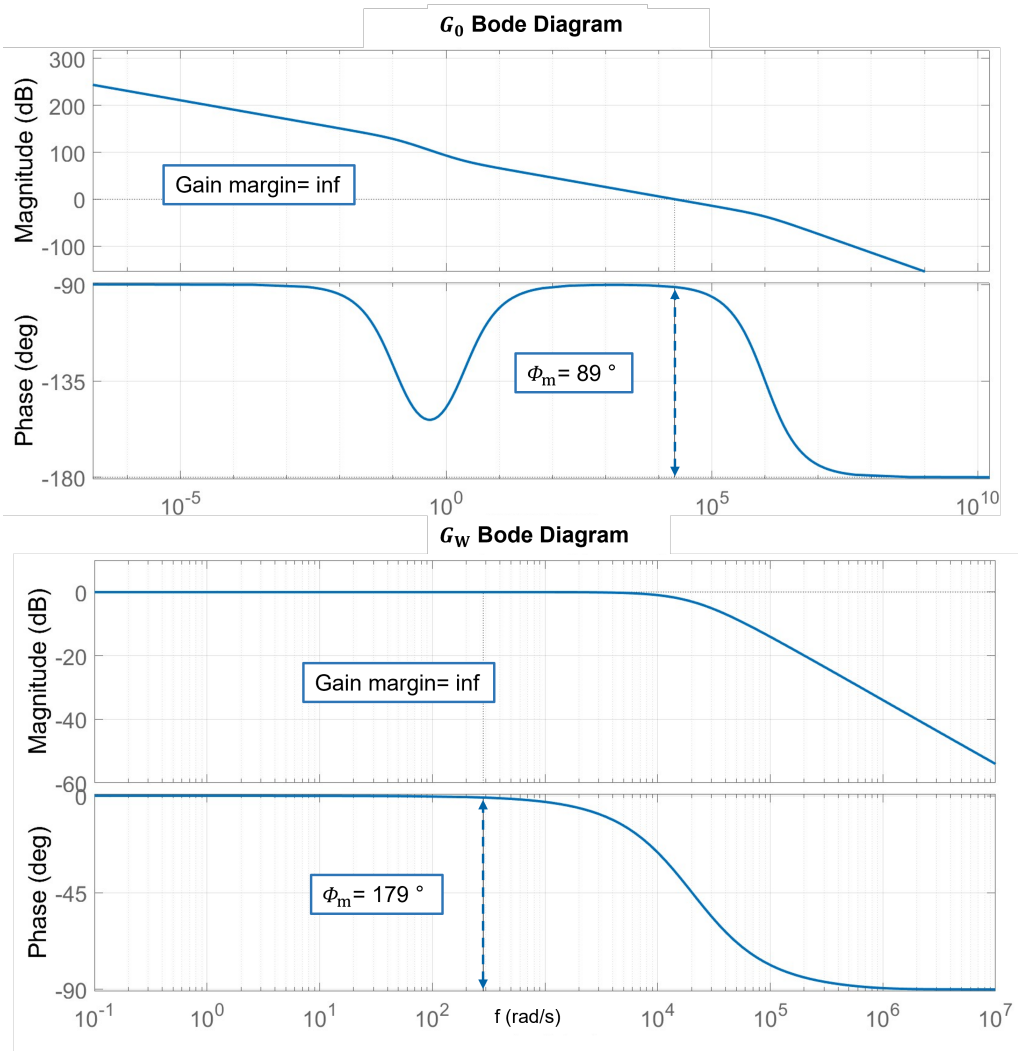

Figure 4.7: Bode plots of open-loop and closed-loop transfer functions. The curves have been obtained with the help of Matlab.

The described control is valid for analog controllers, but in order to implement it on

a digital controller (microcontroller) it must be discretized, and this can be done for example via the Tustin transform [48]. This transform allows to switch from Laplace to z domain:

$$s = \frac{2}{T_s} \cdot \frac{z-1}{z+1} \tag{4.26}$$

where T_s is the sampling period. Combining Eq. 4.26 and Eq. 4.18 the PI transfer function can be rearranged and according to Tustin's method, the continous and discrete time PI functions need to have the same gain, which means $\mathrm{PI}(s)_{|s=0}=\mathrm{PI}(z)_{z=1}$. This leads to a new set of discretized parameters obtained from the continous ones:

$$w_i = \frac{2 \cdot k_{is} \cdot T_s}{2 - k_{is} \cdot T_s}, w_p = \frac{w_i \cdot k_{ps}}{k_{is}} \tag{4.27}$$

where $k_{ps} = k_p$ and $k_{is} = k_i/k_p$, while w_p and w_i are proportional and integral parameters of the discretized controller, respectively. A detailed description of w_p and w_i parameters derivation is provided in [49]. According to the low frequency chosen for the current application (50 Hz), f_c=500 Hz (10 times higher than the switching frequency) and ϕ_m=90° have been chosen to estimate the required w_i and w_p for the different studied cases.

4.2.2 Communication protocol

In order to allow the proposed converter to be scalable and reliable, a communication protocol that can ensure those features is required. Among all the commonly used communication protocols used for the MMC, the EtherCAT protocol has been chosen [50], [51]. An EtherCAT network is composed by a master and usually several slave controllers: the network can be configured in several different ways (ring topology, line topology etc.) depending on the application, but what makes this protocol suitable for this specific application can be summarized in three main features:

- *Redundancy*: the information are sent from the master controller via two independent communication paths; they are equal but opposite in direction. In case of failure of any node of the network, the information is still able to return to the master controller.

- *Synchronization*: the EtherCAT protocol supports the so-called 'Distributed Clocks method' [52]: during the initialization of the network all the jitters are measured and compensated. In this way all the slave controllers can switch simultaneously with a residual latency in the range of 10-50 ns, which is much faster than the switching speed of the power stage.

- *Scalability*: an EtherCAT network can be made of up to 64000 terminals, which means that the developed network and control prototyped on small-scale devices can be later extended to large-scale devices without any need to be significantly changed.

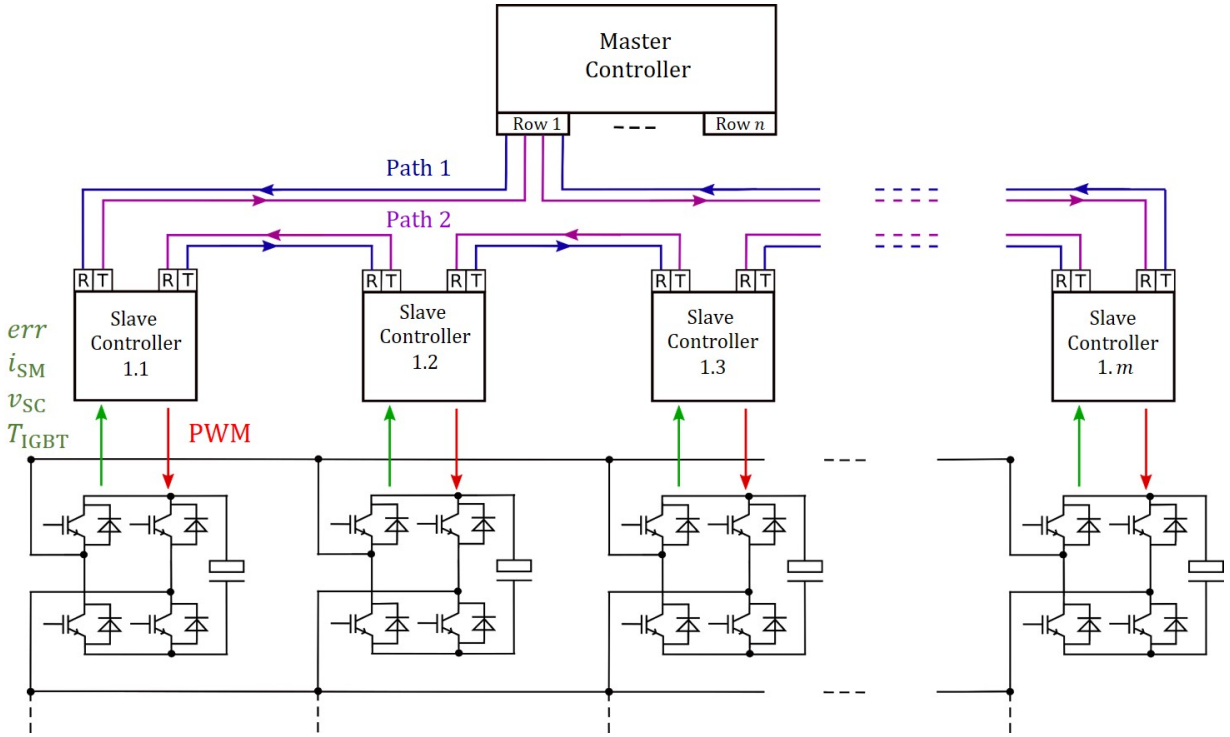

Figure 4.8: EtherCAT network simplified schema for the first row of the converter: the master controller communicates with the first and the last slave controllers via two identical (and opposite in direction) paths. Each slave controller reads its subpackage and place its information into it 'on the fly' in order to keep the communication fast. The whole communication is realised via fiber optic thanks to two EtherCAT media converters per terminal, which are not shown in the schema for simplicity.

Fig. 4.8 shows a simplified version of the communication studied for the proposed topology. The master controller is able to control n different and identical EtherCAT networks (each row has its own network). Each network is composed by m slave controllers (apart from the master) connected in ring configuration, which means that the master communicates only with the first and the last slaves of each network. Therefore the master can send the information package - containing specific subpackages for the different slaves - which is propagated through the slaves 'on the fly', meaning that when the package passes through a specific slave, it reads the relevant information and before implementing the commands it adds to the package the information about its previous cycle, allowing the package to travel to the next controller avoiding any additional delay

(due to the internal cell controller processing time of the information, which is processed after having sent to the next slave the information package).

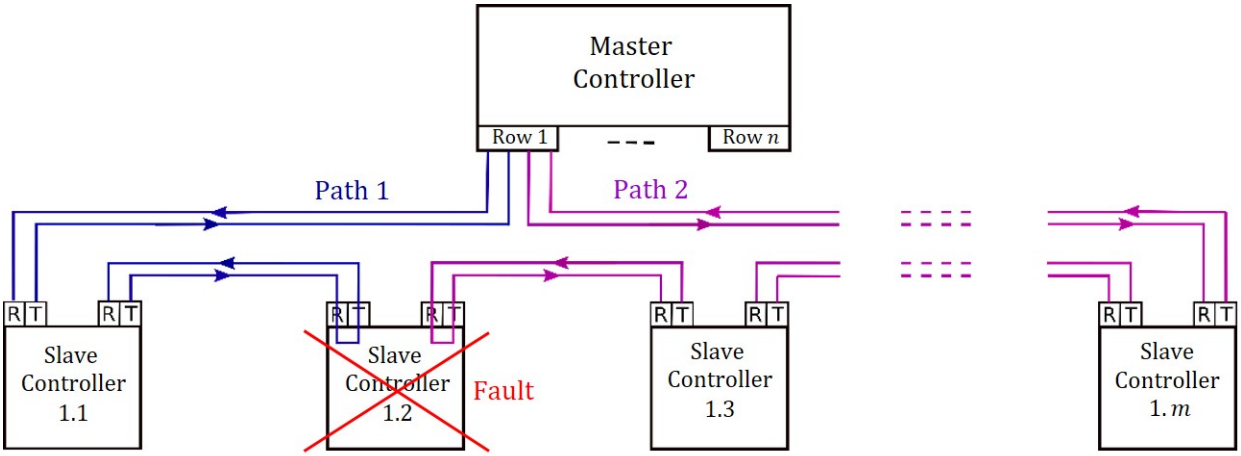

Figure 4.9: Fault example in the communication network of the Row 1: the information can be sent back through the two new line topologies formed between slave 1.1-master and slave 1.3-master. Due to the missing data into the communication package, the master can identify the failed module and the operation can continue.

The package sent from the master controller contains information about switching signals for the IGBT gate drivers and their timing, while the slave controllers provide to the master the information about v_{SC}, i_{SM}, power stage temperature T_{IGBT} and status of the submodule *err*. All the signals are propagated via fiber optic, which means that slave controllers are galvanically insulated among each others and with the master. The redundancy furthermore allows the operation even in case of fault of one terminal in the network. Fig. 4.9 shows an example of failure of a slave controller (Slave Controller 1.2): thanks to the two ports that each EtherCAT terminal has, the two communication paths can be sent back to the 1.1 and 1.3 controllers and continue up to the master. In this way the master still receives both the paths and depending on missing subpackage it can detect the failed controller. The same procedure can take place even in case of a fiber optic cable failure. This features therefore allows to continue the operation (in terms of communication) even in case of fault of one terminal per network, which means that up to n total slave controllers can fail without affecting the health of the communication system.

4.2.3 PLECS model and simulations results

The full-scale converter has been modeled in PLECS to test the developed control strategy and identify potential critical points to be addressed in the prototype. The model is

composed of 23 equivalent modules in series where each of them represents the parallel connection of 96 submodules. This means that all the submodules parameters such as v_{SC}, C_{SC}, ESL, ESR, L_{Filter} and C_{Filter} (shown in Tab. 4.1) have been accordingly adapted. The used v_{SC}, C_{SC}, ESL and ESR parameters are the ones of the supercapacitors modules used to build the prototype described in the next chapter and they are defined on the modules's datasheet. L_{Filter} and C_{Filter} have been estimated according to the procedure described in Ch. 4.1.2. Tab. 4.2 contains the main control parameters used for the simulations, such as the switching frequency f_{sw}, the control frequency f_c and the PI controller constants (k_p and k_i). f_{sw} has been set to 50 Hz in order to reduce as much as possible the load current ripple while respecting the ASDEX Upgrade TF coil contraint. A higher f_{sw} could have even more beneficial effects on the current ripple but the effect of the designed power stage filter could be than reduced (designed to operate with frequencies in the range of 25-125 Hz). k_p and k_i have been estimated according to the procedure described in Ch. 4.5.

Parameter	Value
R_{Load}	14 mΩ
L_{Load}	120 mH
C_{Filter}	3.5 mF
L_{Filter}	1.5 µH
v_{SC}	130 V
ESL	0.5 µH
ESR	10 mΩ
C_{SC}	67 F

Table 4.1: Main electrical parameters used for the PLECS full-scale converter.

Parameter	Value
f_{sw}	50 Hz
f_c	500 Hz
k_p	18.3
k_i	37.6

Table 4.2: Main control parameters used for the PLECS full-scale converter.

The simulations consisted in providing a reference current of 54 kA for about 13 s to the converter, with the aim of generating that current on the load with a precentual ripple value $\Delta i_{\%}$ lower than 0.1 %. The percentual ripple can be expressed as:

$$\Delta i_{\%} = \frac{i_{LoadMAX} - i_{LoadMIN}}{i_{ref}} \cdot 100 \tag{4.28}$$

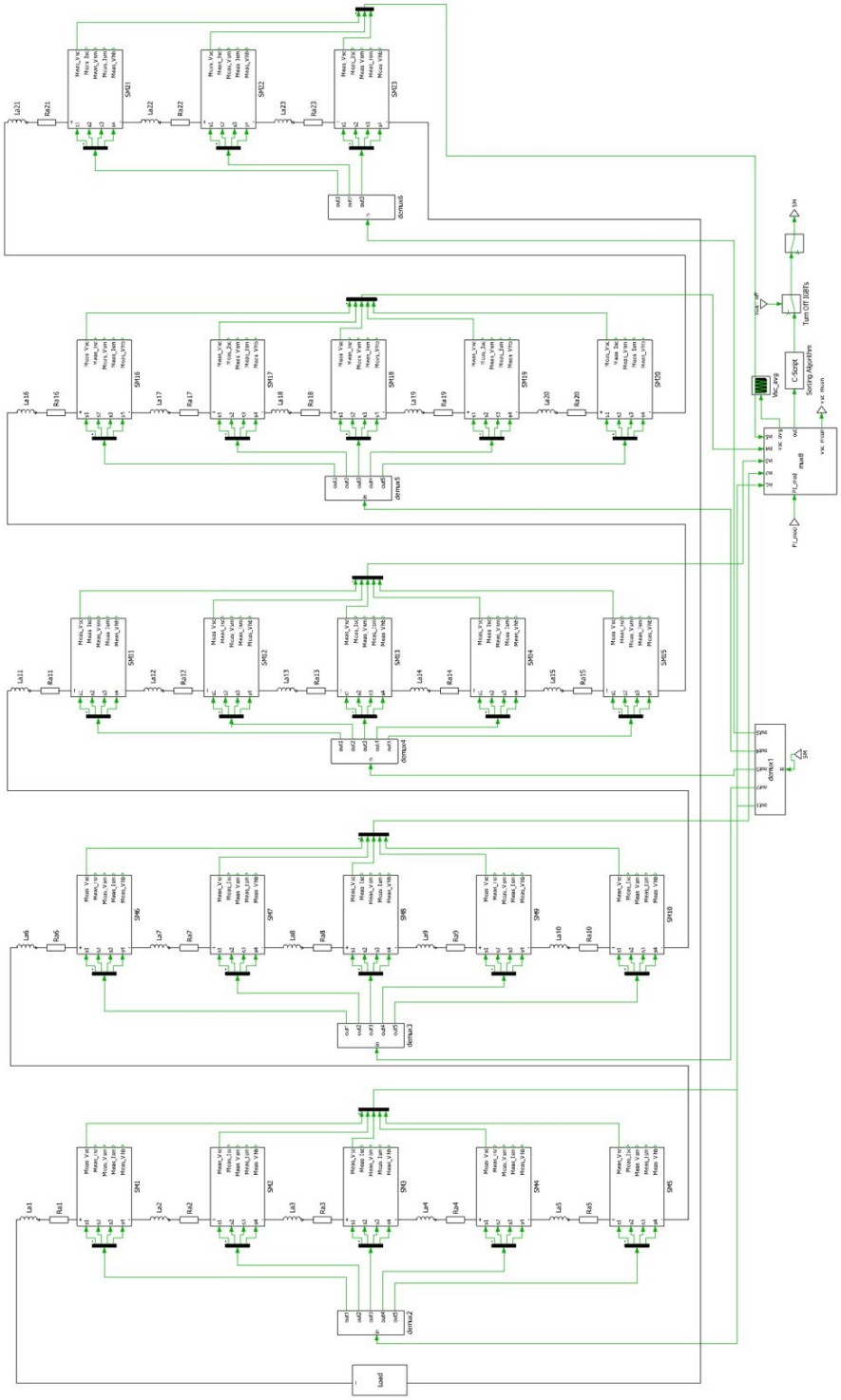

Figure 4.10: Full-scale converter PLECS model: each block (SM1-SM23) represents the equivalent circuit of a row, composed by 96 submodules in parallel.

and according to i_{ref}=54 kA, $\Delta i_{Load} = i_{LoadMAX} - i_{LoadMIN}$ must be lower than 54 A.

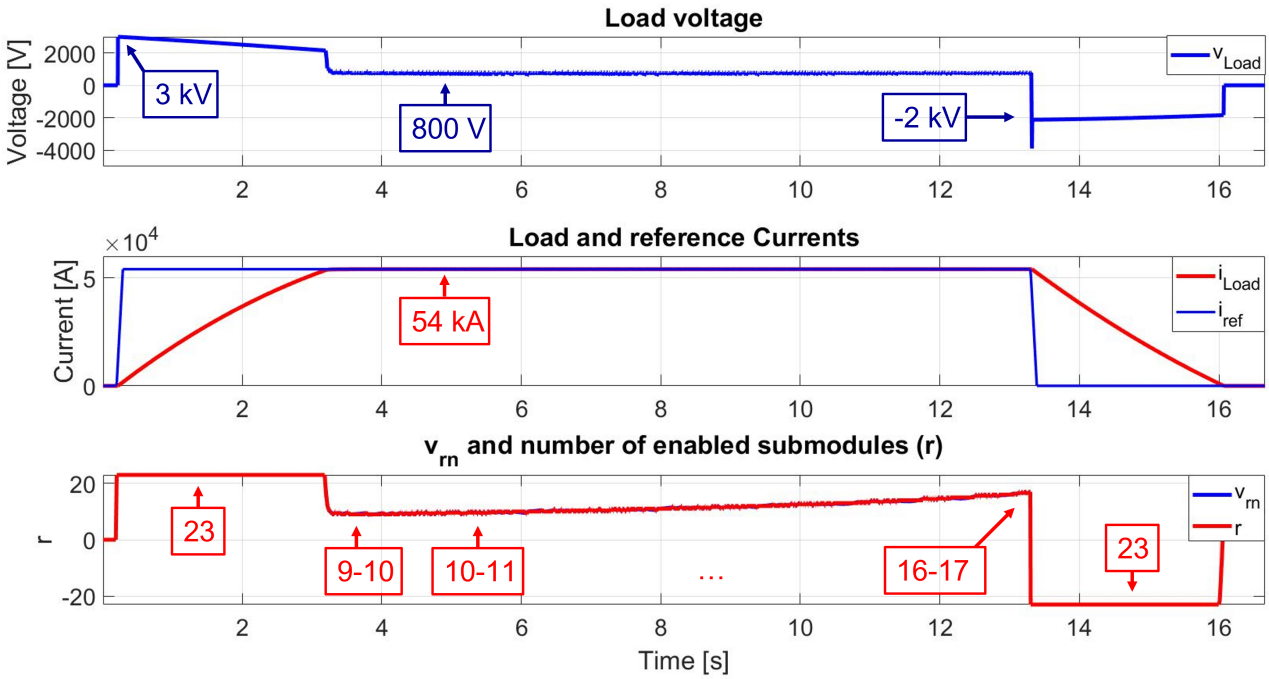

Figure 4.11: PLECS simulation for a standard 10 s long experiment: the converter provides its maximum voltage during the ramp-up phase, while it starts its switched operation during the flat-top and finally recovers the inductive energy of the load during the ramp-down.

Fig. 4.11 shows the results of a simulation. The first plot of the figure is the load voltage, in the center the load current is compared with the reference and at the bottom v_{rn} is plotted together with the number of enabled (state 1) submodules r: during the ramp-up phase all the available modules are in the state 1, providing the maximum voltage in output (3 kV); this phase is the one during which the supercapacitor modules lose the most of their energy since the submodules are continously ON; during the flat-top phase only the ohmic losses of the load have to be covered, meaning that approximately about 800 V are required; during the ramp-down phase finally the inductive energy stored into the load is transfered back into the supercapacitors modules while the current is ramped-down to zero. Fig. 4.12 shows a zoom of the previous figure. The current ripple is now visible and it measures about 20 A, which means that $\Delta i_{Load\%}$=0.04 %. From the last plot of the figure it is also possible to see how the number of enabled submodules (proportional to the output voltage level) oscillates between 10 and 11 according to the v_{rn} value.

The MB block operates with a frequency f_{sw} (see switching frequency of v_{Load}) which

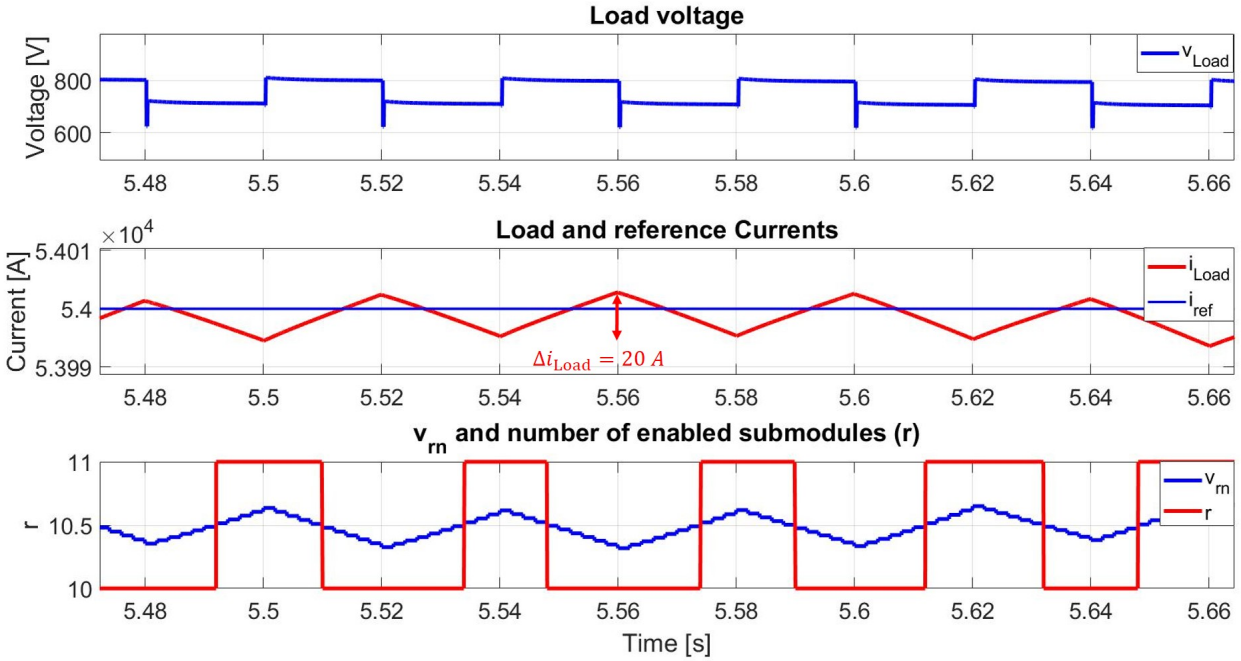

Figure 4.12: Zoom of the previous figure: the subswitching during standard switching events are due to the voltage balancing algorithm, which in order to keep the supercapacitors voltages balanced swaps the submodules multiple times (f_c) during a single cycle.

defines the maximum switching frequency of the load current, while the control is processes with a higher frequency f_c of 500 Hz (defining the several small steps of v_{rn} during a single v_{Load} cycle). In order to properly design and test a single submodule, it is useful finally to analyze the electrical scenario of a supercapacitors module during the converter operation, as shown in Fig. 4.13. The top curve represents the voltage which starts with value of 130 V (fully charged), decreases faster during the ramp-up phase due to the continuous operation and almost linearly during the flat-top phase, reaching a minimum of 60 V. The reason why v_{SCmin} is higher than the value described in Eq. 4.15 is the fact that the total amount of energy has to be sufficient even in case of loss of some modules (one full row plus one supercapacitor module per row in the worst case). Furthermore, the converter has to be able to operate with supercapacitor modules close to the end of their lifetime (double ESR, which means double internal losses). This justifies the voltage difference between Fig. 4.13 and the value provided by Eq. 4.15. During the ramp-down phase finally, the supercapacitor modules recover energy and the voltage raises (load inductive energy shared among all the modules) ending up with 80 V. The supercapacitors current instead has a pulsed DC operation, which means that the current oscillates between 0 and 560 A (54 kA divided by the number of parallel arms).

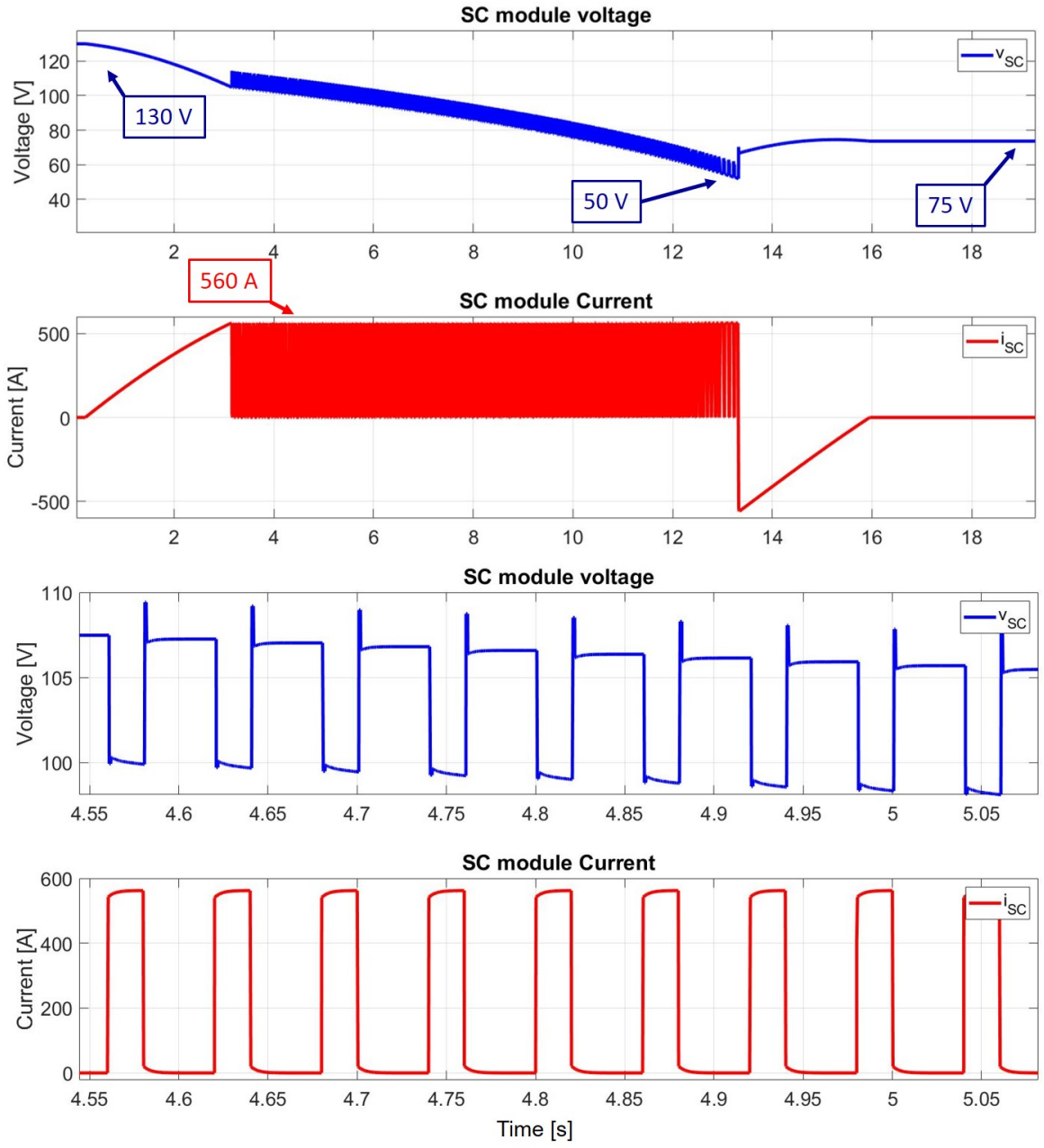

Figure 4.13: Single supercapacitors module electrical scenario during a pulse: the voltage starts from its nominal value (130 V) and loses about 50 V during the whole pulse, while the current is first continous during the ramp-up phase and then pulsed (DC) during the flat-top phase. During the ramp-down phase i_{SC} is negative due to the inductive energy of the load that is recovered and shared among all the submodules. The two lower plots are a zoom of the upper ones.

4.3 Parallelization of several submodules

As described along this chapter all submodules of a row are operated synchronously. The EtherCAT protocol ensures that all the gate drivers can produce the same switching signals with a jitter within the range of 10-50 ns meaning that the submodules can be considered to be synchronized. However when switching from state 1 or 4 (see Tab. 3.3) to a by-pass condition (states 2 or 3) the submodules currents start to decay with a slope that depends on the impedance through which such currents are flowing. The impedance of the busbars connecting the parallel submodules have to be thus designed in a proper manner to ensure a perfect current sharing. Furthermore, another cause of current unbalancing can be the supercapacitor modules ageing, which leads to an icrease of their internal resistance. These two effects are individually analysed in the following subsections.

4.3.1 Busbars impedance desgin

Fig. 4.14 shows the circuit of an arm composed by m parallel submodules to analyze the state 1-to-2 transition, for example: by applying the superposition effect, the load current can be estimated by summing up the single submodule currents contribution.

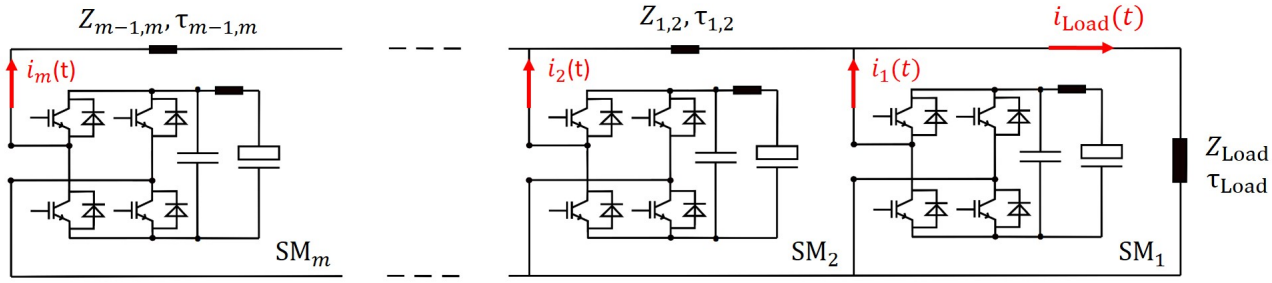

Figure 4.14: Simplified circuit of m submodules in parallel: $Z_{1,2}...Z_{m-1,m}$ are the impedances of the busbars (or cables) connecting the submodules belonging to the same row. Each submodule has a different distance from the load and this can cause currents unbalancing if $Z_{1,2}...Z_{m-1,m}$ are not well designed.

The first current contribution is $i_1(t)$ which can be estimated as:

$$i_1(t) = I_{10} \cdot \mathrm{e}^{-\frac{\mathrm{t}}{\tau_1}} \tag{4.29}$$

where $I_{10} = i_1(0)$ and $\tau_1 = L_{\text{eq1}}/R_{\text{eq1}}$. Since SM$_1$ is the submodule closest to the load, τ_1 can be approximated to τ_{Load}. The second submodule contribution can be expressed as:

$$i_2(t) = I_{20} \cdot \mathrm{e}^{-\frac{\mathrm{t}}{\tau_2}} \tag{4.30}$$

where $I_{20} = i_2(0)$ and $\tau_2 = L_{eq2}/R_{eq2}$. In this case τ_2 can not be approximated with the load time constant due to the precence of a non-negligible impedance between the first and the second submodule. τ_2 can be therefore expressed as:

$$\tau_2 = \frac{L_{\text{Load}} + L_{1,2}}{R_{\text{Load}} + R_{1,2}} \tag{4.31}$$

where $L_{1,2}$ and $R_{1,2}$ are inductance and resistance of the parallel connection between the first two submodules. The same procedure can be applied to the last submodule of the row, which leads to the following current:

$$i_m(t) = I_{m0} \cdot \mathrm{e}^{-\frac{\mathrm{t}}{\tau_m}} \tag{4.32}$$

where $I_{m0} = i_m(0)$ and by assuming $Z_{1,2} = Z_{2,3} = ... = Z_{m-1,m} = Z_c$ (equal and symmetric parallel connections) the time constant of the equivalent circuit seen from the last submodule can be expressed as:

$$\tau_m = \frac{L_{\text{Load}} + (m-1) \cdot L_c}{R_{\text{Load}} + (m-1) \cdot R_c}. \tag{4.33}$$

An unbalanced current sharing among submodules can lead to shorter lifetime of both IGBT and supercapacitor modules and for this reason it is crucial to ensure that all the submodule currents are as equal as possible. A balanced current sharing can be ensured by imposing $i_1(t) = i_m(t)$: if this can be realized, all the submodule currents will have the same dynamics no matter how large is m. Assuming that in steady state conditions all the submodules share the same current $I_0 = I_{10} = ... = I_{m0}$ (verified when the supercapacitor module have the same state of life and R_c is low enough), the previously imposed condition is verified if:

$$\tau_m = \tau_1 \tag{4.34}$$

which, according to Eq. 4.33, leads to:

$$\frac{L_{\text{Load}} + (m-1) \cdot L_c}{R_{\text{Load}} + (m-1) \cdot R_c} = \frac{L_{\text{Load}}}{R_{\text{Load}}}. \tag{4.35}$$

Eq. 4.35 has only one solution which is:

$$\tau_c = \tau_{\text{Load}} \tag{4.36}$$

This condition has to be taken into account during the sizing of the converter, by designing in a proper way the dimensions of the busbars connecting the parallel submodules. If $\tau_c > \tau_{\text{Load}}$, $i_1(t)$ rises faster than the other currents and most of the load current flows through the first submodule during transients. On the other hand, if $\tau_c < \tau_{\text{Load}}$, the first submodule has a slower dynamics than the other ones. Another constraint to take into

account when designing Z_c is R_c which has to be kept as low as possible to keep true the assumption $I_0 = I_{10} = ... = I_{m0}$. This value defines the steady state difference between the submodule currents and it is cumulative, which means that between the first and last submodules there is a voltage drop which depends on m and R_c. Fig. 4.15 shows the same circuit of Fig. 4.14 but in steady state condition. Thus inductances are neglected since they do not play any relevant role in this case and only resistances of the circuit (with their respective voltage drops) are shown.

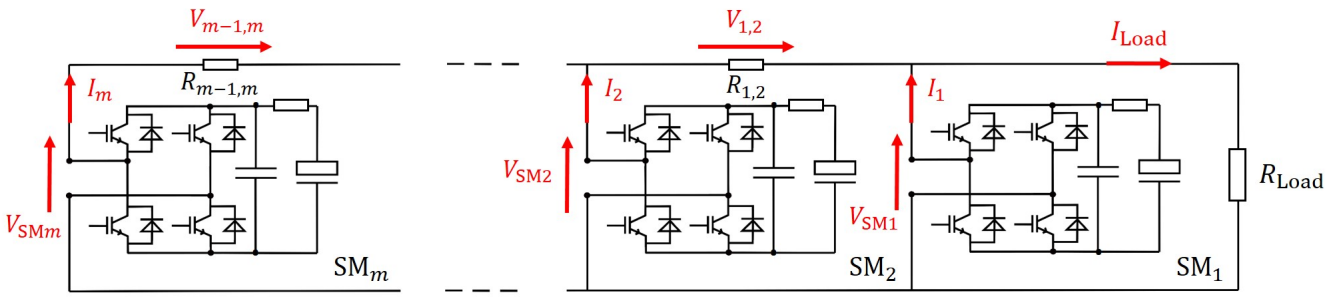

Figure 4.15: Simplified circuit of m submodules in parallel: $R_{1,2}...R_{m-1,m}$ are the resistances of the busbars connecting the submodules belonging to the same row. Each submodule has a different distance from the load and this leads to steady state currents unbalancing which can be limited by minimizing the resistance of the bars. Inductances of the circuit are neglected since they do not play any relevant role in steady state condition.

The assumption $R_{1,2} = R_{2,3} = ... = R_{m-1,m} = R_c$ is still valid, but the voltage drops over the busbars ($V_{1,2}, V_{2,3}, ..., V_{m-1,m}$) are all different from each other, since the currents flowing trough them are different. The voltage $V_{1,2}$ can be estimated indeed as:

$$V_{1,2} = R_c \cdot (I_{Load} - I_1) = R_c \cdot (I_{Load} - \frac{I_{Load}}{m}) = R_c \cdot I_{Load} \cdot (\frac{m-1}{m}). \quad (4.37)$$

All the other voltages can be estimated in the same way. Therefore the voltage drop over the m^{th} busbar is:

$$V_{m-1,m} = R_c \cdot I_{Load} \cdot (\frac{m-(m-1)}{m}). \quad (4.38)$$

In order to define the maximum value of R_c, the maximum losses due to the busbars voltages have to be imposed. The difference between the first and last submodule voltages is indeed the sum of all the bars voltage drops:

$$V_{SM1} - V_{SMm} = V_{1,2} + V_{2,3} + ... + V_{m-1,m} = R_c \cdot I_{Load} \cdot \frac{m-1}{2}. \quad (4.39)$$

With the current full-scale converter assumptions (I_{Load}=54 kA and m=96), the maximum voltage loss value due to the busbars can be imposed to be 10% of the supercapacitor modules voltages (130 V). R_c can be therefore estimated as:

$$R_c = \frac{V_{SM1} - V_{SM96}}{I_{Load} \cdot \frac{95}{2}} = \frac{13}{54000 \cdot 47.5} = 5\ \mu\Omega. \tag{4.40}$$

The estimated value of R_c is valid only with the assumptions of Eq. 4.40. The maximum voltage loss $V_{SM1} - V_{SMm}$ can be imposed for example to be much smaller than 10% of a supercapacitor module voltage, leading to a smaller R_c. On the other hand, if m is smaller, R_c can be chosen higher. Reducing m does not necessarily mean reducing the number of submodules in parallel. The same number of submodules in parallel can be obtained by connecting the load in the center of the row, splitting it in two and halving m, as shown in Fig. 4.16.

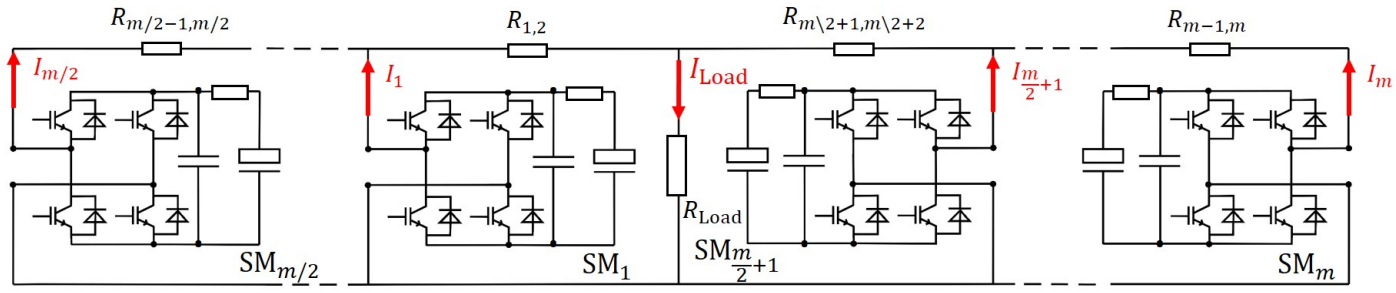

Figure 4.16: Simplified circuit of m submodules in parallel with load connected in the center of the row: this type of connection halves the distance between the load and the last submodule in comparison with the configuration shown in Fig. 4.15.

This would double the maximum R_c of Eq. 4.40 and with the same principle the load could be even connected via a star connection to the submodules ($m = 1$). These are only some of the many alternative solutions and the designer depending on the requirements of a specific application may chose a different one. Another aspect to take into account is the fact that in order to have balanced losses over the busbars, the resistances $R_{1,2} = R_{2,3} = ... = R_{m-1,m}$ may be chosen with different values (decreasing in amplitude from right to left in Fig. 4.15). This would lead to $V_{1,2} = V_{2,3} = ... = V_{m-1,m}$ but, on the other hand, according to Eq. 4.36 the inductances of the busbars should also be adapted. Furthermore, if the busbars are not all equal, part of the flexibility (and scalability) of the converter is lost. If they all have the same value indeed the load can be connected to any of the submodules in the same way, and the configuration can be easily changed. This would not be possible with unequal busbars. For these reasons for the current application the constraint $R_{1,2} = R_{2,3} = ... = R_{m-1,m} = R_c$ will be still applied.

Once R_c has been defined, L_c can be directly estimated by applying Eq. 4.36. Fig. 4.17 shows 4 different simulation results obtained in PLECS with the circuit of Fig. 4.14 with m=4. The supercapacitor modules start with 20 V and are discharged on a ohmic inductive load by alternating states 1 and 2 with a switching frequency of 50 Hz. This

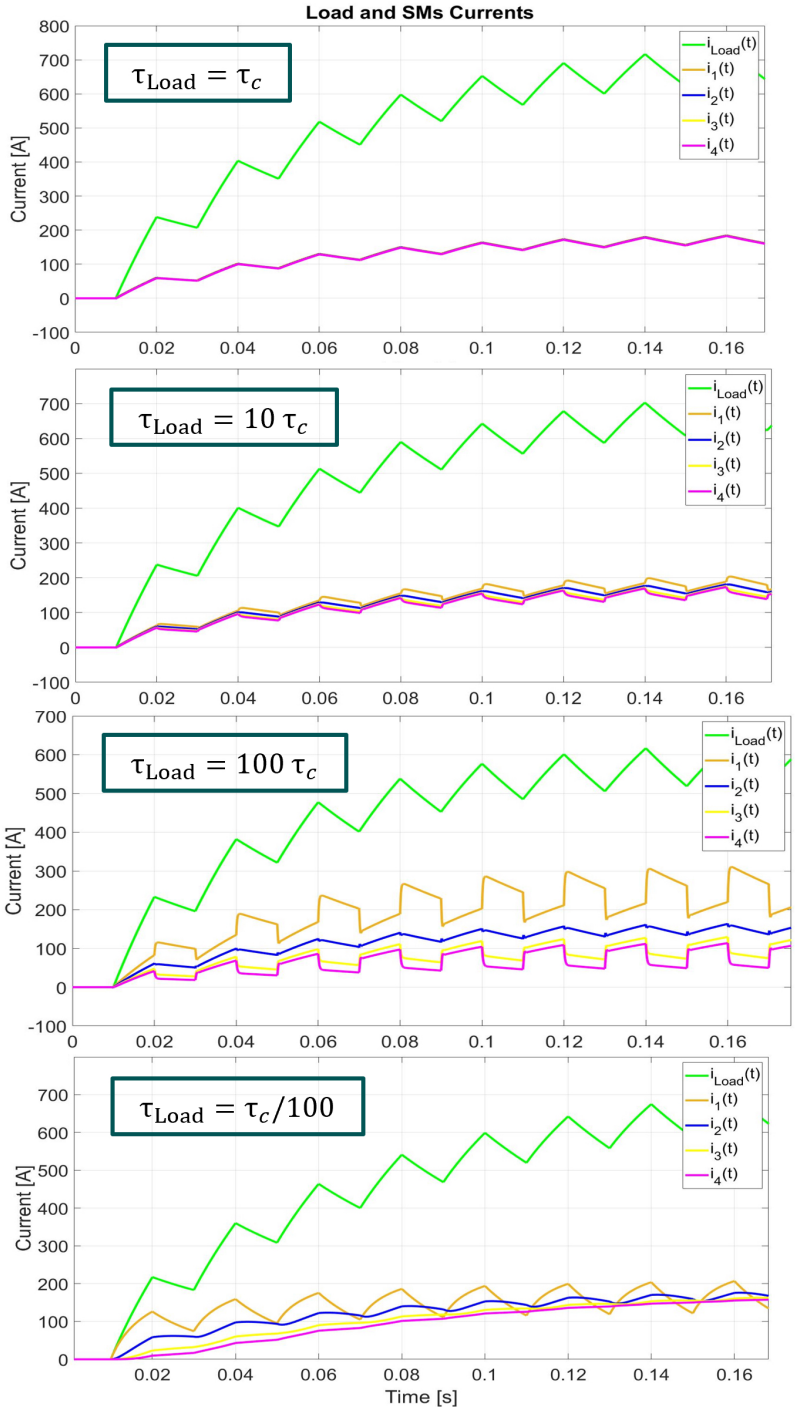

Figure 4.17: Simulation results of 4 parallel submodules with different Z_c: only in the first case $\tau_{Load} = \tau_c$ while in the other 3 cases the effect of unmatching is shown. Top-right and bottom-left plots show unmatching due to a too high resistance in the parallel connections, while the last plot shows the effect caused by a too large L_c.

conditions have been chosen since the results can be later validated via the demonstrator. The only difference among the 4 curves is τ_c: in the first case it perfectly matches the load time constants and the submodules currents are all identical; in the second and third case τ_{Load} is greater than τ_c and this has been obtained by increasing R_c, thus the currents have a steady state difference; the last plot instead shows the case where τ_{Load} is smaller than τ_c due to a lower inductance and therefore i_1 is faster than the other submodules' currents. For all the consideration given above, any impedances in series with the submodules have been neglected: if they would be present, the effect of the time constant unmatching would be reduced or even nullified. A series impedance with a larger time constant would indeed slow down evenly the dynamics of the submodules' currents, since this time this impedance would be the same for all the submodule (this is not the case for the interconnecting impedances). However a series impedance would cause additional continuous losses and for this reason it has been decided to avoid it.

4.3.2 Supercapacitor modules ageing effect

Supercapacitors state of life is mainly estimated by measuring their ESR value, and most of the manufacturers define the end of the life of a supercapacitor module when its ESR is double than its initial value. With the proposed busbars design, a balanced power sharing among the submodules ensures that all the supercapacitor modules' ESR increase evenly with the lifetime of the converter. Once all the ESR double their datasheet value, the supercapacitor modules can be replace with new ones. However, it can happen that a supercapacitor module fails before its foreseen end of lifetime (see Ch. 4.4). If a single supercapacitor module is replaced, its ESR is lower than the aged ones of the other submodules of the same row. This causes an impedance unbalance between the new and the old modules. In order to better understand this fenomena, it makes sense to analyze the worst case scenario that may occur, which consists in the replacement of a supercapacitor module from a row very close to the end of its lifetime. This means that all the old modules present an inner resistance twice higher than the one of the new module, as shown in Fig. 4.18. In this case SM_2 is the newer submodule and its supercapacitor module has ESR_2 which has half of the value of the other modules. This means that - apart from the dynamics of the external arm currents depending also on Z_c and Z_{Load} - once all the submodules are switched synchronously, SM_2 has a different internal dynamics than the other submodules (assuming that they all have the same ESR).

In particular at the time instant 0 when the row is connected to the load switching all the submodules from state 2 to state 1 (see Tab. 3.3), the k^{th} supercapacitor module's current is:

$$i_{SCk}(0) = \frac{v_{SCk}(0)}{ESR_k} \tag{4.41}$$

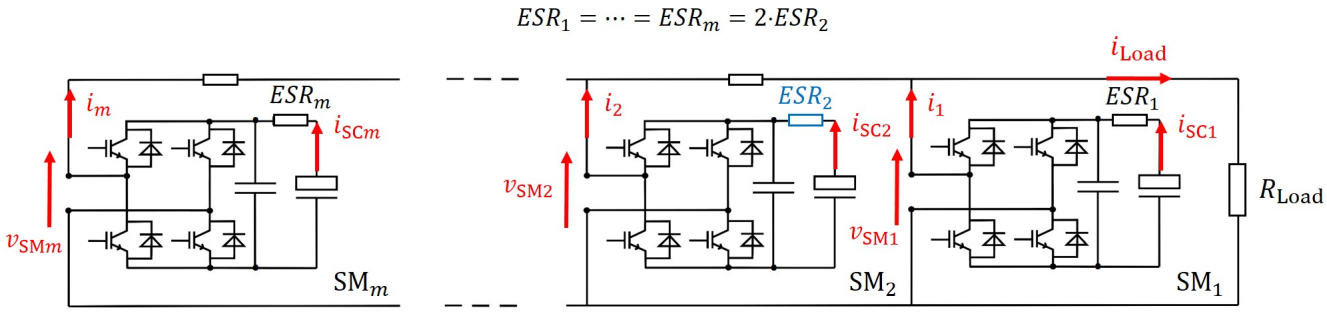

Figure 4.18: Simplified circuit of m submodules in parallel with different ESR: all the submodules except one are at the end of their lifetime, while the different one (SM_2) has been recently replaced and therefore has a lower ESR.

where k=1...m. This means that if the k^{th} supercapacitor module would have the same voltage at the instant 0, $i_{SC2}(0)$ would be double than the other ones, since ESR_2 is half of all the other ESR_k. A double current can induce a failure of the submodule if its components are not rated for such current. However, for this application this condition is not as dangerous as it may be for other applications. As the current is higher in one submodule, its supercapacitor module discharges faster and its voltage level will be for each period a small step lower then the other m-1 parallel modules. By neglecting the submodule power stage filter resistance - which is the same for all the modules - the dynamics of the i_{SCk} current is defined by the formula:

$$i_{SCk}(t) = i_{SCk}(0) \cdot e^{-\frac{t}{\tau_{SMk}}} \tag{4.42}$$

where the time constant τ_{SMk} is:

$$\tau_{SMk} = C_{SCk} \cdot ESR_k. \tag{4.43}$$

In other words, i_{SC2} is twice higher than the other supercapacitor modules's currents only at the instant 0 when the load current is zero (ramp-up phase, see Fig. 4.11), but before the load current reaches any significant value i_{SC2} has the same the value of the other i_{SCk} since the supercapacitor module of SM_2 discharges faster as long as i_{SC2} is higher than the other ones. Therefore, the supercapacitor module will never generate a current double than the rated one and no unwanted faults will be activated. Furthermore, the ESR is not the only resistance present in the submodule. Power stage filter and switches resistances have been neglected (as a worst case scenario) but since they are in the same order of magnitude (if summed up) of the ESR, a halved ESR does not lead to a double current but to a lower value, approximately 3/2 of the other submodules currents in this case. In the case of a different application where there is not such a long ramp-up phase, this condition could be the cause of major problems and counteractions have to be taken into accout to avoid it. A first solution would consist in using all the rows only

when the full voltage is required, and by-pass than the rows where there is a current unbalancing. An alternative soultion instead would consist in accepting a double current in some modules and thus increasing the threshold that would trigger the controllers (master or slave depending on where the safety is implemented) to detect an overcurrent (for example by imposing the maximum current limit as three times the rated value). In order to do so of course all the components must be rated for that. For both the proposed solutions a real-time current measurement has to be provided to the master controller which must be programmed to counteract in one of those ways current unbalancing between parallel submodules.

4.4 Real time fault detection and management

The reliability of the system is one of the main advantages of the proposed converter and for this reason it requires a dedicated section. As for any complex system there exist several fault senarios, and one of the main advantages of this topology is that operation can be stopped if any internal fault occurs. The modular concept separates the total stored energy into n x m smaller storages which can be kept separated even in case of fault. Thanks to the adopted full-bridge submodules it is possible to manage in real-time most of the failures without any need of additional safety switches. The following subsections describe the main faults that can occur: submodule internal fault, row internal short circuit and external short circuit.

4.4.1 Submodule internal fault

Even if well designed, submodules internal components can still be subjects to faults. The most common fault that can occur is the short circuit of one of the 4 IGBT of the submodule. For example in the transition from state 1 to 4, the switch S_2 can fail the opening and if S_1 closes a short circuit occurs, as shown in Fig. 4.19. A short circuit current i_{ss} starts to rise due to the energy stored in C_{Filter} as shown in the right hand side of Fig. 4.19. The raising slope of i_{ss} directly depends on the stray inductance between C_{Filter} and the power stage, represented as L_s in the figure. When S_1 closes, the filter voltage is directly seen from L_s, meaning that:

$$v_{\text{Cf}} = L_s \cdot \frac{\mathrm{d}i_{ss}}{\mathrm{d}t}. \tag{4.44}$$

From Eq. 4.44, by knowing L_s and v_{Cf}, and by imposing the minimum i_{ss} required to detect a short circuit, the minimum reaction time of the gate driver to detect and interrupt i_{ss} by opening S_1 can be estimated. Since L_s is a stray inductance (in the range of tens of nH), it is much smaller than L_{Filter} and ESL and therefore S_1 opens always before the supercapacitor module can contribute to the short circuit current.

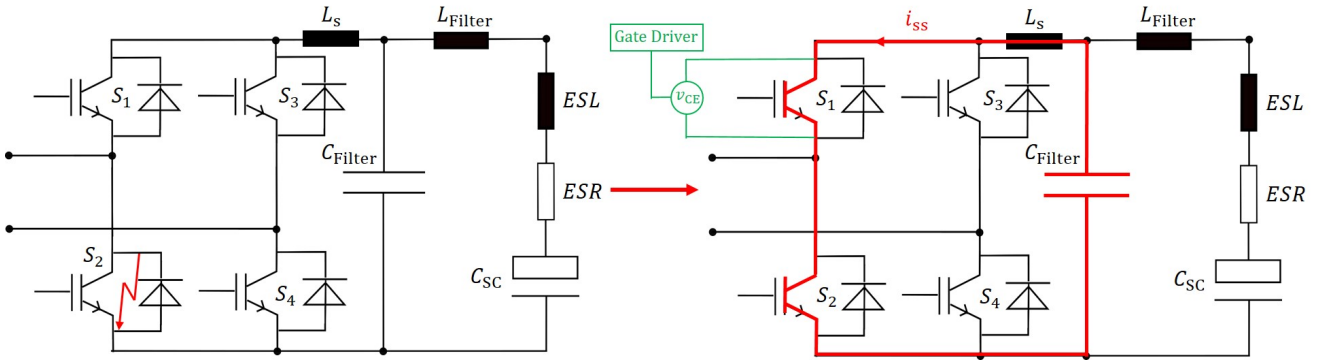

Figure 4.19: Submodule internal fault: in case S_2 does not open before S_1 closes, a short circuit occurs due to the filter capacitance energy that start to discharge through the red path of the figure. The gate driver of S_1 has to be fast enough to detect the short circuit current and interrupt it before it triggers unwanted short circuits in the adiacent submodules.

An important aspect to point out is the fact that this kind of short circuit can not be monitored by a direct current measurement, since most of the current measurement methods would be too slow and/or expensive to counteract i_{ss} before it would reach a relevant amplitude. In order to quickly detect a short circuit indeed the two IGBT v_{CE} of each half-bridge are monitored, as shown for a single IGBT in Fig. 4.19 (in green, but for the other IGBT the same parameter is monitored). Each gate driver has a v_{CE} monitoring circuit intergated [53] which checks v_{CE} after a response time (different for each gate driver and internally defined by manifacturers) at turn-ON to detect a short circuit. If the voltage is higher than the programmed thereshold voltage (V_{th}, lower than the OFF voltage but higher than $V_{CE,ON}$), the driver detects a short circuit at the IGBT and opens immediately both the half-bridge switches. An error signal is sent to the microcontroller and both IGBT stay in the OFF state until the microcontroller resets the error signal [53].

Another parameter to take into account in this regard is L_c (see Fig. 4.20): if it has a similar value to L_s, i_{ss} can flow through the interconnections into the parallel submodules, inducing their gate drivers to detect a short circuit as well and causing the loss of further modules. This has to be avoided in order to be able to distinguish internal to external submodule faults and to continue the operation of the row in case of fault of a single submodule. If L_c is much higher than L_s indeed the short circuit current variation in the interconnecting bars ($\frac{di_{rs}}{dt}$) is much smaller than the one into the submodule ($\frac{di_{ss}}{dt}$), and therefore when S_1 of the failed submodule opens, the parallel submodules still did not detect any short circuit and can continue the operation since the short circuit current rised in them did not reach the thereshold to activate the gate drivers protection. According to the adopted components L_s=50 nH (see Ch. 5.1) and L_c=4 µH (see Ch. 5.2.3). V_{th}=10 V is provided on the gate driver datasheet [53] and by inserting this value into the

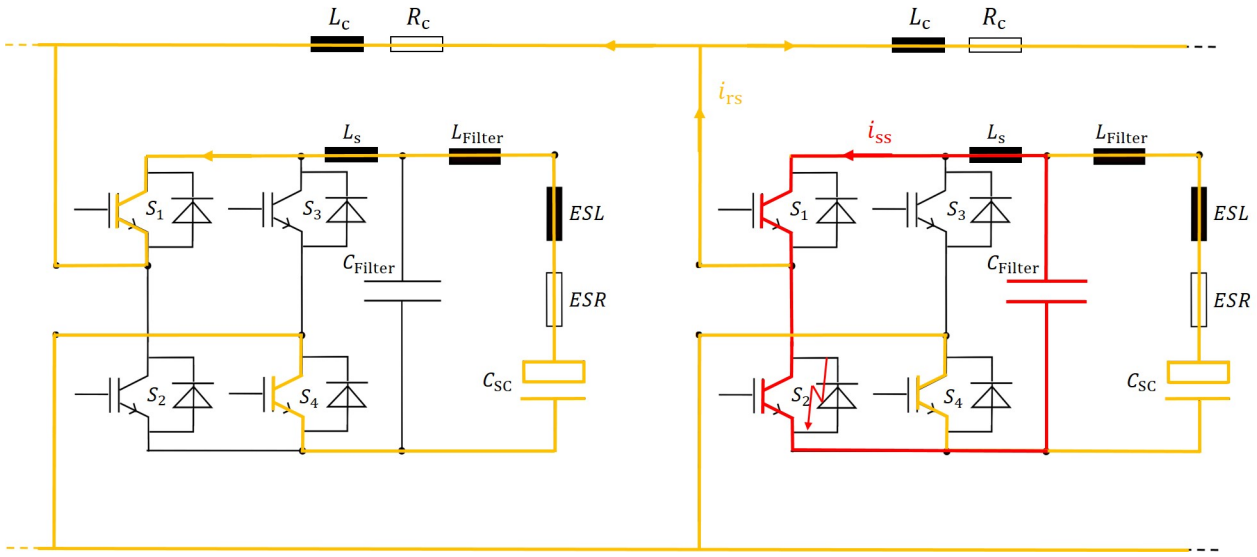

Figure 4.20: Failed and operating submodules in parallel compared: if $L_s << L_c$, i_{ss} (in red) raises much faster than i_{rs} (in orange). In this way the failed submodule can interrupt i_{ss} before the parallel submodules detect any short circuit and the whole row can continue the operation with m-1 submodules.

I_c-V_{CE} charachteristics of the IGBT [54] the minimum short circuit current (I_{ssth}=7300 A) required to trigger the gate drivers can be estimated. The time required from i_{ss} to reach I_{ssth} can be estimated as follows:

$$T_{ths} = L_s \cdot \frac{I_{ssth}}{V_s}. \tag{4.45}$$

Considering the parameters given above and that in case of short circuit the voltage seen from L_s is approximately the supercapacitor module voltage (as a worst case scenario 130 V if internal voltage drops are neglected), the minimum required T_{ths} is 2.8 µs. On the other hand, in order to estimate the time required from the adiacent submodule to detect a short circuit T_{thr}, L_s of Eq. 4.45 has to be replaced by L_c, leading to T_{thr}=224 µs. This means that the gate driver of the failed submodule has to detect and open all the IGBT within maximum $T_{thr} - T_{ths}$=221 µs (neglecting gate driver and IGBT internal delays) in order to avoid that any of its parallel submodules detect a short circuit.

4.4.2 Row internal short circuit

Another fault scenario that can occur is the row internal short circuit, represented in Fig. 4.21. This condition can occur if an external event leads to contact or bridging of the (typically blank) busbars.

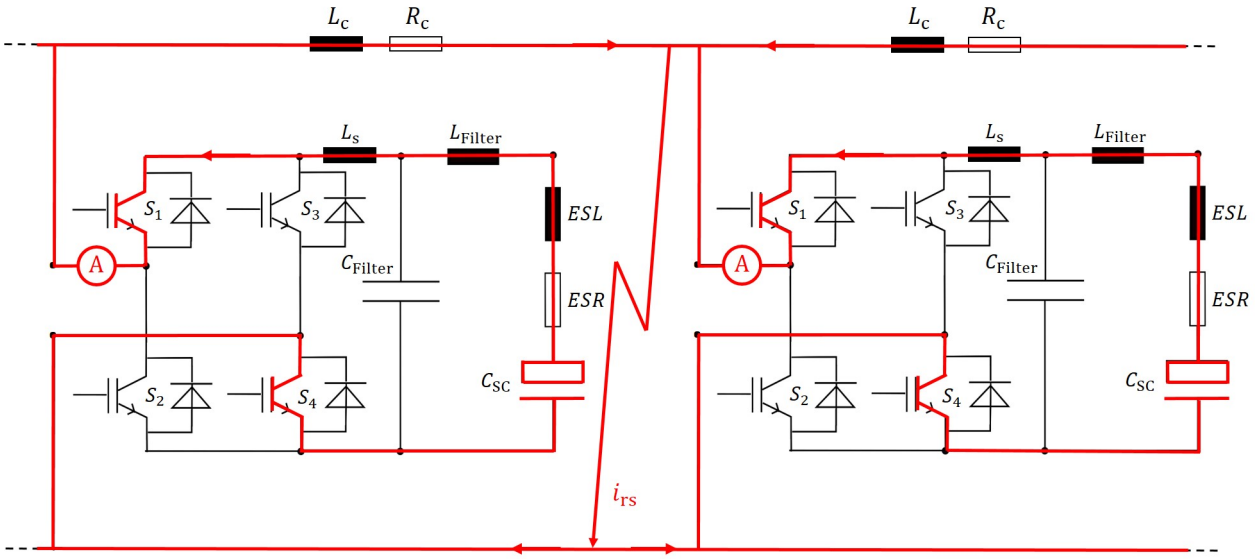

Figure 4.21: Row internal short circuit: once the short circuit current exceeds a specific threshold the submodules controllers force the power stage to a zero-voltage state (by-pass) and send an error signal to the master controller. This means that the master controller is informed about the row status and knows that it is not available anymore for operation.

In this case the short circuit current i_{rs} comes from the discharge of the supercapacitor modules since L_{Filter} and ESL have the same order of magnitude of L_c and for this reason its rising time is much lower than in the case of the submodule internal fault. However, the two submodules closest to the fault are triggered before the other submodules and will turn in freewheeling mode as for the case of the internal submodule fault since their gate driver detect first the fault. This first trigger is caused by the discharge of the filter capacitors as explained in the previous subsection. On a slower timescale, the supercapacitor modules' currents exceed their nominal value and once they exceed a programmed threshold (checked from the microcontroller by monitoring the submodules's currents) the submodules are forced to turn into one of the zero-voltage states (state 2 or 3). Finally, the information is sent to the master controller which deactivates permanently the whole row, until service staff performs repair and manually resets the error memory. A fault of this kind does not allow the row to continue its operation, but the converter can do so with a voltage level less. The total amount of energy is still sufficient to guarantee a proper operation even in case of loss of a whole row.

4.4.3 External faults

DC-side short circuit

An example of DC-side short circuit is shown in Fig. 4.22. This fault can occur during the charging phase, when the current flowing into the supercapacitor modules is much smaller (see Ch. 4.1.3) than the one during the pulse phase. However, if a fault occurs when the supercapacitor modules are charging (for example if the blank DC busbars come in contact), their currents turn from positive (charging) to negative (discharging). Therefore, the fastest way to detect the fault consists in monitoring the charging current by the local microcontrollers and force into a zero-voltage state the submodules in case of unwanted change of sign of current. At the same time, the master controller has to be informed about the error and the switches connecting the rectifier with the grid have to be open. If the switches are not open quickly enough, the formed arc can be fed by the grid current and in this case a fuse on the AC-side (a pyro-fuse for example) has to interrupt the short circuit current. If this fault occurs during the pulse phase, the submodules matrix does not see any short circuit since it is disconnected from the charging circuit.

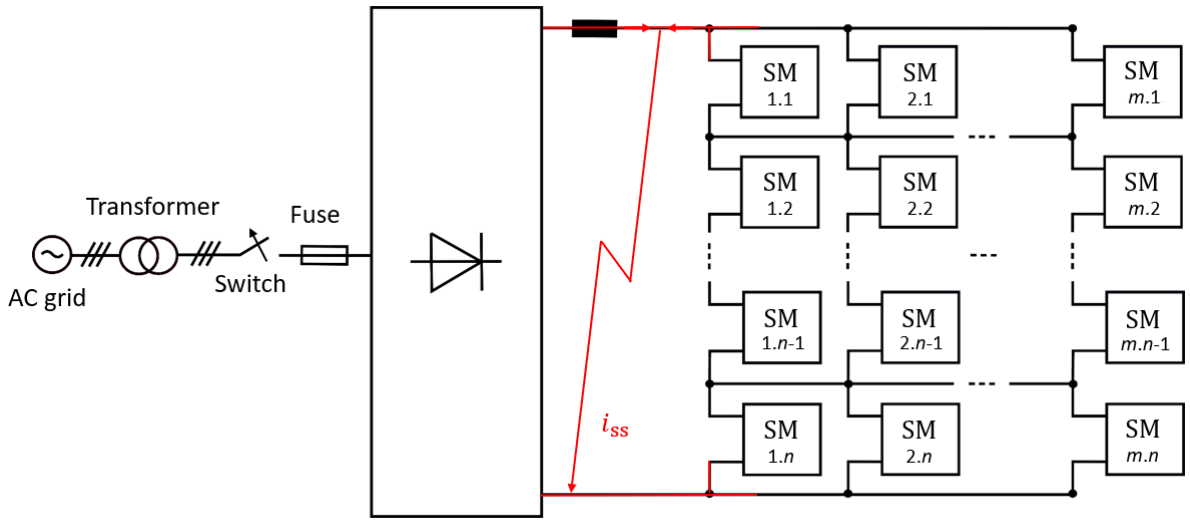

Figure 4.22: DC-side short circuit in charge configuration: all the submodules detect the fault by a change of current direction and are forced by their local microcontrollers to a zero-voltage state. The switches connecting the charging circuit with AC-grid are open and if that is not sufficient, a fuse can interrupt the short circuit current.

Load-side short circuit

If the fault occurs during the pulse phase, the same procedure of the row internal short circuit is valid, with the difference that in this case the whole converter has to stop its operation. In order to detect the short circuit via the submodules current sensors, the minimum current reached by the arc to trigger the fault is m times the submodules maximum current, which is about 108 kA. $\frac{\mathrm{d}i_{\mathrm{ss}}}{\mathrm{d}t}$ is mainly limited by the supercapacitor modules' and filter inductances.

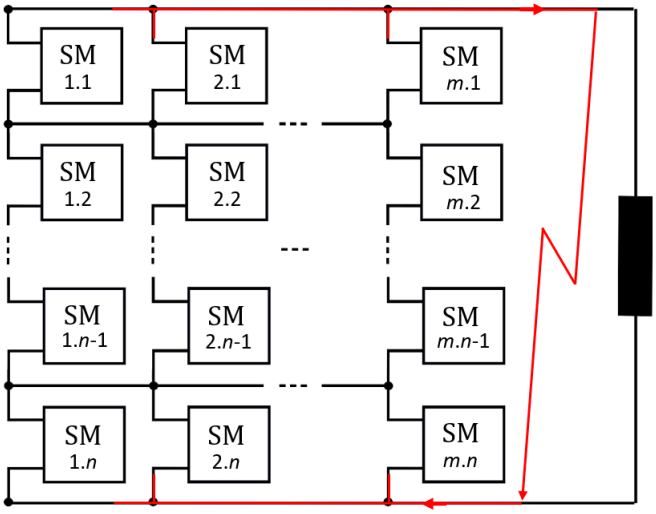

Figure 4.23: Load side short circuit: this fault is detected by the submodules current sensors. The local microcontrollers force to a zero-voltage state their respective submodules.

Therefore, the time required from i_{ss} to reach the overcurrent threshold can be estimated as:

$$T_{\mathrm{thSM}} = (ESL + L_{\mathrm{Filter}}) \cdot \frac{2 \cdot I_{\mathrm{SM}}}{V_{\mathrm{SC}}}, \tag{4.46}$$

where I_{SM}=560 A, V_{SC}=130 V, ESL=1.5 µH and L_{Filter}=1.5 µH (see Ch. 5.1). With the adopted components thus T_{thSM}=21,5 µs. Assuming v_{SC}=V_{SC} for the whole arc formation (in such a short time-scale the voltage can be assumed to be constant), the energy stored from the arch E_{ss} can be estimated as follows:

$$E_{\mathrm{ss}} = \frac{1}{2} \cdot n \cdot V_{\mathrm{SC}} \cdot (2 \cdot I_{\mathrm{SM}}) \cdot T_{\mathrm{thSM}} = 3.5\ \mathrm{kJ}. \tag{4.47}$$

Eq. 4.47 as a worst case scenario does not take into account internal losses of the submodule, which means that the output voltage would be even lower than V_{SC}. Once all the submodules are in one of the zero-voltage states, the voltage feeding the arc can be approximated with the $2 \cdot n \cdot V_{\mathrm{CE,ON}}$ (voltage drop over the two conducting switches of

each submodule). Since this voltage does not exceed a few tens of V (69 V by considering $V_{CE,ON}$=1.5 V, see Ch. 5.1), the arc is extinguished in about 940 μs by discharging its energy into the submodules power stages. The stored energy left into the load is dissipated into its own resistance.

5 The developed demonstrator and experimental results

A small-scale demonstrator (1:550) has been built to validate the designed converter. It is composed by 4 identical submodules, which can be connected in serial, parallel or combined serial/parallel connection. The goal of the demonstrator is to confirm the results of the simulations obained thanks to the PLECS models built stepwise with the prototype, as it will be shown along this chapter. If the results fit together, the prototype can be scaled up without any major problem and the results of the simulations shown in the previous chapter can be used as a reference.

5.1 Submodule development

The first step of building the demonstrator consisted in developing a single independent submodule. Its simplified circuit has been already shown in Fig. 4.2. That schema does not take into account the parasitic elements of the main components such as resistances and inductances of the power stage filter and cables/copper connections. Furthermore, in Ch. 5.1.1 information about the custom electronics developed for the submodule are provided.

5.1.1 Configuration and components

The supercapacitor module

The supercapacitor module is a custom solution built for this specific project from the SPSCAP company. The module is composed of 48 supercapacitor cells in series, each of which has a capacitance of 3200 F and 2.7 V of nominal voltage. The equivalent capacitance of the module C_{SC} is 67 F for a nominal voltage v_{SC} of 130 V. The main technical data of the module are listed in Tab. 5.1 [55], while Fig. 5.1 shows a photo of it.

The module has no active electronics in it and it is treated as a passive single component, even though it presents a passive balancing system for its internal cells: each cell has a resistor connected in parallel through which a leakage current can flow; the cell with

Figure 5.1: Supercapacitor module used for the prototype: the module is composed by 48 x 2.7 V cells in series for a total voltage of 130 V. Being a custom module built for this project, it has been decided to keep it as simple (and passive) as possible avoiding any active electronics in it (e.g. voltage balancing).

the highest voltage will produce a higher leakage current which will discharge the cell faster then the other ones [56]. This process can balance the cell voltages in steady state conditions, but its effect is negligible during the dynamics of the module. Even though there exist much more precise and/or complex balancing systems, they would only be useful if the submodule would be composed by cells connected in parallel: in this case indeed the cells could get unbalanced during charging/discharging phases, but since in the adopted supercapacitor module all the cells are in series, they are all charged/discharged with the same current making very hard any cell unbalanging. For this reason it has been chosen to keep the module as much passive as possible, without the adoption of any active cell balancing system.

Parameter	**Symbol**	**Value**
Number of cells	n_c	48
Cell capacitance	C_c	3200 F
Module capacitance	C_{SC}	67 F
Rated voltage	V_{SC}	130 V
Module energy	E_{SC}	600 kJ
Rated current for 12 s	I_{SC}	800 A
Maximum peak current (1 s max)	I_{SCMAX}	2200 A
Equivalent series resistance	ESR	10 mΩ
Equivalent series inductance	ESL	1.5 μH
Mass	M_{SC}	41 Kg
Operating temperature	T_{op}	-40°C/+45°C

Table 5.1: Main technical data of the used supercapacitors module [55].

The IGBT full-bridge

The IGBT full-bridge has been realised by connecting two "FF600R07ME4-B11" IGBT half-bridge modules from the Infineon Technologies company. These modules have a blocking voltage capability V_{CES}= 650 V, a continuous DC collector current I_c=700 A and integrated antiparallel freewheeling diodes. The main technical data are listed in Tab. 5.2. Each half-bridge module has a negative temperature coefficient resistor which allows to measure its temperature in real-time. However, being operated with a current below its nominal value and only for a few seconds, the temperature rise is negligible during normal operation even without any forced air cooling. The full-bridge is indeed mounted on a heat sink (as shown in Fig. 5.2) which is sufficient to ensure a proper heat dissipation and bring the IGBT to the room temperature during the 15 min of dwell-time.

Parameter	**Symbol**	**Value**
Blocking voltage capability	V_{CES}	650 V
Continuous DC collector current	I_c	700 A
Repetitive peak collector current (1 ms)	I_{cMAX}	1200 A
Gate-emitter peak voltage	V_{GES}	+/- 20 V
Thermal resistance, junction to case	R_{thJC}	0.083 K/W
Thermal resistance, case to heat sink	R_{thCH}	0.04 K/W
Operative temperature	T_{op}	-40°C/+150°C
Collector-emitter ON voltage @600 A	V_{CES}	1.5 V

Table 5.2: Main technical data of the used IGBT half-bridge modules [54].

Each half-bridge has a gate driver board "2SP0115T" mounted on it: the drivers have a fixed dead-time of 3 μs integrated, which ensures that before the upper switch of the half-bridge closes, the lower one is fully open already. 2 Turn-ON and turn-OFF gate resistors are appropriately sized to damp oscillations during switching events. Furthermore, the gate drivers have an integrated short circuit protection which continously monitors the collector-emitter v_{CE} of the switches and in case of short circuit it forces both the gate signals to open the IGBT.

The power stage filter

The power stage filter is composed by one inductive and two capacitive stages. The inductor partially decouples the supercapacitor modules from the power stage, meaning that in case of transient overvoltages only a small fraction of them is seen from the supercapacitors, as explained in details in [57]. The chosen L_{Filter}=1 μH has been obtained by building an air core inductor from the copper positive cable connecting the supercapacitor module to the power stage. The two capacitive stages are composed

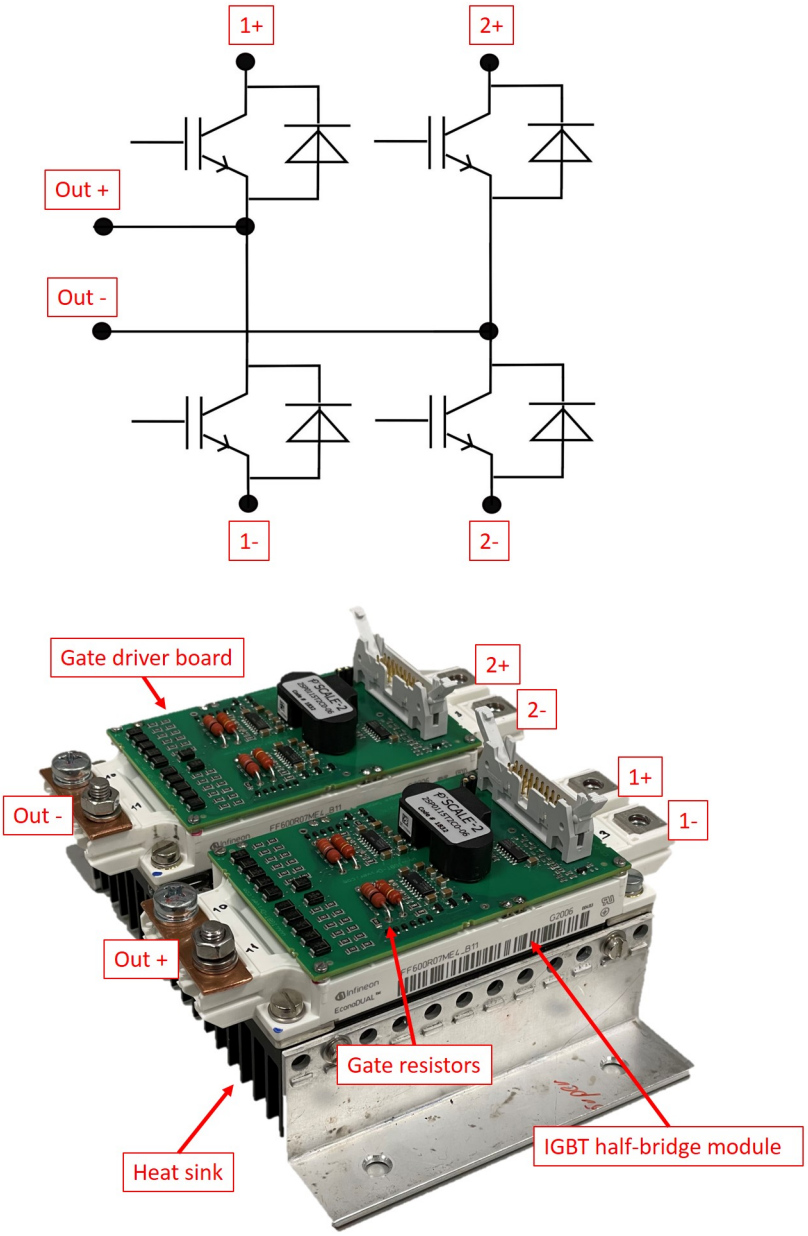

Figure 5.2: Power stage schema (top) and photo (bottom): each half-bridge has a positive, a negative and an output terminal marked in red in both the pictures. By connecting the positive and negative terminals of the first half-bridge with their respective ones of the second half-bridge, a full-bridge can be obtained. The photo shows also the gate driver board with gate resistors mounted and the heat sink used for the prototype.

of two 50 µF MKP1848C foil capacitors and two 3.5 mF ALS70A302KF400 aluminium electrolytic capacitors as shown in Fig. 5.3. The reason why the two stages have not been combined in a single one is the fact that aluminium electrolitic capacitors have an

equivalent inductance too high to be directly placed on the IGBT. On the other hand if the required capacitance (3.5 mF) would have been obtaind only by foil capacitors, the filter would result in a too bulky structure. The filter capacitors can be represented with an equivalent circuit similar to the one of the supercapacitors (shown in Fig. 3.8) while the filter inductor can be represented as a series RL circuit. The equivalent circuit of the filter is shown in Fig. 5.4 and its main parameters are described in Tab. 5.3.

Parameter	**Symbol**	**Value**
Filter inductor's inductance	L_{Filter}	1µH
Filter inductor's resistance	R_{Filter}	6 mΩ
First capacitive stage capacitance	C_{f1}	3.5 mF
First capacitive stage inductance	ESL_{f1}	50 nH
First capacitive stage resistance	ESR_{f1}	12 mΩ
Second capacitive stage capacitance	C_{f2}	50µF
Second capacitive stage inductance	ESL_{f2}	1 nH
Second capacitive stage resistance	ESR_{f2}	5mΩ

Table 5.3: Main equivalent parameters of the chosen filter components.

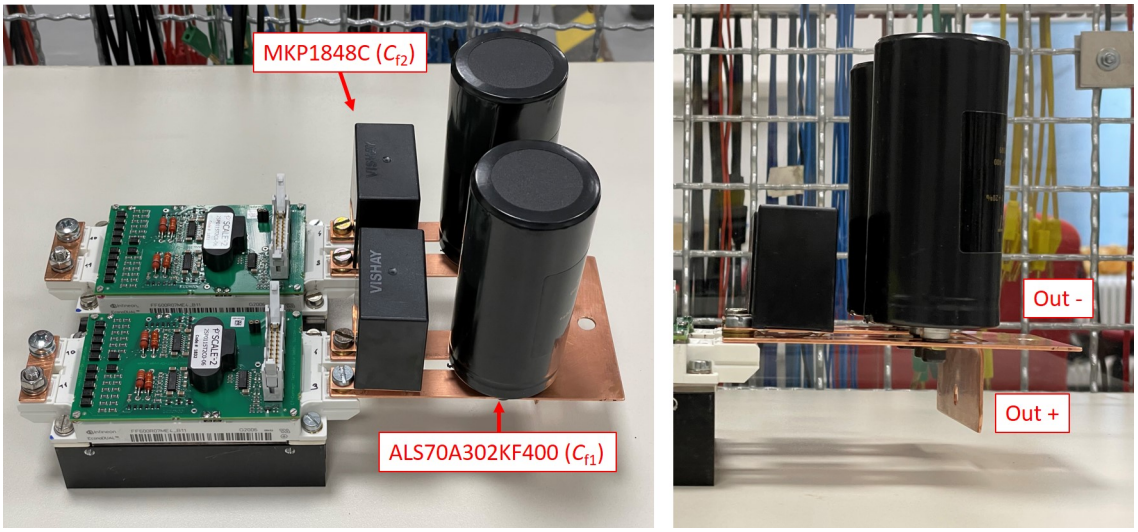

Figure 5.3: Filter capacitors mounted on the power stage: top view on the left, side view on the right. One copper bar output terminal has been bent to 90 degrees with respect to the other one to facilitate the connection with the supercapacitor module.

According to Eq. 4.8 the designed filter provides a f_{co}=1.7 kHz, which means that all the harmonics of i_{SC} with higher frequencies are filtered out. In order to determine the behaviour of the supercapacitor module - in terms of internal losses and thus ESR - an RLC meter has been used to measure the impedance Z_{SC} of the module over a wide range

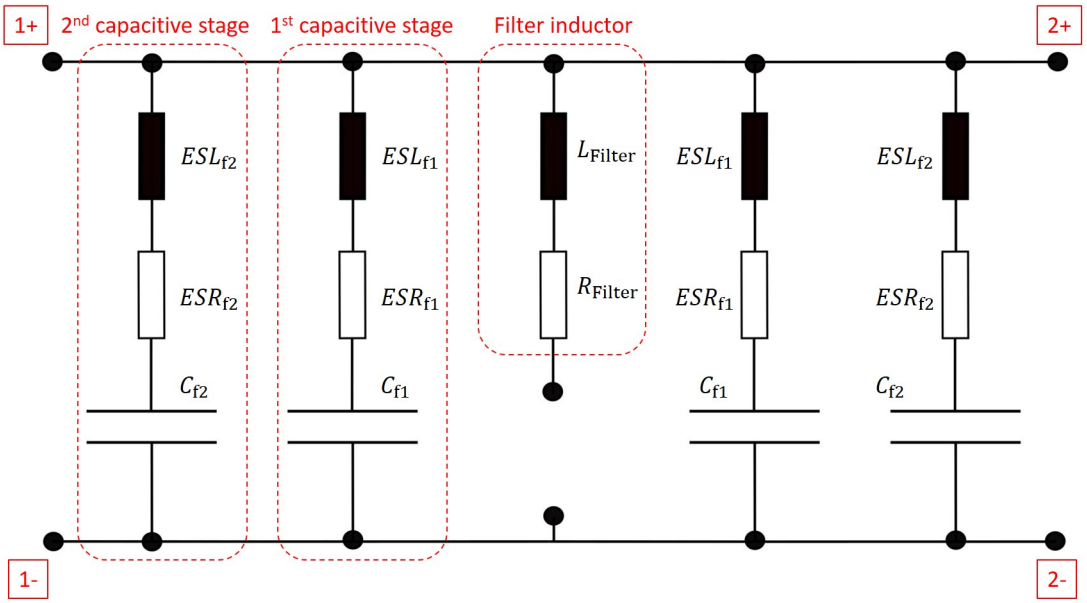

Figure 5.4: Power stage filter simplified schema: the filter is splitted into two symmetrical parts sharing the same filter inductor. Stray inductances and parasitic elements of the copper bars connecting the filter capacitors can be neglected. The terminals 1+/- and 2+/- are highlighted to show the connection points with the two IGBT half-bridges of the power stage (see Fig. 5.2).

of frequencies (from 1 to 10000 Hz) [57]. These measurements provide amplitude ($|Z_{SC}|$) and phase (ϕ_{SC}) of Z_{SC} for each frequency. ESR is the real part of Z_{SC} thus it has been obtained by the formula:

$$ESR(f) = Z_{SC}(f) \cdot \cos \phi_{SC}(f). \tag{5.1}$$

Fig. 5.5 shows the obtained values of ESR for each frequency analysed: for each frequency below 4 kHz (f_{cr}) ESR's amplitude is constant at 10 mΩ which means that its datasheet value is a valid approximation of the actual one. For frequencies above f_{cr}, ESR increases very rapidly to values much higher than double of its DC value. Therefore, the supercapacitor module's operating frequency has to be kept below f_{cr}. According to the full converter requirements, the chosen switching frequency of 50 Hz is below that threshold. However, high frequency harmonics can be still present in the supercapacitors current and for this reason it is important to take into account the condition $f_{co} < f_{cr}$ when designing the filter.

Communication and electronics

The configured EtherCAT network is shown in Fig. 5.6 and it is composed by a master controller, a port multiplier, two media converters and a slave controller. The master

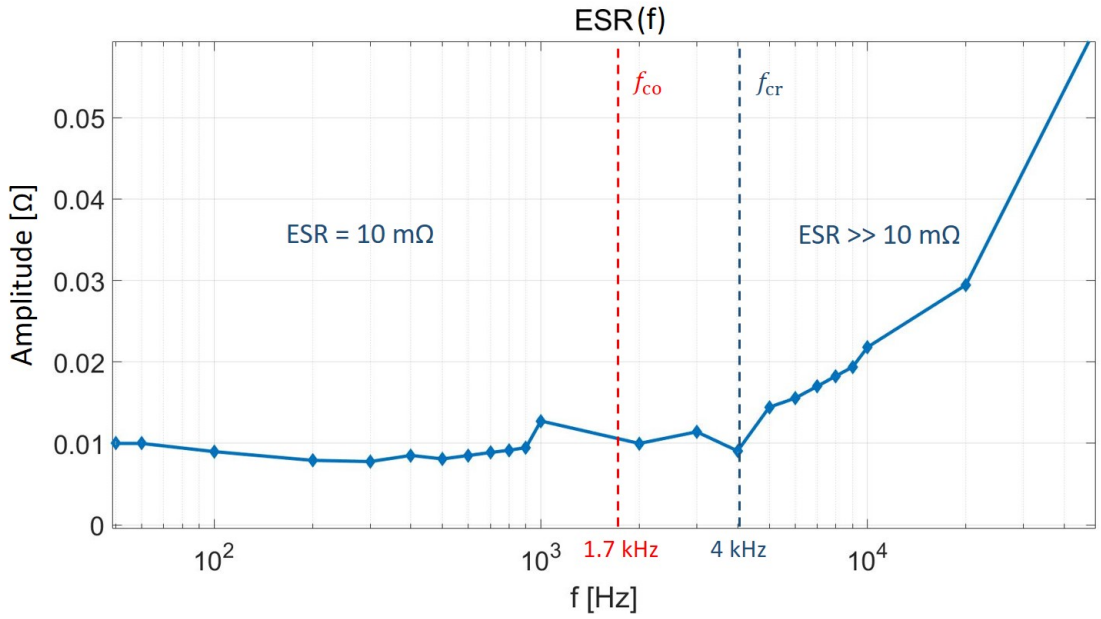

Figure 5.5: Experimentally measured ESR frequency dependency: the designed filter is a low pass filter with a cut-off frequency f_{co}=1.7 kHz. It is important durign the designing phase to keep this value within the safe operating range ($f < f_{cr}$) since a higher ESR leads to higher losses and shorter lifetime of the supercapacitors.

controller has been configured thanks to the TwinCAT software [58] installed on a laptop: this software allows to emulate a programmable logic controller (PLC) on a windows operative system without any need to program a physical controller (PLC, FPGA...). The laptop is connected via Ethernet connection to a CU2508 EtherCAT port multiplier: this component has 1 input and 8 output ports, meaning that up to 8 indipendent EtherCAT netoworks in line topology or 4 in ring topology can be controlled in parallel and real-time by the same master. The output signals of the port multipliers are therefore converted first into fiber optics and than to copper again thanks to two CU1521 EtherCAT media converters in order to ensure galvanic isolation between master and slave. The last terminal of the network is the EtherCAT slave controller (ESC) which is a "XMC4800 Relax EtherCAT Kit" with a XMC4800 microcontroller integrated. The microcontroller board is mounted on an in-house developed board, called "power stage PCB". This board is shown in Fig. 5.7 and it has the following main functions: 1) converting the microcontroller 3.3 V output signals into 15 V level required by the gate drivers; 2) adapting the measurement signals (voltage, current and temperature) for the microcontroller ADC input (3.3 V); 3) providing power supply to the whole electronics of the submodule (microcontroller, measurement systems, EtherCAT devices...). Supercapacitor module voltage and submodules's current are measured thanks to two isolated LEM sensors [59]: the first one is a DVC 1000-P voltage transducer which can measure up to 1 kV AC, while

the second one is a LEM LF 1005-S that can measure up to 1kA AC. The voltage transducer needs 5 V of input voltage and produces an output voltage signal proportional to the input in the range of 0-5 V. The current sensor provides an output current proportional to the measured one and it is loaded with a resistor: depending on the value of such resistor the output voltage (proportional to the output current) can be adjusted in the required range. The temperature as already explained is estimated thanks to the voltage measured over the NTC resistor integrated in the IGBT modules and its value is adjusted by a voltage divider.

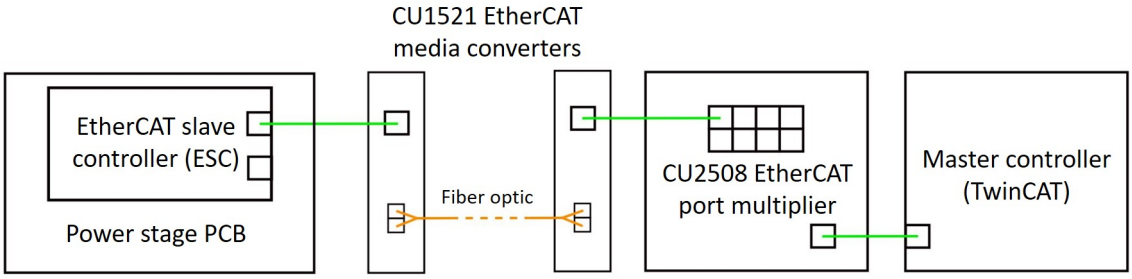

Figure 5.6: Example of EtherCAT network required to control a submodule: the master controller is a virtual PLC realised by the help of TwinCAT. The master communicates via a port multiplier (to keep scalability possible) and two media converters (to avoid electromagnetic interferences) to the slave controller. The slave controller board is directly mounted on the power stage PCB.

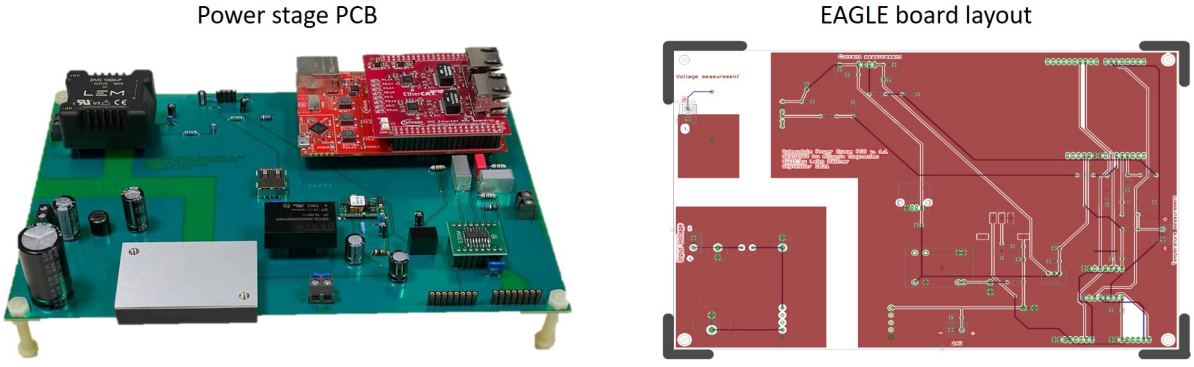

Figure 5.7: Power stage PCB (left) and its EAGLE layout (right): this board acts as an adapter between the microcontroller and measurements components/gate drivers. The board is also used to power all the electronic components of the submodule by taking the power directly from the supercapacitor module. The PCB has been designed on the EAGLE software.

5.1.2 130 V / 750 A operation

In order to validate the designed submodule some experiments have been performed. In the full-scale device each submodule is expected to have mainly a pulsed DC operation, especially for the application of the ASDEX Upgrade TF coil. However in order to keep the project flexible and ready to be used also for AC applications, the single submodule has been tested in AC conditions at its full power (130 V / 750 A). Fig. 5.8 shows a photo of the final setup of the submodule. In the photo the LEM current sensor is visible, while a second CU1521 is present due to the fact that the submodule has been built with the idea to be operated in ring topology (redundancy) with up to three additional submodules. The whole electronics shown in the photo is fixed on an isolated board placed on the supercapacitors module. The submodule has been tested on an ohmic-inductive load to mimic a small-scale magnetic coil. The experiments involved slowly charging of the supercapacitors module first, to discharge them on the load for about 10 s, afterwards. The main goals of the tests are two: the first one is to analyse the switching event and monitor the overvoltages seen from both IGBT and supercapacitors; the second goal is to keep operation continuous for 10 s and check whether all the components have been well designed and/or the submodule needs forced air cooling. For these tests no feedback control has been applied, therefore the load R/L ratio has been chosen in order to provide 750 A of load current with v_{SC}=130 V and at the same time providing a dynamic fast enough to switch from +750 to -750 A during a single switching period. The main parameters of the experiments are described in Tab. 5.4 and the equivalent schema of the setup is shown in Fig. 5.9.

Parameter	**Symbol**	**Value**
Supercapacitors module voltage	V_{SC}	130 V
Submodule current	I_{SM}	+/-750 A
Switching frequency	f_{sw}	25 Hz
Pulse lenght	t_{pulse}	10 s
Load inductance	L_{Load}	50 μH
Load resistance	R_{Load}	0.17 Ω

Table 5.4: Main parameters for the performed 130 V / 750 A experiments.

Fig. 5.10 shows the experimental results of the tests described above. The figure consists of 8 curves: the first 4 curves are v_{SC}, the half-bridge voltage v_{HB}, i_{SC} and i_{SM} (=i_{Load} in this case since operating with a single submodule); the last 4 curves (bottom) represent the same curves but in a different time-scale in order to focus on the transient dynamics. v_{SC}=130 V at the beginning of the test and due to relatively high resistance of the load it drops to 60 V at the end of the experiment. v_{HB} follows approximately the shape of v_{SC} with two main differences: in steady-state condition there are only a

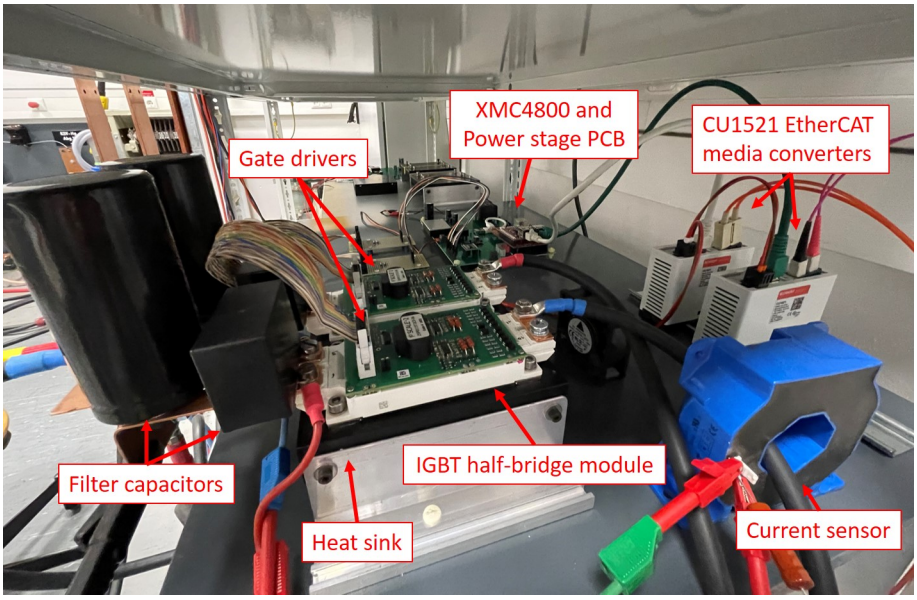

Figure 5.8: Submodule experimental setup: the main submodule components are shown. An additional CU1521 has been added to the first one in order to be able to configure the EtherCAT network in ring topology, which means that redundancy can be ensured.

few volts of difference due to the internal losses of the submodule (mainly generated from the filter resistance), while during transients the difference is larger due to the filter inductance, which reduces the overvoltage seen by the supercapacitors (131 V) but increases the one at the terminals of the power stage (140 V). The supercapacitors and IGBT voltage limits are 135 V and 650 V, respectevely, which means that these operating conditions are sustainable for the chosen components. In terms of current, i_{SC} and i_{SM} have approximately the same amplitude of 750 A at the beginning of the test, but due to the absence of any feed-back control loop they both decrease during the pulse together with the source voltage (v_{SC}). The main difference between i_{SC} and i_{SM} is that the first one is always positive (neglecting fast transient dynamics) while the second one is AC due to the IGBT full-bridge operation. This configuration has the highest $\mathrm{d}i_{SM}/\mathrm{d}t$ (worst case scenario, from -750 to +750 A in a few μs) and therefore the results are valid also for the half-bridge operation (submodule switching from state 1 to state 2 or 3 instead of 4). i_{SC} is basically a DC constant current and due to the fact that the sucpercapcitors modules have been designed for a continuous current of up to 820 A with these conditions no relevant temperature increase has been measured over the module (less than 4 °C). The IGBT are rated for 700 A continous, but i_{SM} does not flow continously into the same IGBT. Each IGBT indeed conducts only during half of each period meaning that they work in discontinous mode and can therefore work with higher currents than the nominal one (i_{cMAX}=1200 A). Without any forced air cooling, the maximum increase of temperature measured over the power stage after 10 s pulses has been 10 °C, far away from the

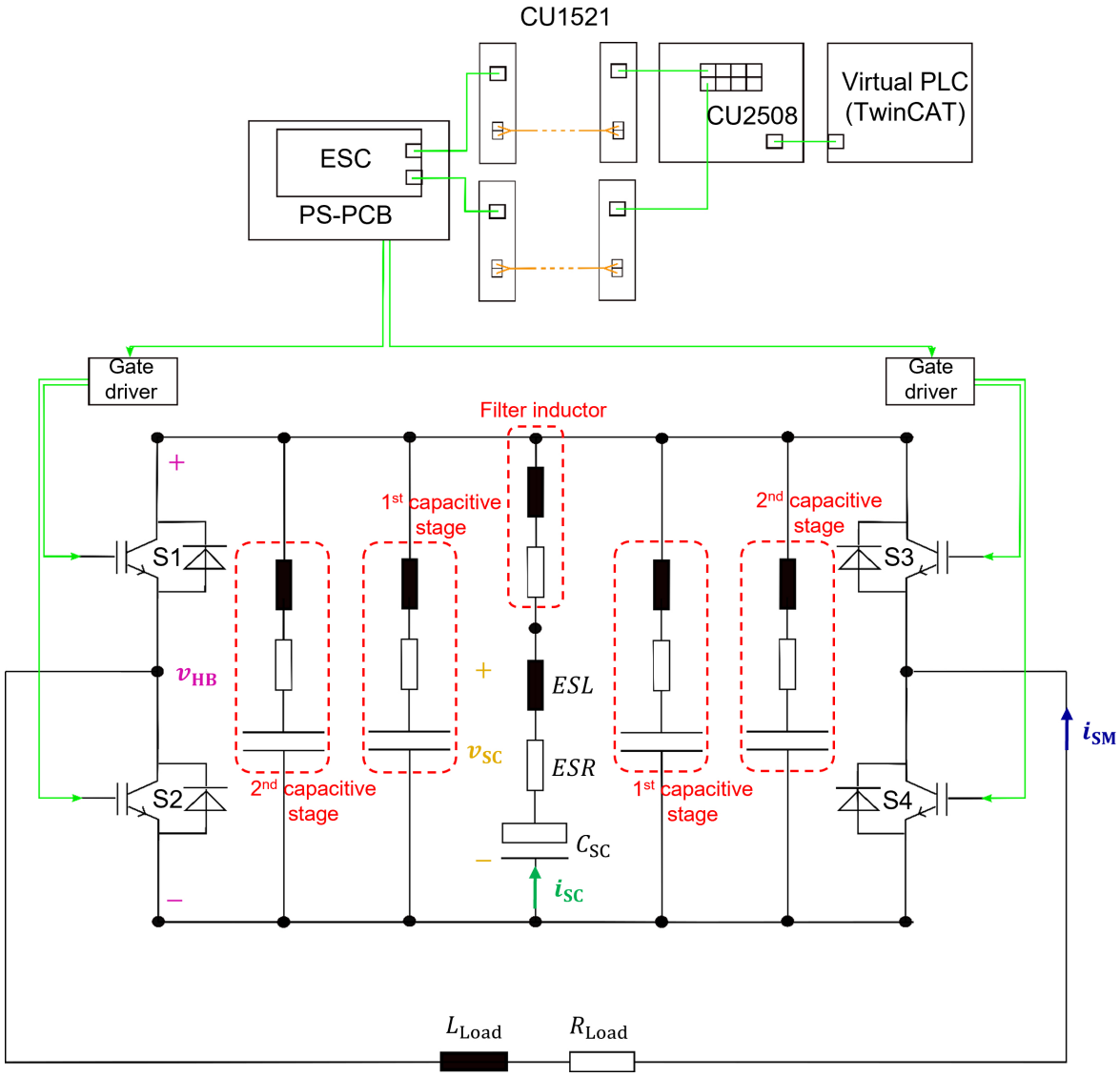

Figure 5.9: Equivalent schema of the submodule experimental setup: four CU1521 allow the ring configuration of the communication network. The power stage filter components have been highlighted in red, while the supercapacitors module is represented by its equivalent circuit.

maximum operating temperature of 150 °C. Some tests have been done also with a 1 W fan and at the same conditions the power stage temperature has been kept constant for the whole pulse. Due to the long dwell-time of 15 minutes (enough to cool down at room temperature without forced air cooling) it has been decided to keep the submodule with natural air cooling. Several submodule components such as filter capacitors and inductor, connection cables and copper bars, can still be optimized, but for the purposes of the above described tests they are sufficient and the safe operation for continous 10 s pulses

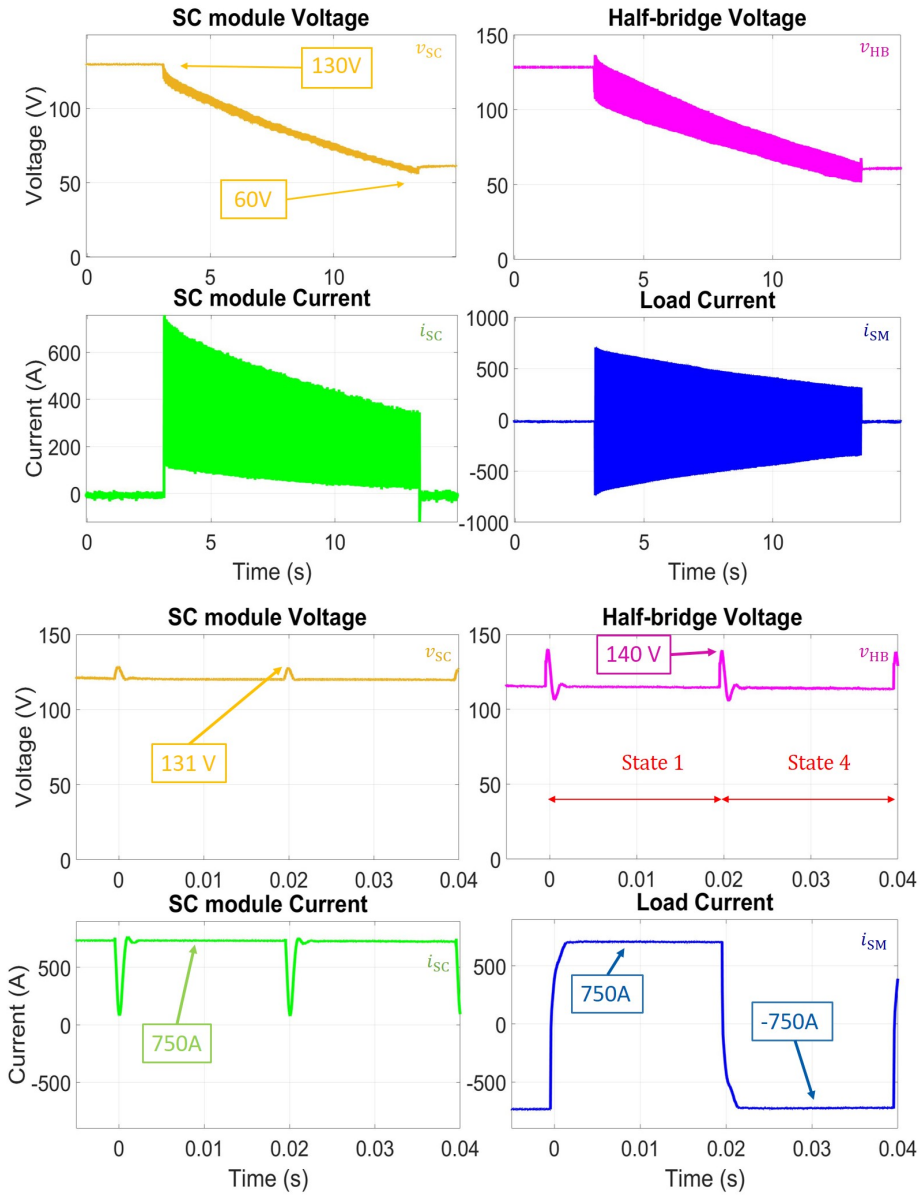

Figure 5.10: Single submodule tests experimental results: the upper 4 plots represent the main submodules electrical parameters measured during a typical 130 V / 750 A pulse. The lower 4 curves represent the same parameters but in a different time-scale to observe their behavior during transients.

has been demonstrated. The next step consists in building three additional identical submodules to test their combined operation, as described in the next section.

5.2 The 4-SM prototype

After having properly designed and tested the single submodule, three additional submodules have been built in order to test them in serial, parallel and combined serial/parallel operation. The serial operation is useful to test the developed control strategy, the parallel one is crucial for the scalability of the system and their combination validates both aspects. Before showing the experimental results, however, an overview of the demonstrator experimental setup is given.

5.2.1 Configuration and components

As already mentioned the developed demonstrator is composed mainly by four submodules, identical to the one described in Ch. 5.1. Its configuration and main components are shown in Fig. 5.11: the submodules are represented with their simplified circuit (measurements signals are omitted from the circuit). The output terminals have been left open since depending on the chosen configuration the load connection can vary. The communication is realised via an EtherCAT network in ring topology: each submodule has two different media converters which are converting the information from fiber optic to copper and vice versa to communicate first with the slave controller and than with the next submodule. The ring topology is fundamental for the parallel operation because of the rendundancy, however in case of serial or mixed operation of the submodules, the network configuration can be rearranged in up to four independent rings thanks to the port multiplier. The four submodules have been placed and mounted on a rack, as shown in Fig. 5.12. The dimensions of the rack are 2 x 0.5 x 0.5 m and it has a dedicated section for each submodule. On the right side of each section there are the output terminals of the submodules: for the parallel configuration copper bars (shown in the photo) have been used to guarantee a proper matching between τ_{Load} and τ_{c} (see Ch. 4.3), while for the serial operation copper cables have been used. The lowest submodule (SM1) is then connected to the output power cables, able to carry more than 2 kA for 10 s.

5.2.2 Serial operation

The first tested configuration of the demonstrator has been the serial one in order to validate the developed control strategy. The main purposes of the described tests were to define a reference load current similar to the one required by the ASDEX Upgrade's TF coil (in terms of shape but scaled-down in amplitude), and to generate an output current

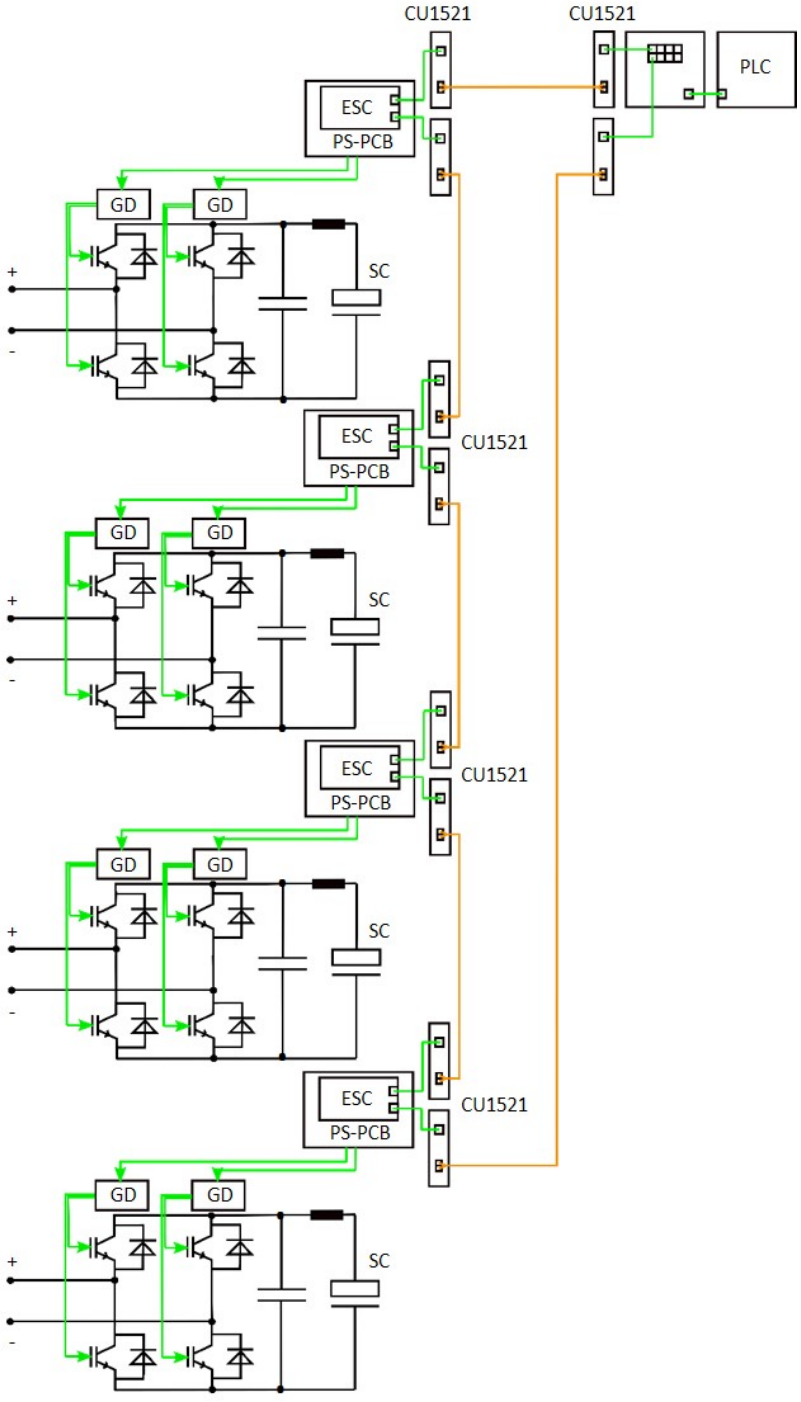

Figure 5.11: Schematic of the demonstrator: the submodules have been represented with their simplified circuit. The schema does not include any load, since depending on the configuration (serial, parallel or mixed) the load connection can change. The submodules are controlled via the EtherCAT protocol with a ring topology: this is fundamental in the case of the the parallel operation. In case of serial (or mixed) operation, instead of a single ring network, four independent rings (or two) can be used thanks to the port multiplier.

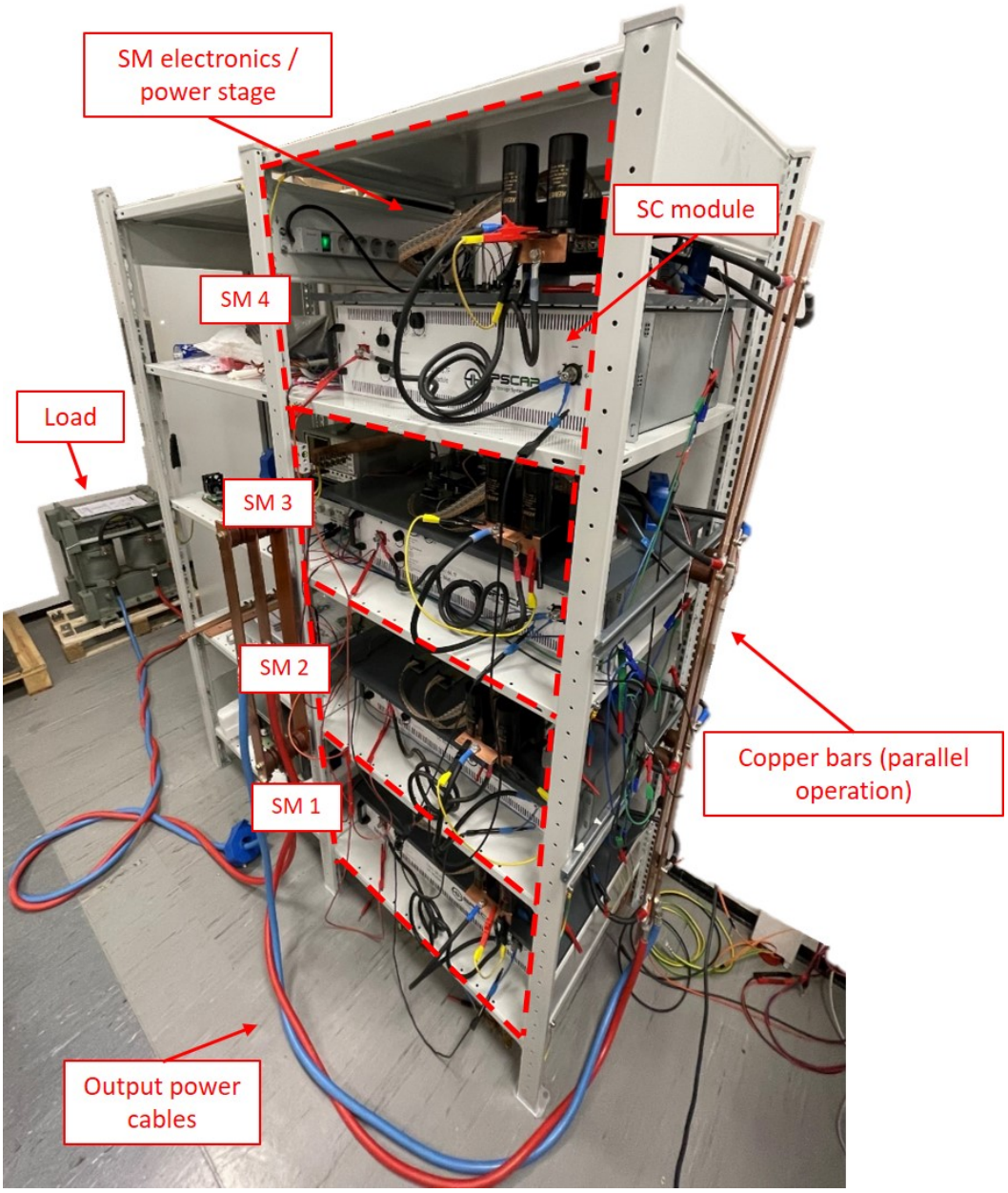

Figure 5.12: The 4-SM demonstrator: the rack is composed of four independent sections containing each a submodule. The output terminals of each submodule are on the right side of the rack and they can be connected either via cables or copper bars (as in the photo). The lowest submodule (SM1) is connected to the output power cables connecting the prototype with the load [60].

as close as possible to the reference, keeping the load current ripple as low as possible with the supercapacitor voltages kept balanced. In other words, the scope of the serial operation is to mimic the full-scale converter operation in a scaled way (only 4 rows are available instead of 23) where each row is composed by a single submodule (instead of 96 in parallel). Fig. 5.13 shows the electrical circuit used for the experiments.

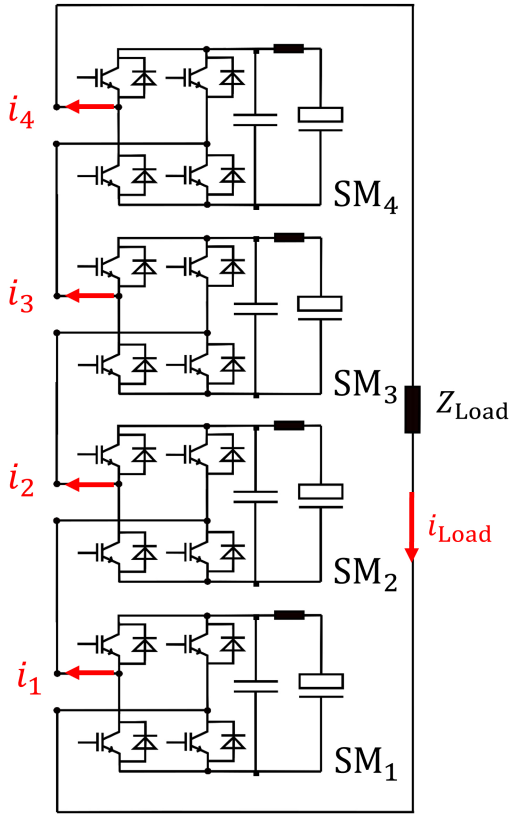

Figure 5.13: Equivalent circuit of the serial operation experiments: the four submodules - by being in series without any parallel submodules - carry all the load current continuously. This current depending on the state of each submodule flows through two of the four switches of each of them.

In this case the load current flows continuously through the four submodules, therefore $i_1 = i_2 = i_3 = i_4 = i_{\text{Load}}$. Two different experiments have been performed in this configuration. The first test consisted in charging the supercapacitor modules at v_{SC}=15 V and to perform then a 1 s discharge with a reference current i_{ref}=200 A. Since the load current ripple depends on L_{Load}, on the switching frequency f_{sw} and on the voltage drop over L_{Load}, a load with a high inductance (5 mH) and relatively low resistance (25 mΩ) has been used. The experimental results of the first test are shown in Fig. 5.14: i_{Load} rises rapidly during the ramp-up phase and reaches its reference with a small overshoot coming from the fact that the controller enables all the available submodules

during this phase; since the submodules (and the controller) are rated for 600 A, its step response is slightly underdamped. During the flat-top phase the controller alternates the number of enabled submodules between 1 and 2 (center curve in Fig. 5.14) in order to limit the load current ripple. This parameter has a maximum of 80 A after the ramp-up which is 40% of the reference current. Once the reference current is zero, the controller disables the 4 submodules and the load current flows through the antiparallel diodes of the submodules half-bridge modules until it reaches zero current (ramp-down phase). The fact that the controller alternated two consecutive voltage levels means that it is properly working. An improper current control would enable/disable too many/too few submodules resulting in a faster load current variation and higher current ripple. The controller enables the submodules depending on their voltage levels according to the voltage balancing algorithm described in Ch. 4.5. Since for this first test reference current and supercapacitor module voltages have been kept relatively low (200 A and 15 V), the voltage balancing algorithm is not as effective as is would be with higher powers. This is mainly caused by two reasons: the first one is the fact that a low supercapacitors current causes a slow discharging of the modules (with respect to the length of the experiment); the second cause is the voltage measurements noise which is not negligible with operating voltages lower than 15 V. The second experiment performed with this configuration consisted in repeating the same pulse of the previous experiment with higher current and voltage. In particular the reference current has been set to 600 A and the supercapacitor modules have been charged at 25 V. The experimental results are shown in Fig. 5.15. As for the first test, the load current reaches as fast as possible its reference (all submodules enabled, see center plot of Fig. 5.15) and the first difference with the previous experiment is the lower current overshoot due to the right controller parameters (tuned for $i_{\mathrm{ref}}=600$ A). An higher load current leads to a faster discharging of the supercapacitor modules, as it can be seen from the bottom curve of Fig. 5.15: the four supercapacitor modules start the pulse with 25 V each and finish it with about 17.5 V (with a maximum difference of 2 V between their voltage mainly caused by noise). The maximum measured current ripple for this experiment is 110 A (also after the ramp-up phase as for the previous pulse) which is higher in amplitude but lower in relative terms if compared with the 200 A pulse. In this case it is indeed 18% of the reference current (against the previous 40%) and this improvement is caused by the higher load current (with the same load) and it would have been even higher if the voltage would have been kept the same. An higher $i_{\mathrm{ref}}/v_{\mathrm{SC}}$ ratio provides a lower voltage difference between source and load resistance, as described in Eq. 4.2. In other words, the converter output voltage can be closer to the resistive voltage drop of the load (lower Δv, see Eq. 4.2) and Δi_{Load} is reduced. Another difference between the two pulses is the change of required voltage levels during the flat-top phase: for the 200 A experiment the output required voltage level oscillates between 1 and 2, while for the 600 A pulse it starts with 1 and reaches 4 (maximum available) at the end of the test.

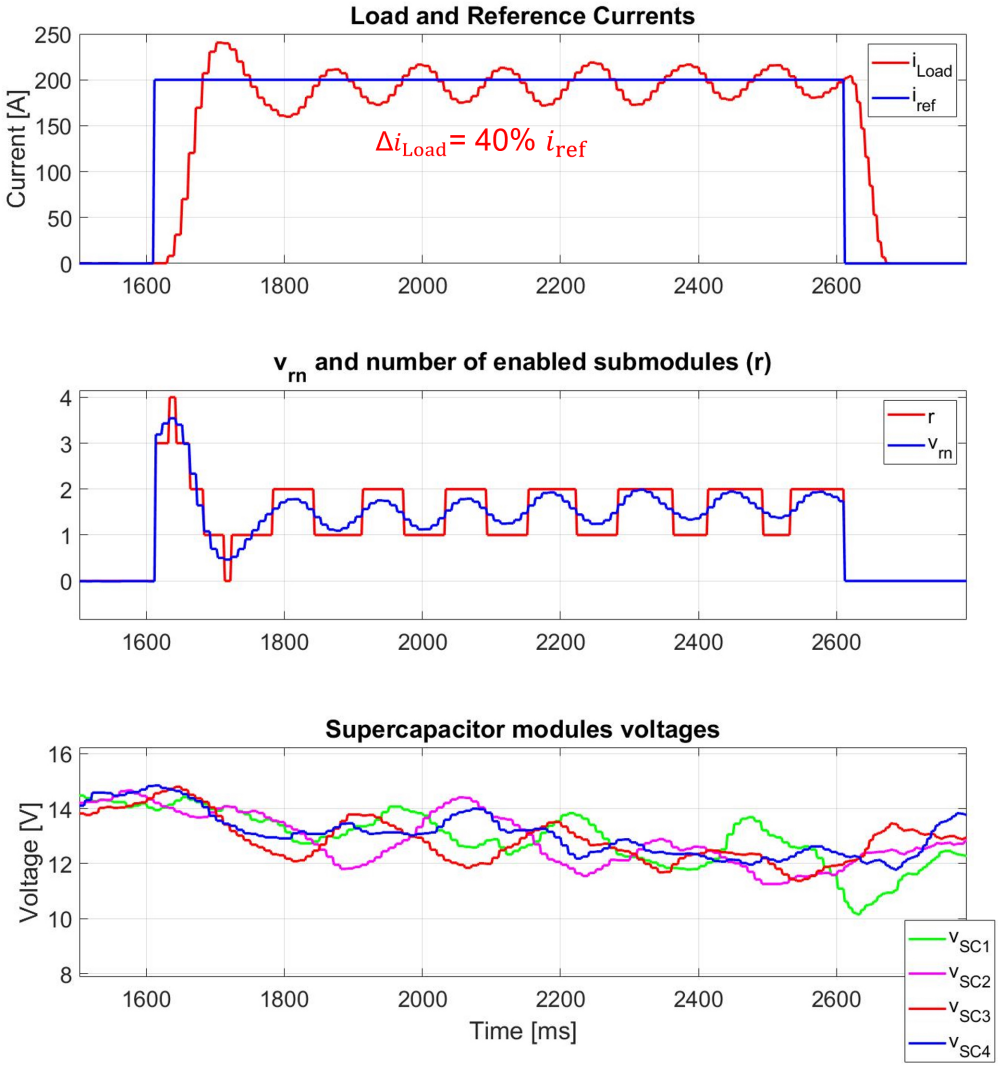

Figure 5.14: Experimental results of a serial operation pulse: two different tests have been done and compared, to show the controller behaviour with different paramters. The first pulse (shown in this figure) has been done with a reference current of 200 A and supercapacitor modules have been charged at 15 V. The maximum measured load current ripple is 40% of the reference current and during the discharge the controller keeps the number of enabled submodules switching from 1 to 2 constantly due to the slow discharging of the supercapacitors.

This difference is caused by the different load current: an higher load current causes a faster discharging of the modules and therefore for the 600 A experiment all the available submodules are required at the end of the pulse to provide the needed output voltage (necessary to generate 600 A). The main limitation of the series configuration is the low power matching between source and load: the sum of all the internal resistances of each

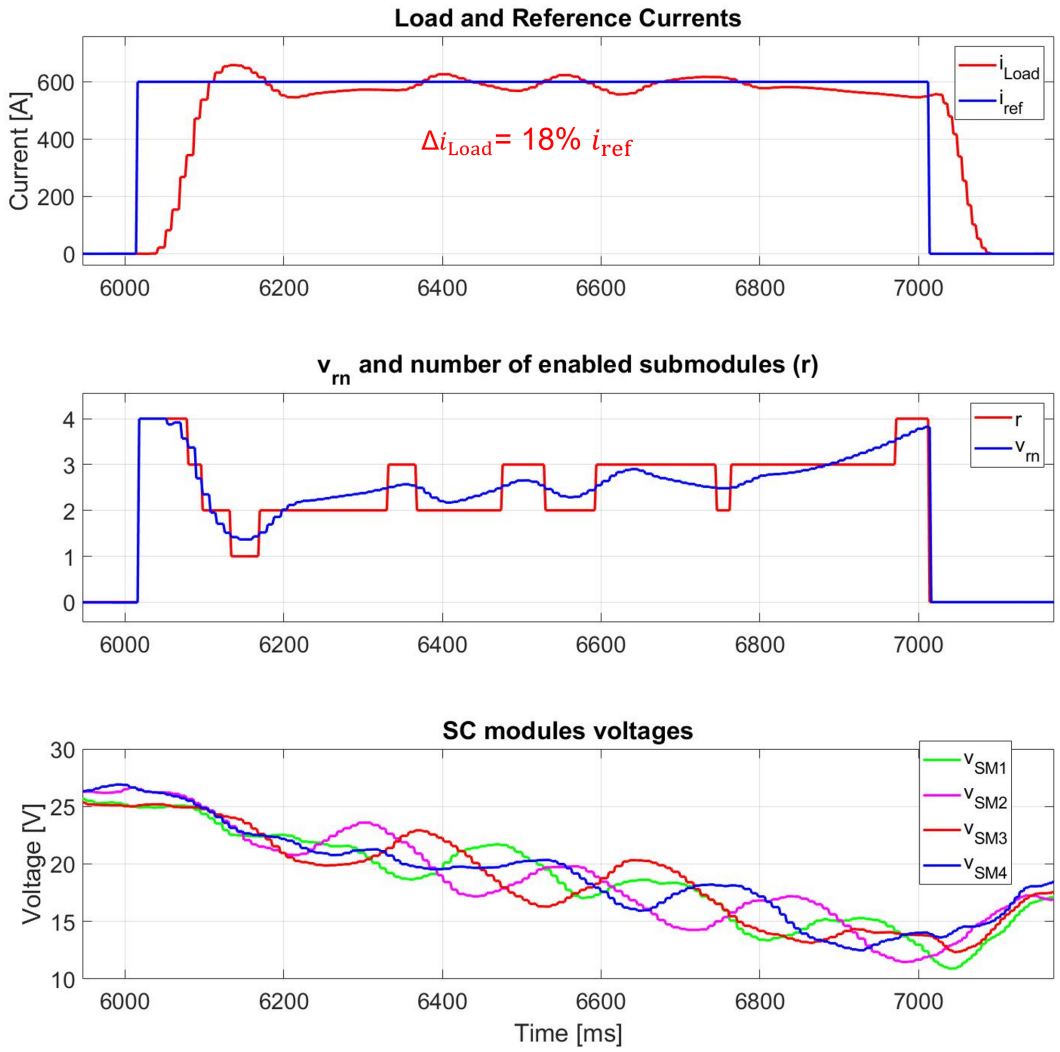

Figure 5.15: Experimental results of a serial operation pulse: the second pulse (shown in this figure) has the same lenght of the first one (1 s, see previous figures) but higher reference current (600 A) and supercapacitor module voltages (25 V). The controller in this case uses all the available submodules since the higher current discharges faster the supercapacitors, and the maximum measured load current ripple is 18% of the reference current due to the higher $i_{\mathrm{ref}}/v_{\mathrm{SC}}$ ratio.

submodule (about 20 mΩ, see Ch. 5.1) are about half of the total load resistance (40 mΩ, mainly composed by R_{Load} and cable resistances). This means that by connecting four submodules in series the total source resistance is double than the load resistance. By connecting several submodules in parallel instead the source total resistance is divided by m (if n does not change) and can became easily negligibile compared to the load resistance. Having a proper power matching is fundamental for a proper power distribution and

avoid to have high source losses. This is the reason why the parallelization of several submodules described in Ch. 4.3 is important and it has been validated in then next section.

5.2.3 Parallel operation

The parallel operation of several submodules has been discussed in Ch. 4.3. The theory has been validated with simulations in PLECS as shown in Fig. 4.17 and the purpose of the test proposed in this section is to confirm - where possible - the simulation results. The experiment indeed consists in charging the supercapacitor modules at V_{SC}=15 V to then discharge them on a 8 mΩ / 750 μH load. The four submodules alternate their states between states 1 and 2 (see Tab. 3.3) with a switching frequency of 50 Hz. The load is an inductor whose time constant is large enough to ensure a continuous conduction mode with these operating parameters. During state 1, S1 and S4 are ON, so the supercapacitor modules are connected to the load: the submodule currents flow through the supercapacitor modules' ESR and filters resistances, which damp any transient oscillations; during state 2 instead the currents by-pass the submodules and they decrease following the natural response of the formed RL circuit according to Eq. 4.32.

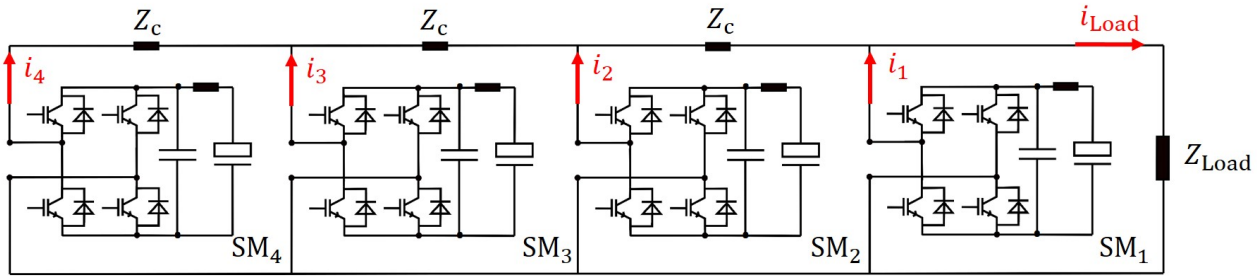

Figure 5.16: Equivalent circuit of the demonstrator in parallel configuration connected to the inductive load: the load current is evenly distributed among the 4 submodules thanks to the design of the busbars connecting them, as described in Ch. 4.3. The impedances in series with the submodules are not represented since they have been minimized and are not the main object of these experiments.

The copper bars have been designed considering as main constraint the load L/R ratio to be equal to 0.09 s. The second considered constraint was the resistance value, to be kept as low as possible in order to reduce losses and additional unbalancing under steady state condition. R_c has been minimized by choosing copper busbars of the maximum available cross section (0.6 x 4 cm) resulting in R_c=0.05 mΩ. This means that according to Eq. 4.39, the voltage loss between first and last modules is:

$$V_{SM1} - V_{SM4} = R_c \cdot I_{Load} \cdot \frac{m-1}{2} = 0.045\ \text{V} = 0.3\% \cdot V_{SC}. \tag{5.2}$$

I_{Load}=600 A has been considered as the highest value reached with the chosen V_{SC}, f_{sw}, and load parameters (see Fig. 5.18). The result obtained in Eq. 5.2 is much lower than the one considered for the full-scale converter proposed in Eq. 4.40 since it scales up with m and load current. The R_c that would be required for a full scale device by imposing the voltage loss of Eq. 5.2 would be impossible to realize and thus for the full-scale converter calculations it has been set to 10% of the supercapacitor module voltage. The required L_c has been calculated via Eq. 4.36:

$$L_c = L_{Load} \cdot \frac{R_c}{R_{Load}} = 4\ \mu\text{H}. \tag{5.3}$$

This value has been physically obtained by fixing a distance of 3 cm between the two busbars. By changing their distance L_c can be modified within the range of 3-6 μH according to the available space of the rack and respecting the minimum distance required for isolation [61]. The experimental results of the proposed tests are shown in Fig. 5.18 and are compared with the PLECS simulation results (Fig. 5.17). Experiments and simulations are compared on three different time-scales. The upper plots show that the load current (in green) is exactly four times the single submodule currents in both states 1 and 2. The central plots show a zoom of the submodule currents, highlighting the proper current sharing (no visible current unbalancing in steady state condition) and simulations and experiments fit well apart from the measurement noise. The last two plots finally compare experimental and simulation results state 1-to-2 transient: although the busbars time constant has been matched with the load one, the prototype has been in-house developed and the exact values of the components can be slightly different from the expected ones. Furthermore, the four submodules have been considered perfectly synchronized in the simulations: the distributed clocks of the EtherCAT network ensures that all the network nodes switch with an average jitter of 10-50 ns with respect to the reference clock (not cumulative). However, higher jitters of up to 500 ns can rarely occur. This is the case of SM_4 in the bottom curve of Fig. 5.18 where an internal current flows among the submodules. Due to the maximum amplitude of the possible jitter however the current unbalancing caused by this fenomena (less than 2 A for 500 μs) can not cause unbalanced discharge of the supercapacitors and the assumption of synchronized switching can still be considered as valid. The shown results therefore validate the theory described in Ch. 4.3 and confirm the scalability of the system (according to described limitations), since a balanced current sharing of the submodule currents leads to a symmetrical distribution of the losses over the parallel submodules, crucial for the lifetime of the supercapacitor modules and their respective power stages.

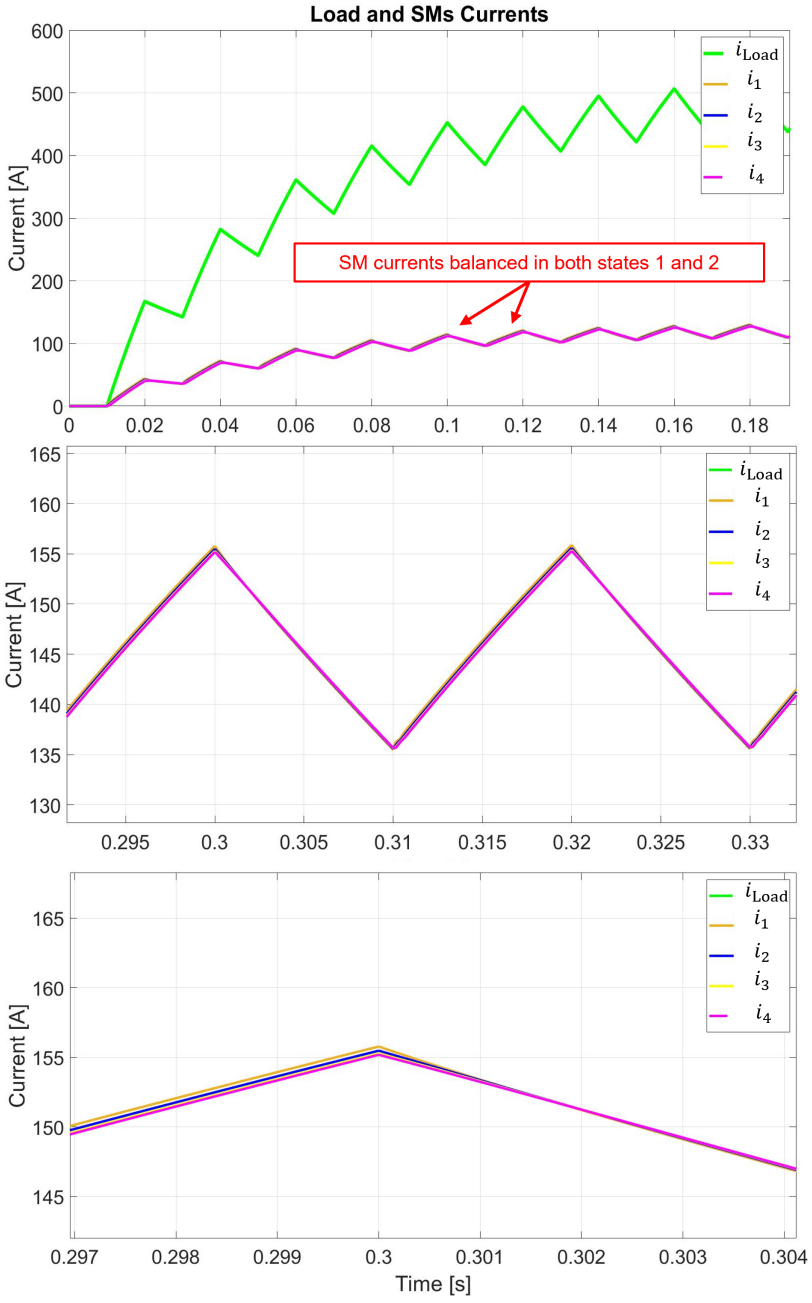

Figure 5.17: Simulations results of the parallel operated prototype: the four submodules receive the same switching commands to switch synchronously from states 1 to 2 with a switching frequency of 50 Hz. The results are shown in three different time-scales. The upper and central plots show that the load current is evenly shared among the submodules in steady state conditions. In the bottom plot they are shown during a transient.

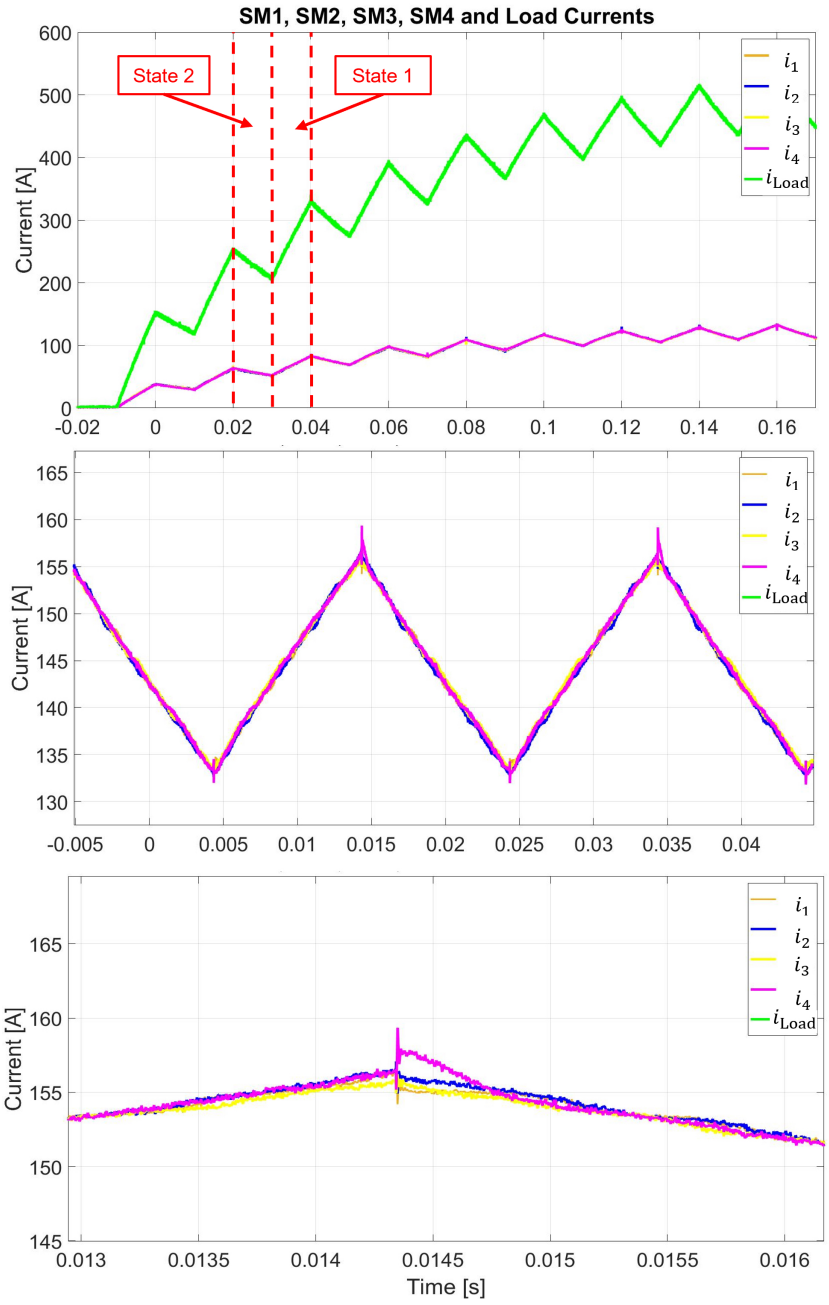

Figure 5.18: Experimental results of the parallel operated prototype: the shown curves validate the simulations shown in the previous figure.

5.2.4 Combined series/parallel operation

After having validated independently serial and parallel operation, the combined serial/parallel operation has been used to repeat the tests done for the serial configuration, but with twice the available energy from the single row, composed first by a single submodule,

while in this case by two of them in parallel. Furthermore, by connecting in parallel two submodules, their ESR (as well as the parasitic resistances of their circuits) have been halved, becoming lower than the load resistance. This was not the case for serial connection of four submodules, where the sum of their circuits' resistances was larger than the load resistance, limiting significantly the possible maximum load current.

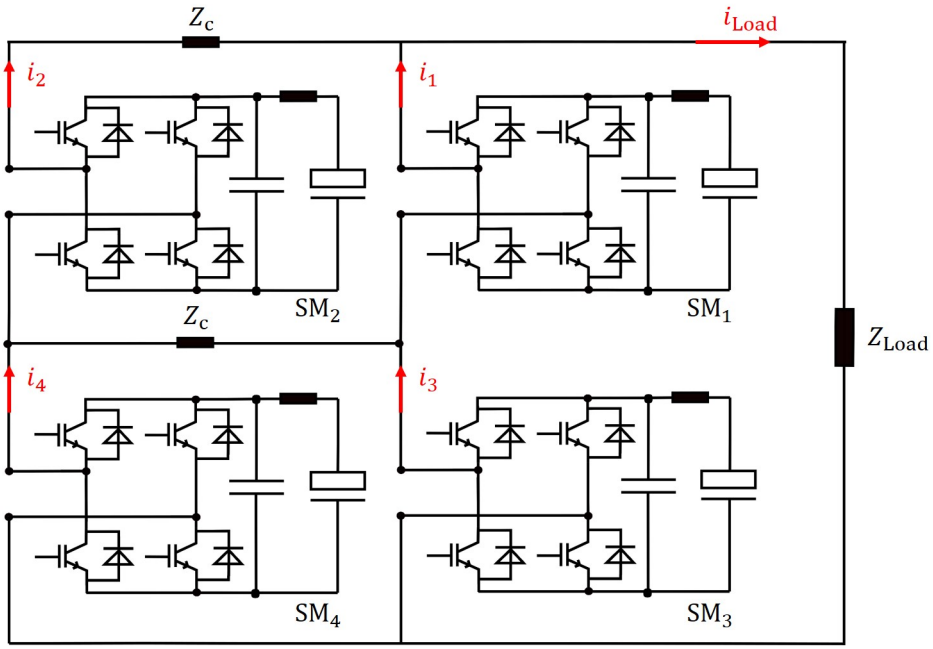

Figure 5.19: Equivalent circuit of the demonstrator in combined serial/parallel configuration: the submodules in parallel switch together as for the case of the full-scale converter, while the two formed rows are enabled/disabled according to the control strategy. Since the submodules belonging to the same row have the same voltage level, only one supercapacitor module voltage per row has been monitored for the control.

Fig. 5.19 shows the demonstrator configuration used for these tests. In this case $i_1 = i_3$ and $i_2 = i_4$ in steady state conditions, therefore $i_{Load} = i_1 + i_2$. The same experiment performed in the serial configuration has been repeated, with V_{SC}=20 V and I_{ref}=600 A. The better power matching between source and load leads in this case to a load current ripple of 45 A (see Fig. 5.20), higher in absolute value than serial operation but much lower in relative terms: in this case it is indeed only 7.5% of the reference current, against the 18% of the previous case (same v_{SC} and load have been used for the tests). The supercapacitor voltages drop from 20 to 12.5 V during the test and recover 2.5 V at the end of it, corresponding to the stored energy into the load inductance. The maximum measured voltage difference between the two rows is about 2.5 V which has also improved in comparison with the series operation: this is due to the fact that with more energy available the row voltage decreases slower considering same switching frequency and

same current (see Fig. 5.14).

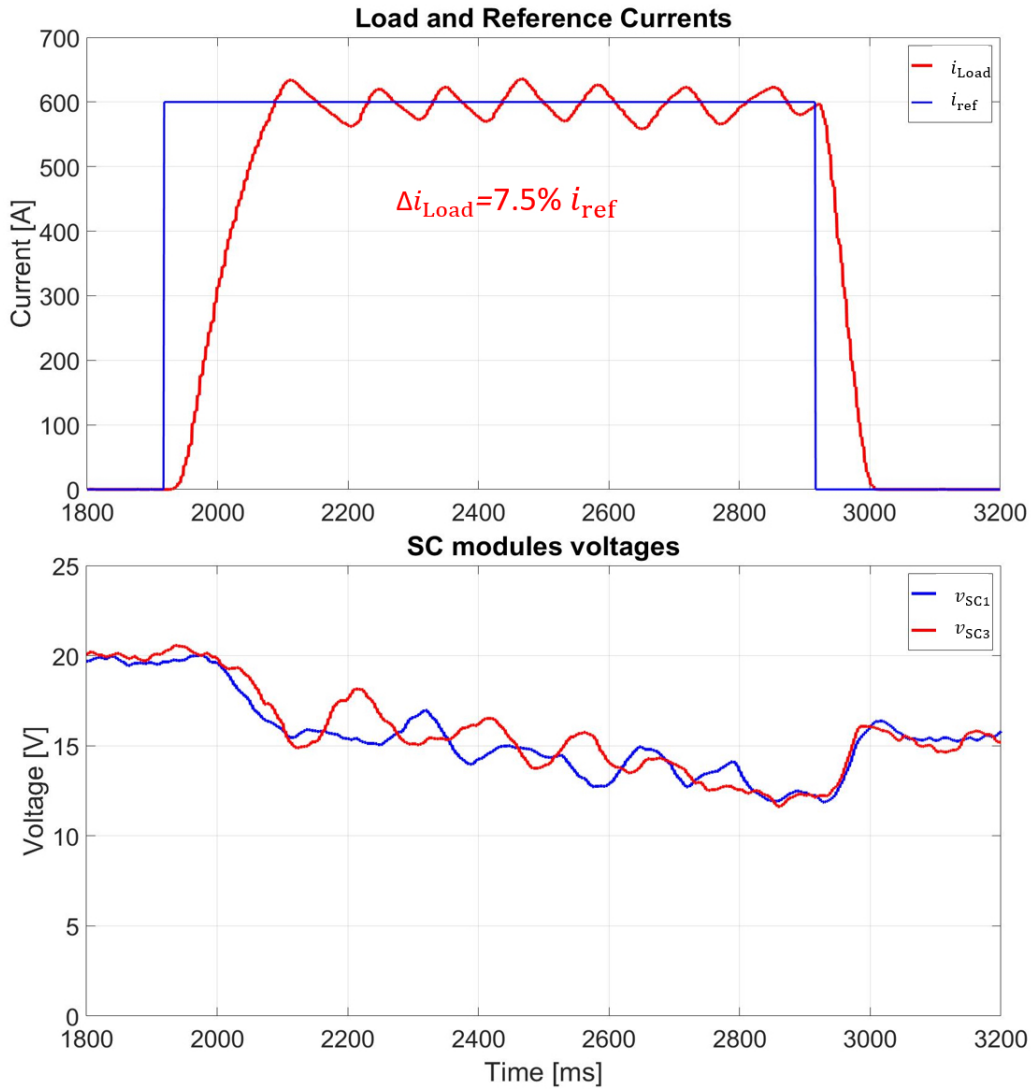

Figure 5.20: Experimental results of the demonstrator tested in combined serial/parallel operation: the load current follows its reference with a ripple of 7.5% as expected (top plot) and the row voltages (bottom plot) are kept balanced during the 1 s pulse thanks to the voltage balancing algorithm, limiting the maximum voltage displacement to 2.5 V. This value decreases (improving the balancing) by increasing the amount of paralleled submodules due to the higher available energy.

The model developed and described in Ch. 4.2.3 has been adapted to 4-SM prototype in the combined serial/parallel configuration. Therefore the 23 equivalent modules have been reduced to 2 blocks, each of which is the equivalent circuit of 2 submodules in parallel. The same parameters of the demonstrator have been used for the simulations in order to simulate the performed experiment. The results of the simulations are shown

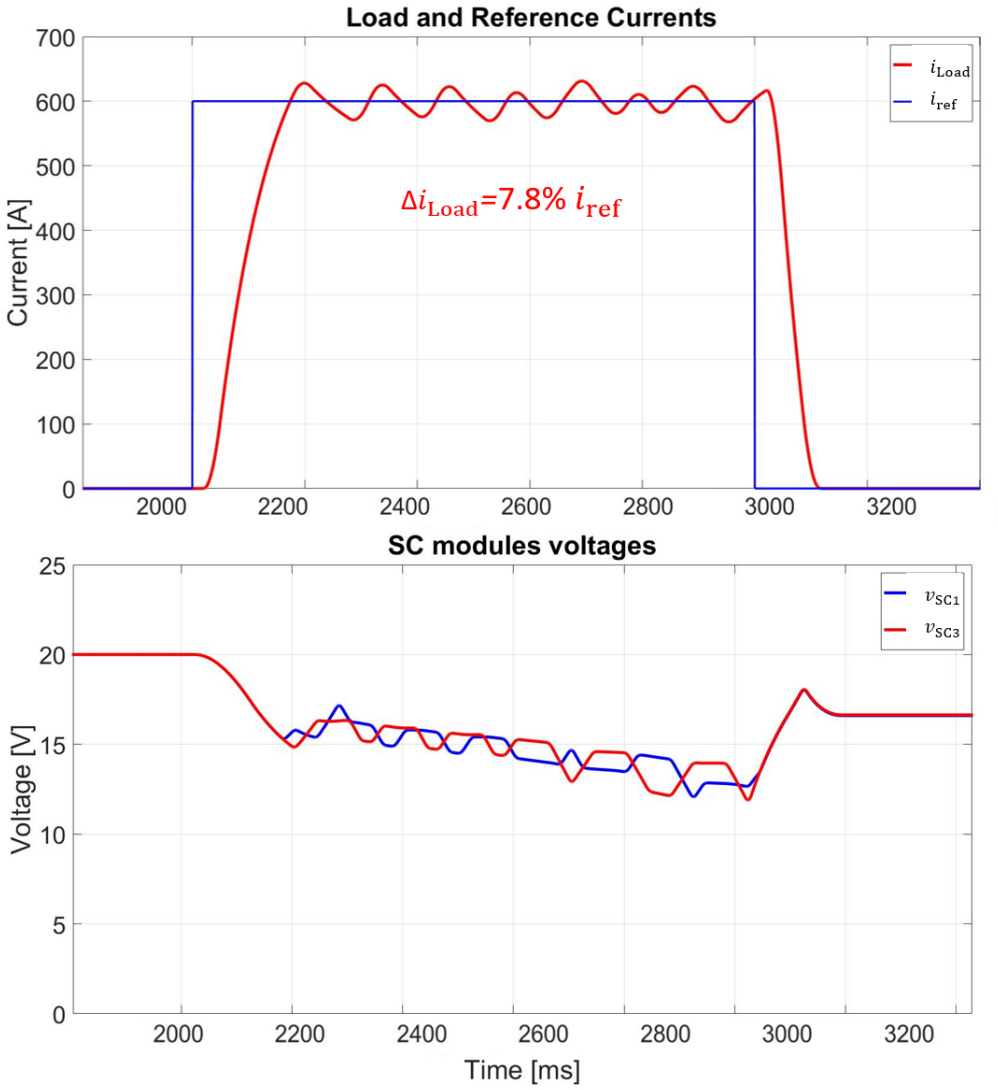

Figure 5.21: The same experiment shown in the previous figure has been simulated in PLECS and the results are very similar to the ones obtained experimentally. This validates the developed full-scale model since the model used for these simulations is an adapted version of it.

in Fig. 5.21. As shown from the curves, the simulation results fit almost perfectly with the experimental results which means that model is a good approximation of the real prototype. The load current ripple produced by the model is 47 A, only 2 A higher than the one obtained with the experiments while the voltage levels of the two rows are basically equivalent to the ones obtained experimentally. Since the model used for these simulations is an adapted version of the one described for the full-scale device, it validates the simulation results shown in Ch. 4.2.3. Therefore the developed model can be used as a reference to scale the prototype to a larger size device.

6 Size estimation and scalability

6.1 Converter efficiency

The converter losses are strictly related to the submodules internal losses. The busbar losses indeed can be negleted since they are several orders of magnitude smaller than submodules losses, which have been described in details in Ch. 4.1.2. In particular the total submodules losses can be estimated mainly via three contributions (see Eq. 4.12): supercapacitor modules, power stage filter and IGBT losses. The IGBT losses can also be splitted in two contributions: conduction and switching losses. However, due to the low switching frequency adopted for this application the switching losses (see Eq. 4.10) can be neglected. Therefore, the efficiency of the converter depends mainly on ESR, i_{SM}, R_{Filter} and $V_{\mathrm{CE,ON}}$ of the IGBT (frewheeling diodes ON voltage is lower but it has been approximated to the one of IGBT to simplify the calculation). Some parameters such as ESR and $V_{\mathrm{CE,ON}}$ however are not constant and depend on supercapacitor modules lifetime and operating temperature, respectively. Thus it makes sense to analyse the converter efficiency for different scenarios, as shown in Fig. 6.1. The figure shows losses distribution among supercapacitor module, IGBT and power stage filter of each submodule for different operating temperatures (25 and 125 °C) at the supercapacitor Beginning Of Life (BOL, ESR= 10 mΩ) and End Of Life (EOL, ESR= 20 mΩ). On the top of the losses distribution, the converter efficiency η_{c} is also provided for each scenario. Fig. 6.1 shows how ESR has a stronger influence than the other parameters on the converter efficiency: between BOL and EOL the ESR variation decreases the converter efficiency by 5 %, while 100 °C of difference of the operating temperature causes the efficiency to drop only of 1%. Furthermore, the ESR temperature dependency has been neglected since it manly increases at the power stage level (IGBT), while the supercapacitor modules will never see an increase of 100 °C. It has been demonstrated indeed that the supercapacitors ESR remains constant with the increase of temperature [32] if the operating temperature is above 0 °C. Only for temperatures below 0 °C ESR is significantly affected by a change of temperature due to the change of viscosity of the electrolyte, but these operating temperatures are not forseen for the current application. Between best and worst case scenario, η_{c} has 6% of difference and it is important to point out that the numbers shown in Fig. 6.1 have been calculated considering the operation during the ramp-up phase, when the converter provides the maximum output power. In particular for the

efficiency calculation a submodule output power of 70 kW has been considered (V_{SC}= 130 V, I_{SC}=560 A always ON during the ramp-up), while during the flat-top it would be much lower since the submodules are not always ON, and when a submodule is by-passed i_{SC}=0.

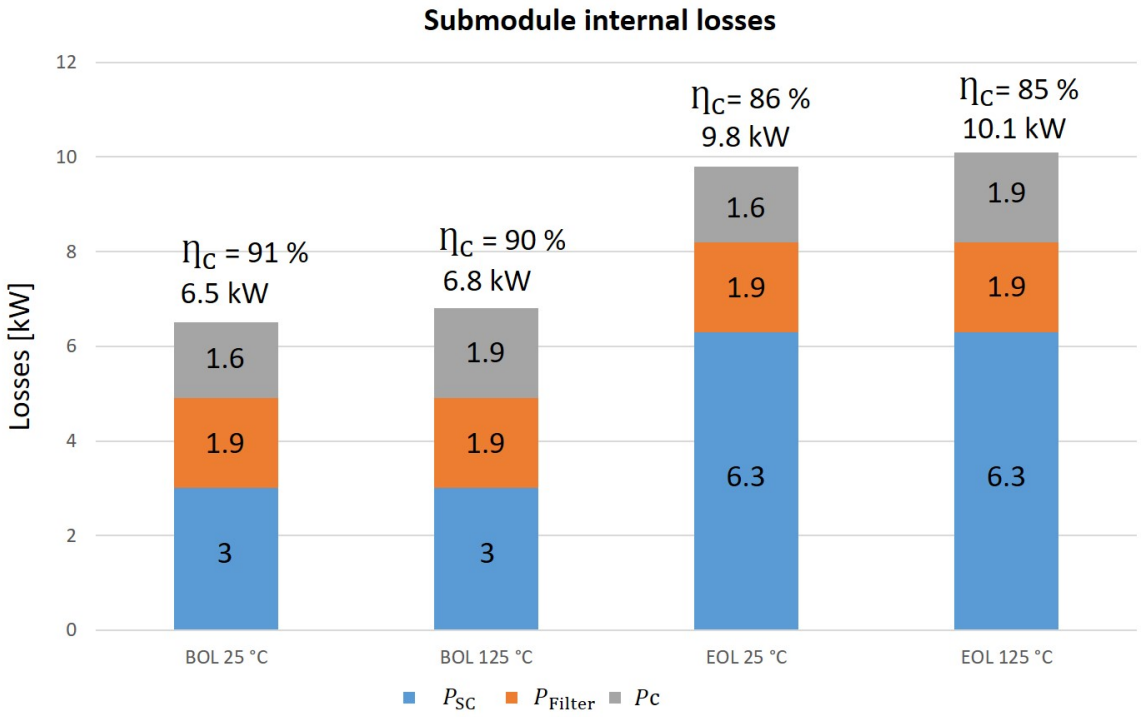

Figure 6.1: Estimated submodule internal losses and efficiency for different scenarios: the different values are due to the different state of life of the supercapacitor modules (BOL and EOL) and temperature (25 and 125 °C) considered for the calculations.

6.2 Size estimation

The reason why the size estimation has been left at the end of the dissertation is the fact that it directly depends on the experimental results of the demonstrator. From the experiments indeed it was possible to estimate that submodule internal losses P_{SM} are approximately the double of the supercapacitors losses P_{SC} (see Fig. 6.1). This relationship is fundamental to estimate the amount of losses of the converter and therefore size it properly. The main constraints used to estimate the number of submodules are voltage, current and energy requirements. The voltage requirement is 3 kV for the ramp-up phase, which is the maximum voltage acceptable by the TF coil. In order to provide a v_{Load}=3 kV with supercapacitor modules of 130 V, 23 rows in series are required. Thus n=23 has

been chosen and the number of arms can be expressed as a function of total number of submodules N_{SM}:

$$m = \frac{N_{SM}}{n}. \tag{6.1}$$

The submodule current i_{SM} can be also expressed as a function of N_{SM}. Considering the required load current is i_{Load}=54 kA indeed:

$$i_{SM} = \frac{54000}{m} = \frac{54000 \cdot 23}{N_{SM}}. \tag{6.2}$$

In terms of energy requirements, the amount of energy required by the TF coil for a pulse E_{TF} is 800 MJ (see Fig. 3.6) and the pulse energy E_p can be defined as:

$$E_p = E_{TF} + E_w \tag{6.3}$$

where E_w is the total amount of energy lost during a pulse. This energy depends on P_{SM}, on the time length of the pulse t_p and on N_{SM}:

$$E_w = P_{SM} \cdot t_p \cdot N_{SM} = 2 \cdot P_{SC} \cdot t_p \cdot N_{SM} = 2 \cdot i_{SM}^2 \cdot ESR \cdot t_p \cdot N_{SM} = 2 \cdot (560)^2 \cdot 2 \cdot 10^{-2} \cdot 10 \cdot N_{SM}. \tag{6.4}$$

According to the charging process and due to the fact that supercapacitors capacitance can vary with their voltage level, not all the stored energy should be used and a fraction of it should be left in the supercapacitor modules in order to ensure that v_{SC} is never lower than 38 V (see Eq. 4.15). The total amount of stored energy can be therefore defined as:

$$E_s = E_p + E_u \tag{6.5}$$

where E_u is the unused energy and can be expressed as:

$$E_u = N_{SM} \cdot \frac{1}{2} \cdot C_{SC} \cdot v_{SC}^2 = N_{SM} \cdot \frac{1}{2} \cdot 67 \cdot (38)^2. \tag{6.6}$$

The total number of submodules can be finally calculated as:

$$N_{SM} = \frac{E_s}{E_{SC}} = \frac{E_{TF} + E_w + E_u}{E_{SC}}, \tag{6.7}$$

where E_{SC}=600 kJ (see Tab. 5.1). By combining Eq. 6.7 with Eq. 6.4 and 6.6 it turns out that the number of required submodules is 2200. This leads to a total stored energy of 1.15 GJ, with 150 MJ of unused energy (38 V left per module) and 200 MJ of lost energy (due to internal losses, see Fig. 6.1). According to m=96, the single submodule current is i_{SM}=560 A. In terms of volume, the demonstrator rack containing 4 submodules has a volume of about 0.5 m^3 (2 m x 0.5 m x 0.5 m), therefore 550 racks containing 2200

submodules would require 275 m^3. Some additional volume has to be taken into account to have direct access to all the submodules in case of need of replacement. By considering an additional volume of 125 m^3 thus the total volume required amounts to about 400 m^3, approximately the same volume occupied by the flywheel generator EZ2. The volume that would be occopied by rectifier/charger has not been considered since this has not been take into account for EZ2 as well, which has actually also an additional room for the cooling system that has also not be counted to compensate the 900 MJ of difference of total stored energy between the two systems (2 GJ for EZ2, 1.15 GJ for the proposed system).

Parameter	**Symbol**	**Value**
Number of submodules	N_{SM}	2200
Number of submodules in parallel	m	96
Number of submodules in series	n	23
Total stored energy	E_s	1.15 GJ
Energy internally dissipated	E_w	200 MJ
Energy dissipated in the load	E_{TF}	800 MJ
Unused energy	E_u	150 MJ
Rated load current	I_{Load}	54 kA
Rated submodule current	I_{SM}	560 A
Rated load voltage	V_{Load}	3 kV
Rated submodule voltage	V_{SC}	130 V
Supercapacitor modules mass	M_{SCtot}	90 t
Total converter mass	M_{tot}	120 t

Table 6.1: Main parameters of the proposed converter.

6.3 Scalability limits

This dissertation has provided the main information required to scale up the developed prototype. However, although this concept is theoretically scalable without hard limitations, there are actually constraints that can became limitations depending on the application for which this concept has to be used. Starting from the charging phase, the main limitations are the pre-charging current i_{PC}, the rectifier voltage v_i and the minimum voltage per module v_{SCmin} which is required to start the boost charging phase. i_{PC} has to be at least one order of magnitude higher than the leakage current of the supercapacitor modules (if not active balancing circut is present) since otherwise the pre-charging time would significantly increase (it would became infinite if the two currents would be the same). v_i has an upper hard limit given by the minimum voltage level reached at the end of

each pulse by the whole submodules matrix. If v_i is higher than $n \cdot v_{SCmin}$ at the end of a pulse, the converter can not be charged again by connecting it directly to the diode rectifier (see the boost charging phase, Ch. 4.1.3). Another contraint to take into account is the charging time, both for pre-charging and boost-charging phase. According to the current application the pre-charging time has to be short enough to charge at v_{SCmin} all the supercapacitor modules before the start of the first pulse of the operaiton day. The boost-charging time instead has to be shorter than the dwell time of ASDEX Upgrade which is 15 min. Switching to the communication protocol, the main limitations are the maximum number of nodes per EtherCAT network (64k) and the fact that only one failed node per network can be handled without interrupting the normal operation. This means that maximum n submodules can simultaneously fail (during the same pulse) without the need to loose any row. If more than one submodule per row fail however the full row where this happens can be by-passed and operation can continue with a voltage level less available. In terms of hardware, the main scalability limit of the communication is the port multiplier which currently has only 8 outputs, which means that it allows to operate up to 4 networks in ring topology. If the system needs to be scaled up and $n>4$, a new port multiplier is required. This is also the main limit of the maximum number of rows that can be operated in series. The serial operation of several row does not have any other hard limitation apart from isolation contraints to be taken into account. The parallelization of several submodules instead is different and there are some rules to take into account if scaling up. If busbars and load have the time constant matched the current is equally shared among the parallel submodules during transients, but a cumulative steady state current difference is still present due to the resistance of the busbars, as shown in Eq. 4.39. By minimizing the busbars resistance the losses over the busbars are also minimized, but with very large m the difference of current between first and last submodules of the matrix can become relevant. This is the main limit of the parallelization of submodules and by imposing the maximum acceptable losses between first and last submodules (with a given busbars resistance) the maximum m can be estimated from Eq. 4.39. Furthermore, another constraint to take into account is the cross section of the busbars. The busbars closest to the load have to carry almost the whole load current ($m - (1/m)$ times it) while the farthest ones have to carry $1/m^{th}$ of it. This means that the cross section of closest busbars should be larger than the other ones, but in order to be able to change the configuration (for example by connecting the load to the converter through a different point) all the busbars should be evenly sized.

7 Conclusion

7.1 Validated results

The presented dissertation described the work conducted to develop a MMC demonstrator composed of 4 submodules. Before building the prototype, a PLECS model has been developed and some simulations have been performed to find out the best way to build it. The main crucial points studied and/or validated can be summarized as follows:

- *Control strategy*: the developed control strategy has been tested on the prototype, validating the model for the full-scale device that ensures a load current ripple of 0.04% of the load current reference (the requirement of the ASDEX Upgrade TF coil is 0.1%);

- *Filtering needs*: the supercapacitors modules can not be directly connected to their respective power stages, but they require a filter. All the relevant information about filter sizing have been provided in Ch. 4.1.2;

- *Reliability*: the converter is fault tolerant and can operate without any interruption in case of failure of up to one submodule per arm thanks to its real-time fault detection system. The fault of a single submodule, of a whole row and external short circuits have been individually analyzed and a proper counteraction has been proposed in Ch. 4.4 for each different scenario;

- *Scalability*: the parallel operation experiments validated the scalability of the converter. If a proper time constant matching between load and source is ensured, the scalability of the converter is limited only by the ohmic losses of the busbars which can be quantified via Eq. 4.39;

- *Flexibility*: the designed converter is capable of 4-quadrant operation. This means that apart from this specific application, it can be used to power different loads for fusion and/or non-fusion applications. In this regard the bandwidth of the designed converter (25-125 Hz) should be properly adapted (i.e power stage filter and controller, see Ch. 4.5 and 4.1.2).

7.2 Critical points and challenges for a full-scale device

Even though the main goals of the project have been achieved, there still are some critical points to be faced before proceeding with the building up of a full-scale converter. These points can be summarized as follows:

- *Power stage filter optimization*: the designed power stage filter is a laboratory prototype (see Ch. 5.1). Therefore it is not optimized both in size and cost, and a proper optimization is recommended in case of scaling up of the converter;
- *Losses reduction*: due to the main application for which this prototype has been built, losses (shown in Ch. 6.1) minimization has been not the main focus of the work. In case of usage of the proposed converter for applications where low losses are a priority, this has to be kept into account;
- *Control optimization*: one of the main limits of the propotype control comes from the adopted 'plug&play' microcontrollers and by upgrading them the speed of the control can be significantly improved. Furthermore, the EtherCAT port multiplier used for the prototype supports up to four indipendent networks in ring topology and therefore in case of need of more that four rows a proper port multiplier should be designed accordingly for the specific application.

The above described points are the main recommendations for a potential scaling-up and/or an optimization of the demonstrator. Apart from those, there are several additional small points that may be optimized/changed which are however not relevant for the proper operation of the converter. Defining if or which other components should be upgraded will be a task that future designer/s should face depending on the application of the converter.

8 Author publications, students and curriculum vitae

8.1 List of main publications

[62]	C. Terlizzi, **A. Magnanimo**, F. Santoro, S. Bifaretti, Development of a Scalable MMC Pulsed Power Supply through HIL Methodology *Energies*, 2023, 16, 4106. DOI: https://doi.org/10.3390/en16104106
[60]	**A. Magnanimo**, G. Griepentrog, F. Santoro, C. Terlizzi, M. Teschke, Development of a MMC demonstrator for nuclear fusion devices power supplies. *Fusion Engineering and Design*, 2023, Volume 188. DOI: https://doi.org/10.1016/j.fusengdes.2023.113433
[47]	C. Terlizzi, D. Berardi, S. Bifaretti, **A. Magnanimo**, F. Santoro, M. Teschke, Voltage balancing algorithm of a MMC-like topology for pulsed power applications, *2022 AEIT International Annual Conference (AEIT)*, 2022. DOI: https://doi.org/10.23919/AEIT56783.2022.9951782
[57]	**A. Magnanimo**, M. Teschke, G. Griepentrog, Full-bridge submodule development of a MMC-like topology for ASDEX Upgrade Toroidal Field Coils Power Supply, *IEEE Transaction on Plasma Science*, 2022. DOI: https://doi.org/10.1109/TPS.2022.3179624
[27]	**A. Magnanimo**, M. Teschke, G. Griepentrog, Supercapacitors-based power supply for ASDEX upgrade toroidal field coils, *Fusion Engineering and Design*, 2021, Volume 171. DOI: https://doi.org/10.1016/j.fusengdes.2021.112574

Table 8.1: List of the publications where the candidate has been the first or one of the main authors.

8.2 List of supervised students

[63]	R. Maltry, Bachelor's thesis in Electrical Engineering, *Technical University of Darmstadt*, 'Entwicklung eines Ansteuerkonzepts für einen 3-phasigen MMC Umrichter mit Aufbau und Test der Ansteuerelektronik'.
-	A. Aminger, training during Bachelor's in Energy Engineering, *Montanuniversitaet Leoben*, 'Filter optimization of a converter module based on supercapacitors'.
-	L. Haffner, training during Bachelor's in Energy Engineering, *Hochschule Kempten*, 'PCB's optimization via EAGLE'.
-	F. Herschmann, training on PCB soldering during Bachelor's in Physics, *Technical University of Munich*.
[49]	D. Berardi, Master's thesis in Energy Engineering, *University of Rome 'Tor Vergata'*, 'Development of the voltage control strategy for a MMC-like topology applied to ASDEX Upgrade'.

Table 8.2: List of supervised students.

8.3 Curriculum vitae

Antonio Magnanimo
born on 4th February 1994
in Naples, Italy

Experience

- Feb 2019 - Mar 2023: Doctoral research associate at *Max-Planck-Institute for Plasma Physics* in Garching, Germany.
- Mar 2018 - Jul 2018: Trainee at *EUROfusion* in Garching, Germany.

Education

- Mar 2019 - Jun 2023: PhD candidate at *Technical University of Darmstadt* in Darmstadt, Germany.
- Mar 2017 - Sep 2017: Exchange semester at *Technical University of Munich* in Munich, Germany.
- Sep 2012 - Dec 2018: Bachelor's and Master's Degree in Electrical Engineering at *University of Naples Federico II* in Naples, Italy.

Awards

- Dec 2019: EUROfusion Engineering Grant award.

9 Appendix

9.1 Used measurement systems

9.1.1 Voltage measurement

Voltage signals have been measured in real-time with LEM DVC 1000-P transducers. These transducers can read up to 1500 V and have primary and secondary circuits galvanically isolated. The output pins provide a 0-5 V voltage signal which is proportional to the voltage measured at the primary side. This signal is adapted to the submodule microcontroller thanks to a resistive divider. In parallel to that, a redundant measurement per signal has been realized with a high voltage differential probe connected to an oscilloscope to read and store data offline. The used voltage probes are 'LeCroy HVD3206A 2 kV, 120 MHz High Voltage Differential Probe' models, while the oscilloscope is a 'Teledyne LeCroy WaveSurfer 3024Z 200 MHz Oscilloscope' which is able to save .mat files in order to directly read them on Matlab.

9.1.2 Current measurement

The submodule currents have been measured through four independent LEM LF 1005-S current transducers. They are closed loop (compensated) transducers using the Hall effect and can read a primary current of up to 1000 A per transducer. The secondary current has a nominal value of 200 mA. By choosing a proper measuring resistance it is possible to read a voltage over this transducer proportional to the primary current and with an amplitude adapted to microcontroller input.

9.1.3 Temperature measurement

The temperature has been monitored on the power stage level. In particular each IGBT half-bridge is equipped with a NTC resistor, which is a temperature-dependent variable resistor. The higher the temperature, the lower the resistance of the resistor and vice versa. Tha datasheet of the adopted IGBT provide data about the temperature dependance of the NTC resistor and therefore a voltage signal proprtional to the change of temperature of the IGBT junction can be measured and sent to the microcontroller in real-time.

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