Tailoring Properties of Printed Field-Effect Transistors by Design and Material Changes

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Doctoral thesis in Materials and Earth Sciences by Felix Joachim Neuper

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Zusammenfassung

Mit der zunehmenden Digitalisierung in allen Lebens- und Arbeitsbereichen inklusive digitaler Kennzeichnung oder gar elektronischer Rückmeldungen von einzelnen Bauteilen oder Konsumartikeln stellt sich die Frage nach neuen Möglichkeiten, Schaltungen schnell und einfach zu produzieren. In diesem Zusammenhang muss auch die Massenproduktion von Transistoren, den Grundbausteinen elektronischer Logiken, neu überdacht werden, um die vergleichsweise aufwändige Produktion von Siliziumchips zu überwinden. Hierbei hat sich das Drucken elektronischer Elemente in den letzten Jahren als vielversprechende Methode hervorgetan. Leiterbahnen, Solarzellen oder Displays sind als gedruckte Elektronik bereits vielfach in industriellen Produktionsprozessen integriert worden.

Im Gegensatz dazu konnten bisher keine verlässlichen Prozesse für gedruckte Transistoren in industriellem Maßstab etabliert werden. Organische und anorganische Halbleitermaterialien haben oft diametral unterschiedliche Eigenschaften: organische Materialien sind in der Regel p-Halbleiter und warten mit einfacher Verarbeitbarkeit und mechanischer Flexibilität auf. Anorganische Systeme sind in der Regel n-Halbleiter, spröde und bedürfen hoher Prozesstemperaturen. Diese Nachteile anorganischer, insbesondere oxidischer Halbleiter, werden jedoch durch die oftmals wesentlich besseren elektronischen Eigenschaften und besserer Umweltstabilität ausgeglichen.

Um besonders niedrige Betriebsspannungen bei trotzdem ausreichend hohen Strömen zu erreichen, empfiehlt sich, die Polarisierung des Kanals über einen Elektrolyt statt eines Dielektrikums umzusetzen, da die Ausbildung von Helmholtz-Doppelschichten lokal sehr starke Felder erlaubt. So können Bauteile mit typischen Spannungen kommerziell verfügbarer Batterien betrieben werden.

Im Rahmen dieser Arbeit konnten erfolgreich neue und verbesserte Methoden für die Darstellung gedruckter Feldeffekttransistoren umgesetzt werden, die die Entwicklung hin zu einer Produktion von Einheiten mit vorhersehbaren Eigenschaften in hohen Stückzahlen unterstützen. Ausgehend von planaren Feldeffekttransistoren mit versetzten Gattern,

wurden drei Verbesserungsmöglichkeiten untersucht: eine vertikale Geometrie, dotierte Kanäle und ein alternativer Elektrolyt.

Der Wechsel von einer planaren zu einer vertikalen Bauweise erlaubt die Kanallängen von der Auflösung der Materialdrucker unabhängig zu machen und auf die Dicken der abgeschiedenen Filme zu reduzieren. Somit können Längen von zweistelligen Mikrometern auf Submikrongröße verkleinert werden. Da die Kanallänge direkt proportional zum Strom an der Senke ist, kann hier eine deutliche Verbesserung erreicht werden. Jedoch muss hierfür der Kanal porös dargestellt werden, um eine große Oberfläche mit Elektrolyt in Kontakt bringen zu können. Hierbei wurde ein bekanntes System mit SnO_2-Kanal durch eine vereinfachte Darstellungsmethode mit schnell verfügbaren Materialien verbessert und erfolgreich ein funktionales Bauteil dargestellt.

Um die wichtige Kenngröße der Schwellspannung, diejenige Gatterspannung, ab der ein Kanal vom isolierenden in den leitenden Zustand wechselt, verlässlich darzustellen und individuell einstellen zu können, wurde eine In_2O_3-Präkursorentinte mit variabler Chromdotierung entwickelt. Durch diese Dotierungen konnte die Schwellspannung linear zur Dotantkonzentration verändert werden, jedoch unter deutlichen Verlusten in den Ausgangsströmen.

In einer dritten Versuchsreihe wurde der üblicherweise genutzte Kompositpolymerfeststoffelektrolyt durch Al_2O_3 ersetzt. Statt eines dielektrischen Polarisationsverhaltens resultierte jedoch aufgrund niedriger Synthesetemperaturen im Atomlagenabscheideverfahren ein Material mit geringer Dichte und vielen Hydroxyfunktionalitäten, das als Elektrolyt agiert. In Abhängigkeit der Luftfeuchtigkeit kann die Funktionalität der so erhaltenen Transistoren beeinflusst werden, da die Elektrolyteigenschaft auf an der Al_2O_3-Oberfläche generierten Protonen basiert.

Im Rahmen dieser Arbeit konnten somit erfolgreich drei Alternativen für die Produktion gedruckter, anorganischer Feldeffekttransistoren aufgezeigt werden und ein Beitrag zu Weiterentwicklung dieser Technologie geleistet werden.

Abstract

Due to the increasing digitalization in all areas of life and work, including digital signatures or even electronic feedbacks from single component parts or consumer articles, the question for new possibilities for quick and simple manufacturing of circuits arises. In this respect, also mass production of transistors, the core building units of electronic logics, has to be reconsidered in order to overcome the often complex production of silicon chips. In this scope, printing of electronic components has presented itself as a highly promising method within the recent years. Conductive paths, solar cells, or displays have already been integrated as printed electronics in manyfold industrial production processes.

In contrast to this, so far, no reliable processes for printed transistors in an industrial scale have been established. Organic and inorganic semiconducting materials often have properties with diametral differences: while organic materials use to be p-type semiconductors and come up with simple processability and mechanical flexibility, inorganic systems tend to be n-type semiconductors, brittle and in need of high processing temperatures. These disadvantages of inorganic, especially oxidic semiconductors however are compensated by often severely better electronic properties and increased environmental stability.

In order to achieve very low operation voltages while maintaining sufficiently high currents, it is recommended to realize channel polarization via electrolytes instead of dielectrics, as the formation of Helmholtz double layers allows for locally very high fields. By this, units can be operated at voltages typical for commercially available batteries.

Within the scope of this work new and improved methods for the processing of printed field-effect transistors were successfully implemented, contributing to the development towards large-scale production of devices with predictable properties. Starting form planar field-effect transistors with displaced gates, three possibilities for improvements have been examined: a vertical geometry, doped channels and an alternative electrolyte.

By changing from a planar to a vertical device geometry, channel lengths may become independent from the material printers' resolutions and can be reduced to the thickness of the deposited films. By this lengths may be shrunk from a two-digit micron range to submicron values. As channel lengths are directly correlated with output currents, a severe improvement can be realized. However, in this case the channel must be porous in order to allow a large surface being covered by electrolyte. Within this work, a known system with an SnO_2 channel could be improved by developing a simplified production method with quickly available materials, successfully resulting in a fully functional device.

For reliably tailoring the central property of the threshold voltage, i.e., the gate voltage at which the channel changes from an insulating to a conducting state, on a per-device level, an In_2O_3 precursor ink with varying chromium doping has been developed. Through this doping, the threshold voltage could be changed linearly with the dopant concentration, however under severe loss in the output current.

In a third experimental series, the usually applied composite solid polymer electrolyte has been replaced with Al_2O_3. However, instead of a dielectric gating, a material with low density and many hydroxy functionalities acting as an electrolyte was created due to low temperatures during the atom layer deposition process. Depending on the humidity, the functionality of such transistors can be changed as the electrolytic properties are based on protons generated on the Al_2O_3 surface.

Within this work, three alternatives for the production of inorganic field-effect transistors could be successfully shown and a contribution towards the further development of this technology was made.

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List of Abbreviations

ALD	atomic layer deposition
CMOS	complementary metal oxide semiconductor (device)
CSPE	composite solid polymer electrolyte
D	drain
EBL	e-beam lithography
EG	electrolyte gating/gated
EGFET	electrolyte-gated field-effect transistor
FET	field-effect transistor
G	gate (in devices), gap (for semiconductors)
IoT	internet of things
NDR	negative differential resistance
OLED	organic light-emitting diode
R2R	roll-to-roll (processing)
RH	relative humidity
S	source
SEM	scanning electron microscopy
SS	subthreshold swing
TGA	thermogravimetric analysis
th	threshold
TMA	triethyl aluminium ($Al(CH_3)_3$)
XRD	X-ray diffractometry
XRR	X-ray reflectometry

1. Introduction

1.1. On the Increasing Demand for Printed Field-Effect Transistors

One of the currently heavily forced transitions in industry is the digitalization of work processes at any step from production to management. While this evolution towards computer-based workflows, commonly referred to as digital revolution, is openly visible in office works, as nearly all desk jobs include personal computers nowadays, new aspects have risen in interest lately: data mining and big data, as well as the internet of things.

Data mining hereby means statistical analysis of large information sets ("big data") in order to extract valuable information and patterns. E.g., this is needed for optimizing a production process, predicting customer behavior or even training artificial intelligence systems as well as in the scientific areas dealing with combinatorial synthesis and screening for specific properties in the products. [1]

Internet of things on the other hand refers to enabling direct, digital communication between devices independent of human interaction. [2, 3] While it might sound like an absurdly unnecessary and sci-fi gadget to have one's mixer suggest making banana milk as both the bananas in the fruit basket and the milk in the fridge report being on the verge to spoil, a direct feedback loop from sensor devices (and analyzing the big data amounts they create) can further automatize industrial production processes and allows for real-time adjustments. This is interesting, e.g., in continuous chemical reactors or as one way to flexibly manage urban traffic. On an end-user level, medical applications have come into focus where patients' health data are continuously monitored and the need for medication or iatric intervention is reported in real-time or even applied by an automatic dispenser. [4] Apart from optimizing known processes, a whole new management of supply chains by IoT-technology is anticipated, where each part has a unique identification number – effectively being an internet protocol (IP) address – and can report its spatial position,

position in the production chain, state of passed quality tests and many more properties to the smart, self-organizing factory. [5] With version 6 of the internet protocol (IPv6) formally $3.4 \cdot 10^{38}$ globally unique IP addresses are possible and even the address space commonly given to a single household already allows for up to $1.8 \cdot 10^{19}$ unique addresses. [6, 7]

This sparks the question on how to apply this unique labeling and the digital logics they require. Processes will have to be able to produce electronic devices in large quantity with high reliability at low unit costs while preferably being attached to flexible substrates to allow applying these intelligent labels to components as adhesive tags or to incorporate them into the packaging. In this respect new materials in combination with printing technology have been established as promising alternative to replace previously industry standard processes that rely on batch-wise production due to the need for high vacuum methods or monocrystalline materials. Currently, technologies such as printed (organic) light-emitting diodes, printed solar cells, printed resistors, printed conductive lines, and printed radio-frequency identification (RFID) antennas already have reached significant industrial application in replacing traditional analogues or are on the verge to do so and even are applied to flexible substrates in many cases. [8–18] With this respect the traditional understanding of printing as recreating text or images from a master needs to be redefined to applying material inks onto a substrate, with focus on material properties rather than the optical appearance of the print result.

For high throughput production, roll-to-roll processing is considered the most relevant option. In R2R a rolled-up, flexible substrate is fed through a printer line and the patterned substrate collected on another roll at the end. Several printing methods are well established and applicable for this. Coarsely they can be classified by whether the substrate is in contact with the printing machine and in how many dimensions the structuring is possible. [19] They include gravure printing, transfer-printing, screen printing, slot-die coating, and flexographic printing and have been vastly applied to produce electronic devices and components. [8, 20–23] Structured layouts are not a necessity in all cases. E.g., for OLEDs or solar cells, spraying or doctor blading can be a valid method for film applications as the aim lies in creating large areas of active material. [24–27]

The aforementioned printing methods suffer from major disadvantages: either they rely on a pattern master that needs elaborate manufacturing or allow no patterning at all. Inkjet printing on the other hand stands out as being a drop-on-demand technology, i.e., ink ejection from a nozzle can be selectively managed and thus patterns need digital masters only. That means it can be freely designed in a software suite. [21] Additionally to full flexibility in patterning, it is a direct writing method, meaning the ink is directly applied,

and thus material losses on patterning masks or master cylinders or because of etching steps are excluded. This makes ink-jet printing especially interesting for applications with many design changes, expensive or sparsely available materials, and use-cases where ink is applied in very low-density patterns. The latter case applies, e.g., in printed ring oscillators, where channel materials only make up a comparably small area of the final devices. [28–30]

In current scientific literature, ink-jet printing is one of the standard techniques for manufacturing printed electronics and due to its versatility can be considered the first laboratory scale method for developing devices before a transfer and scale-up to R2R production is applied. While this scale-up and technology adaption by industry is successful for many electronic components, especially field-effect transistors – the core and key components of any digital logic – have not yet found their way into industrial production by printing methods, despite huge interest from industry and vast research activities in the field.

This can be attributed to a few FET-specific problems and requirements. In general, it can be noted that organic semiconductors can often be dissolved and thus be readily printed, however, their intrinsic mobilities are comparably low. Inorganic SCs on the other hand show good mobilities but either need to be printed as particles, and thus particle-particle contacts limit the overall performance, or they have to be derived from precursors, and as such often need annealing steps that can hardly be combined with using temperature-sensitive flexible polymer or paper substrates and also suffer from brittleness. [31–36] Another factor is that organic SCs usually are p-type while inorganic tend to be n-type. p-type inorganic and n-type organic SCs tend to have mobilities far below the typical values of n-type inorganic and p-type organic SCs, respectively. [37, 38] Thus basic logics, like inverters, that usually rely on complementary metal oxide semiconductor technology face several challenges. But also the printing technology itself sets limits to transistor performances: on the one hand current high-throughput methods are limited in their resolutions. Commonly, drop diameters of an ink-jet printed material are in the range of 20-50 μm. Thus, channel lengths and therefore maximum currents are limited in standard in-plane layout FETs. Performance changes arising from random printing variations challenge the demand for high reproducibility in reliable logic arrays and inflexibility in varying central performance parameters limit the freedom in circuit design. Last but not least printed electronics are targeted to end-user and mobile applications thus battery-driven, low voltage operation is desirable. This makes electrolytic gating a valuable candidate over dielectric gating, as in general lower operation voltages are possible. [39, 40] However electrolytes face new problems in, e.g., environmental stability and long-term reliability.

1.2. Motivation and Outline

The focus of this thesis is to provide pathways for tackling the aforementioned challenges printed field-effect transistors are facing and hindering them from being adapted into an industrial-scale application.

Taking the well-established concept of printed, in-plane, CSPE-gated FETs with displaced gates as starting point, each component as well as the general layout offer manyfold potentials for optimization as shown in fig. **1.1**. [41] In general, an FET consists of four different materials, one for each component: the substrate, the passive structure (source, gate, and drain), the channel, and the electrolyte or dielectric. A fifth material may be possible if a top gate, i.e., a conductive element atop the electrolyte and above the channel is introduced. Of course each material selection can be considered separately and shall be discussed briefly here.

In case of the substrate, it must be decided between a rigid or flexible material, if it can withstand the annealing conditions, and if surface treatment is necessary for ensuring proper material adhesion and ink spread. The passive structure can either be printed – allowing a continuous process but with drawbacks on conductivity and resolution – or, e.g., sputtered in combination with EBL – a high resolution method but a three-step batch process (structuring, deposition, lift-off). The considerations regarding channel material and ink make-up have been discussed in the previous section, however, the possibility of using doping for shifting semicoductor properties shall be mentioned here explicitly. Gating can be regarded from the method, the material, and the layout side. In case of the method, only two options are available: dielectric gating – typically associated with fast response times – or electrolyte gating – allowing lowering the operation voltage and more feasible for printing. For dielectrics already a vast variety of high-κ materials is available, many of which, however, need more elaborate deposition methods. [42] Regarding electrolytes, one has to choose between, e.g., CSPEs, ion gels, or ceramic electrolytes, each coming with different advantages and disadvantages in ionic conductivity, environmental stability and processability. [41] Additionally, different positions of the gate can be regarded: a displaced gate, only possible with electrolyte gating due to the ability of ions moving through the electrolyte. A back-gated system, where a conductive substrate acts as the gate electrode and is covered by a dielectric atop which the printed materials are deposited. And a top gate, as mention earlier, in this case, the gate electrode is placed atop the electrolyte or dielectric. This already leads to more general considerations for the layout itself, which may be in-plane or vertical, and the dimensions of each component both in the plane as well as the perpendicular thickness. Here, for example, short distances

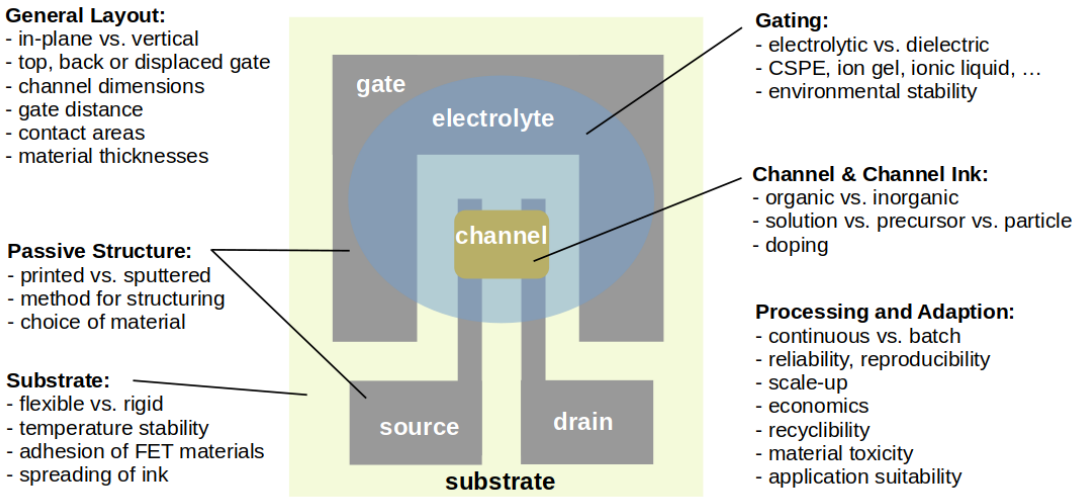

Figure 1.1.: Typical layout of a printed, in-plane CSPE-gated FET with displaced gate and selection of possible optimization considerations

between gate and channel are desirable but bear the danger of creating short circuits during manufacturing, small dimensions are limited by printing resolution, or too sparse material use may limit performance, e.g., too thin metal leads introducing considerable resistances – internally or due to too small contact areas with the channel. Furthermore, printing as deposition method introduces new requirements regarding suitability of a material in ink-form, ink stability or ink composition necessities for the selected printing method. Materials and processes may also not just be optimized separately: contact resistances and possible chemical reactions between the components are to be considered. Beyond the scope of a single device, industrial adaptation will also depend on further factors, e.g., if the process is suitable for scale-up or for high-throughput methods, if the device performance has a reliable window for the properties and low failure rates, and if the materials and devices suit to the desired application, e.g., biocompatibility in medical systems. And of course even factors beyond the actual performance need to be considered, such as pricing and availability of the materials, economics and safety of the processing, and recyclibility of the devices. Often the desired properties and methods may be diametrical to each other, e.g., the good electrical performances of inorganic SCs contrast the desire for flexible substrates, well-performing materials being expensive (e.g. gold as conductor), or design limitations in all-printed devices, just to name a few.

As can be seen, it has to be clearly selected and defined, which properties shall be optimized. Of course, on the level of single-device processing in laboratory scale, the focus on one property may come at the cost of disregarding another. While accepting to stick with rigid substrates, high-temperature processes, and batch processes, three different fields out of the aforementioned optimization parameters have been selected and examined separately.

First of all, the limitations of device performances due to the upper limits of printing resolution have been tackled in a vertically aligned FET, where the channel length is defined by the far smaller film thickness instead of the drop diameter. Chapter **4** describes a new and vastly simplified method for preparation of a vertical channel with highly regular porosity. Advancing from an earlier described system by Baby et. al., the necessary materials could be substituted by chemicals with better availability and manageability, the channel structure be changed to more regular porosity, and the process temperature be reduced. [43]

Secondly, in chapter **5**, the problem of reproducibility and predefining of electrical performances in printed FETs have been overcome by the – to the best knowledge of the author – first systematic examination of chemical doping in printed FETs with oxide SCs. Within this chapter, a linear correlation between threshold voltage and Cr dopant content in In_2O_3 is shown, including statistically sound separation between the different device properties.

The third field, examined in chapter **6**, introduces an alternative gating based on the highly environmentally stable, yet low-cost, Al_2O_3. Despite being a ceramic, the material acts as electrolyte with humidity-dependent performance. Performance changes with humidity, including the device reaction times, and the mechanism behind are discussed.

The fundaments for understanding FETs and the methods used within this work are laid in chapter **2**, and the experimental realization described in chapter **3**. Finally, a summary of this thesis and an outlook on future projects based on it can be found in chapter **7**.

2. Theoretical Background

Major parts of the theory and functionality of FETs in this chapter are based on the standard textbooks by Neamen, Sze, and Fiore without further mentioning. [44–46]

2.1. Field-Effect Transistors

Field-effect transistors are the core unit in current logic devices and silicon technology is based on it. In order to understand how a printed transistor operates, the basic concept of FET functionality must be examined. In a first, simplified view, transistors can be considered as switches that allow or deny, or, more generally, increase or reduce, a current flow between a source and drain electrode. To achieve this, a so-called channel that has a variable resistance which can be influenced depending on a third input signal is necessary.

2.1.1. Semiconductor Materials

The foundation of any transistor is a channel made from a semiconductor, a material class, where availability of free charge carriers, and thus resistance, may be influenced by external stimuli without decomposition.

In contrast to conductors, defined by an energetic overlap of the valence and conduction band or partially filled valence bands (fig. **2.1a,b**), and insulators, defined by a large energy gap between valence and conduction bands (fig. **2.1d**), semiconductors have energy gaps (E_G) of up to 4 eV (fig. **2.1c**).

Given the Fermi-Dirac distribution (eq. **(2.1)**) describing the occupation probability p of a particle state with energy E in thermal equilibrium at temperature T, and with the

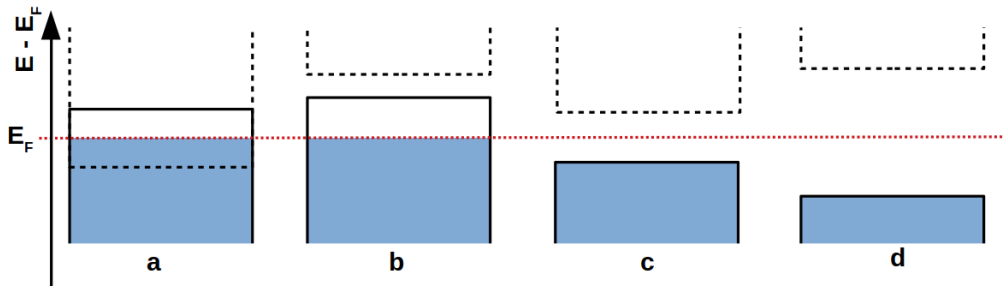

Figure 2.1.: Band model depiction of a) a conductor with overlapping valence and conduction bands, b) a conductor with a partially filled valence band, c) a semiconductor and d) an insulator; E_F defines the Fermi level, energies normalized to E_F, blue colored areas represent filled states for the ground state of the respective material

Boltzmann constant k_B, the Fermi level is the potential energy level with the occupation probability $p(E_F) = \frac{1}{2}$. In a semiconductor this Fermi level is between valence and conduction band and and as such usually does not match an allowed particle state.

$$p(E) = \frac{1}{exp(\frac{E-E_F}{k_B T}) + 1} \tag{2.1}$$

When analyzing eq. **(2.1)** at absolute zero, one will see that all states with $E < E_F$ are occupied, while states with higher energies are unoccupied. With increasing temperatures, the probability of occupying states above E_F is non-zero (fig. **2.2a**). Transferring this occupation setup to a semiconductor following the band model from fig. **2.1c** results in the generation of electron-hole pairs where each electron that is being promoted to the conduction band and the hole it leaves in the valence band can be used for charge transport as electrons may occupy empty, spatially neighboring states and holes may be occupied by neighboring electrons, respectively (fig. **2.2b-d**). That means the concentration of charge carriers can be controlled by temperature or other ways of exciting an electron from the valence to the conduction band, e.g., by photons.

A much more reliable, vastly applied and considerably a key capability of semiconductors is, however, using doping as means to control both the charge carrier concentration as well as the kind of the majority carriers, i.e., whether electrons in the conduction band (n-type semiconductor) or holes in the valence band (p-type semiconductor) are both higher in concentration as their counterpart and mainly contribute to the total current. During

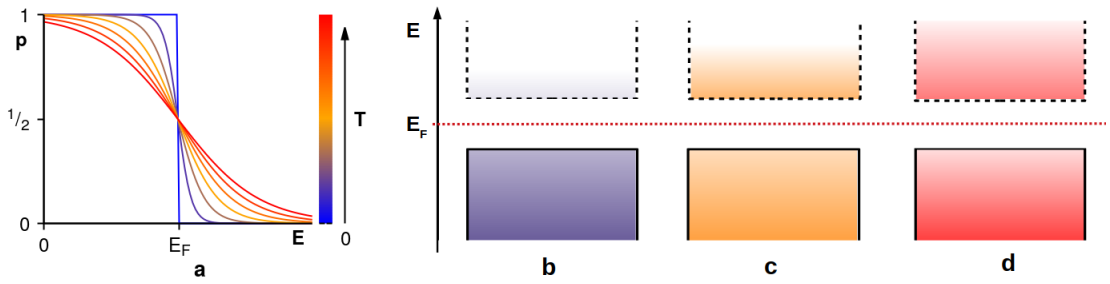

Figure 2.2.: a) Schematic depiction of Fermi-Dirac distributions with the same Fermi level E_F at different temperatures T, b to d) change in the population of valence and conduction band in a semiconductor with increasing temperatures; temperatures increase as indicated by color

doping new energetic states in the band gap are created, either unfilled (acceptor) states near the valence band or filled (donor) states near the conduction band (fig. **2.3a,b**). In general, the concentration of major charge carriers is depending on the concentration of intrinsic carriers, i.e., thermally created ones, and extrinsic carrier numbers that arise from the doping states. It is notably possible to dope with acceptor and donor states in the same material (so-called compensated semiconductor), the effective dopant concentration then arises from the difference in concentration of n- and p-type doping. Based on temperature the influence of intrinsic and extrinsic carriers on the total concentration varies. At very high temperatures, the total concentration is governed by the thermal creation of charge carriers, i.e. intrinsic carriers make up the major part. At intermediate temperatures, the carrier concentration is determined by the effective dopant concentration only, as it can be assumed that all dopant states are ionized and intrinsic carriers have a concentration far below the doping concentrations. That means the concentration is based on extrinsic carriers only. At very low temperatures, the thermal energy is so small that less and less electrons can be promoted from the valence band into acceptor states or donor states into the conduction band, respectively, i.e., full ionization of the doping states is no more given. This temperature range is called the freeze-out region, where thermal effects govern both intrinsic and extrinsic carriers. (fig. **2.3c**)

Focusing on n-type devices operated at room temperatures as is done within this work, the total, effective carrier concentration n_0 at thermal equilibrium and under assumption

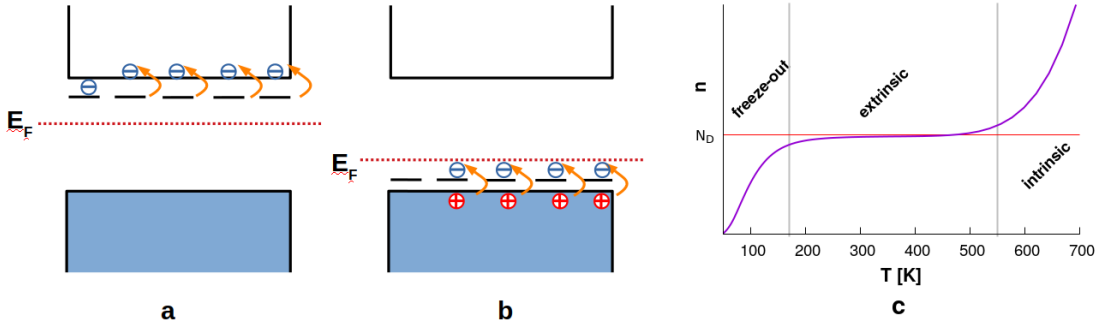

Figure 2.3.: a) n-doping: electrons from donor states are promoted into the conduction band as charge carriers, b) p-doping: electrons from the valence band are promoted into acceptor states, leaving holes as charge carriers c) temperature dependence in charge carrier density in an n-doped semiconductor with a dopant concentration of $N_D - N_A$ where $N_D > N_A$ (after [47])

of total ionization of all dopant states is given as

$$n_0 = \frac{N_d - N_a}{2} + \sqrt{\frac{(N_d - N_a)^2}{2} + n_i^2} \tag{2.2}$$

where N_d and N_a are the concentrations of donor and acceptor states, respectively, and n_i the intrinsic carrier concentration. Assuming that extrinsic carriers by far exceed intrinsic carriers ($N_d \gg n_i$), this even simplifies to $n_0 = N_d - N_a$.

The generation of doping states can be achieved in two ways. Extrinsic doping means incorporating foreign dopant atoms into a crystal lattice with a different number of valence electrons than the atoms they replace. I.e., if a a dopant occupies a cation position and contributes more valence electrons than the atom it replaces (e.g. Sn^{4+} on an In^{3+} position in indium oxide), it increases the number of electrons in the electronic band, effectively n-doping the system. Analogously, replacing an atom at an anionic position that needs to absorb less electrons to reach its favored ionic state, will likewise increase the number of electrons in the band system, e.g., Cl^- at the position of O^{2-}. For the change in carriers to come into effect, a delocalization of the electron or hole, respectively, into the spread-out molecular orbitals of energy states near the band gap is necessary. This is only possible if the dopant state – which itself is localized to the dopant atom – is energetically close to the conduction or valence band, respectively, so that an electron transfer – which

creates the delocalized n- or p-carrier – is possible at room temperature. If a semiconductor is tolerant towards heavy extrinsic doping without phase separation, it will eventually always have an extremely high number of available carriers for charge transport. In such cases the semiconductor is called degenerate and behaves like a metallic conductor.

Intrinsic doping on the other hand follows from crystallographic defects in non-stoichiometric compounds. In many cases of oxide semiconductors this equals oxygen vacancies, effectively leading to n-type semiconductors as not all electrons from the metal atoms may be bound by a matching non-metal atom. In contrast to extrinsic doping, the number of vacancies is not determined by the stoichiometry of precursor compounds, but rather depends on conditions during synthesis or the synthesis method itself, e.g., the partial pressure of oxygen during sputtering, the temperature during oven annealing, ALD-parameters and overall resulting grain boundary morphologies to name a few. [48]

2.1.2. The Metal-Semiconductor Contacts

In a transistor the current flow between source and drain is mainly based on the conductivity of the channel material which itself is set via an external stimulus. Thus, the properties of the semiconductor play a major role, however, it must not be forgotten, that also the metal leads, and especially the contact between the leads and the channel also influence the transistor characteristics.

Both, the isolated metal and semiconductor, have specific Fermi levels that are given as material properties but usually differ from each other. This is depicted for an n-type semiconductor in fig. **2.4**. The interconnected system however has a unified system of electronic states and thus a Fermi level of the combined system is formed. This leads to the bands of the semiconductor bending in the contact area depending on whether the Fermi level E_{Fm} of the metal is lower or higher than the Fermi level E_{Fs} of the semiconductor.

In the first case, a potential barrier Φ_B formed that hinders electron injection from the metal to the semiconductor and a so-called rectifying contact is generated. With the increased energy levels of E_{C} at the contact, also the reverse electron flow is hindered by the difference between E_{C} in the bulk material and at the contact area. (fig. **2.4a,b**)

In the other case, no potential barrier between the occupied states in the metal and the semiconductor's conduction band is present and thus electron injection is not hindered. (fig. **2.4c,d**)

While the rectifying contacts are used as diodes, transistor applications demand for a seamless transfer of the charger carriers between metal and semiconductor. Therefore, ohmic contacts are preferred there.

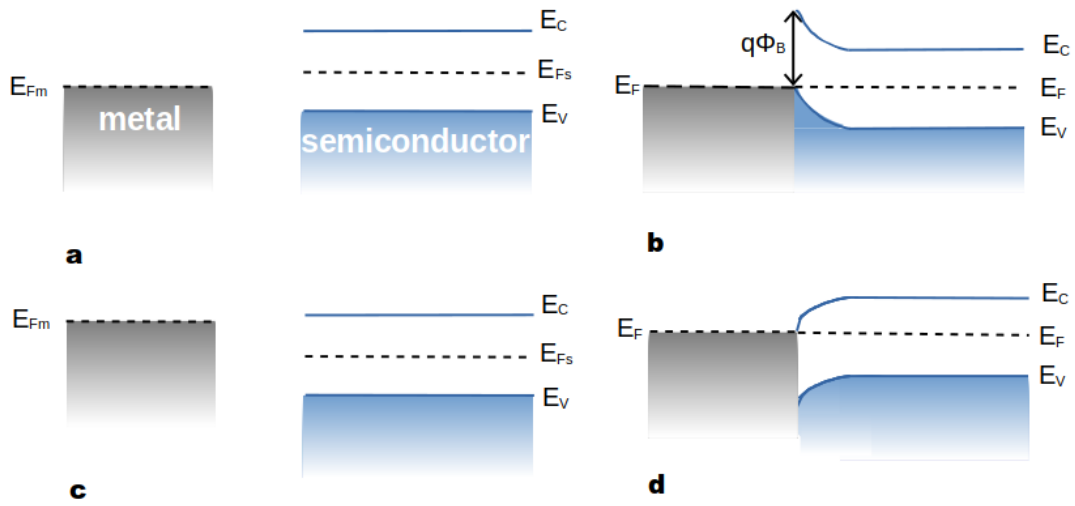

Figure 2.4.: a) metal and n-type semiconductor with the Fermi level E_{Fm} of the metal being lower than the Fermi level E_{Fs} of the semiconductor, b) once connected, a rectifying contact is formed; c) metal and semiconductor with $E_{\mathrm{Fm}} > E_{\mathrm{Fs}}$, d) once connected an ohmic contact is formed

2.1.3. The Field-Effect

As stated earlier, the charge carrier concentration in a semiconductor may be influenced by external stimuli which is the central property that allows switching between a conductive and insulating state. This external signal may be temperature – as shown in the Fermi-Dirac distribution – or photons with sufficient energy to enhance electrons from the valence to the conduction band. As a result, semiconductors are applied in, e.g., thermometers and photodetectors. In a transistor, however, the external signal is electric. In the case of junction transistors, the resistance of the channel is controlled by a current applied, whereas in field-effect transistors the resistance is voltage-controlled.

As all devices within this work function similar to metal-oxide-semiconductor field-effect transistors (MOSFETs), the focus in the following lies on this type.

In a MOSFET, the channel is positioned between source and drain and covered by the metal gate electrode over the full length of the channel. Gate and channel are separated by a dielectric which should both be a good insulator and have a very low shielding effect versus electric fields. In fig. **2.5a**, a schematic side view of a typical MOSFET is shown. If a voltage is applied between source and gate, the dielectric insulator becomes polarized and thus influences the energy bands on the channel surfaces. As the gate bias typically is applied relative to the source, the depth of the induced change in carrier concentration is dependent on distance to the source, leading to a profile as shown in fig. **2.5b**. Once V_{GS} exceeds the threshold voltage V_{th}, conductivity is given throughout the channel length, and applying a voltage between source and drain can be used for inducing a current. Before a deeper understanding of transistor characteristics is explained in sec. **2.1.5**, it should be understood, how a gate bias leads to changes in carrier concentration in the channel surface.

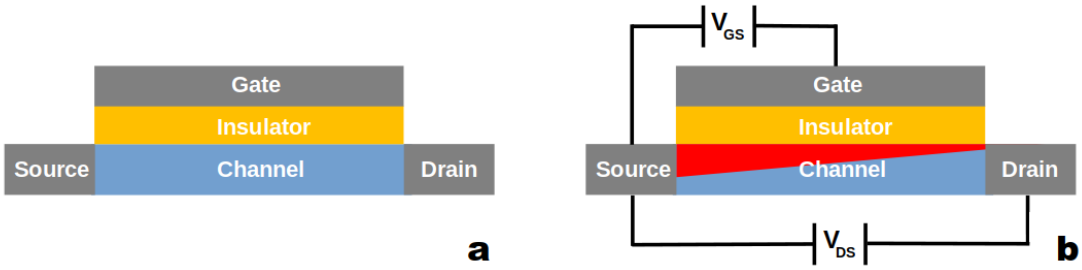

Figure 2.5.: a) generic layout of an FET device, b) with applied voltages during FET operation, red indicates availability of charge carriers as induced by V_{GS}

Fig. **2.6a** shows the energetic diagram at a certain position along the channel in the flat band case for an n-type semiconductor. In this ideal situation, the Fermi level of the gate electrode matches the Fermi level of the (n-type) semiconductor and so the number of majority charge carriers in the channel surface equals the value of the (doped) bulk material. A few electron hole pairs exist at room temperature due to the Fermi-Dirac distribution, however the conductivity is governed by the intrinsically available majority carriers. The insulator acts as energetic barrier denying charge carrier transfer between gate and channel. While this situation is unlikely to appear naturally, the flat band case may be reached easily by applying a corresponding voltage to the gate.

Once a positive V_{GS} is applied the Fermi level of the gate electrode is shifted downwards (fig. **2.6b**), and electrons from the valence band will accumulate at the channel surface and be able to act as additional charge carriers and the channel is highly conductive. This situation is called accumulation mode.

If a negative V_{GS} is applied, the excess electrons stemming from the doping are removed due to a higher hole concentration. The channel is depleted even of the intrinsically available charge carriers and becomes insulating. The depletion mode is shown in fig. **2.6c**.

As soon as a very low V_{GS} is applied, the intrinsic energy level at the surface rises above the Fermi level, and thus, the minority carriers have a higher concentration than the majority carriers at the surface. The channel again is conductive. This inversion mode is shown in fig. **2.6d**.

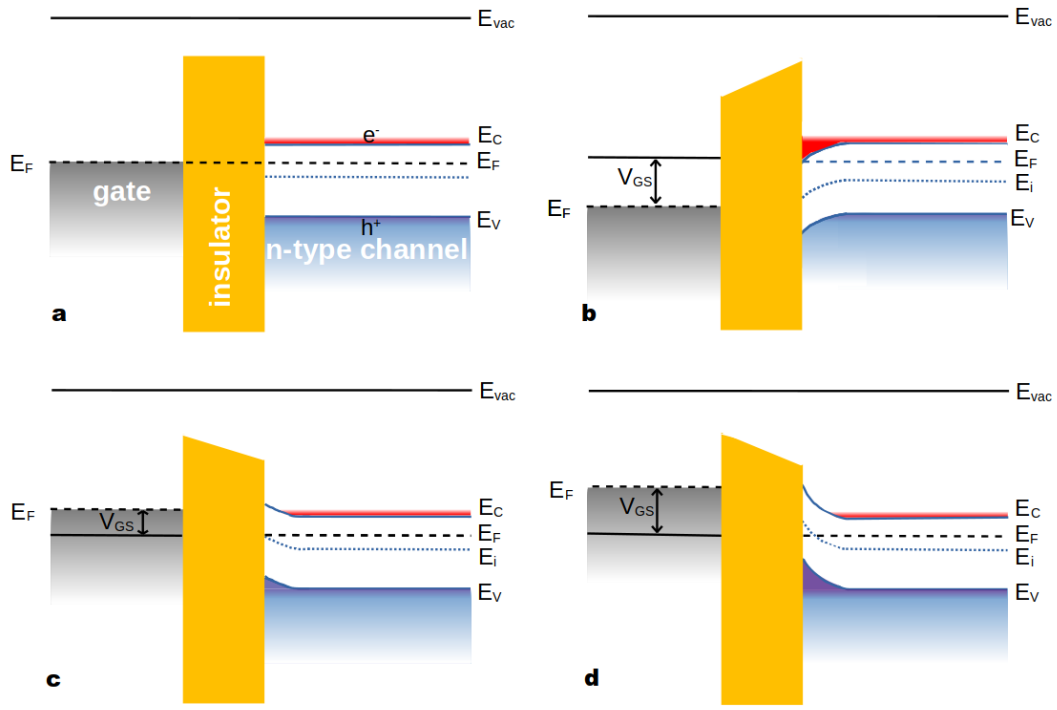

Figure 2.6.: Carrier distributions in the channel at the gate-insulator-channel contact area. a) flat band case, b) accumulation mode, c) depletion mode, d) inversion mode

All devices within this work will be n-type transistors operated in accumulation mode.

2.1.4. Electrolyte Gating

In most current applications, the insulator is a dielectric and the system gate-insulator-semiconductor can thus be regarded as a parallel plate capacitor. Any bias V_G on the gate will induce a charge Q in the channel. The two items are connected by the capacitance C via

$$Q = CV_G \quad \text{with :} \quad C = \frac{\kappa \epsilon_0 A}{d} \tag{2.3}$$

where κ is the dielectric constant/relative permittivity, ϵ_0 the vacuum permittivity, A the area of the system and d the thickness of the dielectric. While the area is determined by the FET geometry, an ideal insulator has a very small thickness and a high permittivity. The thickness has a lower limit due the breakdown voltage. The permittivity is a material property, and the polarizability depends on the material itself as well as crystallinity, crystallographic orientation, and the chemical composition of the material.

The alterative to this is to replace the dielectric by an electrolyte. In an electrolyte, mobile cations and anions are available. If a bias is applied to the gate, ions will be attracted or repelled at this surface depending on their charge, while the same happens at the electrolyte semiconductor surface with the respective counterions. A schematic of the ion distribution and the charge density in an electrolyte is depicted in fig **2.7**.

The ion distribution on one electrode can be described using the Stern model which combines a rigid Helmholtz double layer at the contact area with a diffuse layer of an exponentially decreasing electric potential and accordingly charge and ion concentrations until the potential drops to 0. This distribution is mirrored on the other side with the complementary charges.

Especially the Helmholtz layer can be considered as a very high-capacitance system according to eq. **(2.3)**, as the effective distance between the charges are in the single-particle size range.

As the ions can move through the electrolyte along electric fields, it is possible to go away from the sandwiched structure of channel-dielectric-gate and use a displaced-gate, in-plane geometry, where the gate is located next to the channel and both are covered with the electrolyte. A schematic of such a device is shown in fig. **2.11**.

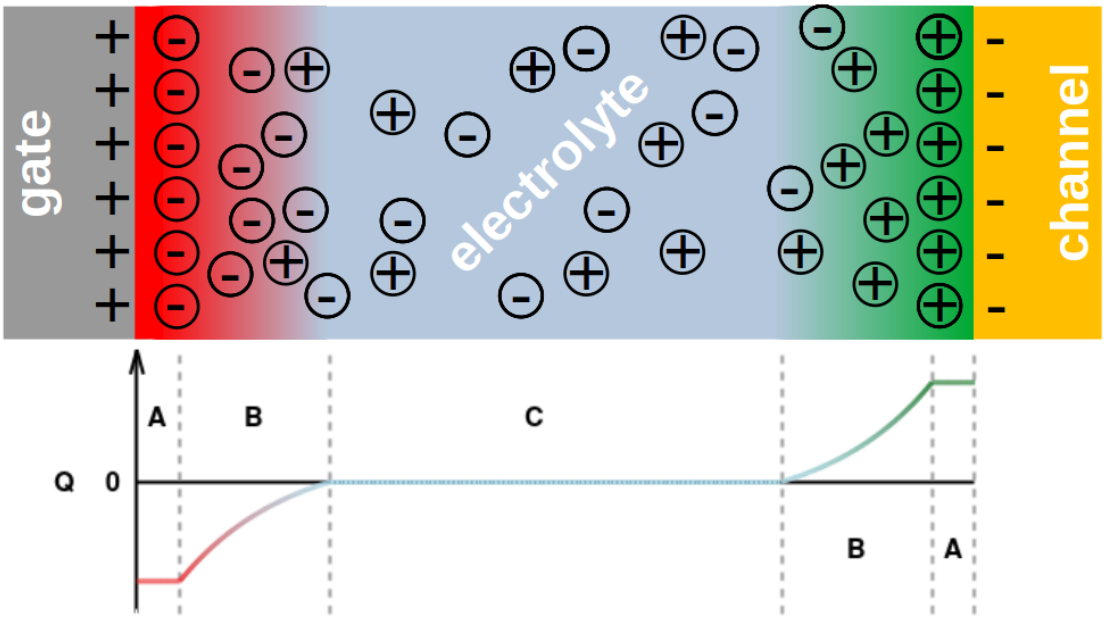

Figure 2.7.: top: schematic of ion distribution in the electrolyte with a positive bias applied at the gate: anions are attracted to the gate and cations are pushed to the channel, inducing a negative charge; bottom: corresponding charge density with (A) Helmholtz double-layer, (B) diffuse layer with exponential charge decline, (C) neutral electrolyte with matching numbers of ions and counterions

Due to the liquid nature of the electrolyte, it may not only be printed but is also highly conformative towards the channel surface. In general, electrolyte gating allows for lower gating voltages due to the strong field in the Helmholtz double layer easily inducing a conductive channel. The concepts for the polarization of charge carriers in the semiconductor as described in the previous section still apply.

Often the electrolytes are composite solid polymer electrolytes, that offer a solid polymer backbone instead of a liquid system. These CSPEs have seen various applications in both batteries as well as printed FET technology. [41, 49]

Using protons instead of salts as ions for electrolyte gating has been shown in water-gated devices. [50, 51] Notably ion movement here is governed by the Grotthus mechanism, that describes hopping of protons between water molecules and is considerably faster

than the actual movement speed of a specific proton. [52] This mechanism may also be expanded from solutions to surfaces with protic or proton-accepting functionalities or absorbed protic solvents. [53]

2.1.5. Functionality of Field-Effect Transistors

When operating an FET, one major question is when does the semiconductor change from an insulating to a conductive state – or to be more precise – when does the channel form as conductive path between source and drain electrode. The necessary gate voltage to form this is called threshold voltage V_{th} and is a unique property of each individual device and prone to manyfold influences. Just to name a few, it is e.g. dependent on the channel material, its orientation and crystallinity, the gate insulator material and thickness, or the contact quality between insulator and semiconductor. While often semiconductor and channel are used interchangeably, *semiconductor* describes the material and building element, while *channel* strictly speaking only stands for the regions in a semiconductor that have excess charge carriers available that may be used to create a current.

In fig. **2.8**, the different modes of the channel depending on V_{GS} and V_{DS} are depicted for an n-type device. In the first case (a), the gate voltage is below the threshold voltage and no channel is created. As explained in the previous section, formally for lower gate voltages, the inversion mode conductivity is possible then, but not further regarded here. In the second case (b), the channel is equally formed at the semiconductor surface. Once a drain voltage is applied (c) a profile with a smaller channel towards the drain contact is formed since electrons are extracted. This may also be understood as the drain voltage polarizing the channel contrary to the gate bias. The carrier density Q at a given point x along the channel – which spans from 0 to length L – is given as:

$$Q(x) = C'(V_{\mathrm{GS}} - V_{\mathrm{th}} - V(x)) \tag{2.4}$$

where C' is the areal double layer capacitance at the semiconductor insulator contact and $V(x)$ the voltage between x and the drain. At the pinch-off point (d), $Q(L)$ drops to 0, and a further increase of V_{DS} (e) will not increase the current as all available charge carriers are already contributing to I_{D}.

Fig. **2.8f** shows a typical I-V-characteristic, also-called output curve, of an n-type semiconductor at a given $V_{\mathrm{GS}} > V_{\mathrm{th}}$. I_{D} may be derived from eq. **(2.4)** by knowing that the local current density $J(x)$ is a function of the carrier densities and their drift velocity

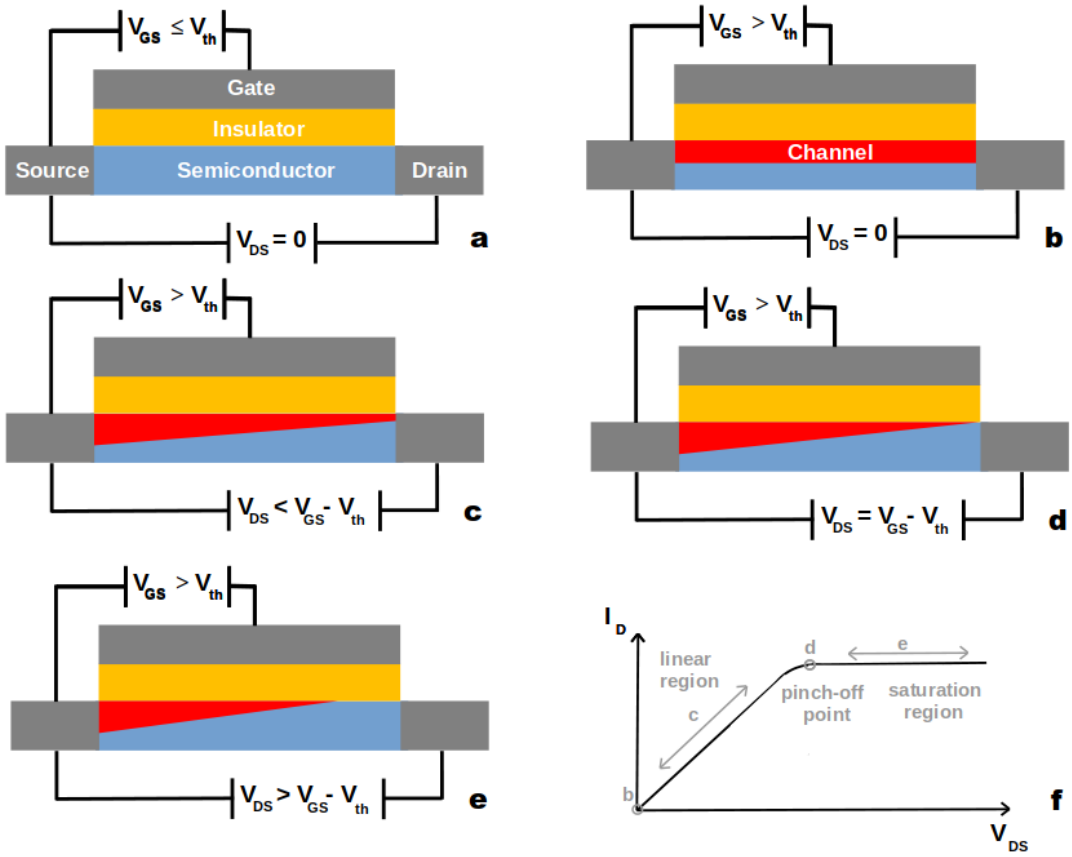

Figure 2.8.: Distribution of the channel at varying V_{GS} and V_{DS} settings: a) no channel is formed, b) channel is equally distributed, c) linear-region: channel becomes smaller towards drain contact, but still is established though the whole length d) pinch-off point: channel vanishes at drain contact e) saturation region: channel vanished before drain contact, a pinch-off region without channel is formed; f) typical I-V-characteristic with indicators which channel schematic applies

v_n. Note that in the following, channel polarization will be assumed as being a pure surface phenomenon and thus the depth of the polarization is regarded as constant and small and will be factored in the spatial and areal values for charge and current density,

respectively, and be denoted as $Q'(x)$ and $J'(x)$.

$$J'(x) = Q'(x)v_n \tag{2.5}$$

The drift velocity itself is a function of the electric field E (in this case between source and drain) and the electron mobility μ. The latter is a material property that describes the relation between electric field and drift velocity and may be regarded as a term describing internal movement restrictions of charge carriers.

$$v_n = \mu E = \mu \frac{\mathrm{d}V(x)}{\mathrm{d}x} \tag{2.6}$$

Substituting eqs. **(2.5)** and **(2.6)** into eq. **(2.4)**, forms

$$J'(x) = C'\mu \frac{\mathrm{d}V(x)}{\mathrm{d}x}(V_{\mathrm{GS}} - V_{\mathrm{th}} - V(x)) \tag{2.7}$$

The current densities may now be transformed to the current via the channel width W, as $I = J'W$. Using this relation and separation of variables, eq. **(2.7)** may be integrated:

$$I \int_0^L \mathrm{d}x = C'\mu W \int_0^{V_{\mathrm{DS}}} (V_{\mathrm{GS}} - V_{\mathrm{th}} - V(x))\mathrm{d}V(x) \tag{2.8}$$

Leading to the description of the I-V-curve:

$$I_D = C'\frac{W}{L}\mu((V_{\mathrm{GS}} - V_{\mathrm{th}})V_{\mathrm{DS}} - \tfrac{1}{2}V_{\mathrm{DS}}^2) \tag{2.9}$$

The linear region can now be described by assuming that $V_{\mathrm{DS}} \ll V_{\mathrm{GS}} - V_{\mathrm{th}}$ and thus neglecting the quadratic term in eq. **(2.9)** leading to the linear function in V_{DS}:

$$I_D = C'\frac{W}{L}\mu(V_{\mathrm{GS}} - V_{\mathrm{th}})V_{\mathrm{DS}} \tag{2.10}$$

At the pinch-off point, V_{DS} equals $V_{\mathrm{GS}} - V_{\mathrm{th}}$ and thus the saturation current is given as:

$$I_{\mathrm{D,sat}} = \frac{C'W}{2L}\mu(V_{\mathrm{GS}} - V_{\mathrm{th}})^2 \tag{2.11}$$

To be more precise, the mobility μ should be replaced by the field-effect mobility μ_{FET} of the same dimension. This value represents the effective mobility of an individual device that is dependent not only on the ideal mobility of the material, but as well as manyfold factors, e.g., semiconductor crystallinity and grain sizes, electrical grain contacts, channel dimensions, or metal semiconductor contact. In general, the field-effect mobility is highly process-dependent.

2.1.6. Operation of Field-Effect Transistors

Fig. **2.9** shows typical device characteristics of a printed EGFET. In **(a)** a series of output curves with increasing V_{GS} is shown, whereas for the purple graph V_{GS} is still below V_{th} and thus there is no current. The dotted line is the quadratic function of the positions for the pinch-off points where the saturation current is reached as described in eq. **(2.11)**.

When a transistor is operated with a constant V_{GS}, the transfer characteristic is obtained by varying V_{GS} as shown in **(b)**. It is typical for electrolyte-gated devices to show a certain hysteresis when V_{GS} is swept up and down. This can be attributed to a delayed response of the ionic movements to the gate bias, or ions and charge carriers being tapped in locally favorable states (trap states). [54] Saturation in I_D versus V_{GS} occurs due to the limitations of channel polarization.

Outside a certain range for V_{GS}, the electrolyte will be electrochemically decomposed, generally this is visible in an increased (absolute) value for the gate current I_G, a value describing leakage into the gate electrode. In dielectric-gated devises leakage current may occur due to pinhole connections or beyond the breakdown voltage of the insulator. A schematic of typical leakage currents are shown in fig. **2.10**. In case **(a)**, the electrolyte is stable, case **(b)** corresponds to fig. **2.9b**. In a reasonable device leakage currents must be several orders of magnitude smaller than I_D in order to ensure a clear differentiation between on- and off-states.

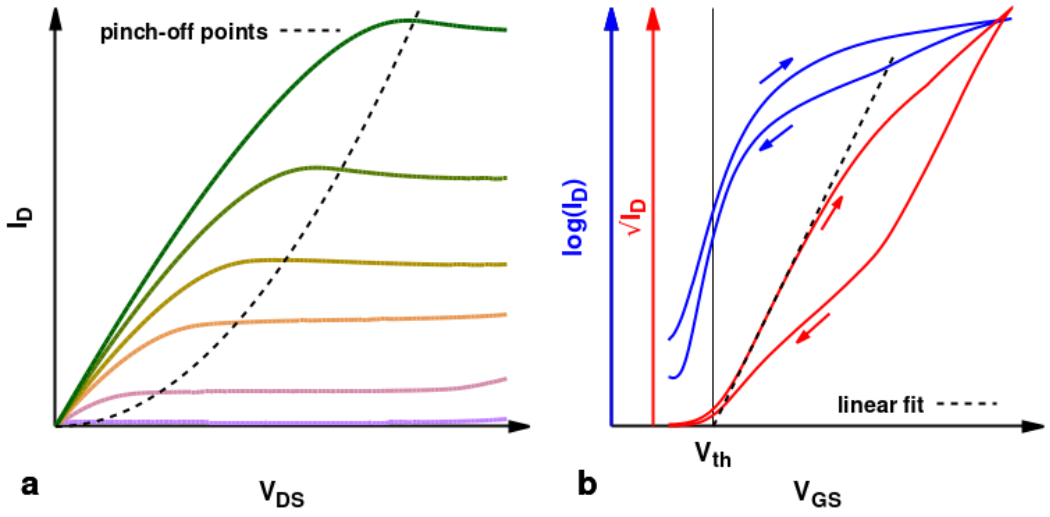

Figure 2.9.: Typical device characteristics; a) output curves at increasing V_{GS}, in the case of the purple graph, V_{GS} is below V_{th} and no current present, the dotted graph marks pinch-off points, where $V_{DS} = V_{GS} - V_{th}$ (see eq. **(2.11)**; b) transfer characteristics (blue) and square root of I_D (red) with linear fit for determining V_{th} at $I_D = 0$

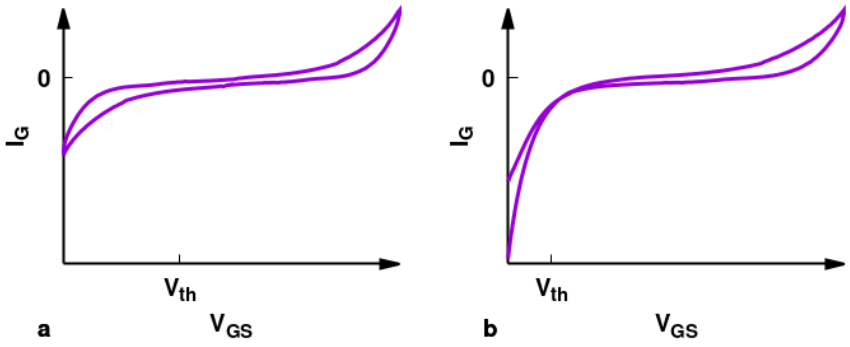

Figure 2.10.: Typical leakage current curves, a) electrolyte is stable within operational range, b) electrolyte is decomposed at lower voltages (curve matching to fig. **2.9b**)

2.1.7. Obtaining Key Properties of Field-Effect Transistors

Threshold Voltage

As should be obvious by now, V_{th} is a key property of FETs. It may be obtained by rewriting eq. **(2.11)** as

$$\sqrt{I_D, sat} = \sqrt{\frac{C'W}{2L}\mu_{\mathrm{FET}}}\ (V_{\mathrm{GS}} - V_{\mathrm{th}}) \tag{2.12}$$

creating a linear correlation between $I_{\mathrm{D,sat}}$ and V_{GS}, with V_{th} easily determined at $I_D = 0$. In fig. **2.9b**, this fit is already shown. This so-called square root method approach allows for fitting a simple function to a reasonable large amount of data points and thus can be considered as stable versus statistical measurement variations.

Field-Effect Mobility

With the linear fit, μ_{FET} may be extracted from the obtained slope a via

$$a = \sqrt{\frac{C'W}{2L}\mu_{\mathrm{FET}}} \Rightarrow \mu_{\mathrm{FET}} = \frac{2a^2L}{C'W} \tag{2.13}$$

For this the areal capacitance C' and the geometry values W and L have to be known. Fig. **2.11a** depicts a typical layout of a printed, in-plane, displaced gate, electrolyte-gated field-effect transistor. Source, drain and gate are made from a conductor, the printed channel interconnects source and drain leads, and a printed electrolyte covers both, the channel and gate, and ideally as little of the source and drain leads as possible. As the sizes for W and L in this work usually lie in the two-digit micron range, these two values may be obtained from an optical microscope.

The determination of C' on the other hand is more complex. As explained in sec. **2.1.4**, each electrode-electrolyte-contact site acts as a capacitor, thus the system gate-electrolyte-channel can be considered as two capacitors in series. However, often it is not possible to fully exclude contact between the electrolyte and the source or drain leads, as shown in fig. **2.11a**. Therefore on the capacitance on the channel side consists of two capacitors

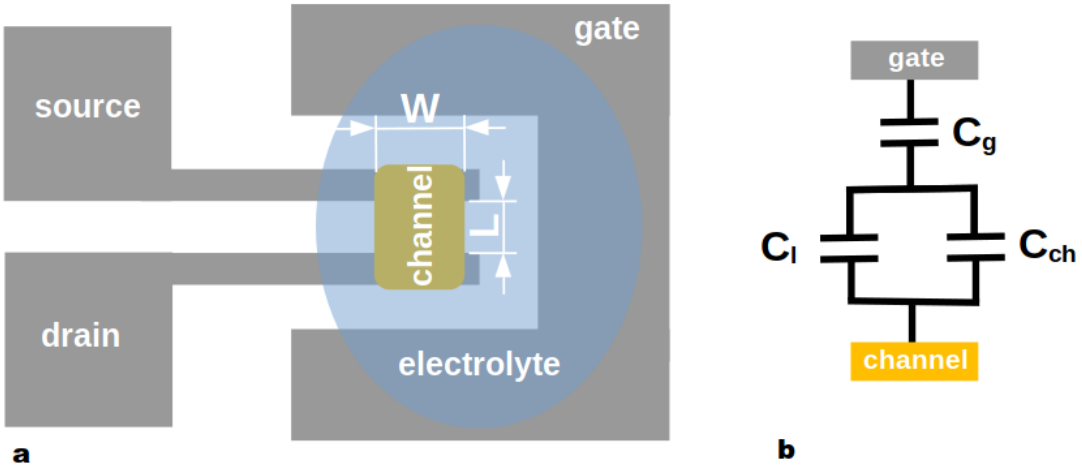

Figure 2.11.: a) typical layout of a printed electrolyte-gated field-effect transistor with channel width W and length L indicated; b) circuit depiction of the capacitors in the gate-electrolyte-channel/leads system with capacitances between electrolyte and gate (C_g), source/drain leads (C_l), and channel (C_{ch}), respectively

in parallel stemming from the channel and lead contact areas, respectively. The total capacitance C_{tot} can be measured by short-circuiting source and drain and applying a bias versus the gate. C_{tot} now can be expressed as

$$\frac{1}{C_{tot}} = \frac{1}{C_g} + \frac{1}{C_l + C_{ch}} \tag{2.14}$$

As the contact area on the gate side is very large, so is the capacitance there, and thus $C_g \gg C_l + C_{ch}$ making $1/C_g$ negligible in the above equation:

$$C_{tot} = C_l + C_{ch} = C_{l,ar} A_l + C' A_{ch} \tag{2.15}$$

$$\Rightarrow C' = \frac{C_{tot} - C_{l,ar} A_l}{A_{ch}} \tag{2.16}$$

Where $C_{l,ar}$ and C' are the areal capacitances of the leads and channel, respectively. A_l and A_{ch} are the corresponding contact areas which, again, can be gained from optical measurements. $C_{l,ar}$ must be obtained from reference devices no channel. Applying the same logic as eqs. **(2.14)** and **(2.15)** when neglecting C_{ch} in fig. **2.11b**, it follows that

$$\frac{1}{C_{tot,ref}} = \frac{1}{C_g} + \frac{1}{A_{l,ref} C_{l,ar}} \quad \wedge \quad C_g \gg C_l \tag{2.17}$$

$$\therefore C_{l,ar} = \frac{C_{tot,ref}}{A_{l,ref}} \tag{2.18}$$

$C_{tot,ref}$ and $A_{l,ref}$ again can be obtained from electrical or optical measurements, respectively.

It should be noted that despite C' seemingly being a material property, it should still be obtained individually for each device to ensure that possible process variations are taken into account.

Drain Current On-Off-Ratio

For a good differentiation between an open and a closed channel, the ratio between the currents in the on- and off-state, $I_{D,on} / I_{D,off}$, is of relevance, where $I_{D,on}$ and $I_{D,off}$ are the maximum and minimum currents in a transfer graph, respectively. Usually this should span several orders of magnitude.

Subthreshold Swing

As can be seen in fig. **2.9b**, I_D is already rising before the threshold voltage is reached. While this rise is small in absolute numbers (I_D is depicted on a logarithmic scale), this so-called subthreshold swing describing the rise between the minimum drain current $I_{D,min}$ and the current $I_{D,th}$ at $V = V_{th}$ is an indicator for surface trap states. [55] It is determined in terms of voltage change per decadic change of the current as

$$S = \frac{\mathrm{d}\, V_{GS}}{\mathrm{d}\, log_{10}(I_D)} \tag{2.19}$$

but may also be described using the double layer capacitance of the gating material C_{dl} and the capacitance contribution from trap states C_t at a given temperature T:

$$S = ln(10)\frac{k_{\mathrm{B}}T}{q} \cdot \frac{C_{\mathrm{dl}} + C_t}{C_{\mathrm{dl}}} \tag{2.20}$$

In an ideal device, no surface traps exist, and thus $C_t = 0$. This allows calculating the theoretical lower limit of S, which at room temperature is 60 $\frac{mV}{dec}$.

2.2. Printing Technology

For fully understanding printed FET technology, not only the basics of FETs, but also the borders set by the printing technology must be understood. Laboratory scale printing often means having variable layouts and many varying inks, possibly expensive or in need of an effortful synthesis, and thus only available in sparse amounts. For this reason, printing methods that allow using little amount of ink, applying it directly onto the substrate, and easily changing the printing design have established themselves in the first step of research on printed materials. Within this work ink-jet printing and microplotting is applied and hence a deeper understanding of these technologies is necessary. Both are drop-on-demand technologies, i.e., the ejection of a droplet can be individually controlled and thus the deposition may occur both contactless and by applying any digitally designed pattern. This makes drop-on-demand technologies highly versatile towards design changes and besides a digital design no actual physical template needs to be produced.

2.2.1. Ink-Jet Printing

In ink-jet printing, a print head is equipped with nozzles that have piezoelectric crystals attached. Once the print head has reached the correct position over the substrate, the piezo element is used for squeezing out ink as desired. In fig. **2.12** schematics of the nozzle and the steps during printing are depicted. When printing with an ink-jet system, first, the design is created digitally and ink deposition points are defined in the structures. After deposition, the droplets will spread on the substrate, depending on the interactions between ink and substrate, as well as drying speed, and merge to form the desired structure. Eventually, the ink will dry fully. Optionally the substrate may be heated during

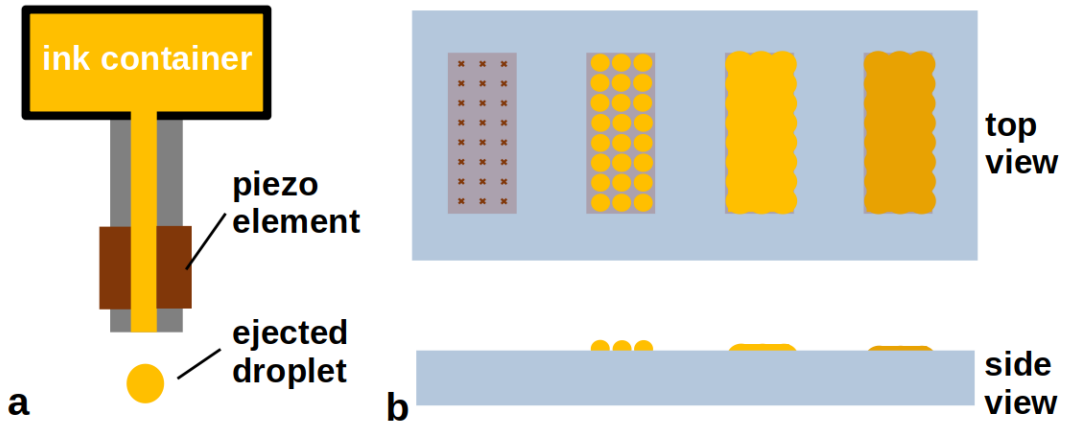

Figure 2.12.: a) jetting nozzle of an ink-jet printer b) steps during ink-jet printing on a substrate (blue) with top (top) and side (bottom) view; from left to right: digitally designed pattern with calculated ink deposition positions, drop pattern directly after deposition, ink spreads and droplets combine to continuous pattern, final structure after ink has fully dried

deposition in order to speed up the drying process, which may also be used to influence the spreading. Deposition point distances can be varied according to the expected spread radius after deposition. If desired multiple layers may be deposited.

For creating a good and sharp pattern, it must be ensured that the interaction between ink and substrate neither leads to the ink spreading out too far nor a lotus effect. If the interaction is too repellent, the droplets may merge into a single large drop, if the spreading goes too far, the structures become too large. In either case the thickness of the films will also be outside the desired values. E.g., a better interaction with polar inks may be reached by treating the substrate in an oxygen plasma before deposition.

Drop sizes of the system used within the scope of this work are in the 10 pL range. The diameter of a single dried-in droplet will therefore be in the lower two-digit micron range and the resolution of the patterns is limited by this value.

To ensure good printability, the inks must lie within the approximate window of $1 \leq Z \leq 10$ where Z is a function of the density ρ, surface tension σ, and viscosity μ of the ink as

well as the diameter d of the drops. [56]

$$Z = \frac{\sqrt{\rho\sigma d}}{\mu} \tag{2.21}$$

Inks outside this window may either be too viscose to be ejected, too thin to be retained even if no jetting signal is sent or – in less extreme cases – lead to satellite drops during jetting, that may spoil the printed structure.

2.2.2. Microplotting

In the microplotting technique, a glass capillary is dipped into an ink reservoir and takes up the ink via capillary forces. Once placed over the substrate, the ink may be released by an ultrasonic signal that is created via a piezo crystal to which the capillary is attached. The frequency of the signal is varying with the setup and chosen as the resonance frequency of the system. In general, droplet diameters with this technique are slightly larger than with ink-jet printing, but of course vary depending on capillary size, ink viscosity and interaction between ink and substrate. Within this work, ink has been applied using the system as a pen writing device. For this the ink-filled capillary is brought into contact with the substrate and the ink is released due to adhesive forces between ink and substrate, possibly supported by an ultrasonic pulse for the initial release. After that, the capillary is slightly raised and moved across the substrate in the desired pattern, and the ink released from the capillary solely based on adhesion to the substrate and surface tension with already deposited ink.

In general, microplotting allows for usage of inks with larger particle sizes, as the capillary opening is wider than the nozzles in ink-jet printing and has less tendency to clog.

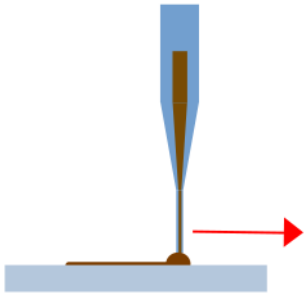

Figure 2.13.: Ink application by moving an ink-soaked glass capillary above the substrate; the ink is dragged out of the capillary due to its surface tension

2.2.3. Limitations

While being an effective method for applying material in defined patterns at desired positions, there are also a few limitations in printing that need to be considered.

Coffee Ring Effect

Once a droplet is deposited on the substrate, the outer contact line is pinned due to interaction with the surface. As the solvent evaporates more rapidly on the edges due to the curvature of the drop's surface, a material flow towards the edges is created. [57] Effectively, this will lead to more material being deposited on the edges, but the effect is dependent on the contact angle with the substrate and the loading with colloidal particles. [58]

The coffee ring effect may be reduced by changing the ink composition. Adding a high viscosity component will suppress particle movement, a solvent mixture from liquids with differing vapor pressures will influence the evaporation on the edges due to accumulation of the component with the higher boiling point, or changing the pH will lead to variations in the interactions with the surface and between particles. [59, 60] Other approaches include adding nanofibers or changing the shape of the particles themselves. [61, 62]

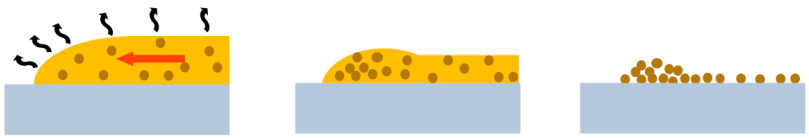

Figure 2.14.: Coffee ring effect, from left to right: solvent evaporation at the edge is quicker, due to the larger relative surface, creating a mass flow towards the edge; particles are dragged with the solvent and accumulate at the edge; particle distribution after the droplet dried

Resolution and Scale-Up

Reports have shown drop volumes of 500 fL leading to a 20 μm diameter in the deposited blot. [63] However, the necessary small nozzle will also limit the possible inks, particle loadings and particle sizes. A 10 pL droplet, as applied withing this work, will lead to blot diameters of 50-70 µm.

Ink-jet printing is considered the technology with the highest resolution, however is comparably slow. A scale-up for high production throughput will therefore demand for a change to roll-to-roll printing, which usually are contact-based methods, have lower resolution and will also demand for an adaption of the ink compositions. [64]

Printing Accuracy

Printing accuracy and reproducibility are key factors for ensuring constant device characteristics and are especially necessary for producing complex logics consisting of multiple device build groups. Droplet positioning may be inaccurate due to variations in ejection speed or angle, additionally, satellite drops may lead to unwanted pattern effects. Fig. **2.15** shows a selection of possible printing errors with the results varying from changed properties to fully inoperable devices. In case of the channels, the ideal positioning is symmetrical versus the leads as to acquire the same channel widths on source and drain, and a good coverage of the leads. The electrolyte should cover a large area of the gate contact in order to create high capacitance, must cover the whole channel to ensure full channel activation, and should be as little as possible in direct contact with the source and drain leads as not to create parasitic capacitances and leakage currents. For top-gated devices, it is important, that the electrolyte has no pinholes and that the top gate is placed well above the channel.

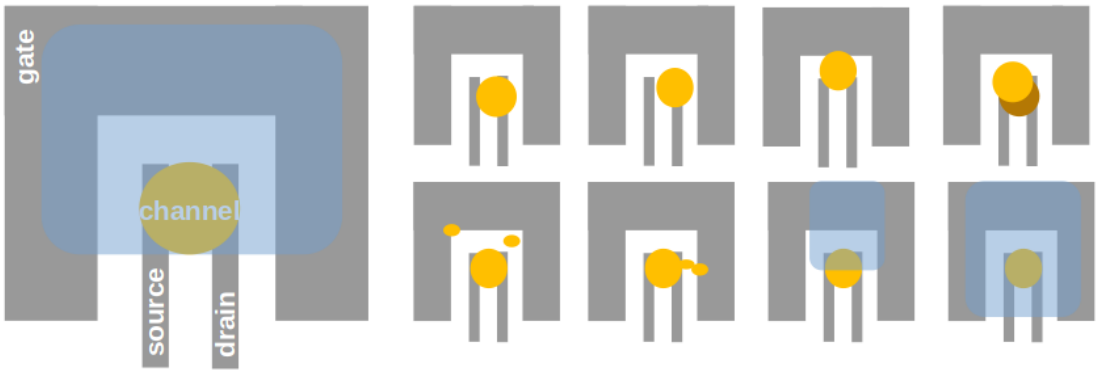

Figure 2.15.: Ideal print (left) and printing errors (right) along rows: misplaced channel leading to different widths on each lead, missing contact to one lead, short circuit with gate, second printing layer misaligned, satellite drops (fully functional device), satellite drops leading to short circuit, channel only partially covered by electrolyte, electrolyte overly covers source and drain leads

Printing errors may be corrected to some extent, e.g., missing electrolyte can be added or a missing contact between channel and lead may be established by a second printing step.

2.3. Thin-Film Deposition Methods

Next to printing, within this work, two additional thin-film deposition methods are applied.

2.3.1. Atomic Layer Deposition

Atomic layer deposition is a deposition method that relies on chemical reactions between the surface and a gaseous reactant, that may not react with itself. Once the reactant has covered all possible reaction sites of a surface, the layer self-terminates. By alternately using two or more matching precursors, a material can be deposited layer by layer with atomic precision. [65] ALD is known for its extremely good surface conformity and the possibility to even uniformly cover porous structures. The concept is shown in fig. **2.16**

for synthesis of Al_2O_3 from $AlMe_3$ and H_2O on a surface with hydroxy functionalities, e.g., an oxide that was exposed to humidity.

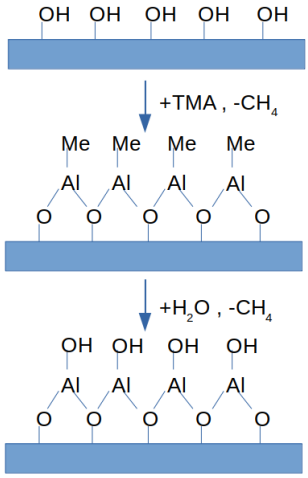

Figure 2.16.: Schematic of an ALD-cycle, top to bottom: substrate with hydroxy functionalities, addition of aluminium from $AlMe_3$ as precursor upon release of CH_4, water as precursor for oxygen again leads to a hydroxy-functionalized surface

2.3.2. Sputtering

In sputtering, material is deposited onto a substrate by bombarding a source target with reactive or inert particles in order to eject material from the source and condensate it onto the target. The high energetic particles needed for the bombardment are created by a glow discharge plasma. [66] By changing the gas concentrations during sputtering, the properties of the deposited material can be influenced. This includes both roughness and defect concentrations. [67, 68]

2.4. Material Analysis

2.4.1. X-Ray Diffractometry

X-ray diffractometry relies on the reflection of monochromatic X-rays at the planes of a crystal. As reflected waves between two different parallel planes will have a path distance, constructive interference is only possible if the incident angle θ matches so that the path distance is an integer multiple of the wavelength λ. In an ideal, infinite crystal, all other interferences will be destructive, and thus the plane distance d can be obtained from Bragg's equation:

$$n\lambda = 2d\sin(\theta) \tag{2.22}$$

Notably manyfold crystal planes may be defined in a structured system, leading to specific diffractometry patterns for different materials. If ions in a crystal lattice are substituted, the different size will lead to a change in the unit cell size, and thus a shift of the peak positions in the diffractogram.

2.4.2. X-Ray Reflectometry

In X-ray reflectometry, the change in refraction angles between materials with different electron densities are exploited. The sample is exposed to an X-ray near parallel to its surface. As the interference of the waves reflected at the different phase boundaries will vary between constructive and destructive depending on the incident angle, oscillation in the detected intensities will occur. However, the reflection will be disturbed by rough sur- and interfaces. Using the oscillation frequency and the intensity reduction of the reflected waves, thickness, density, and roughness of the material layers in the sample can be determined.

2.4.3. Thermogravimetric Analysis

In TGA, a sample is heated in an inert or reactive atmosphere and the mass change measured. Using the stoichiometry of possible chemical reactions, decomposition processes occurring at specific temperatures can be determined.

2.4.4. Scanning Electron Microscopy

In SEM, a sample is exposed to a ray of electrons accelerated by high voltages. As the electron reflection is based on the electronic density of a material, its conductivity and surface, the reflected electrons may be used for creating an image of the sample. The higher the acceleration voltage, the deeper the electrons may enter the sample.

2.5. Printed EGFETs in Current Research

Printed EGFETs with displaced gates are considered the starting point of this thesis, and therefore, an overview of the current state of research on this topic is necessary.

In general, the term printing has a very wide definition – applying material or its precursor from a solution – which means also, e.g., spin-coated semiconductors where the device dimensions are later defined by the applied leads are typically categorized within printed electronics. [41] The same broadness of the field applies to the channel materials: organic SCs, and graphene- or nanowire-based channels do remain big topics and so does dielectric gating. [41, 69–72] Therefore, the view on the state of the art will focus on inorganic, ceramic channels, direct writing methods, and electrolytic gating, which is still a huge field in current research activities.

Within this field, one may distinguish between amorphous and crystalline oxides, where the former allow flexibility in the composition and the latter naturally fixed stoichiometries only. The most important amorphous oxidic SC might be indium gallium zinc oxide. IGZO has been shown to have a vast compositional range where it remains amorphous, yet acting as a semiconductor. [73] Amorphous systems have two advantages: instabilities in processing, i.e., fluctuations in the ink composition are more tolerable, and properties are independent of material orientations. Stoichiometric compounds, on the other hand, have, in general, shown better mobilities, but are more sensitive towards defects – which, on the other hand, may be positively exploited by systematic doping. [41, 74] The most commonly applied crystalline oxide SCs are ZnO, SnO_2, and In_2O_3. While ZnO has been shown with already considerable mobilities of up to 62 $\frac{cm^2}{Vs}$, the latter two both have gone far beyond 100 $\frac{cm^2}{Vs}$ in ink-jet printed FETs. [75–77] Notably, this is in the same range as reports for polycrystalline Si in printed systems. [78, 79] Using alterative annealing approaches in order to reduce the harsh temperature regime, UV-assisted temperature annealing and self-annealing particle inks have been successfully demonstrated with In_2O_3 but lead to considerably lower mobilities between 5 and 13 $\frac{cm^2}{Vs}$. [80, 81]

Electrolytic gating remains popular with researchers in the field, due to the advantages already discussed in sec. **2.1.4**: the possibility of printing the materials and the resulting high surface conformity, as well as operation in the low range of typical battery voltages. [41] Typical problems with hygroscopy of ion gels are not necessarily transferred to ion gels, i.e., blends of a polymer with an ionic liquid. Recently, a system, self-gelating at room temperature, sticky to surfaces, and stable versus ambient conditions, has been described. [82] However, humidity-dependent behavior has been seen earlier in CSPEs. [83] Even the assumingly low frequencies of EG have been overcome in various examples in devices with switching speeds of several hundred Hz often using top-gated systems. [75, 83, 84]

The reliability of printed EGFETs has risen to the stage that more complex electronic logics such as ring oscillators or latches, i.e., single-bit data storage devices, could be realized. [83, 85] However, printing still accounts for certain random process variations. This effect already has be exploited in cryptographic applications using physical unclonable functions. Here, a random cipher derived from the printing process fluctuations is created and considered as irreproducible. [86]

In conclusion, using printed EGFETs based on In_2O_3 and SnO_2 can be considered a sound basis for the works in this thesis. Detailed insights regarding the current research in the parameters chosen for optimization within the scope of this thesis – printed vertical FETs, channel doping, and alternative gating materials – are discussed in the respective chapters.

3. Experimental Part

3.1. Ink Preparation

3.1.1. Precursors for Pristine and Chromium-Doped Indium Oxide

Parent solutions of 0.1 M $In(NO_3)_3 \cdot xH_2O$ (99.99 % Sigma-Aldrich), and 0.025 M $Cr(NO_3)_3 \cdot 9H_2O$ (99.99 % Alfa Aesar), respectively, in a 4:1-(v/v)-mixture of deionized water and glycerin, as well as the pure solvent mixture have been prepared. Salt solutions were ultrasonicated for 5 minutes and all solutions stirred for at least half an hour leading to transparent solutions. The respective doping concentrations were achieved by mixing the solutions according to the below table and again intense stirring for at least half an hour to ensure a homogeneous distribution of the dopant. The final inks have been directly used for printing within the same day. This ink preparation is a variation of an established recipe for pure In_2O_3-precursor inks. [77] For the experiments involving ALD-derived Al_2O_3 as electrolyte, a 0.05 M $In(NO_3)_3$ ink has been prepared directly without parent solutions.

Ink	V_{In} [ml]	V_{Cr} [ml]	$V_{solvent}$ [ml]	doping ratio [In:Cr]	$n_{Cr}/(n_{Cr}+n_{In})$ [%]
1	1	0	1	40:0	0
2	1	0.1	0.9	40:1	2.5
3	1	0.2	0.8	40:2	5.0
4	1	0.3	0.7	40:3	7.5
5	1	0.4	0.6	40:4	10.0
6	1	0.5	0.5	40:5	12.5

Table T3.1.: Volume and molar ratios for different doping concentrations

3.1.2. Composite Solid Polymer Electrolyte

The CSPE is prepared following an established route [87]. At 80 °C, 0.3 g poly-(vinylalcohol) are dissolved in 6 g of DMSO under stirring. Separately 70 mg $LiClO_4$ are dissolved in 0.63 g propylene carbonate under stirring. Once both mixtures are fully dissolved, the PVA solution is added to the salt solution and stirred over night at 60 °C. The resulting clear liquid is filtered through 0.45 µm PTFE syringe filters and then directly used in the printing.

3.1.3. Precursor for Porous Tin Dioxide

54 mg of $SnCl_2 \cdot 2H_2O$ are dissolved in 4 ml of a 3:1-(v/v)-mixture of deionized water and isopropanol by 10 min of ultrasonication followed by 5 min of stirring. To the white and turbid but stable solution, 1 ml of hydroxylate functionalized polystyrene beads with a diameter of 200 nm (Polysciences Inc., 2.5 % w/v suspended in H_2O) was added and intensively shaken. The inks were used without further processing on the same day.

3.1.4. Commercially Available Inks

Graphene has been printed using a commercially available ink by Sigma-Aldrich with a flake size of 0.3-2 µm. Poly(methyl methacrylate) (PMMA) in anisole is a typical resist for e-beam lithography and was also applied for temporarily covering contact areas during ALD. Both inks were used for the respective applications without further treatment.

3.2. Device Preparation

Unless stated otherwise, all inks were applied with a Dimatix DMP 2831 materials printing system using cartridges with 10 pL-nozzles.

3.2.1. Vertical Field-Effect Transistors with Porous Channels

The devices with vertical porous channels have been prepared as shown in fig. **3.1**. First Pd-passive structures are created using e-beam lithography and 50 nm of sputtered Pd with a 3.5 nm Cr seed layer. The bottom lead has a width of 1 µm and all electrodes are designed with large contact pads for attaching the measuring equipment. Second the ink (see sec. **3.1.3**) is printed as two overlaid single drops. After drying, the top lead with a width of 2 µm is applied via e-beam lithography and sputtering 50 nm of Pd or W, respectively, without seed layer in either case. The lift-off is done with Acetone for no more than 1 min. The sample is annealed in air using an oven and a heating rate of 4 °C/min from room temperature to 400 °C and maintaining the heat for 1 h before cooling down to 200 °C or less before taking the samples out of the oven. During the annealing, the polystyrene beads were completely burnt away leaving a porous, sponge-like structure in the channel material. Once cooled down to room temperature, the CSPE (see sec. **3.1.2**) has been applied in five layers. It was ensured that the electrolyte covers the porous channel and a large part of the gate electrode, while trying to cover as little of the source and drain leads as possible.

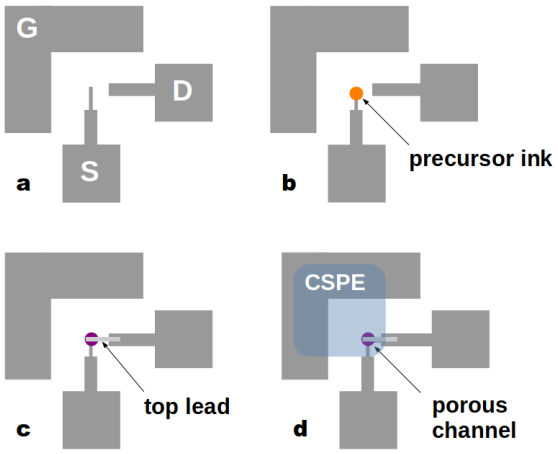

Figure 3.1.: a) **G**ate, **S**ource, and **D**rain contacts from platinum as obtained via EBL; b) precursor as printed; c) after applying W top lead via EBL and annealing; d) final device after applying electrolyte

Alternatively to the use of electrolyte, vFETs with dielectric gating were prepared analogously by application of 10 nm Al_2O_3 via ALD after step **c** and subsequently printing

silver or graphene inks likewise to the electrolyte in step **d**. ALD was applied in several tries using 180 cycles at 130 °C and 200 °C, respectively. After applying the conductive inks, the devices were annelead at 200 °C on a hotplate for 30 min.

3.2.2. In-Plane Field-Effect Transistors with Doped Channels

Commercially available glass substrates with sputtered ITO coatings (R $\leq$ □) were structured by ablation lasering using a TRUMPF TruMicro 5000 system at a laser frequency of 800 MHz and a power of 3 W in a grid pattern leaving a predefined gap of 50 µm between source and drain leads.

After cleaning the substrates by ultrasonication in iPrOH for 5 min and rinsing twice with iPrOH and deionized water, channel inks (see sec. **3.1.1**) were printed in two, in a second series four, layers. Once the ink has dried at RT, channels were annealed in air with a box furnace by heating to 400 °C within 2 h, maintaining the temperature for 2 h and cooling down to RT overnight. Finally, the CSPE (see sec. **3.1.2**) was printed with the same system in eight layers and it was insured to cover the channel and a large portion of the gate electrode. Before measuring the CSPE was allowed to dry for 2 h in ambient conditions.

Reference samples without channel for capacitance measurements received the same temperature treatment as applied for the annealing step.

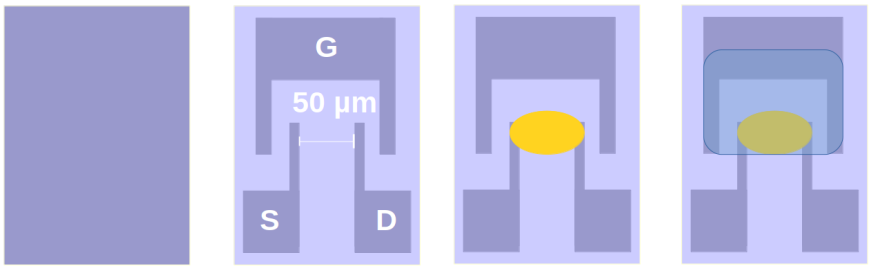

Figure 3.2.: Production steps from left to right: ITO glass before ablation lasering; passive structure with (S)ource, (D)rain, and (G)ate electrodes; channel (yellow) after printing and annealing; printed CSPE (light blue)

3.2.3. FETs with ALD-Derived Al_2O_3 as Solid Electrolyte

ITO-substrates have been patterned by ablation lasering with channel lengths predefined to 20 µm. Two layers of the undoped In_2O_3 precursor ink as described in sec. **3.1.1** have been applied of single printed drops in two layers between drain and source electrodes using the Dimatix printing system. Annealing was done in air by heating from RT to 400 °C within 1.5 h, maintaining the temperature for 1.5 h and cooling down over night.

Contact pads have been covered with poly (methyl methacrylate) dissolved in anisole using a glass capillary before starting the ALD process. Al_2O_3 was applied by alternating trimethyl aluminium and H_2O in 350 cycles at 130 °C using a Picosun R-200 Advanced system. This resulted in a 20 nm layer of the target material. The cycle number was determined and confirmed in each ALD-process by controlling the thickness of the deposited Al_2O_3 via XRR-measurements on fresh silicon wafers with thermal SiO_2 coating as reference samples. The contact pads were freed of Al_2O_3 by lift-off in acetone and in a first series, a commercially available silver nanoparticle ink (particle size 2-4 nm) was applied as top gate with a Sonoplotter system and annealed in air on a hot plate at 150 °C for 30 min. Since devices with silver top gating have shown considerable large leakage currents and increased rate of short circuits, the top gate material was replaced by graphene using a commercially available ink (Sigma-Aldrich, flake size 0.2-3 µm) and annealed on a hotplate at 200 °C for 30 min.

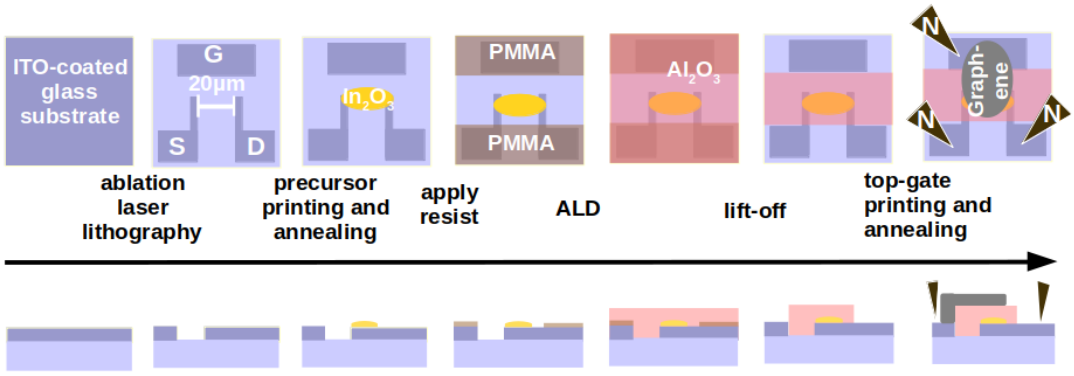

Figure 3.3.: Production steps from left to right (top: top view, bottom: side view): ITO glass before ablation lasering; passive structure with (S)ource, (D)rain, and (G)ate electrodes; channel (yellow) after printing and annealing; PMMA resist; post-ALD; after lift-off; with graphene (or silver) top gate and position of measurements contact (N)eedles

3.3. Material Characterization

3.3.1. Scanning Electron Microscopy

Scanning electron microscopy has been done using a Zeiss Leo 1530 system, no conductive coating has been applied.

3.3.2. Thermogravimetric Analysis

The ink as prepared in sec. **3.1.3** has been air-dried as well as a reference sample of the pure polystyrene suspension. Either sample was placed in alumina crucibles and has been analyzed with a NETZSCH TG 209F1 Libra at a heating rate of 4 °C/min from RT to 400 °C in a 20 ml/min air flow in order to match annealing conditions. Only the $SnCl_2$-containing sample resulted in a white powder after TGA, while the pure polystyrene sample completely vanished.

3.3.3. X-Ray Diffractometry

X-ray diffractometry was done using a Bruker D8 Advance with Kα-radiation within the respective angle ranges.

Chromium-Doped Indium Oxide

1 ml of each ink as prepared in sec. **3.1.1** has been annealed according to sec. **3.2.2** in glass petri dishes. After cooling, the powders were scratched off and used for acquiring the XRD-patterns. Rietveld analysis was done with the TOPAS V.5.0 program suite.

Porous Tin Dioxide

The powder remaining after TGA as in sec. **3.3.2** was analyzed as is.

3.3.4. X-Ray Reflectometry

The thickness and density of ALD-derived Al_2O_3 was confirmed by XRR measurements. To do so a reference sample on a silicon wafer covered by thermal SiO_2 was co-processed during the Al_2O_3 deposition for devices according to sec. **3.2.3**. XRR was measured with a Bruker D8 Discovery system using Kα-radiation. A fitting curve has been generated with the LEPTOS program suite (v.2.03) in the range of $0.4° \leq 2\theta \leq 4.0°$ with thickness, roughness, and density of Al_2O_3 as optimization variables. Properties of the underlying wafer were fixed to the wafer specifications as provided by the manufacturer and are given with a thickness of 200 nm, a roughness of 0.1 nm, and a density of 2.2 $\frac{g}{cm^3}$.

3.3.5. Scanning Electron Microscopy

SEM micrographs have been obtained using a Zeiss Jena Leo1530 at the indicated electron beam acceleration voltages. Samples were used as in the measurements, however before applying printed CPSE.

3.3.6. Optical Measurements

Optical images have been obtained with a Leica M165 C microscope. Areal measurement have been done using the ImageJ program suite. [88]

3.4. Device Characterization

All electrical device Characterizations have been executed at RT using a SUSS MicroTec MLC-150C probe station with Agilent 4156C measuring units. If not stated otherwise, relative humidity was set to 50 %. Voltage settings for acquiring transfer and output characteristics, respectively, vary between experiments and are stated with the respective graphs.

V_{th} values were extracted using the square root method as described in sec. **2.1.7** after applying a linear fit via a least squares regression analysis. Subthreshold swings were determined following eq. **(2.19)** by leveling over 5 measurement points and using the steepest value acquired. In cases with sweep measurements, these analyses were done using forward curves only.

Pulsed Measurements

During pulsed measurements, a rectangular signal between 0 V and 1 V was applied as V_{GS} with a frequency of 1 Hz. Before recording data, at least 5 full cycles were applied.

Varying Humidity

In the case of measurements with varying humidity, the measurement device was placed in a sealed box and the humidity level regulated with a humidifier and flushing with dry nitrogen, respectively. Before measuring, the respective humidity was maintained for at least 30 seconds to ensure that the material has adapted to the environmental changes unless stated otherwise.

3.5. Statistical Analysis

For proving differing average V_{th} values in the doping experiments, statistical tests have been applied.

Shapiro-Wilk tests for normal distribution have been performed on each set with samples of the same doping concentration. For neighboring sets, F-, and t-tests, where the t-test has been chosen according to the result of the F-test, were applied. All tests were run as implemented in the R programming language version 3.5.2 with a confidence level of 95 %. [89] The null hypotheses of the F-test is matching variances between the two sets, in case of the t-test it is identical means.

The correlation coefficient has been extracted with gnuplot version 5.4 which was also used for creating all data graphs in this work. [90]

4. Vertical Field-Effect Transistors with Porous SnO_2-Channels

4.1. Current research in the field

The output current of an FET is directly proportional to the ratio of channel width to length, as can be directly seen from the general equation of the saturation current in a field-effect transistor eq. **(2.9)**. It is therefore a standard target in transistor technology to reduce lengths as can be easily derived from the development of the design rules as defined in the *International Technology Roadmap for Semiconductors* and its successor the *International Roadmap for Devices and Systems*. Starting from more than 600 nm in the early 1990s, the current generation uses 5 nm technology. [91] Similarly, in printed field-effect technology, reducing the channel length is one key aspect for reaching the goal of applicable systems. Nevertheless, printing technology faces a key limitation in this respect: printing resolution is limited to a two-digit micron range even with droplet volumes on the pL scale. [77] Therefore, output currents in FETs using in-plane geometries are limited if the channel lengths are not artificially predefined to smaller values, e.g., by lithographically setting the channel lengths via the passive structured design.

While the diameters of a printed film from a single drop are limited in the micron range, the film thicknesses reach into the nm-range. This already has led to the development of systems with vertically aligned channels sandwiched between source and drain electrodes. The first design suggestion was reported by Ma and Yang as early as 2004, where C_{60}-fullerene as semiconductor was placed between two metal contacts. The system was rested on a dielectric and the gate, i.e., using a full layer-by-layer design with back-gate layout [92]. This approach was among others refined by Liu et al. who already could report current densities of up to 3 mA/cm^2 [93]. However, both methods use evaporation instead of ink-based technologies for manufacturing. In 2017 Swathi et al. took a first step towards printed technology by applying the semiconductors in the their systems via

dipping or spin-coating, respectively [94]. In their case, they created a permeable base transistor, functioning similar to a bipolar junction transistor, where the base is located within the semiconductor.

The major breakthrough in terms of a printed vFET has been reached in 2017 by Baby at al. [43] Several unique aspects could be presented within their work: the change from an organic to an inorganic semiconductor, heavy reduction of the operation voltages from tens to hundreds of volts down to 2 V, as well as current densities in the 100 kA range. In their work, the SnO_2 has been created as a porous material and consequently soaked with an electrolyte in a system with only 50 nm distance between source and drain. These tremendous improvements are on the one side based on the better mobilities of SnO_2 but the major contribution arises from the direct contact between electrolyte and semiconductor in contrast to the back-gate geometries in preceding works. Nevertheless, the method suffers from a few drawbacks: comparably high annealing temperatures and a very complex template polymer not available commercially.

The following works are directly built on Baby's methods and aim to tackle these drawbacks by introducing a simplified manufacturing route, a commercially available spacer polymer and lower annealing temperature. The regular porosity achieved with the new template polymer is a first step towards applying dielectrics onto the channel surface in a vFET.

4.2. Material Characterization

The precursor ink consists of a solution of $SnCl_2 \cdot 2\,H_2O$ in a mixture of water and isopropanol merged with an aqueous dispersion of 200 nm polystyrene beads with hydroxylate surface.

In comparison to Baby's approach, the highly corrosive liquid $SnCl_4$ was replaced by the solid and less harmful $SnCl_2 \cdot 2\,H_2O$, and the template polymer is commercially available and has a predefined structure. Additionally, the annealing temperature is reduced by 100 °C. Full experimental details are listed in sec. **3.2.1**.

In order to ensure that the desired semiconductor is obtained and that the template polymer does not leave any residues in the material, the residues after air-drying the precursor ink and the spacer suspension, respectively, are analyzed by thermogravimetry. By using artificial air and a temperature profile matching the annealing applied during

device preparation, it was ensured that the resulting material is identical to the one in devices.

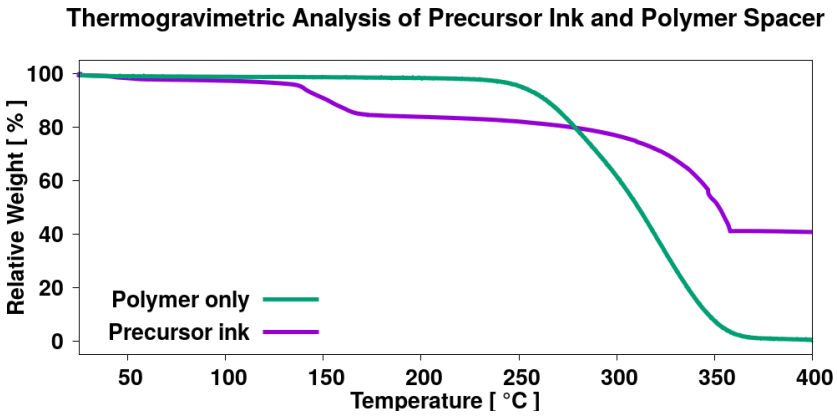

Figure 4.1.: Thermogravimetric analysis of the precursor ink and the polymer beads in the range of 25 °C to 400 °C

Fig. **4.1** shows the TGA profiles for the two samples. First of all, it can be noted, that the polymer is completely combusted at the final temperature of 400 °C. It should be pointed out, that the polymer consists of polystyrene spheres with hydroxylate surface functionalization, i.e., they are composed of hydrogen, carbon, and oxygen atoms only. Besides leaving only CO_2 and H_2O as products from combustion in air, these atoms are not known dopants for SnO_2. Decomposition starts at ca. 230 °C and is completed at ca. 370 °C. These values are in the range of reported degradation temperatures for polystyrene and deviations from literature values can be traced back to property variations in polymeric compounds arising from, e.g., different chain lengths and surface functionalities. [95,96]

The TGA curve for the precursor ink can be interpreted as follows: The weight loss of 6 % until 140 °C can be attributed to solvent evaporation. The comparably sharp 8 % weight loss between 140 °C and 160 °C match a dehydration process from $SnCl_2(OH)_2$ to $SnOCl_2$. This is a result from dissolved $SnCl_2 \cdot 2\,H_2O$ being easily oxidized, leading to an oxidation state of +IV for Sn and consequently forming a mixed chloride-hydroxide species in water. [97] In the final step between 230 °C and 360 °C, SnO_2 is formed in parallel to the combustion of polystyrene leaving a white powder accounting for 41 % of the original mass. Assuming a complete formation of $SnCl_2(OH)_2$ as intermediate, and considering the weight loading of 25 mg/ml in the polymer solution, theoretically 46 % should be obtained. With regard to the initial loss attributed to remaining solvent, this is

reasonably close to the measured value. With respect to the ink preparation as described in sec. **3.1.3**, the theoretical percentage is calculated via:

$$\frac{m(\mathrm{SnO_2})}{m_{\mathrm{in}}} = \frac{m(\mathrm{SnCl_2 \cdot 2\,H_2O})\dfrac{M(\mathrm{SnO_2})}{M(\mathrm{SnCl_2 \cdot 2\,H_2O})}}{m(\mathrm{SnCl_2 \cdot 2\,H_2O})\dfrac{M(\mathrm{SnCl_2(OH)_2})}{M(\mathrm{SnCl_2 \cdot 2\,H_2O})} + m_{\mathrm{PS}}} \tag{4.1}$$

with:

m_{in}		– initial mass of $SnCl_2(OH)_2$ in TGA
$m(\mathrm{SnCl_2 \cdot 2\,H_2O})$	$= 54\,\mathrm{mg}$	– according to recipe from sec. **3.1.3**
m_{PS}	$= 25\,\mathrm{mg}$	– polymer suspension with 2.5 % (w/v)
$\mathrm{M(SnCl_2 \cdot 2\,H_2O)}$	$= 225.6\,\mathrm{g\,mol^{-1}}$	
$\mathrm{M(SnCl_2(OH)_2)}$	$= 223.6\,\mathrm{g\,mol^{-1}}$	
$\mathrm{M(SnO_2)}$	$= 150.7\,\mathrm{g\,mol^{-1}}$	

While the pure polymer sample had no residue, the precursor ink resulted in a white powder that was analyzed by XRD. As can be seen in the powder diffractogram in fig. **4.2**, the precursor ink is fully converted to SnO_2 with no other phases or side products detectable. In conclusion, a vFET manufacturing process with prolonged annealing at 400 °C in air will be sufficient in order to obtain the desired semiconductor.

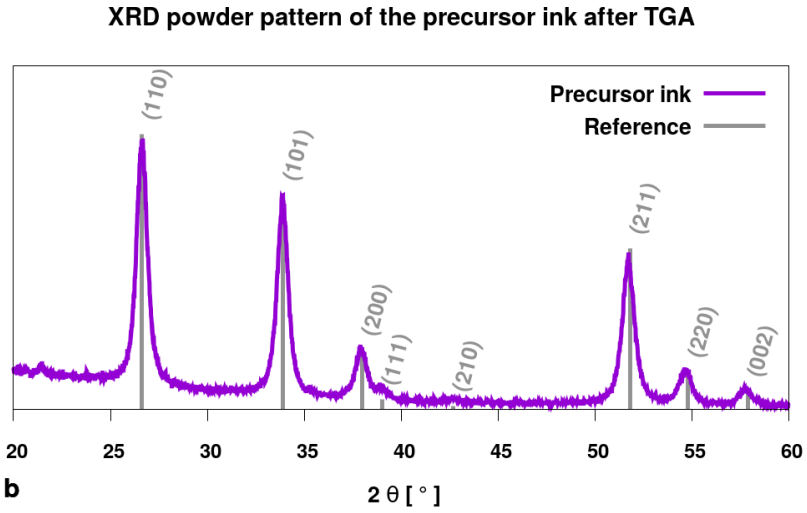

Figure 4.2.: XRD powder pattern of powder resulting from the precursor ink after TGA analysis in the 2θ-range from 20 ° to 60 °, reference pattern for SnO_2: ICSD 9163

4.3. Optimizing the vFET Manufacturing Process

In general, the vFET production process must be separated in to five steps: preparation of planar passive structures, printing the precursor ink, applying the top lead onto the precursor droplet, annealing the ink, and printing the electrolyte.

For estimating the ideal ratio between polymer spacers and semiconductor precursor in the recipe, it is assumed that the precursor fills up the empty space between the equally sized polymer spheres. As a starting point, ideal packaging is presupposed, leaving 26 % of free space between the spheres that needs to be filled up with semiconductor. This leads to a loading of 67 $\frac{mg}{mL}$ polystyrene suspension via:

$$\frac{m(SnCl_2 \cdot 2\,H_2O)}{V(PS)} = V_{\text{free}} \cdot X_{PS} \cdot \rho(SnO_2) \frac{M(SnCl_2 \cdot 2\,H_2O)}{M(SnO_2)} = 67\,\frac{mg}{mL} \tag{4.2}$$

with:

$V(PS)$		– volume of polystyrene suspension
V_{free}	$= 26\,\%$	– free volume in closed packing
X_{PS}	$= 2.5\,\%$	– loading of polystyrene suspension
$\rho(\text{SnO}_2)$	$= 6.95\,\text{g/cm}^3$	

$M(\text{SnCl}_2 \cdot 2\,\text{H}_2\text{O})$ and $M(\text{SnO}_2)$ as in eq. **(4.1)**

Fig. **4.3**(left) shows the results of using the above mass loading in the precursor ink after annealing in an SEM micrograph. With this loading, several crystallites formed and the high stackings of SnO_2 spheres were likely to form cracks during annealing. Subsequently, the mass loadings of $SnCl_2 \cdot 2\,H_2O$ have been reduced to 80 % (54 mg) and 60 % (40 mg) of the value estimated in eq. **4.2**. Structures arising from these recipes with reduced loadings can be seen in fig. **4.3**(middle and left). While the loading of 40 mg leads to vast gaps and often only single layers of SnO_2 spheres, a loading of 54 mg obtains a closely connected, honeycomb-like structure. The result of this ink mixture allows for a nicely connected three-dimensional network yet suppresses the formation of separated crystallites. Consequently, this ink setup was chosen for the manufacturing of the vFETs.

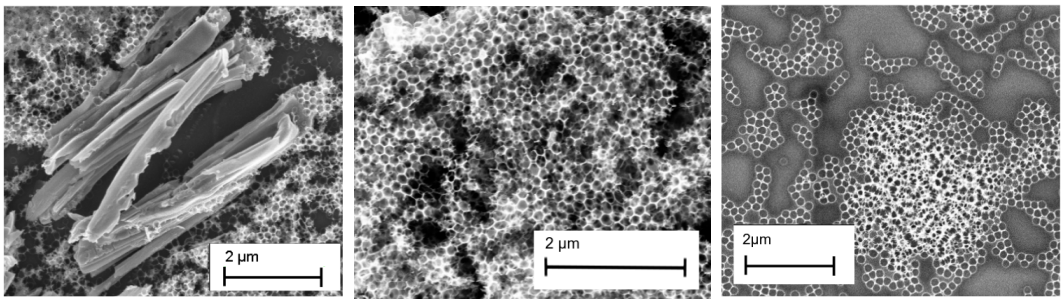

Figure 4.3.: SEM micrographs of printed vFET-precursor inks with varying SnO_2-precursor mass loadings after annealing; left: crystallite and cracks forming with a mass loading of 64 mg, middle: optimized results with goof coverage and well-formed honeycomb structure at a mass loading of 54 mg (80 %), right: gaps and separated spherical SnO_2 structures at a mass loading of 40 mg (60 %)

As described in the production process in sec. **3.2.1**, tungsten has been applied for the top lead. Originally, palladium has been in use, just as for the other passive structure elements, however, as shown in fig. **4.4**, these systems suffered from fringes, cracks and deformations. This behavior can be explained with the low thickness of only 50 nm and the

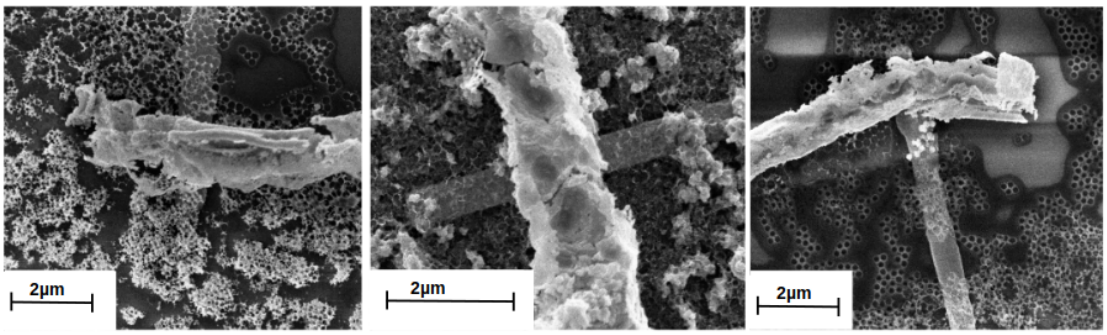

Figure 4.4.: SEM micrographs of three different samples with Pd top leads. Fringing, cracking and bending is clearly visible as a result form the head treatment due to the comparably low melting point of Pd and the small thickness applied.

melting point of Pd at 1555 °C. An increase of thickness for the top lead would require a thicker resist for e-beam lithography, eventually leading to longer acetone exposure times during lift-off. As acetone also dissolves polystyrene, the spacers would be attacked. It is therefore not possible to enhance top lead stability by increasing the thickness. Consequently, tungsten was chosen as material for the top leads due to the high melting point of 3422 °C and the low thermal expansion coefficient of $4.5 \cdot 10^6 \frac{m}{mK}$ which is up to three times smaller than for other typical passive structure metals like Au, Pt, or Pd. [98, 99].

Fig. **4.5** shows SEM micrographs of reference samples in top and side view (**a-c**) and a final device with tungsten top lead in two different magnifications (**d,e**). In the reference samples, the honeycomb structure is nicely visible. In fig. **4.5b** the filigrane structure of the SnO_2 channel is visible with a material thickness of only a few nanometers. In the side view, it is visible that the height of the final structure typically ranges between one and three layers of the polymer template spheres. At the current point, it was not possible to find a manufacturing method that allows for a more evenly distributed layering of the precursor. Most likely, once a droplet is printed, the solvent evaporates and the precursor and polymer spacers start to form agglomerates that eventually precipitate. This leads to a certain randomness in the material distribution and explains void areas in fig. **4.5a**. In Fig. **4.5d** the post-annealing droplet dimensions of about 50 µm in diameter are clearly visible and the huge difference of diameter and thickness of the deposited material becomes apparent when comparing to the side view SEM micrograph. Fig. **4.5e** shows that the problems with deformations in the top lead are successfully avoided by replacing Pd with W.

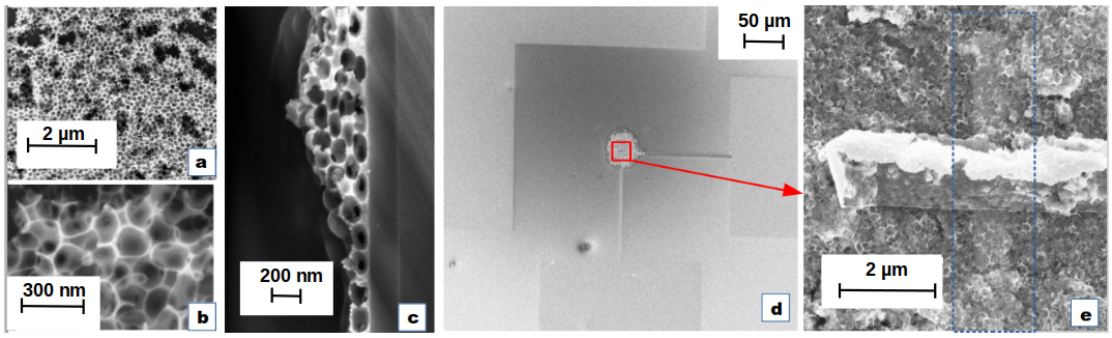

Figure 4.5.: SEM micrographs of reference samples in top (a,b) and side view (c), as well as of a final device with W top lead in (d). (e) shows an enhanced area of (d) (marked in red). The top lead in (e) has a width of 2 µm and the bottom one of 1 µm (position enhanced by blue markers).

4.4. Electrical Characterization

The application of a printed electrolyte for the gating brings several advantages for devices with porous structures. First of all, it is possible to use a displaced gate setup simplifying production. Second, the electrolyte ink can penetrate the porous structure and allows for a smooth coverage of the channel. And third, as typical for electrolytes, the operation voltage can be very low.

Fig. **4.6** shows FET-characteristics for the device from fig. **4.5d**. The device is fully operational in the 1 V regime. Notably, the output curves show bumps before leveling out, as is typical for negative different resistance behavior. In literature, there are many reasons discussed for NDR, with trap states being the most probable reason here. [100,101] These trap states arise from defects in the crystal structure due to the nature of the polycrystalline oxide. Additionally, the porous structure highly challenges the semiconductor's internal grain contacts, as well as the contact with the leads, both being typical sources for trap states. Despite the small vertical lead overlap area of 2 µm^2, an $I_{D,on}$-current of 3.3 µA could be achieved, leading to a current density of 167 A/cm^2. It must be noticed that stray currents following diagonal paths outside of the vertical overlap area cannot be excluded in this device setup. This device shows a threshold voltage of 50 mV and a subthreshold swing of 240 mV/decade, small hysteresis and very low gate currents in the range from -150 pA to 65 pA. The $I_{D,on}/I_{D,off}$-ratio spans 4 orders of magnitude.

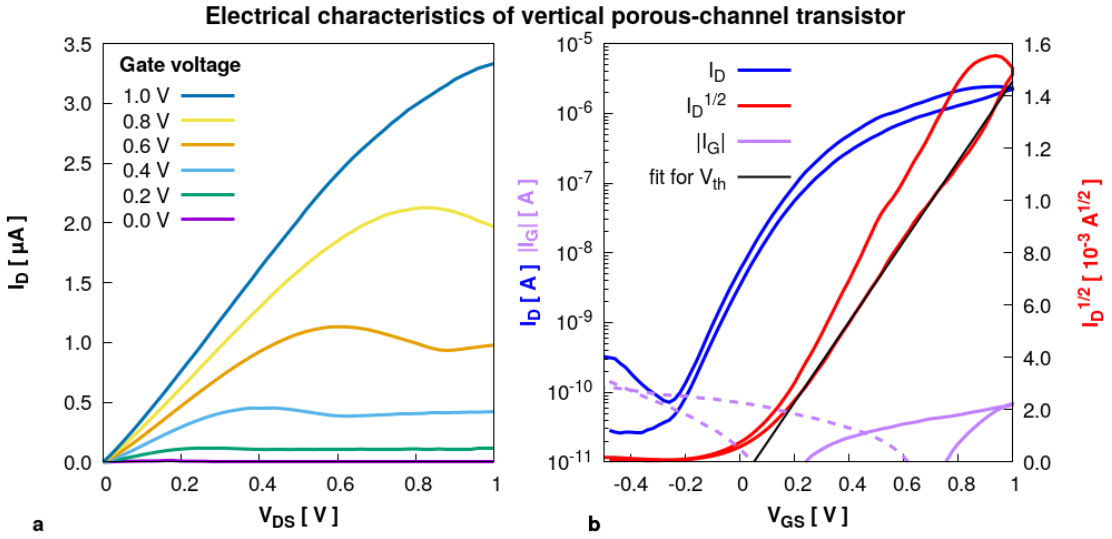

Figure 4.6.: Electrical characteristics of a vFET; a) output curves for $V_{GS} = 1\,V$, b) transfer curve at $V_{DS} = 1\,V$, negative gate currents are indicated by dashed lines due to the logarithmic scale

In order to better understand such devices and their behavior, further device series have been prepared and the measured voltage range expanded. Fig. **4.7** shows characteristics for a vFET device that has been measured in the 2 V-range. Despite a typical transistor behavior with NDR in the output curves up to $V_{GS} = 1.2\,V$, currents are massively rising after $V_{GS} = 1.3\,V$ in all cases. While the device shows almost no hysteresis and a threshold voltage of 0.44 V, the subthreshold slope is comparably high at 675 mV/decade. Notably, the transfer curve does not show a clear minimum nor a strong tendency to flatten in the higher ranges and leakage currents are two orders of magnitude larger than in the case of the previously discussed device.

In fig. **4.8** the same device has been examined, however, the definition of source and drain were swapped. The output curves immediately show the rising behavior in a much stronger manner and the threshold voltage dramatically shifts to -0.65 V.

Fig. **4.9** is a combination of the unbiased output curves, i.e., at $V_{GS} = 0$ from fig. **4.7a** and fig. **4.8a**. Due to the inverse definitions of source and drain, the values of fig. **4.8a** are point mirrored at the origin in the combined graph. This conversion is possible for an unbiased gate only. It is is a typical voltage-current behavior for a metal-semiconductor-

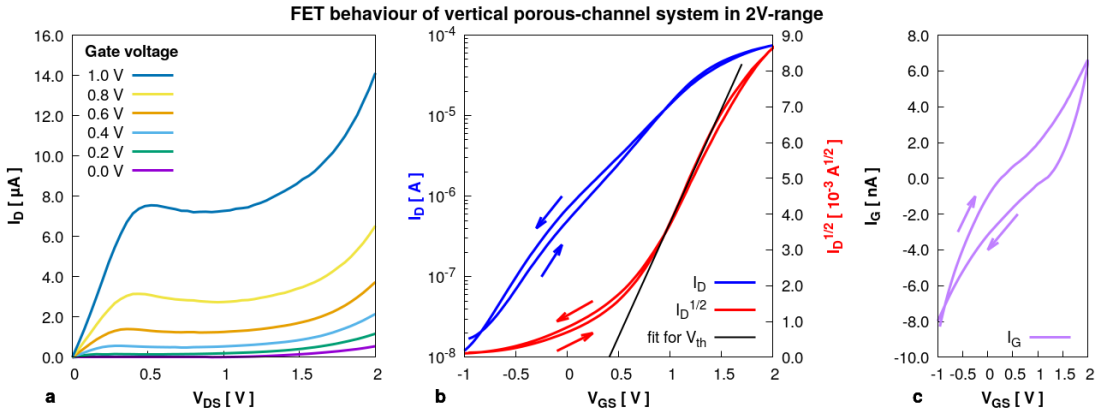

Figure 4.7.: Electrical characteristics of a vFET with expanded voltage range; a) output curves, b) transfer curve at $V_{DS} = 2\,V$, c) gate leakage current during b

metal system, also known as back-to-back Schottky diodes. A series of such devices for SnO_2 has been examined and modeled by Chiquito et al. in 2012. [102] While these sandwich devices usually lead to the expectation of a symmetrical behavior, the vFETs in this work use two different metals and thus clearly different Schottky barriers.

For determining the barrier behavior, the work functions of materials used in production for the top (W) and bottom (Pd) leads have to be compared to the one of the semiconductor. The reversed measurement definition changes the conventional current flow source $\rightarrow$ channel $\rightarrow$ drain from Pd $\rightarrow$ SnO_2 $\rightarrow$ W to W $\rightarrow$ SnO_2 $\rightarrow$ Pd. This reversed definition will be called inverse or inverted setup in the following. The device behavior then depends on the respective metal-semiconductor contacts and the direction of the applied field. Tab. **T4.1** lists the work function values from literature for the three materials in the vFET. Due to the nature of the production process via sputtering and precursor annealing, all materials can be considered polycrystalline. In the case of the contact between W and SnO_2, the metal has a smaller work function than the semiconductor. According to the general equation eq. **(4.3)** for the height of the Schottky barrier for electrons Φ_{Bn} and with the fact that the Fermi level of an n-doped semiconductor, as is SnO_2, is close and above its valence band energy χ, this would lead to a small, possibly even negative value. [45] Negative values for a Schottky barrier lead to a mere ohmic contact behavior, which is not observed in fig. **4.9**. Realistically, surface states in both the semiconductor and the metal lead to certain number of charge traps that nevertheless will result in a barrier behavior at this contact. [103, 104] The vFET layout with the porous channel and

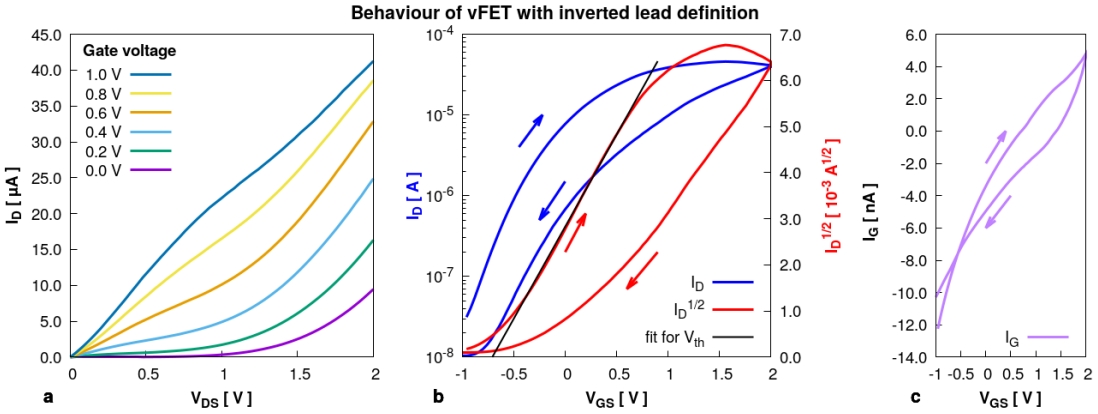

Figure 4.8.: Electrical characteristics of the vFET from fig. **4.7** with inverse definition of source and drain during the measurements; a) output curves, b) transfer curve at $V_{DS} = 2\,V$, c) gate leakage current for (b)

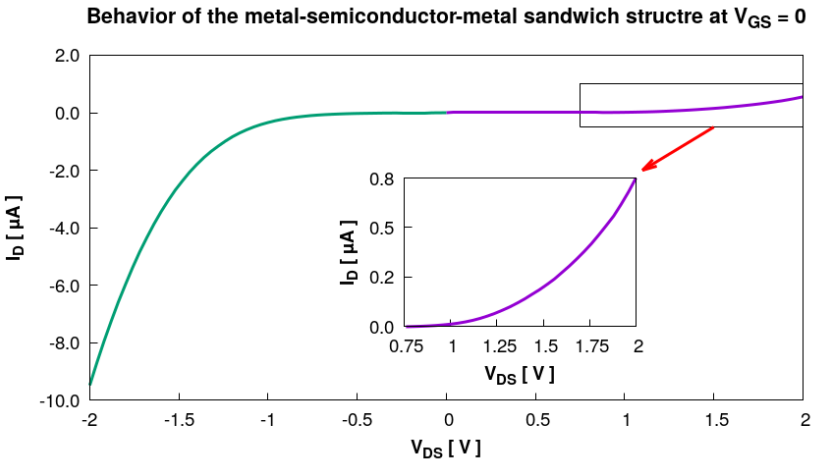

Figure 4.9.: Output curve at $V_{GS} = 0$ derived from the values of fig. **4.7a** (purple) and inverted values from fig. **4.8a** (green), *inset*: enhancement of the marked area for better visibility of the current rising behavior

Material	Pd	SnO_2	W
Φ [V]	5.12	4.75	4.55

Table T4.1.: Work function values Φ for materials in vFET devices (all polycrystalline) as taken from literature [105, 106]

the production process with the top lead sputtered on the pre-annealed channel precursor leads to many potential defects at the contact site.

$$\Phi_{Bn} = \Phi_M - \chi \tag{4.3}$$

For the contact between Pd and SnO_2, a barrier according to eq. **(4.3)** is to be expected with the reasonable assumption that the difference between the Fermi level and the valence band in the semiconductor is smaller than the difference between the work functions of metal and semiconductor. Again, surface states will increase the barrier at this contact site. In conclusion the Pd-Sn_2O contact will have a much larger Schottky barrier than the W-SnO_2 contact and neither is ohmic.

With this knowledge regarding the metal semiconductor contacts, the output characteristics from fig. **4.7a** and fig **4.8a** are easily explained. In either case output curves are the sum of a back-to-back Schottky diode and a transistor behavior. However, only in the non-inverted operation setup, i.e., when the top tungsten lead is the drain and the bottom palladium lead the source, the barrier is high enough to delay the current breakthrough so that an FET-type operation mode is possible in the 1 V-regime. This unidirectional transistor behavior opens a very interesting usage mode: overall the device can be considered a diode where the reverse blocking behavior may be turned off by applying a gate voltage. Taking the full 2 V-range into account it behaves like a Zener diode where the reverse blocking for low voltages may be turned off.

One possibility for explaining the strong hysteresis behavior in the inverse setup are bottlenecks in this device's porous structure that lead to a slowed down electrolyte reaction in the inverse setup. As will be shown later on with another device, hysteresis behavior is not directly linked to the inverse setup.

The strong and early influence of the back-to-back Schottky diode behavior and the very large leakage currents lead to the assumption of defects in the porous structure, i.e., areas with no polymer spacer sphere deposited during printing or with a collapsed top gate during production leading to a direct metal-semiconductor-metal sandwich with only

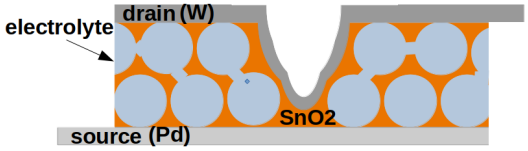

Figure 4.10.: Schematic for areas with no deposited spacer during printing (not to scale); this leads to a metal-semiconductor-metal sandwich with only a few nanometers of SnO_2

a few nanometers of semiconductor in between. Fig. **4.10** shows a schematic of these geometry defects. In such cases the back-to-back Schottky diode is associated with the so-called short channel effect. [45] At this point the distance between source and drain is so small that the voltage applied at the drain may already be capable of polarizing the channel, leading to the effects as seen here.

For avoiding this, both the ink composition as well as the printing process need to be further optimized to ensure a full coverage of the bottom lead with both precursor and spacer.

That hysteresis behavior and negative threshold voltages are not linked to the direct and strong rise of the output current in the reversed measurement setup, is shown in the graphs in fig. **4.11**. Threshold voltages for this device are 0.35 V (non-inverted setup) and 0.13 V (inverse setup), respectively. As can be seen, in either case the hysteresis behavior is very small and the threshold voltage shifts to lower, yet positive values. Nevertheless, the immediate rise in the output currents for the inverted operation setup is still given.

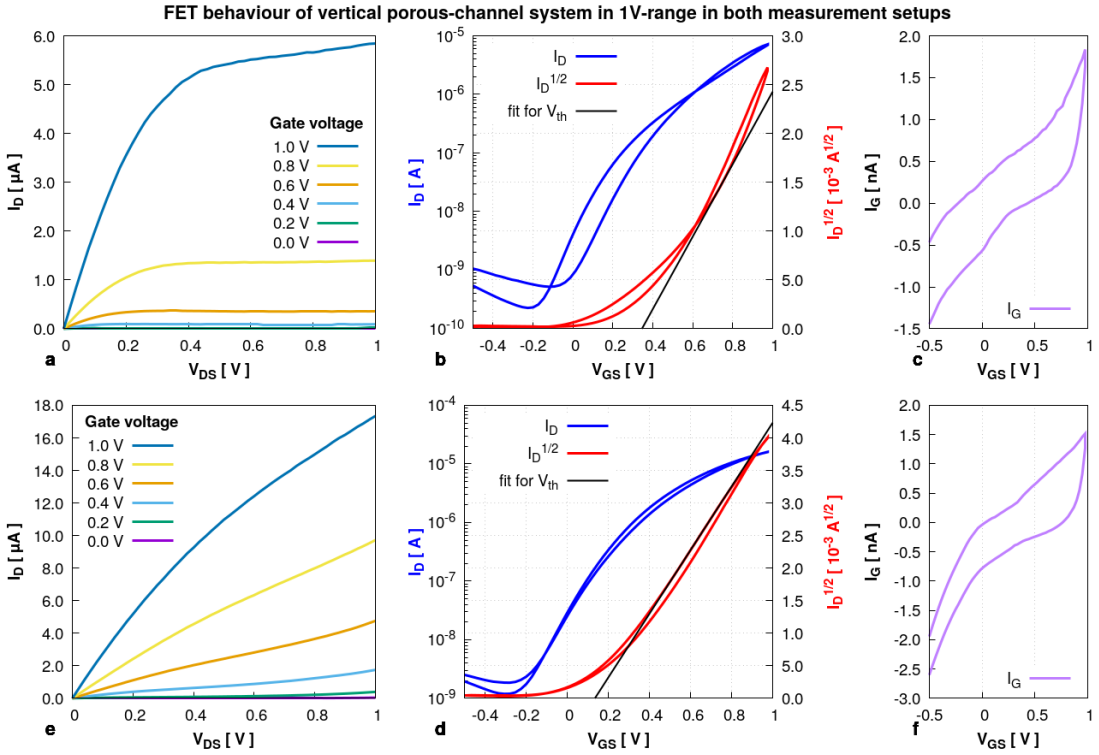

Figure 4.11.: Device characteristics with a) output curves, b) transfer curve for $V_{DS} = 1\,V$, and c) leakage currents in the non-inverted setup; d), e) and f) accordingly for the inverted setup

4.5. ALD-Coating of the Porous Channel

The use of electrolyte gating in the porous vFET systems has two advantages. On the one hand, the electrolyte ink may well penetrate into the pores, with soaking possibility even supported by capillary effects. On the other hand, it allows for a displaced gate layout facilitating production. However, the inner resistance of electrolyte lowers the electrical performance with increasing gate distances. [107] In order to overcome these limitations, it was tried to apply a dielectric onto the porous system via ALD, then establish the electrical gate contact with conductive inks.

Fig. **4.12a and b** show the result of coating a reference sample with 10 nm of Al_2O_3 via ALD. In comparison to the SEM micrograph of the sample before ALD (fig. **4.12c**), a clear and selective coating of the filigree structures is visible and the transparency is reduced.

Despite this, up to date, all devices with the dielectric applied showed short circuits between channel and gate, independently of the temperatures during ALD or whether silver or graphene ink was used for establishing the gate contact. The highly irregular inner structure and difficult pathways for precursor molecules during ALD – with pores allowing access to the system only available at the sides of the sandwich structure of lead, porous semiconductor and lead – result in many possibilities for pin-holes. The different deposition temperatures of 130 °C and 200 °C should have led to an electrolyte- or dielectric-type gating behavior for Al_2O_3, respectively, as will be discussed in chap. **6** in more detail. To successfully overcome this problem, it is suggested to increase the precursor soaking time to allow full pore penetration. Additionally, the temperature during deposition should be increased further as the qualities of deposited films are highly temperature-dependent. Even increased cycle numbers may lead to a reduced number of pin-holes. However, the thickness of the Al_2O_3-layer is limited as not to clock pores before the gate contact material may be inserted, otherwise leading to dead channel regions. The possible problems regarding the use of silver ink in combination with Al_2O_3 will be discussed in chap. **6**.

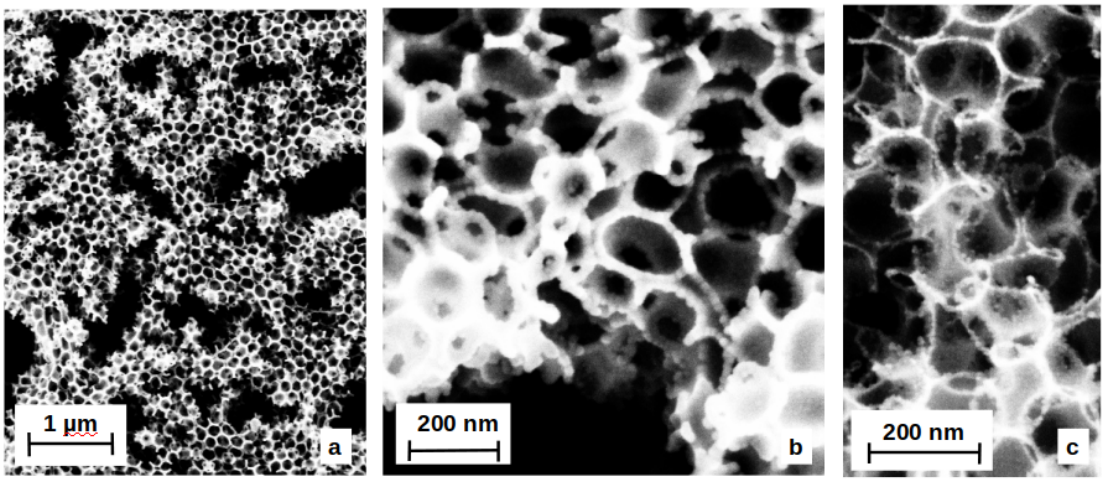

Figure 4.12.: a and b) SEM micrographs of a porous SnO_2 sample with 10 nm Al_2O_3 coating via ALD in different magnifications, c) SEM micrograph of same sample before ALD

4.6. Conclusion

In this chapter, it could be shown that production of a vFET based on porous SnO_2 using commercially available 200 nm polymer spacers and a simplified production route is possible. In comparison to preceding works, the processing temperature was successfully reduced from 500 °C to 400 °C. However, it must be assumed that several areas in the porous system lack spacer or collapsed to metal-semiconductor-metal sandwich structures during production. This leads to short-channel behavior, and in the inverted setup, to high currents even for V_{GS} below the threshold voltage. In the non-inverted setup, typical FET-type operation is possible in the 1 V-regime. This unidirectional usage behavior is successfully explained by the difference in the Schottky barriers at the metal semiconductor interfaces resulting from the two different metals applied. Overall, such devices can be considered diodes with tunable reverse blocking.

Finally, it was tried to produce a series of ALD-gated vFET devices. While coating with Al_2O_3 seems uniform in SEM micrographs, all devices were short circuited. Nevertheless, the topic of ALD-coated porous vFET devices remains an interesting and promising topic that requires more research and would open a whole new set of possible devices.

5. Tailoring Properties of In_2O_3-Based, Printed FETs by Cr-Doping

5.1. Current Research in the Field

In the silicon industry, doping is not only a necessity to overcome the poor intrinsic conductivity of silicon, but also the key component to the technology by allowing to define p- and n-type semiconductor sections on a chip as well as conductive paths via overdoping. [108] The need for property tailoring has even lead to co-doping with p- and n-dopants simultaneously, e.g., for reduction of the band gap and correcting negative impacts of dopants on other desired properties. [109, 110]

Oxide semiconductors on the other hand usually are intrinsically (or unintentionally) doped due to lattice defects following oxygen vacancies. [111] This allows for tailoring properties by controlling the extend of lattice defects during production e.g. by varying the oxygen partial pressure in sputtering processes. [112–114] Nevertheless, extrinsic (intentional) doping as well is very common in oxide semiconductors. This includes ZnO doped with Al or Ga or SnO_2 doped with Zn.

Focusing on In_2O_3 as the base material in this chapter, intrinsic n-type conductivity is commonly explained as following unintentional doping via oxygen vacancies. [48] The actual mechanism behind it has been questioned through several theoretical calculations of point defects in In_2O_3. [115, 116] It was calculated, that single point oxygen defects would act as deep donors that cannot contribute to the electron density in the conduction band. However, other findings argue that at ambient temperatures the vacancy may diffuse quickly enough to provide the necessary oxygen exchange for acting as a shallow donor. [117, 118] Other theories suggest that multiple oxygen site defects combine in order to provide a shallow donor level or even that hydrogen may actually be the true dopant leading to n-type semiconductor behavior. [119] The effects of the latter dopant

have been proven in sputtering experiments under presence of H_2O. [120, 121] In conclusion, it may be said that the reason for the as-prepared n-type behavior of In_2O_3 is not yet fully understood. However, considering the wet-chemistry approach in this work, H-doping most likely plays a more prominent role as should be expected in systems prepared by sputtering.

When it comes to intentional, chemical doping, the most prominent derivative of indium oxide must be indium tin oxide (ITO), a degenerate semiconductor with a typical In:Sn-ratio of 9:1 widely applied as transparent conductor in numerous applications such as displays, solar cells, and sensors in both science and industry. [122] Other typical dopants are W, Ti, Zn, Zr, or Mo [123–128]. All of these dopants positively contribute to the n-doping of In_2O_3 and thus lead to either degenerate semiconductor systems or lowered threshold voltages. Following experience with printed indium oxide FETs, threshold voltages are already comparingly low, often negative. [129] Thus, in order to allow more freedom for creating electronic logics, a dopant with the opposite effect is needed. Within the scope of this work, Cr was selected as this dopant for several reasons: reliable formation of a single phase, substitutional doping, p-type dopant, and low-cost material. [130, 131] Cr:In_2O_3 is well described in literature as it is discussed as a dilute magnetic semiconductor. [132–134] I.e., semiconductors doped with transition elements making them magnetically sensitive and by this allowing spin-selective electronic behavior. [135, 136]

5.2. Material Characterization

A series of six sets with Cr-doped In_2O_3 samples, starting from the undoped material and replacing up to 12.5 % of the In-atoms by Cr, are examined with respect to the change in electric characteristics of FETs made thereof. Stoichiometry and dopant concentrations of said sets are listed in tab. **T5.1**. In order to ensure an even dopant distribution and a well printable system, inks have been prepared from solutions of $In(NO_3)_3$ and $Cr(NO_3)_3$ mixed in the respective ratios. For material characterization, each ink has been annealed at 400 °C and examined via powder XRD. Experimental details are given in sec. **3.1.1**.

As shown in fig. **5.1**, the reflexes of the 0 %-sample match the reference data for the cubic phase of In_2O_3 and no side phases are detectable. [137] With increasing dopant concentration, a right shift of the reflexes is visible, but the systems show no phase separation. In accordance with Bragg's equation (see eq. **(2.22)**), reflex shifts towards higher angles stand for smaller unit cells. This matches the expectations for substitutional doping, as

Chemical composition	Dopant content (corresponding sample names)
In_2O_3	0 %
$In_{1.95}Cr_{0.05}O_3$	2.5 %
$In_{1.90}Cr_{0.10}O_3$	5.0 %
$In_{1.85}Cr_{0.15}O_3$	7.5 %
$In_{1.80}Cr_{0.20}O_3$	10.0 %
$In_{1.75}Cr_{0.25}O_3$	12.5 %

Table T5.1.: Cr-doping contents in the samples and the derived names

Sample	Cr via Rietveld [at-%]	Lattice parameter [nm]
0 %	0	1.011830
2.5 %	2.0±0.5	1.009489
5.0 %	3.0±0.9	1.009029
7.5 %	6.7±0.2	1.007849
10.0 %	8.1±0.4	1.001450
12.5 %	11.5±1.0	1.001310

Table T5.2.: Cr-content (in at-% of metal component) and lattice parameters from Rietveld-refinement of data from fig. **5.1**

the ionic radius of Cr^{3+} with 61.5 pm is considerably smaller than the one of In^{3+} with 80.0 pm. [138] Rietveld refinement was applied to the XRD-patterns and the determined Cr-contents and lattice parameters are shown in tab. **T5.2**. The lattice parameter for the undoped sample is in good accordance with the literature value of 1.0117 ± 0.0001 nm, but Cr-contents are systematically underestimated. In literature quantitative Rietveld analysis has been described with a comparably high error, especially in the presence of amorphous material. [139] As these reference samples were annealed on amorphous glass substrates and the resulting material scratched off, it can not be excluded that glass was carried over. With this in mind, the resulting data can be regarded as matching to the desired atomic composition. In conclusion and in accordance with literature, it is thus assumed that the dopant is evenly distributed in the material and that no side phase is present. Any changes in the electronic behavior thus can be assumed to be a direct result from doping.

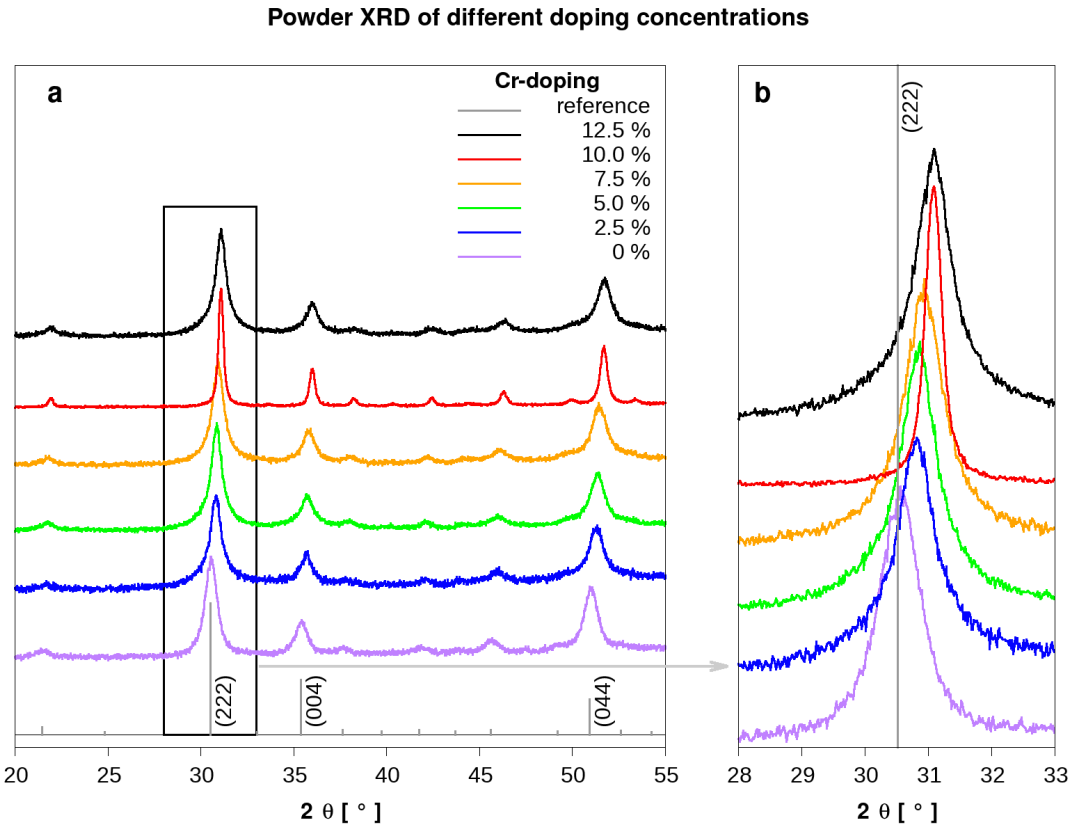

Figure 5.1.: Powder XRD patterns of the channels for 0 % to 12.5 % Cr:In_2O_3, a) patterns in the range of 20° to 55°, b) magnification of the (222) reflexes in the range of 28° to 33° for better visibility of the shifts; reference pattern of In_2O_3: ICSD 169420

5.3. Electrical Characterization

Within the scope of this work, two device series have been produced. The initial series consisting of sets of ten devices per Cr-concentration was prepared by printing two layers of the channel precursor for each device. Only four out of ten devices for each set resulted in functional FETs. While the desired increase in V_{th} was successfully achieved, the doping also led to a decrease in $I_{\mathrm{D,on}}$ of up to 97 % compared to the undoped samples.

In order to overcome these problems, a second series with four printed layers of the precursor was prepared, resulting in five to ten functional FETs out of ten prepared devices. On-current loss with increased doping was reduced to a maximum of 60 %, and the variances within each set were severely reduced. While the slope of the increase in V_{th} in this series matches the behavior of the first series, the threshold voltages were systematically shifted towards positive values. This shows that while doping is reliable and predictable, intrinsic channel material properties are only one of the many factors influencing device characteristics and process stability. Due to the increased threshold voltages, the voltage range during characterization was broadened for these sets in order to ensure fully saturated output curves.

Experimental details of the device production are described in sec. **3.2.2**.

5.3.1. Devices with two channel layers

Out of ten devices in each set with two printed channel layers, six were non-functional, either due to the channel not connecting source and drain or due to short circuits with the gate following printing irregularities. The other devices were fully functional and showed typical FET-type behavior. Fig. **5.2** shows output and transfer curves for two example devices with no and maximum doping, respectively. Device characteristics for devices of this series with other Cr-concentrations can be found in the appendix (sec. **TA.1**). The output curves in fig. **5.2a** and **c** saturate below 1 V in both cases, and a shift of V_{th} is clearly visible in the transfer curves (fig. **5.2b** and **d**). While surface trap states cannot be excluded, it is assumed that the hysteresis behavior mainly arises from a well-known problem with the electrolyte gating mechanism where slow ion movement through the CSPE leads to a delayed gate bias response. [140] This has also been shown by Singaraju et. al where hysteresis could be severely reduced by shorter electrolyte ion pathways via top gate geometries. [141] Similarly, devices where pure ionic liquids have been replaced with ionic gels as gating electrolytes have led to smaller hystereses. [40] In fig. **5.2a**, the

output curves at V_{GS} of 0.8 V and 1.0 V show bumps before saturation. This typical NDR-behavior and conditions for its appearance have been discussed earlier in sec. **4.4** and can be applied here, too. Namely, it is assumed that trap states exist in the system. Notably, $I_{D,on}$ of the doped sample is reduced to 2.5 % of the value in the undoped sample for $V_{GS} = 1.0$ V. Characteristics for other doping concentrations can be found in the appendix at sec. **A.1.2**.

In fig. **5.3** a comparison of the output curves for all doping concentration at $V_{GS} = 1.0$ V is shown using one device from each set. The continuous current decrease with increasing doping concentrations is clearly visible. This is caused by dopant ions acting as scattering centers which is known to decrease field-effect mobility. [48, 130, 142] Additionally, the rising threshold voltages directly lower the output current with the proportionality of $I_D \sim (V_{GS} - V_{th})^2$ as given by the MOSFET-equation in eq. **(2.11)**. The leakage currents for these devices are in the range of -1.5 nA to 1.0 nA as shown in fig. **5.4** and can be considered reasonably small.

Fig. **5.5** shows threshold voltages and $I_{D,on}$ and $I_{D,off}$ values for all functional devices of this series. Each set of devices with the same Cr-concentration has a variation in the threshold voltages. Especially the sets with 2.5 % and 5.0 % Cr are visibly overlapping in V_{th}.

The threshold voltages of the sets have been analyzed statistically in order to examine if the average values differ. Therefore, each set was first tested for normally distributed values via the Shapiro-Wilk algorithm. Secondly, the variances of neighboring sets were tested for equal variances via an F-test. Finally, depending on the result of the F-test, the corresponding two-sample, two-sided t-test for significancy of differing average values was applied. The confidence intervals were set to 0.05 for all tests.

The results of the statistical analysis are shown in tab. **T5.3**. All sets are normally distributed and each pair of neighboring sets shows the same variances. However, the average threshold values for the sets with 2.5 % and 5.0 % Cr-doping cannot be differentiated. Standard deviations were in the range of 28 mV to 60 mV. Despite this overlap, a linear regression with a high correlation coefficient of r = 0.94 can be fit to the data showing that three samples with 5 % Cr-doping have systematically low V_{th} values, while other sets have only single outliers or evenly spread values. It is unclear whether the errors in the 5.0 %-set result from an undetected error during ink preparation or rather unpredicted printing variations. The spread and outlier values in the other sets show that printing variations may be of higher influence than the doping in this series.

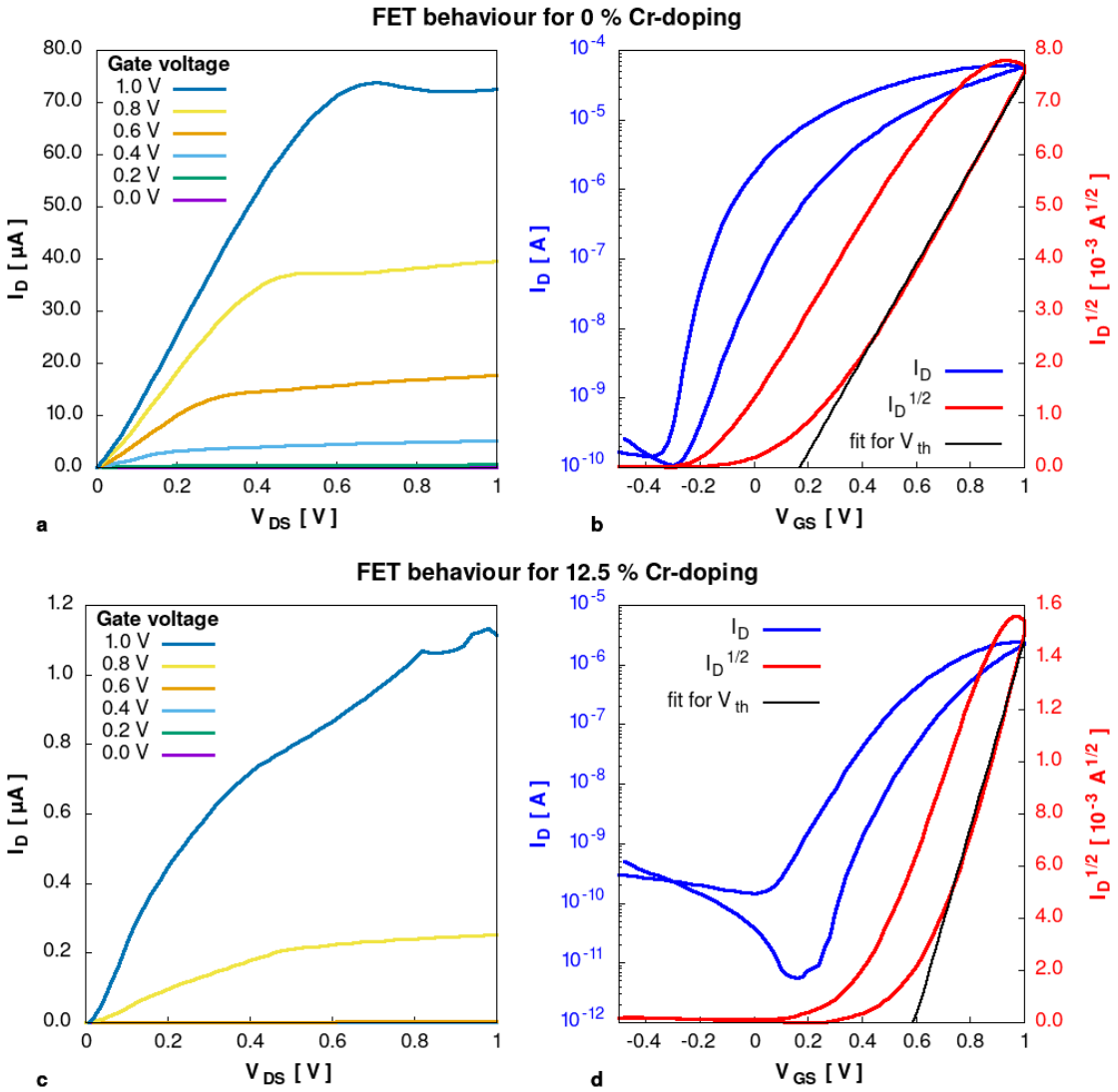

Figure 5.2.: a) and b) output and transfer curves for undoped indium oxide c) and d) output and transfer curves for 12.5 % Cr-doping, transfer curves are measured at $V_{GS} = 1\,V$

$I_{D,on}/I_{D,off}$-ratios span four orders of magnitude when regarded through all sets and even five when regarding some of the sets individually, e.g., in the case of the 5%-Cr-doped

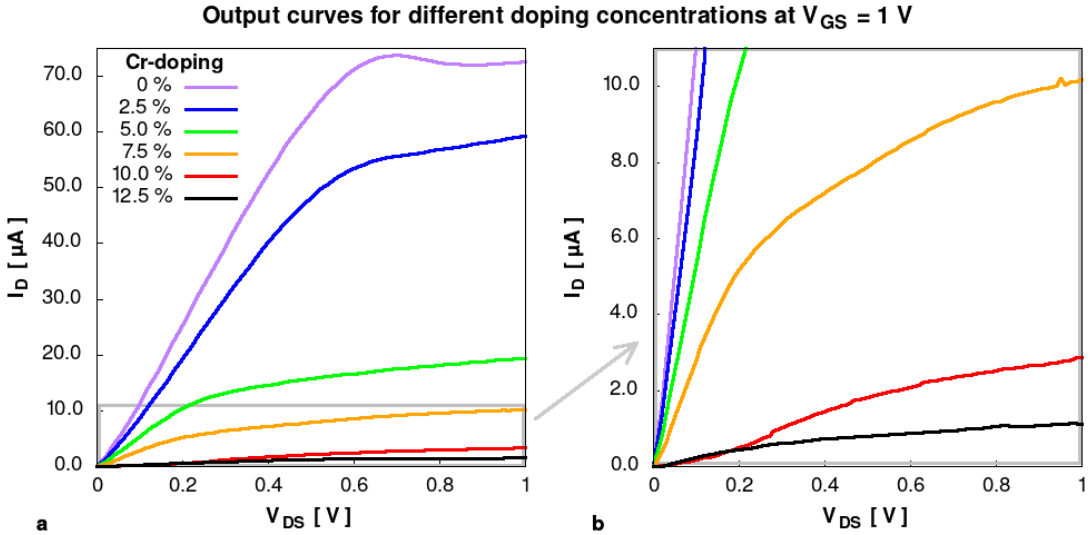

Figure 5.3.: a) output curves at $V_{GS} = 1\,V$ for different Cr-doping concentrations, b) magnification of (a) for smaller I_D; the 0 %- and 12.5 %-samples are identical to the ones in fig. **5.2**

samples. While a general trend towards shrinking $I_{D,on}$-values with increasing dopant concentration is visible, this cannot be fit to a quadratic regression as the MOSFET-equation (2.11) would suggest with the given linear change in V_{th} even when excluding the 5 % Cr-set. Most likely a change in μ_{FET} following the introduction of scattering centers has an additional influence on the currents as well as variations in the printing quality regarding channel widths or contact with the leads. This is especially visible in the variances of the $I_{D,off}$-values within each set. For the latter, no clear trend emerges despite a decrease at higher dopant concentrations being visible. It may be assumed that at these concentrations the introduction of scattering centers as well as changes to the crystallisation behavior lead to severely reduced electrical conduction qualities.

In all cases the subthreshold slopes were in the range of 180 to 280 mV/dec without a systematic relation to doping concentrations.

The full series data can be found in the appendix in sec. **TA.1**.

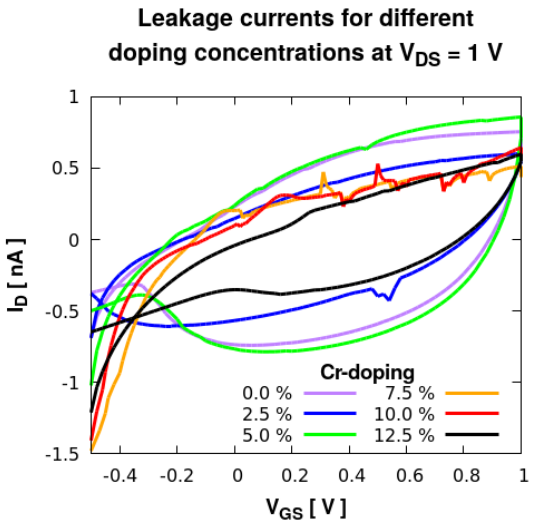

Figure 5.4.: Leakage currents for $V_{DS} = 1\,V$ for different Cr-doping concentrations; the devices are identical to the ones used in fig. **5.3**

Cr-Doping	**0.0 %**	**2.5 %**	**5.0 %**	**7.5 %**	**10.0 %**	**12.5 %**
Mean [V]	0.187	0.301	0.293	0.396	0.491	0.566
σ [V]	0.060	0.057	0.039	0.028	0.029	0.035
Shapiro-Wilk	0.197	0.085	0.061	0.0753	0.993	0.119
F-Test		0.925	0.550	0.595	0.968	0.740
t-Test		0.034	0.823	0.005	0.003	0.016

Table T5.3.: Statistical analysis data for each doping set with two printed channel layers, F- and t-test results are given for neighboring sets, in F-tests, green indicates identical variances, in t-tests green indicates differing means

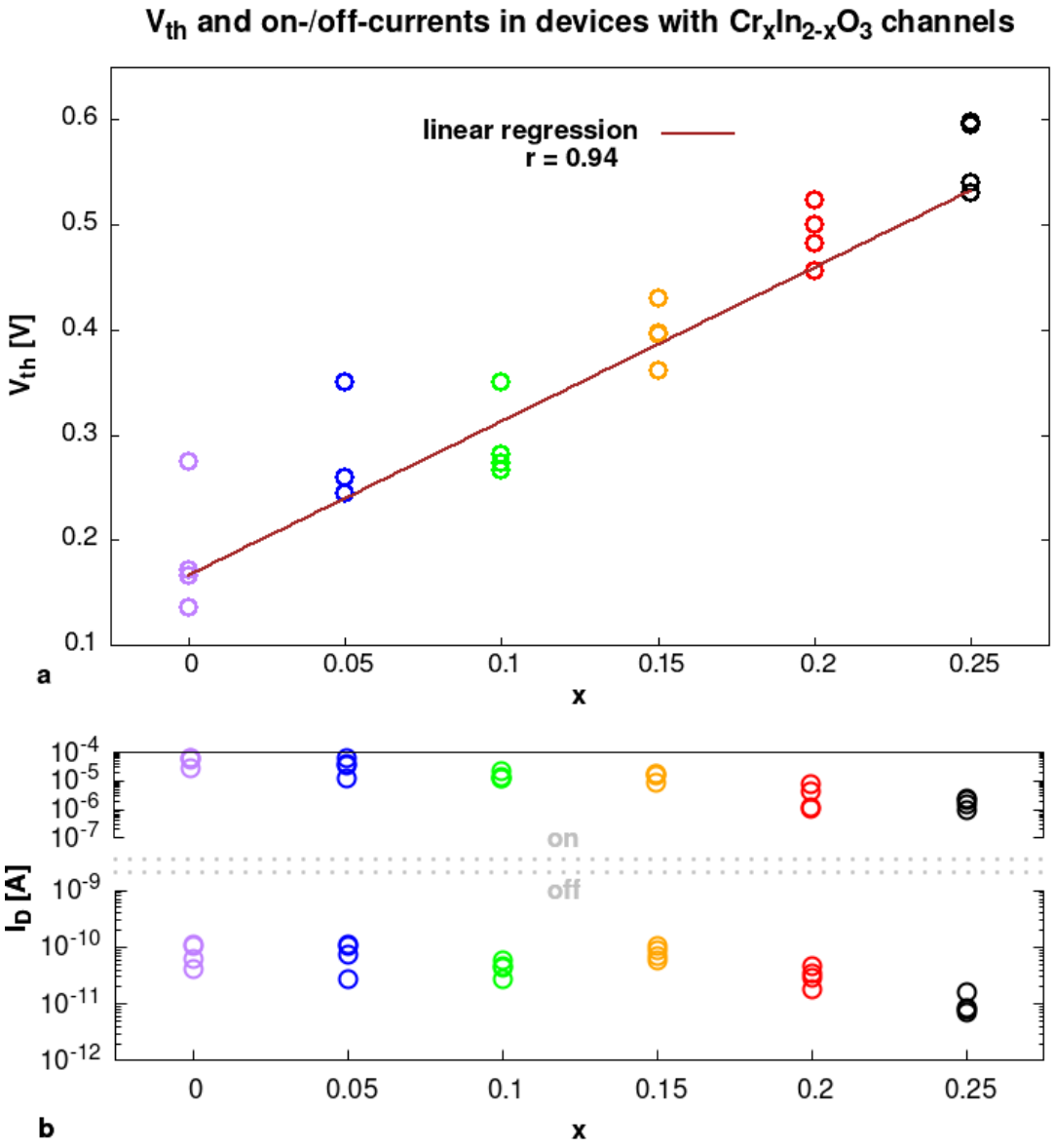

Figure 5.5.: Threshold voltages (a) and on- and off-currents (b) of each device by Cr-content

5.3.2. Devices with four channel layers

Due to the shortcomings in the expected systematic V_{th} change and the high failure rate of devices with two printed layers of channel ink, a second series was printed with four layers of precursor ink. The target was to increase the tolerance towards printing errors leading to reduced device failure rates and smaller variances within each set.

With this approach, five up to ten out of ten devices for each set have proved to be functional showing a clear improvement towards the previous series, however, still a not fully satisfactory production reliability. Fig. **5.6** shows a devices of the undoped set and one with maximum doping. In comparison to the previous series, the measurement window has been increased to a maximum V_{DS} of 2 V and V_{GS} ranging from -1 V to 2 V. Again, NDR-behavior is visible in the output curves of both samples, as well as hystereses in the transfer curves. This can be linked to surface trap states and delayed electrolyte response as already discussed in more detail in the previous section for devices with two printed channel layers. In contrast to fig. **5.2**, both output graphs show strong increases in I_{D} in regions with $V_{\text{GS}} > 1.5\,\text{V}$. The voltage range in applications thus should be limited below this value.

Fig. 5.7 shows output and leakage currents for one device selected from each doping concentration set. Output and transfer curves for the other Cr-concentrations can be found in the appendix (sec. **A.2.2**). The electrolyte possibly is permanently affected at these higher voltage values, as can be seen from the the strong increase in the leakage currents for V_{GS} near the margins of the measurement range (fig. **5.7b**). Notably, the magnitude of the leakage currents matches the values from the previous series (fig. **5.4**) in the range of -0.5 V$\leq$ V_{GS} $\leq$ 1 V.

The leakage currents are not systematically linked to the doping concentrations. Reasons for this most likely arise from printing variations leading to, e.g., more electrolyte in direct contact with source and drain electrodes due to the channel possibly not fully covering source and drain in the contact areas as well as differences on the lateral distance between channel and gate in case of non-central positioned channels. Variations in the printing results have been sketched earlier in fig. **2.15**. Despite the strong increase, the range of $\pm$12 nA is small in comparison to the actual output currents. Subthreshold slopes were in the range of 90 to 210 mV/dec. While this is in general an improvement to the two-layer systems, again no systematic relation to the doping concentration can be established.

Fig. 5.8 shows threshold values, and $I_{\text{D,on}}$- and $I_{\text{D,off}}$-values for all functional devices in this series. The variations within each set were effectively and clearly reduced in com-

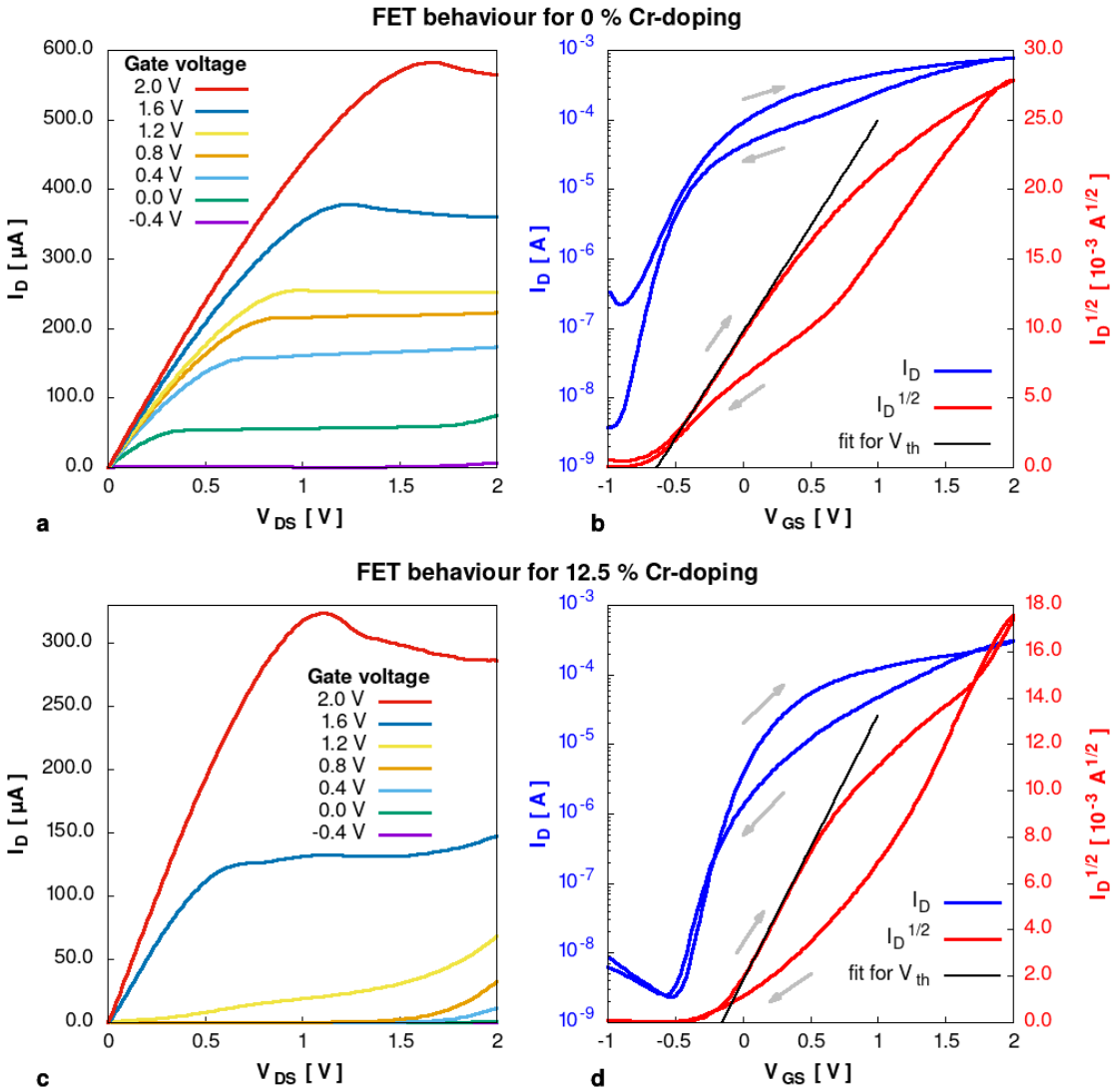

Figure 5.6.: a) and b) output and transfer curves for undoped indium oxide; c) and d) output and transfer curves for 12.5 % Cr-doping, transfer curves are measured at $V_{DS} = 1\,V$

parison to the previous series with two printed layers. Additionally, the threshold voltages were shifted to negative values in the range of -0.7 V to -0.1 V. These changes arise

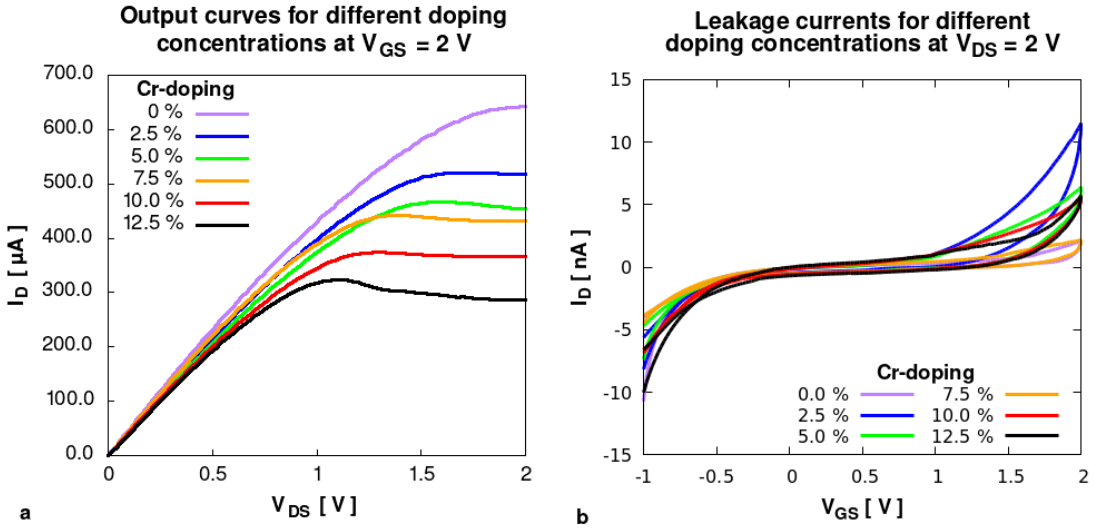

Figure 5.7.: a) Output curves for one selected device from each doping concentration set at $V_{GS} = 2\,V$ b) corresponding leakage currents at $V_{DS} = 2\,V$

from the increased layer count leading to a better channel structure, i.e. electrical grain-to-grain contacts, on the microscopic scale and more tolerance with respect to printing variations. This makes the influence of the channel material the prominent factor in the value of V_{th}. On top of this, the correlation of the linear regression is heavily improved.

The full detailed data is attached in the appendix in sec. **TA.2**.

Again, the sets have been statistically analyzed likewise to the series with two printed layers. Each set can be clearly separated from each other as is shown in tab. **T5.4**

The reduction in $I_{D,on}$ cannot be fully explained via V_{th}, as can be easily derived from the standard MOSFET-equation below

$$I_D = \mu_{FET} \frac{W C_{ch,ar}}{2L} (V_{GS} - V_{th})^2 \tag{5.1}$$

In order to better understand the reduction in $I_{D,on}$, devices from each set were selected for determining the field effect mobilities. As discussed in sec. **2.1.7**, this needs determination of both channel dimensions as well as specific capacitances. Dimensions are derived using images of the devices from an optical microscope.

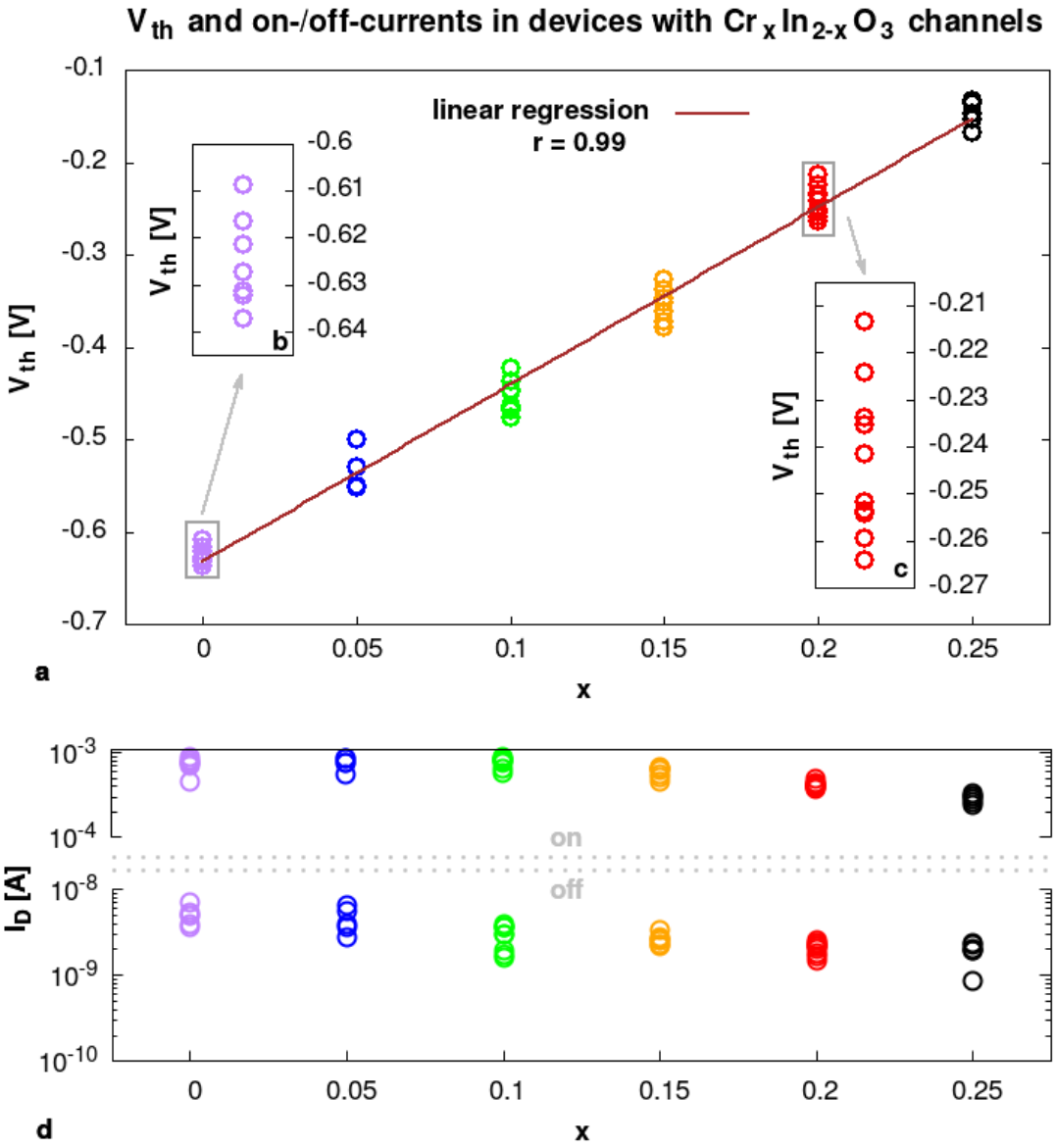

Figure 5.8.: a) Threshold voltages with inlets b) and c) showing enhancements of the stacked values for 0 % and 10.0 % Cr-doping; d) on- and off-currents for each device by Cr-doping content

Cr-Doping	**0.0 %**		**2.5 %**		**5.0 %**		**7.5 %**		**10.0 %**		**12.5 %**	
Mean [V]	-0.625		-0.527		-0.455		-0.375		-0.243		-0.145	
σ [V]	0.010		0.025		0.017		0.019		0.016		0.013	
Shapiro-Wilk	0.803		0.131		0.497		0.614		0.616		0.312	
F-Test		0.048		0.331		0.768		0.643		0.662		
t-Test		0.00		0.00		0.00		0.00		0.00		

Table T5.4.: Statistical analysis data for each doping set with four printed channel layers, F- and t-test results are given for neighboring sets, in F-tests green indicates identical variances, in t-tests green indicates differing means

The selection criteria for eligible devises were near equal widths in the contacts lines between channel and either lead, and alignment of these contact lines so that that a near rectangular channel is formed, since eq. **(5.1)** is valid for a rectangular channel only. Additionally, clear visibility of the overlap of the leads with the channel or electrolyte, respectively, was required in order to minimize errors in the optical measurement.

Fig. **5.9** demonstrates this for two rejected and one accepted device. Only device **c** reliably can be determined to show a rectangular channel geometry.

Notably, all three FETs were fully functional. Especially considering device **a**, either the contact can be established along the lead surface perpendicular to the plane, that arise from the ablation process (compare to sketch in fig. **5.10**) or the channel is partially invisible in the optical microscope. As enhanced with the orange rectangle in fig. **5.9a**, inconsistent drying of the electrolyte layers leads to chromatic aberrations visible in all sample images. Additionally, the round shape of the printed droplets also leads to stray currents along curved paths, a limitation that is unavoidable in the given setup due to the nature of printing. Taken together, the possibility of undetected contacts, chromatic aberrations, and non-ideal channel shapes are severe error sources when measuring the channel widths, the relevant areas for specific capacitance determination, and during calculation of μ_{FET}, respectively.

Despite these limitations, a nearly linear trend towards lower field effect mobilities with rising doping concentrations could be obtained, as shown in fig. **5.11**. This is in accordance with the expected behavior as the Cr-atoms act as scattering centers in the In_2O_3 lattice and fits to earlier findings in literature. [130] Additional doping effects on the crystallization that negatively influence the field effect mobilities of the total device cannot be excluded. Possibilities for such are e.g. changed grain sizes or local agglomerations of Cr.

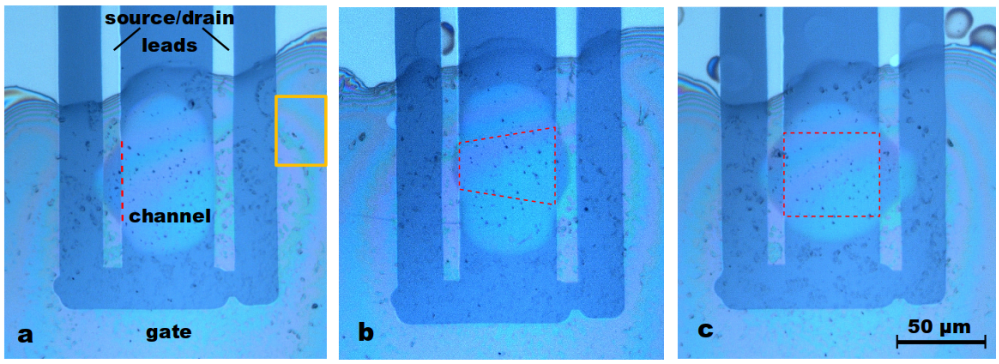

Figure 5.9.: Microscopic images of devices showing the contact between channel and leads. a) contact width only visible on one lead (left, dashed line); within the orange rectangle, chromatic aberrations from inconsistent drying of the electrolyte layers are visible as changes between blue and purple, b) contact widths severely differ, leading to trapezoid channel geometry, c) ideal case with equal channel contact widths aligned on the same height, leading to a rectangular channel shape

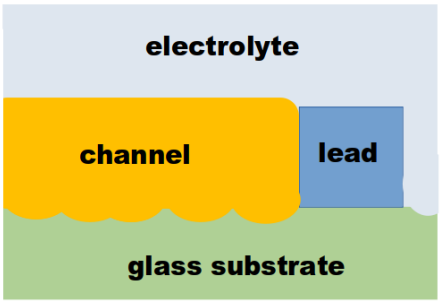

Figure 5.10.: Sketch of a section view showing channel and lead contacting on the side surface of the lead created during ablation lasering of the ITO glass substrates, the substrate is roughened due to the conditions during ablation

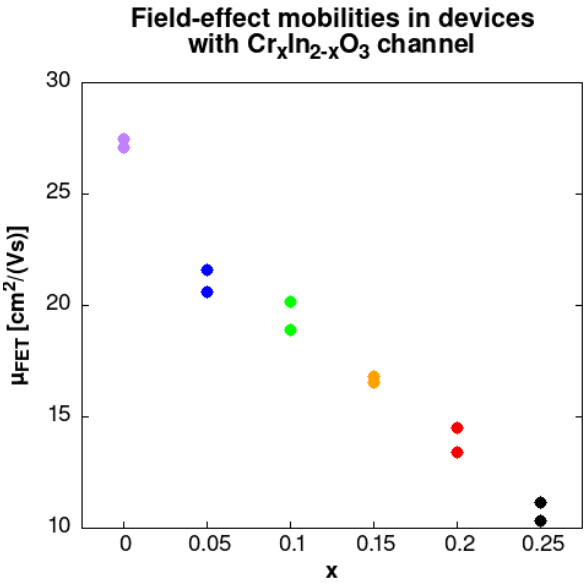

Figure 5.11.: Field effect mobilities for different doping concentrations

With the decrease in μ_{FET} and the increase in V_{th}, the lowered output currents with rising Cr-concentrations can now be fully understood.

5.4. Conclusion

In this chapter it was shown that wet-chemistry doping of the precursor inks can be used as a reliable method to influence major FET characteristics. Doping In_2O_3 channels with Cr allowed for linearly increasing V_{th}, however, comes with severe reductions in the output currents due to increased threshold voltages as well as lowered field effect mobilities arising from the introduction of Cr as scattering centers. Additionally, it shown that the material is but one of the influences on FET characteristics in printed electronics: doubling the printed channel layers has not only systematically lowered V_{th} for all devices and thus made a change from normally-off to normally-on systems; it also increased reliability versus production of non-functional devices due to more tolerance against errors arising from droplet placement variations.

With this work proving that wet-chemistry doping is a simple and very reliable method for influencing key characteristics, many new research fields are available. Next to the examination of other dopant-channel-systems, it remains interesting how the loss in on-currents may be overcome. Possibilities include applying different ink thicknesses, changing FET-geometries, or combinations of different dopants.

6. ALD-Derived Al_2O_3 as Solid Electrolyte

6.1. Current Research in the Field

The differences between the mechanisms of electrolytic versus dielectric gating have been discussed earlier in sec. **2.1.4**. While electrolytes there have been shown to have a huge advantage in low-voltage applications due to the high local polarization in the Helmholtz double layer, one of the major problems is long-term stability: ionic liquids are highly hygroscopic, and salt-solution based systems may irreversibly dry out. This leads to the need of encapsulation or favors side-reactions. [143–145] Alternatives include self-assembling ionic gels, which recently made interesting progress. [146]

Typical dielectric materials on the other hand are usually very stable towards environmental influences. They include oxides, nitrides, oxynitrides, or silicates of, e.g., aluminium, hafnium, silicon, or zirconium. [42] In contrast to liquid-based electrolytes, which can be printed, such dielectrics need to be applied via deposition methods that allow for both, high crystallinity and good, pinhole-free conformity towards the channel material. This is a necessities to ensure good polarizability of the material and transfer of the polarization into the channel free of short circuits.

Focusing on Al_2O_3, which is popular due to the low material costs, the high relative permittivities of usually $\kappa \approx 10$ and dielectric strengths of 20 kV/mm and more, this usually means ALD-deposition at temperatures of at least 200 °C. [147–152] This conflicts with most of the substrate materials in consideration for flexible electronics being polymers leading to maximum deposition temperatures in the range of 100-130 °C. ALD-derived alumina at these temperatures usually are of low crystallinity or even amorphous and have reduced densities. [153, 154] Despite its high chemical stability and even use as moisture-blocking corrosion barriers, the surface of alumina is able to chemically adsorb water leading to hydroxy surface functionalities. [155–159] Lowering deposition temperatures has been proven to have a clear impact on increasing amounts of hydroxy functionalities in ALD-derived Al_2O_3 when exposed to humidity. [154, 160–164] As this process

is fully reversible but leads to a notable change in capacitance, alumina produced via anodization methods has been established as common material in for moisture sensors, vastly applied in industrial products. [165–168]

Within the scope of this work, the humidity-dependent capacitance is to be exploited by applying Al_2O_3 onto printed FETs. Relying on the Grotthus mechanism – i.e. proton mobility by hopping in systems with absorbed water molecules and dangling hydroxy groups – Al_2O_3 is to be used as solid electrolyte. The higher the humidity, the more layers of water are chemosorbed, later physiosorbed, increasing the network for proton movements. [169, 170] This allows for combining the very good environmental stability of the material with the low-voltage advantages of electrolyte gating. However, it must be assumed that the network for proton movements is not as reliable and far-reaching as in a CSPE, as previously applied in this work. Therefore, printed top gates will be added. Typically high-surface Al_2O_3 for applications in sensors is created by anodization from the metal. [170, 171] This method is not reasonably applicable here as the harsh conditions may as well alter other components of the FET and preceding deposition of Al metal would be necessary. ALD on the other hand fulfils several advantages: full control of the thickness, good surface conformity, low temperatures due to the need for high-surface Al_2O_3, and otherwise mild process conditions.

6.2. Material Characterization of the ALD-Derived Alumina

The alumina is derived from a low-temperature ALD process at 130 °C using TMA and H_2O as precursors. A detailed experimental description is given in sec. **3.2.3**. Before using the low-density alumina, as solid electrolyte, the thickness and density must be understood. Obviously, the thickness is in direct correlation with the number of ALD-cycles, however, dependent on the deposition temperature the density of the material changes. Using the known parameters of the underlying wafer as starting conditions (sec. **3.3.4**), the reference sample is suitable for investigation of the Al_2O_3 layer via XRR. By varying thickness, roughness, and density of the deposited Al_2O_3 in the range of $0.4\,^\circ \leq 2\theta \leq 4.0\,^\circ$ only a non-satisfactory accordance between fitted curve and experiment could be achieved. Allowing optimization also for the values of the underlying SiO_2, the fit between measured and simulated reflectometry graphs was severely improved under correction of the SiO_2 thickness to 170 nm (from 200 nm) while maintaining roughness and density. As shown in fig. 6.1, the fit can be considered near identical to the measurement.

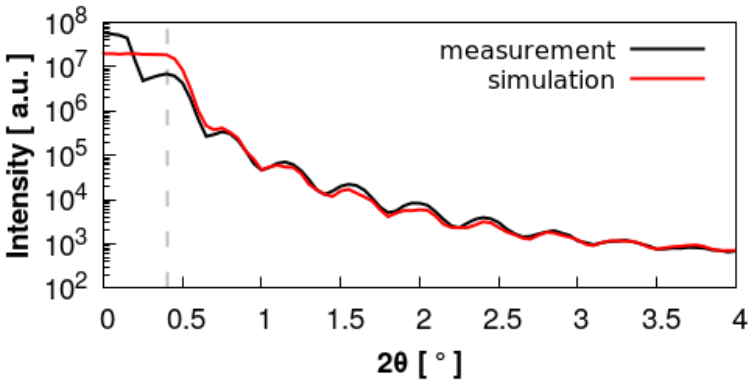

Figure 6.1.: XRR-plot showing measured (black) and simulated (red) curves for the range of 0° to 4°, gray dashes indicate the beginning of the fitting range at 0.4 °; the simulation curve was optimized with respect to the parameters of thickness, surface roughness and density of Al_2O_3 only

properties of ALD – Al_2O_3	
thickness [nm]	20
roughness [nm]	0.2
density [g/cm^3]	2.7

Table T6.1.: Material properties of ALD-derived Al_2O_3 as derived from XRR-measurements after process optimization

The determined material properties of the ALD-derived Al_2O_3 are shown in tab. **T6.1**. The density of 2.7 g/cm^3 is severely smaller than the value of 4.0 g/cm^3 (for corundum) hinting that the material is present in the desired form with many hydroxy functionalities. [172]

The thickness of Al_2O_3 as applied to the devices, was optimized to 20 nm because lower values would lead to an increased number of short circuits in the resulting FETs and thus were not considered as reproducible processes.

6.3. Devices with Ag Top Gates

In a first series of devices, Ag has been applied as top gate material due to the high conductivity of the metal and low annealing temperature of the nanoparticulate ink. The FET characterization is shown in fig. **6.2**. While the output curves look promising, and the transfer curve shows no hysteresis and a V_{th} of -0.27 V, the leakage currents closely follow the drain current evolution with rising gate bias. At maximum gate bias, the leakage current reaches 10 % of the drain current value.

This leads to the assumption of locally extremely thin Al_2O_3 layers that break down even at very low local fields or simply pinhole type gate oxide shorts. This also explains why the gate current is only reasonably small when the gate voltage is set to $V_{GS} = -V_{th}$, i.e. the channel polarization zeroed, as even the field created by the polarization arising from the metal-insulator-semiconductor contact already overcomes the dielectric strength.

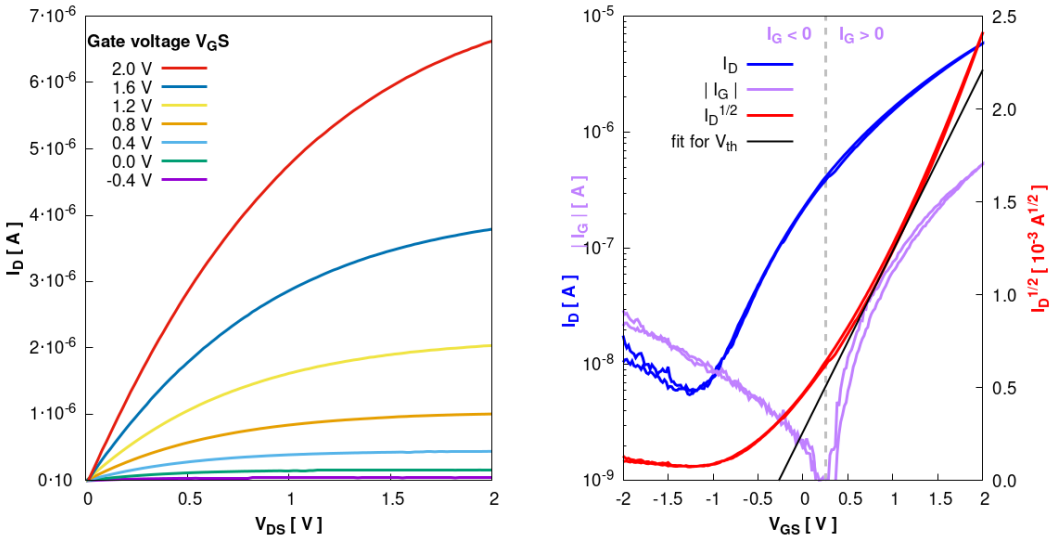

Figure 6.2.: FET characteristics of a device with Ag top gate. a) output curves; b) transfer curve, gate leakage current and linear fit to $\sqrt{I_D}$ for V_{th} determination at $V_{DS} = 2\,V$

6.4. Devices with Graphene Top Gates

Following the high leakage currents in Ag top-gated devices and a high process failure rate due to short circuits, the top gate material was replaced with graphene by adopting an established method from literature where the good conductivity of the material is shown. [141] An SEM micrograph of a resulting device is shown in fig. **6.3**.

Characteristics of a typical graphene top gated device from this set in the 1 V-regime is shown in fig. **6.4**. In comparison to the device with the silver gate, the threshold voltage is shifted to a positive value of 0.45 V and the output curves saturate showing clear NDR behavior. NDR typically is associated with trap states in the channel, which in printed systems is very likely due to surface roughness and grain boundary contacts. However, in this case another option arising from the solid electrolyte may be considered: local differences in the material density or connection of the proton network may as well lead to the channel being locally differently polarized, i.e., the electrolyte not providing a constant bias throughout the system. In comparison to the Ag top-gated device from the previous section, gate currents are reasonably small in the range of $\pm$ 25 nA and do not

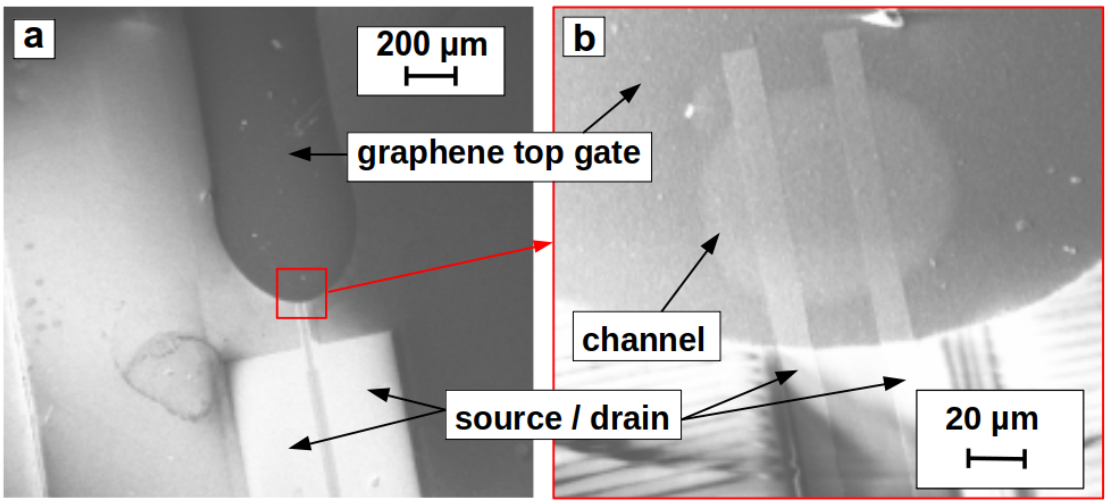

Figure 6.3.: SEM micrographs of the device a) micrograph of the whole device, the red square marks the area enhanced in b), where the printed channel beneath the carbon top gate is visible; the acceleration voltage has been increased from 5 kV in a) to 10 kV in b) order to penetrate through the carbon top gate

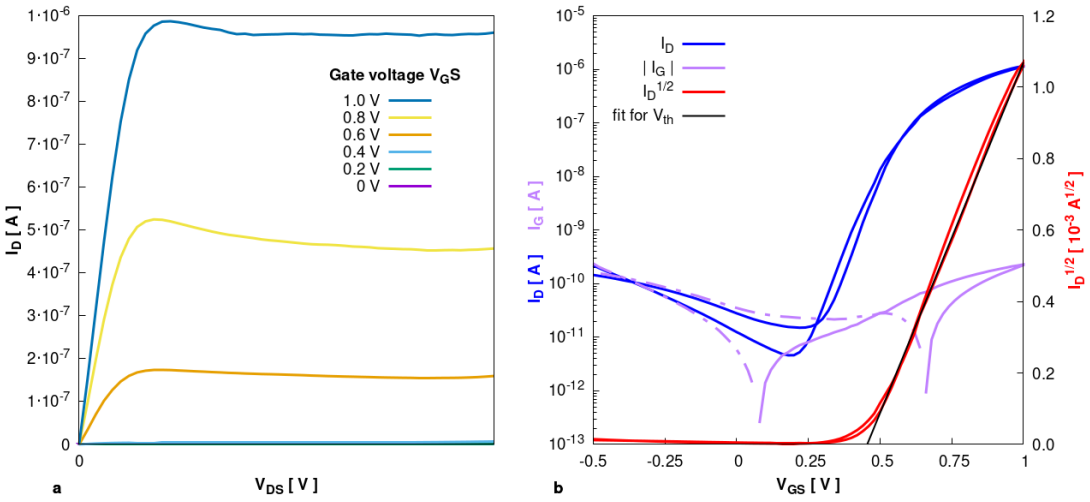

Figure 6.4.: FET characteristics of a graphene top-gated device a) output curves and b) transfer curve with gate leakage current and linear fit to $\sqrt{I_D}$ for V_{th} determination at $V_{\text{DS}} = 1\,\text{V}$; the gate current is shown as absolute value and dashed where negative

follow I_{D}. The hysteresis behavior, especially for the gate current, indicates electrolyte-type gating as slow ion movements upon gate bias changes will lead to delayed responses in the measured currents.

In order to understand the better performance of graphene versus silver as top gates, first of all chemical reactions must be ruled out. While there are reports of silver oxide – which may be present on the nanoparticle surfaces – acting as catalyst for H_2O electrolysis, this option can be ruled out as it would otherwise lead to a drastic increase in I_{G} once the relevant potential is reached. [173] This is not present in fig. **6.2b**. A report regarding dendrite formation when applying printed silver contacts in CSPE-gated FETS also does not apply here, as the Ag-top gated device is stable for many usage cycles. [174] In contrast, alumina is often used as passive carrier material for silver-based catalyst. [175,176] Most likely pinholes exist in the Al_2O_3 but only the small silver nanoparticles (size 2-4 nm) may fill these material defects, while the graphene flakes with 2-3 orders of magnitude larger sizes (0.2-3 µm) simply are deposited above these holes. That way no pinhole effects appear and the increase in V_{th} can be explained as resulting from the effectively thicker electrolyte layer.

6.5. Humidity Dependence of Device Characteristics

6.5.1. FET Characteristics

For measuring the humidity dependence of the gating mechanism, a device was placed in a sealed box at room temperature and the relative humidity was varied between 20 % and 90 % in steps of 10 %. The device was allowed to adjust to a humidity change for at least 1 min before obtaining the measurements.

The behavior versus humidity is determined based on the forward measurements of transfer characteristics at each humidity using a range of -0.25 V $\leq V_{GS} \leq$ 1.75 V at V_{DS} = 1 V. V_{GS} was limited to this value as above 1.75 V severe increases in the gate currents appeared, most likely following electrochemical reactions on the alumina surface. V_{DS} was selected in order to ensure low-voltage operability given as desired. The resulting graphs are shown in fig. **6.5a**. As can be seen, very low relative humidities below 30 % lead to the device showing non-characteristic behavior in the transfer curve. It must be assumed that the electrolyte is dried out at such low humidities and I_D is solely governed by the intrinsic channel resistance. The notable change between 20 % and 30 % RH can be attributed to absorbed water in Al_2O_3 leading to a surface polarization of the channel but still no interconnected network for proton movements. Additionally, tunneling effects allowing electron movements have been described in Al_2O_3 moisture sensors as governing effect for conductivity changes at low humidities. [177]

At RH of 40 % and higher, the device shows typical FET transfer characteristics. With increasing RH, V_{th} shrinks from 0.66 V at RH = 40 % to 0.43 V at RH = 90 %. Threshold voltages have been determined using the square root method and are shown in fig. **6.5b**. Both, $I_{D,on}$ and $I_{D,off}$ increase with humidity, but as can be seen with the shrinking $I_{D,on}/I_{D,off}$-ratio in fig. **6.5c**, $I_{D,off}$ is rising overproportionately. Ratios are shrinking from $5.4 \cdot 10^7$ to $3.4 \cdot 10^5$. Such behavior has also been reported earlier during investigation of humidity dependency of a CPSE-gated device. [129] Following this report, it must be assumed that the carrier concentration in the channel surface is directly influenced by the changed material properties of the Al_2O_3 upon water adsorption, explaining both the increase in $I_{D,off}$ and the lowering of V_{th}. This is also in accordance with the observed conductivity change between the states with dried out electrolyte at 20 % and 30 % RH. I_D at V_{GS} = 1 V rises with RH from 95 µA to 309 µA which now may be explained as the result of two effects. First, the lowered threshold voltages, and second the increased capacitance of the electrolyte as known from sensor applications. [165–167, 178] Nevertheless, the transfer curves saturate in the same order of magnitude in the range of 567-688 µA.

Possibly at higher gate biases, ion hoppings are possible that are otherwise energetically hindered, leading to a better channel polarization.

In order to ensure that different $I_{D,on}$ values are not merely a result of slowed ion movements through the electrolyte due to a less continuous hopping network at lower RH, measurement speeds have been reduced. However, no change in I_D could be detected and the values also remain constant when V_G is maintained over longer periods of time.

Gate leakage currents increase with humidity, especially at higher values. This is a direct result from the increased number of ions in the electrolyte, especially the very strong increase above $V_{GS} = 1\,V$ may even be the result of electrochemical reactions. However, the values are still in the nA-regime as shown in fig. **6.5d**.

The stability of the behavior towards humidity changes has been examined by cycling RH between 20 % and 90 % up and down several times in 10 % intervals. At each interval step, transfer curves have been recorded, while curves labled *C1* and *C1-up* match the ones from fig. **6.5a**. In fig. **6.6**, the transfer curves for four selected relative humidities are shown. As can be seen, the characteristic for higher humidities are highly reproducible. Deviations between the curves at one RH most likely arise from the device being very sensitive even towards small humidity changes. Since there is no clear trend between the deviations, they can be assumed random.

In the case of RH = 20 %, the initial behavior could not be reproduced after the device has been in a humid environment, but cycles 2 and 3 show similar characteristics with a linear rise in I_D by two orders of magnitude. Once exposing the device to a dry atmosphere for 30 min, this behavior is severely reduced and after a full day in dry nitrogen atmosphere, the initial behavior, ruled by the intrinsic resistance of the semiconductor, is reestablished. It must be assumed, that the desorption of surface water faces a higher energy barrier for the first molecular layer. Typically, at this point the molecules are chemisorbed to the Al_2O_3 unlike consecutive surface water molecules that are physiosorbed.

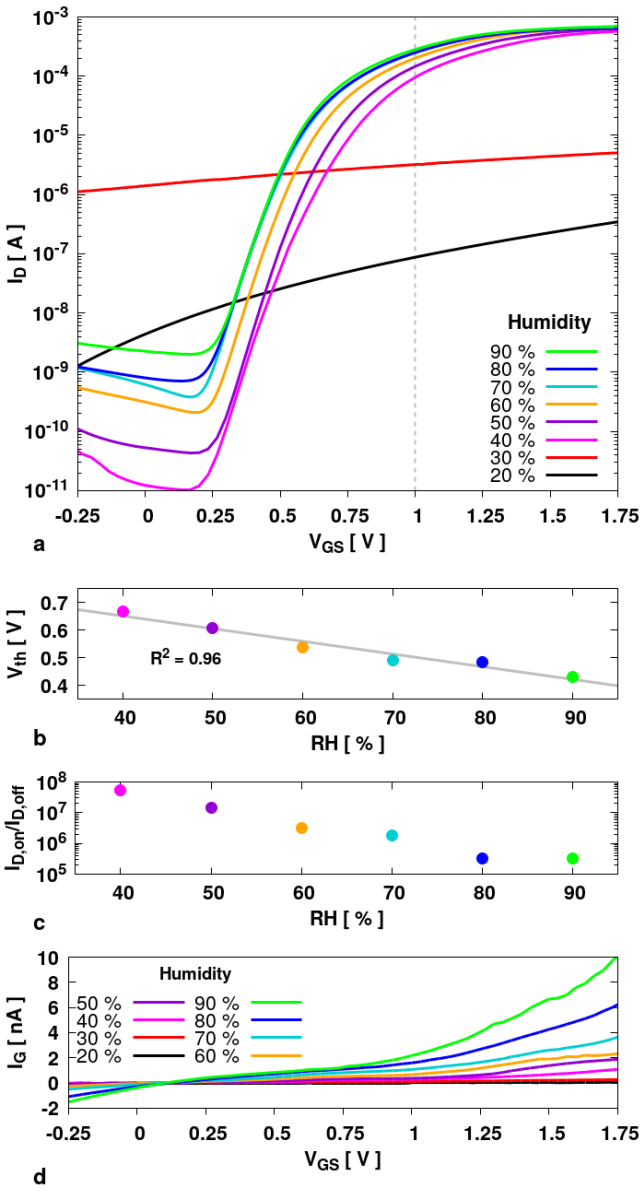

Figure 6.5.: a) transfer characteristics at different RHs in the range of $-0.25\,\mathrm{V} \leq V_{GS} \leq 1.75\,\mathrm{V}$ at $V_{DS} = 1.0\,\mathrm{V}$, gray bar at $V_{GS} = 1\,\mathrm{V}$ to mark responding current values for pulsed measurements; b) threshold voltage versus relative humidity for functional devices with linear fit (gray); c) $I_{D,on} / I_{D,off}$-ratios versus relative humidity for functional devices; d) gate leakage currents for transfer curves in a)

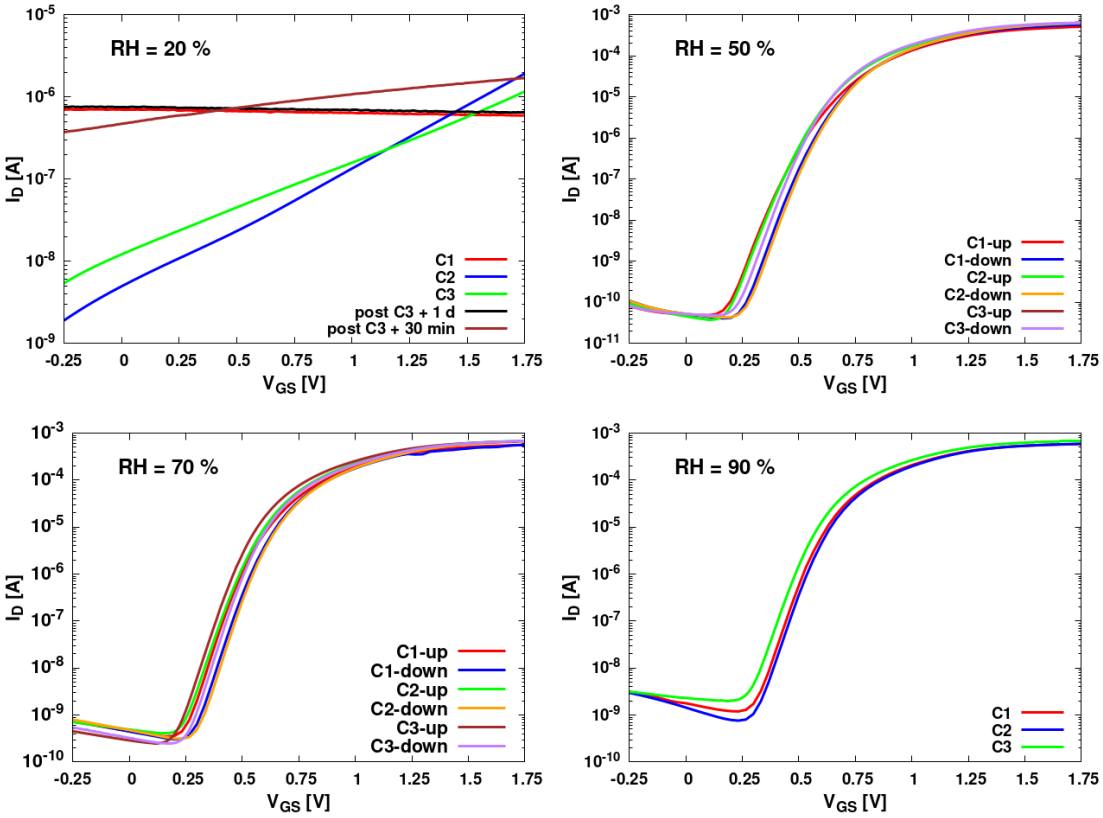

Figure 6.6.: Transfer curves at different relative humidities after cycling the relative humidity up and down between 20 % and 90 %; the integer after *C* indicates the cycle number, *up* and *down* whether the curve has been recorded while increasing or decreasing RH, as RH = 20 % and 90 %, respectively, are corner points, this does not apply to these graphs

6.6. Time Dependence of I_D

In order to gain an insight into the switching speed of the device, a gate bias of 1 V was applied as rectangular pulse at 1 Hz, and I_D and I_G observed over time. The choice to set V_{GS} to 1 V was made to fully ensure that electrochemical side reactions are minimized and low voltage operation is maintained.

In fig. **6.7**, the evolution of I_D and I_G during V_G pulses are shown for different RH. In contrast to higher RH, where $I_{D,on}/I_{D,off}$ ratios span several orders of magnitude, on- and off-currents at RH = 30 % are in the same order of magnitude (compare to fig. **6.5**). Therefore, the value of I_D has been leveled with the minimum drain current $I_{D,min}$ for better visualization.

For RH = 30 %, the profile matches a device with quick response times (with respect to the given pulse frame) as would be expected for a semiconducting material solely governed by its intrinsic resistance. After a sharp rise, the final current is quickly established. However, a certain negative differential resistance behavior shows at the beginning of the pulse and the current does not fully saturate. While there are multiple possible explanations for NDR as discussed earlier, the slow increase in I_D may result from residual humidity in the electrolyte leading to a very weak contribution of electrolyte-type gating with very slow and hindered ion movements due to the dry nature of material.

Starting with RH = 44 %, the effect of an increasing electrolyte-type gating becomes apparent by both severely slowed I_D built-up profiles as well as increasing current values. Notably, up until RH = 74 %, I_D does not saturate, contrary to higher relative humidities. This may be explained due to the increasing number of surface ions that are formed with more absorbed water, leading to both more available charge carriers in the electrolyte as well as an increasingly interconnected network for ion hopping. More ions in the electrolyte will lead to a better surface polarization and thus higher I_D values, a better network will lead to faster ion movements and thus a quicker saturation of I_D. Notably for RH = 86 % and higher, the final I_D values also match to values that could be derived from fig. **6.5a** at V_G = 1 V.

This effect also shows in the gate currents (black curves in fig. **6.7**), where at low humidities only a single pulse is visible, i.e., after an initial polarization, zero or very little ion movements happen. At RH of 74 % and higher, I_G shows a slower decline. These profiles match typical electrolyte capacitor charging profiles, aligning with the concept of electrolyte gating effectively being a capacitor element. At higher RH, I_G does not fall back to zero, which may be indicative of ongoing electrochemical reactions. However,

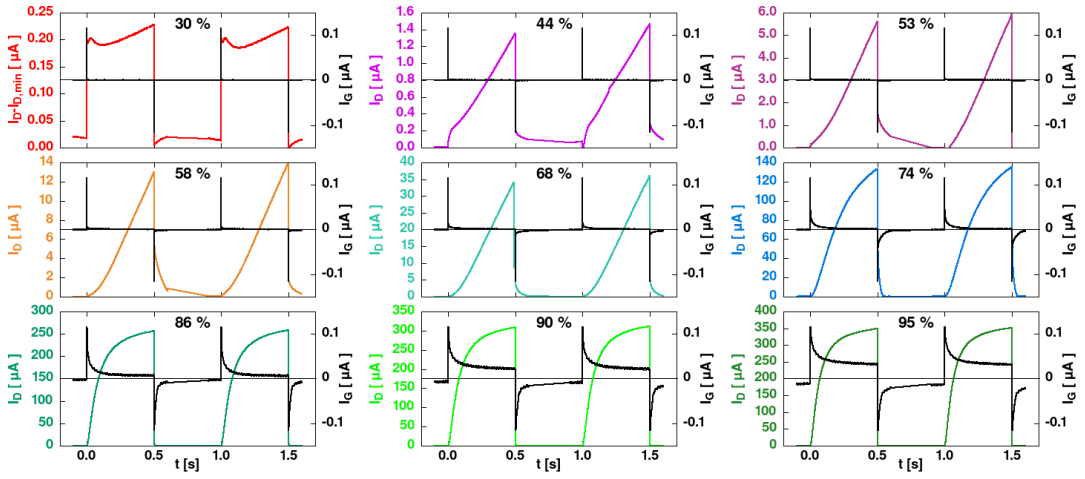

Figure 6.7.: I_D (colored) and I_G (black) at different RHs in pulsed measurements; the output currents at RH = 30% have been corrected by the minimum drain current ($I_{D,min}$) for visualization reasons due to $I_{D,off}$ being several orders of magnitude higher in this case (compare to Fig. **6.5a**)

hysteric charging behavior of the electrolytic capacitor, as described in literature, may also influence this current behavior. [179]

Upon analyzing the current built-up behavior (see enhanced view in fig. **6.8**), it becomes apparent, that at humidities below 58 %, an initial sudden increase in I_D is visible. This may be due to dielectric gating behavior that vanishes with increasing surface ion generation in favor of a fully electrolytic gating. Once the surface is sufficiently saturated (RH of 74 % and higher), the sudden increase in I_D with the pulse is related to the good ion network and high surface polarization capabilities of the electrolyte. This increased sensitivity is also the reason for the noise at $t < 0$ where the electrolyte reacts to the noise of the pulse generator which relies on a Fourier series.

Using pulse lengths of 10 s, the periods until saturation was reached were determined. Saturation hereby is defined as I_D reaching 95 % of the I_D value at $V_{GS} = 1$ V from fig. **6.5a**. As shown in fig. **6.9**, saturations occur between 0.7 s and 7.5 s, systematically increasing with decreasing humidity. Again this sustains the model of hindered ion movements in a dry electrolyte.

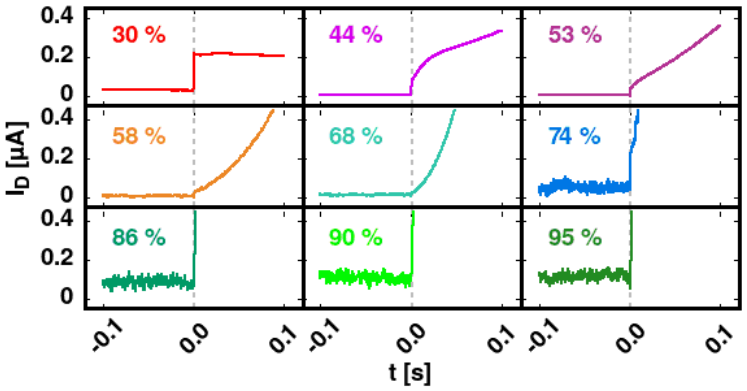

Figure 6.8.: Enlarged view of the I_D rising behavior in Fig. **6.7** at gate bias switches

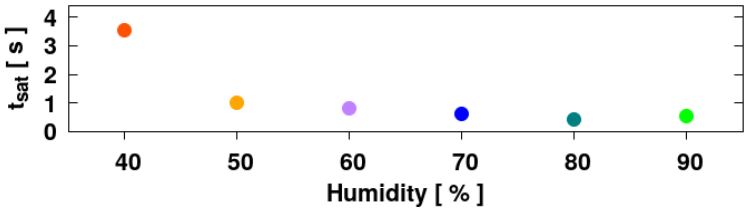

Figure 6.9.: Time to reach 95 % saturation in I_D after applying V_{GS} of 1 V to an unbiased device

6.7. Conclusion

Within this chapter an FET device relying on low-density, low-temperature ALD-derived alumina as gating material is shown. With this approach, the typical composite solid polymer electrolyte could be replaced by a single material which is known for its high chemical and environment stability while maintaining the good drain currents known from CSPE-gated systems. Early attempts using printed silver as gate contact had shown high leakage currents, assumingly due to pinhole contacts. This problem could be avoided by switching to graphene contacts due to the larger particle size bridging over pinholes.

As the electrolytic character of Al_2O_3 is dependent on suface-absorbed water molecules which provide both ions and a network for ion movements, the humidity density was thoroughly examined and shown to be fully reversible. The channel polarization capability of the electrolyte increases with humidity leading to a vast increase in I_D. On the other hand, the device may be deactivated at very low humidities by effectively drying out the electrolyte. Using pulsed measurements, the electrolytic gating mechanism was further confirmed, and it was shown that drain current saturation only occurs in a reasonable time at higher humidities.

Al_2O_3 may be effectively applied as electrolyte, however, further research will be necessary in order to both reduce switching times and decrease I_D-dependency of the external humidity.

7. Summary and Outlook

Printed, inorganic field-effect transistors can be optimized in manyfold ways. Within this work, three option have been examined: a change of the geometry in order to overcome printing resolution limitations, a systematic change of the materials through doping of the channel, and replacing the electrolyte by an inorganic alternative.

Within the first option, a previously described system with a porous, vertical SnO_2 channel was further optimized by replacing the template polymer and the oxide precursor with simpler materials while also reducing the process temperature by 100 °C. At an overlap area of only 2 μm^2, currents in the µA range were obtained at operation voltages of only 1 V. A fully functional device with current densities of up to 167 $\frac{A}{cm^2}$ was obtained, with an on-off-ratio spanning four orders of magnitude.

However, the system still has a few drawbacks: the production process needs several lithographic steps and the usage of two different metals in the contacts leads to the formation of a Schottky barrier making the device only a unidirectional FET. This on the other hand opens the possibility to use it as Zener-diode.

The porous channel was created in a highly regular pattern with large pore sizes matching the template polymer sphere diameters of 200 nm. This opens the interesting possibility of coating the channel surface via ALD allowing, e.g., for dielectric- or solid electrolyte-gated devices, possibly with closely applied gate metal instead of a displaced gate setup. Up to date it was not possible to create a pinhole-free insulator layer and the issue remains a research topic. Most importantly, the very good current densities in such setups would allow balancing the disadvantages of materials with non-optimal electronic properties. Especially p-type oxide semiconductors are known to show lower field-effect mobilities and a complementary metal oxide semiconductor system with a planar n-type and vertical p-type FET with matching currents seems feasible and could mean a breakthrough in the application of metal oxide semiconductors.

In the case of doped precursor inks, a very simple, scalable, yet highly reliable method for influencing the threshold voltage of a printed FET was successfully shown. The linear dependency between dopant concentrations and V_{th} makes this method especially appealing as transistor properties may now be predicted in a simple manner. The shift of V_{th} by ca. 0.5 V at operation voltages of 1 V, i.e. spanning over a large interval of the operation voltage range, shows the great potential of this method. However, a major drawback is given regarding the output currents suffering from both the increase in V_{th} as well as a loss in mobility due to the crystal defects stemming from the dopant.

Nevertheless, the simplicity and reliability of this method allow for manyfold variations and different dopant combinations and open a vast range of materials and designable properties with very little effort.

Finally, the exchange of the CPSE by low-density ALD-derived Al_2O_3 led to a device with a solid oxide electrolyte showing humidity-dependent gating behavior. It was successfully shown that the mechanism is based on proton movements along surface hydroxy functionalities and absorbed water molecules in accordance with the Grotthus mechanism. Not only could the polymer-based electrolyte be replaced by a highly stable material, but it was also shown that ALD can be used as an effortless method to obtain a solid electrolyte from a comparably basic material. The strong humidity-dependency comes with the drawback of low reaction times, but excels at generating very high currents. The performance breakdown with a dried-out electrolyte has been shown to be fully reversible making such devices ideal candidates for applications that explicitly ask for humidity-based operations with strong tolerance towards harsh humidity values on the upper and lower end of the scale.

In general, this work has further proven that printed field-effect transistors based on inorganic oxide semiconductors can be operated at very low voltages while still being fully functional. This work has proven again that printed FETs allow for a vast range of optimization approaches: from doping a component to replacing the electrolyte up to a full redesign of the established geometries. The topic of printed FETs remains an interesting and vast field for research activities – also because of the challenges material printing has to offer.

A. Appendix

A.1. Cr-Doped Channels with Two Printed Layers

A.1.1. Series Data

Cr-doping	$I_{D,on}$ [A]	$I_{D,off}$ [A]	$\log_{10}(I_{D,on}/I_{D,off})$
0 %	$6.09 \cdot 10^{-5}$	$1.08 \cdot 10^{-10}$	5.75
	$6.57 \cdot 10^{-5}$	$1.08 \cdot 10^{-10}$	5.78
	$5.27 \cdot 10^{-5}$	$6.39 \cdot 10^{-11}$	5.92
	$1.75 \cdot 10^{-5}$	$4.02 \cdot 10^{-11}$	5.84
2.5 %	$6.37 \cdot 10^{-5}$	$1.10 \cdot 10^{-10}$	5.76
	$1.28 \cdot 10^{-5}$	$2.79 \cdot 10^{-11}$	5.66
	$3.51 \cdot 10^{-5}$	$1.03 \cdot 10^{-10}$	5.53
	$3.76 \cdot 10^{-5}$	$7.23 \cdot 10^{-11}$	5.72
5.0 %	$1.38 \cdot 10^{-5}$	$4.49 \cdot 10^{-11}$	5.49
	$1.22 \cdot 10^{-5}$	$2.72 \cdot 10^{-11}$	5.65
	$1.25 \cdot 10^{-5}$	$4.64 \cdot 10^{-11}$	5.43
	$2.07 \cdot 10^{-5}$	$5.80 \cdot 10^{-11}$	5.55
7.5 %	$1.70 \cdot 10^{-5}$	$5.96 \cdot 10^{-11}$	5.45
	$8.64 \cdot 10^{-6}$	$8.89 \cdot 10^{-11}$	4.99
	$1.65 \cdot 10^{-5}$	$1.07 \cdot 10^{-10}$	5.19
	$1.63 \cdot 10^{-5}$	$6.95 \cdot 10^{-11}$	5.37
10.0 %	$1.17 \cdot 10^{-6}$	$4.61 \cdot 10^{-11}$	4.40
	$4.34 \cdot 10^{-6}$	$1.77 \cdot 10^{-11}$	5.39
	$7.47 \cdot 10^{-6}$	$3.41 \cdot 10^{-11}$	5.34
	$1.04 \cdot 10^{-6}$	$2.95 \cdot 10^{-11}$	4.55
12.5 %	$2.43 \cdot 10^{-6}$	$8.29 \cdot 10^{-12}$	5.47
	$1.50 \cdot 10^{-6}$	$8.11 \cdot 10^{-12}$	5.47
	$9.97 \cdot 10^{-7}$	$1.65 \cdot 10^{-11}$	4.78
	$2.10 \cdot 10^{-6}$	$7.07 \cdot 10^{-12}$	5.47

Table TA.1.: Individual values for on- and off-currents and V_{th} by doping percentage for series with 2 printed channel layers

A.1.2. Device Characteristics

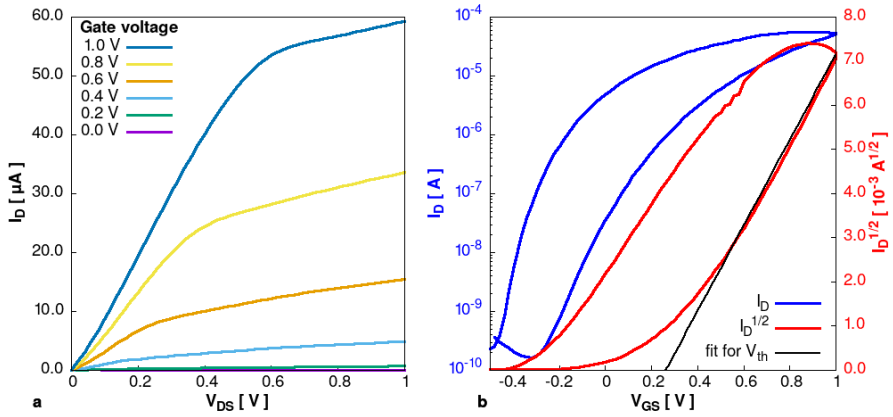

Figure A.1.: Device characteristics for a device with 2.5 % Cr-doping and two printed layers

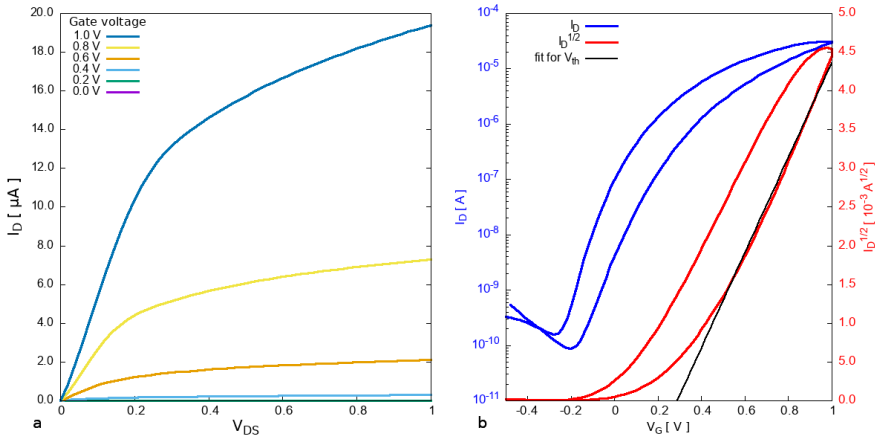

Figure A.2.: Device characteristics for a device with 5.0 % Cr-doping and two printed layers

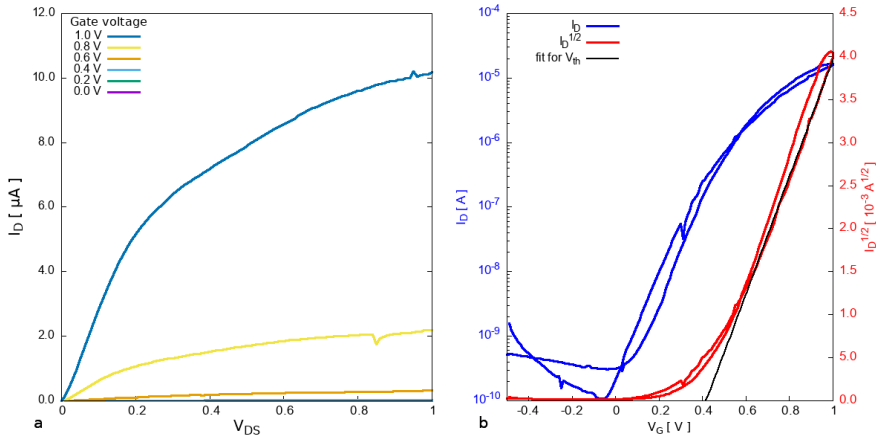

Figure A.3.: Device characteristics for a device with 7.5 % Cr-doping and two printed layers

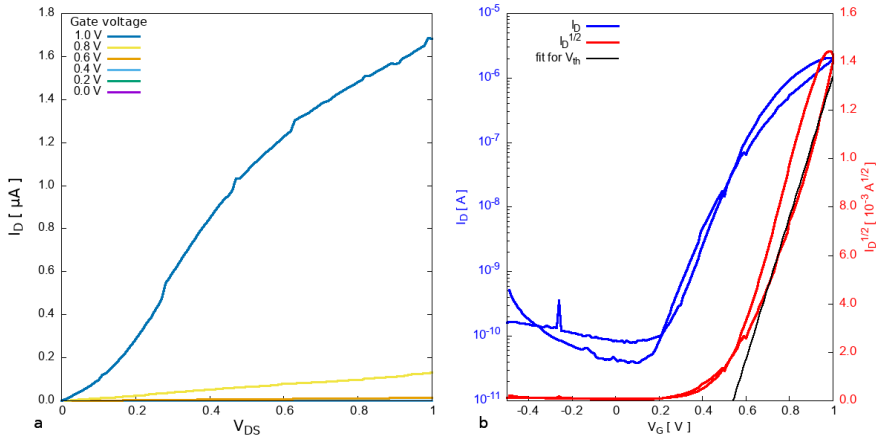

Figure A.4.: Device characteristics for a device with 10.0 % Cr-doping and two printed layers

A.2. Cr-Doped Channels with Four Printed Layers

A.2.1. Series Data

Cr-doping	V_{th} [mV]	$I_{D,on}$ [A]	$I_{D,off}$ [A]	$\log_{10}(I_{D,on}/I_{D,off})$
0 %	-609	$4.59 \cdot 10^{-4}$	$7.00 \cdot 10^{-8}$	4.82
	-616	$8.90 \cdot 10^{-4}$	$5.40 \cdot 10^{-9}$	5.22
	-621	$7.68 \cdot 10^{-4}$	$5.02 \cdot 10^{-9}$	5.18
	-627	$7.76 \cdot 10^{-4}$	$3.70 \cdot 10^{-9}$	5.32
	-631	$7.06 \cdot 10^{-4}$	$4.96 \cdot 10^{-9}$	5.15
	-632	$8.23 \cdot 10^{-4}$	$3.98 \cdot 10^{-9}$	5.32
	-637	$7.76 \cdot 10^{-4}$	$1.28 \cdot 10^{-9}$	4.78
2.5 %	-500	$5.56 \cdot 10^{-4}$	$6.55 \cdot 10^{-9}$	4.93
	-501	$7.72 \cdot 10^{-4}$	$3.96 \cdot 10^{-9}$	5.29
	-530	$8.52 \cdot 10^{-4}$	$2.78 \cdot 10^{-9}$	5.49
	-551	$7.71 \cdot 10^{-4}$	$3.65 \cdot 10^{-9}$	5.32
	-551	$8.72 \cdot 10^{-4}$	$5.53 \cdot 10^{-9}$	5.20
5.0 %	-423	$5.73 \cdot 10^{-4}$	$3.68 \cdot 10^{-9}$	5.19
	-437	$6.50 \cdot 10^{-4}$	$3.00 \cdot 10^{-9}$	5.34
	-446	$8.18 \cdot 10^{-4}$	$1.61 \cdot 10^{-9}$	5.71
	-448	$8.05 \cdot 10^{-4}$	$1.94 \cdot 10^{-9}$	5.62
	-463	$7.77 \cdot 10^{-4}$	$1.75 \cdot 10^{-9}$	5.65
	-463	$9.07 \cdot 10^{-4}$	$3.64 \cdot 10^{-9}$	5.40
	-467	$8.66 \cdot 10^{-4}$	$2.94 \cdot 10^{-9}$	5.47
	-468	$8.29 \cdot 10^{-4}$	$3.87 \cdot 10^{-9}$	5.33
	-476	$8.31 \cdot 10^{-4}$	$3.65 \cdot 10^{-9}$	5.36
7.5 %	-326	$5.57 \cdot 10^{-4}$	$2.79 \cdot 10^{-9}$	5.30
	-339	$6.61 \cdot 10^{-4}$	$2.57 \cdot 10^{-9}$	5.41
	-347	$6.57 \cdot 10^{-4}$	$2.32 \cdot 10^{-9}$	5.45
	-352	$6.38 \cdot 10^{-4}$	$2.21 \cdot 10^{-9}$	5.46
	-361	$5.19 \cdot 10^{-4}$	$2.31 \cdot 10^{-9}$	5.35
	-372	$4.49 \cdot 10^{-4}$	$2.71 \cdot 10^{-9}$	5.22
	-378	$6.78 \cdot 10^{-4}$	$3.39 \cdot 10^{-9}$	5.30
	-379	$6.53 \cdot 10^{-4}$	$2.56 \cdot 10^{-9}$	5.41
10.0 %	-213	$4.23 \cdot 10^{-4}$	$2.42 \cdot 10^{-9}$	5.24
	-224	$4.46 \cdot 10^{-4}$	$2.17 \cdot 10^{-9}$	5.31
	-234	$4.26 \cdot 10^{-4}$	$1.66 \cdot 10^{-9}$	5.41
	-235	$3.94 \cdot 10^{-4}$	$2.01 \cdot 10^{-9}$	5.29
	-242	$3.96 \cdot 10^{-4}$	$1.49 \cdot 10^{-9}$	5.42
	-252	$4.93 \cdot 10^{-4}$	$2.53 \cdot 10^{-9}$	5.29
	-254	$3.72 \cdot 10^{-4}$	$1.77 \cdot 10^{-9}$	5.32
	-254	$4.39 \cdot 10^{-4}$	$2.38 \cdot 10^{-9}$	5.27
	-259	$4.11 \cdot 10^{-4}$	$2.17 \cdot 10^{-9}$	5.28
	-264	$4.05 \cdot 10^{-4}$	$2.19 \cdot 10^{-9}$	5.27
12.5 %	-133	$2.79 \cdot 10^{-4}$	$2.32 \cdot 10^{-9}$	5.08
	-135	$2.38 \cdot 10^{-4}$	$8.58 \cdot 10^{-10}$	5.44
	-137	$3.04 \cdot 10^{-4}$	$1.95 \cdot 10^{-9}$	5.19
	-147	$3.36 \cdot 10^{-4}$	$1.96 \cdot 10^{-9}$	5.23
	-153	$3.08 \cdot 10^{-4}$	$2.30 \cdot 10^{-9}$	5.13
	-168	$2.62 \cdot 10^{-4}$	$2.00 \cdot 10^{-9}$	5.12

Table TA.2.: Individual values for on- and off-currents and V_{th} by doping percentage for series with 4 printed channel layers

A.2.2. Device Characteristics

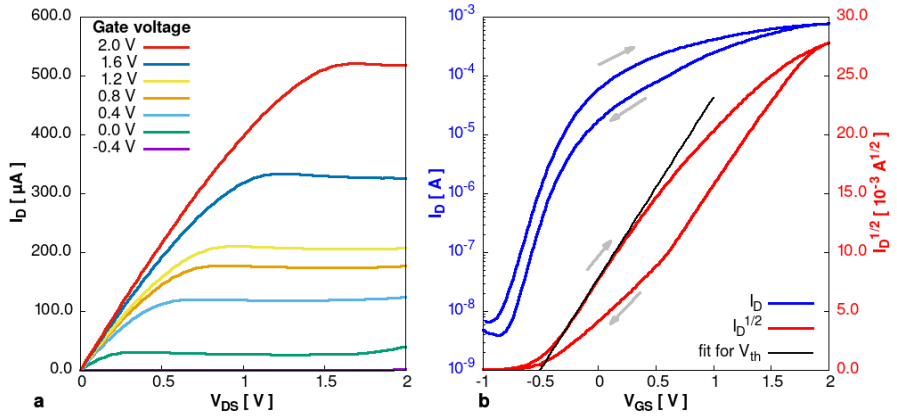

Figure A.5.: Device characteristics for a device with 2.5 % Cr-doping and two printed layers

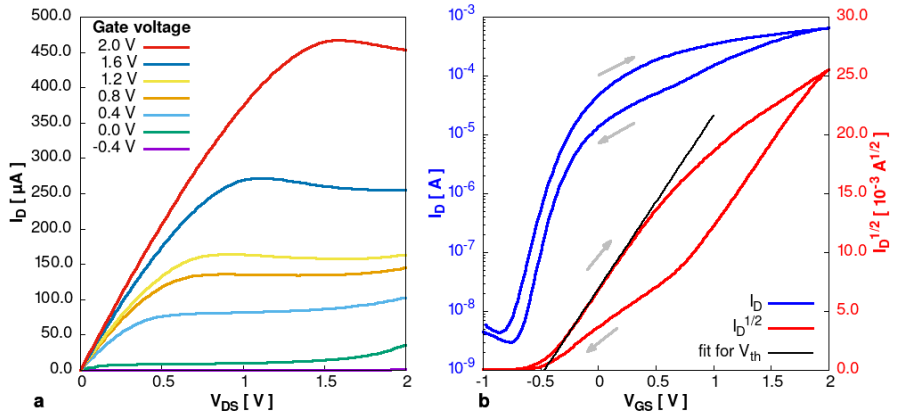

Figure A.6.: Device characteristics for a device with 5.0 % Cr-doping and two printed layers

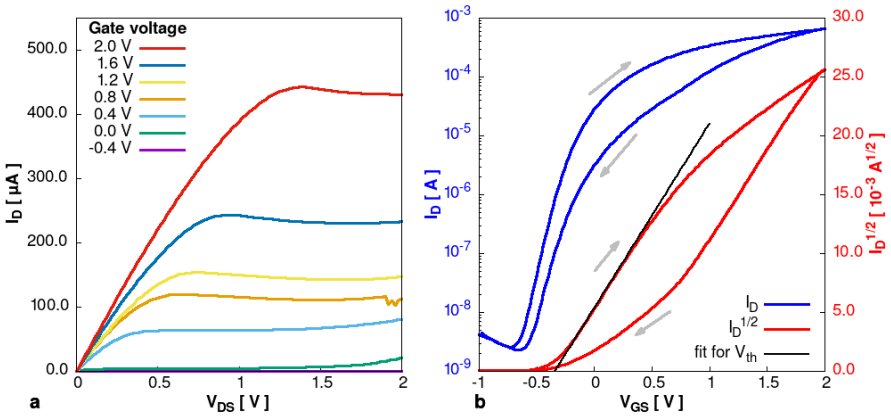

Figure A.7.: Device characteristics for a device with 7.5 % Cr-doping and two printed layers

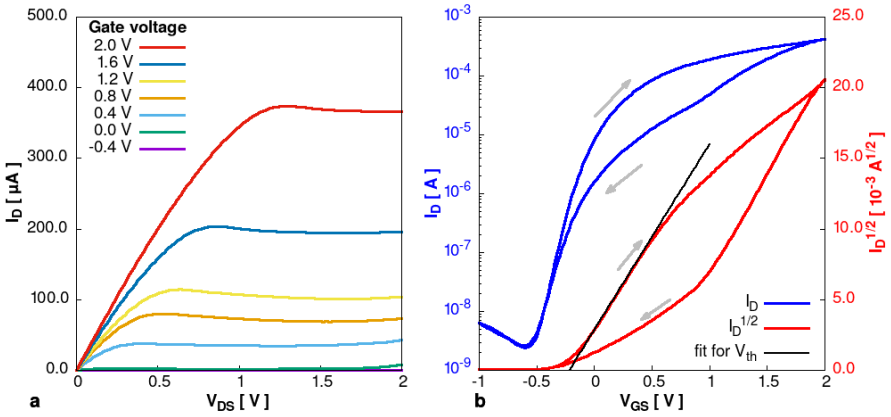

Figure A.8.: Device characteristics for a device with 10.0 % Cr-doping and two printed layers

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