Optimized Operation of Interleaved Motor Drive Inverter by means of Model Predictive Control

Optimierter Betrieb von parallelgeschalteten Wechselrichtern mit Interleaving-Drosseln unter Einsatz einer modellprädiktiver Regelung

Zur Erlangung des akademischen Grades Doktor-Ingenieur (Dr.-Ing.)
Genehmigte Dissertation von Morris Fuller aus Burgwedel
Tag der Einreichung: 29.11.2022, Tag der Prüfung: 08.03.2023

1. Gutachten: Prof. Dr.-Ing. Gerd Griepentrog
2. Gutachten: Prof. Dr.-Ing. Joachim Böcker
Darmstadt, Technische Universität Darmstadt

TECHNISCHE UNIVERSITÄT DARMSTADT

Electrical Engineering and Information Technology Department

Institute for Power Electronics and Control of Drives

Optimized Operation of Interleaved Motor Drive Inverter by means of Model Predictive Control
Optimierter Betrieb von parallelgeschalteten Wechselrichtern mit Interleaving-Drosseln unter Einsatz einer modellprädiktiver Regelung

Accepted doctoral thesis by Morris Fuller

Date of submission: 29.11.2022
Date of thesis defense: 08.03.2023

Darmstadt, Technische Universität Darmstadt

Bitte zitieren Sie dieses Dokument als:
URN: urn:nbn:de:tuda-tuprints-235751
URL: http://tuprints.ulb.tu-darmstadt.de/23575
Jahr der Veröffentlichung auf TUprints: 2023

Dieses Dokument wird bereitgestellt von tuprints,
E-Publishing-Service der TU Darmstadt
http://tuprints.ulb.tu-darmstadt.de
tuprints@ulb.tu-darmstadt.de

Preface

This doctoral dissertation is the result of my research activities at the Institute for Power Electronics and Control of Drives, TU Darmstadt. The work I carried out at the institute in fact began as early as 2014, which is the year I wrote my Bachelor thesis under the supervision of Kevin Hermanns and Gerd Griepentrog. Many educative student projects, interesting excursions, long meetings, intermittent frustration, delightful Christmas parties, a challenging Master thesis and my employment as research associate followed. I am thankful for the opportunities, advice and trust I experienced over this time. I also want to thank my former colleagues and Gerd Griepentrog for their time and effort they provided for ideas, guidance and feedback, as well as Joachim Böcker for co-supervising this dissertation. I sincerely hope it is visible that the quality of this thesis reflects the entirety of this input.

It appeared that over the time I was intensifying my research work and trying to deepen my focus, the ever-changing world was shifting up a gear. Severe diseases and losses in the family, but also the omnipresent COVID-19 pandemic and Russo-Ukrainian War are the tragic proof. Despite of this, I learned to even more so be grateful for what I have: My caring and supportive parents, the relieving grounding and refreshing positivity of my friends, and the help and patience of my lovely girlfriend. And I am looking forward to our youngest, little family member, whom I will soon be able to meet in person. Although it seems unlikely any of you will read the pages to follow, I dedicate this work to you.

With all my love, thank you.

Morris Fuller
Mainz, November 2022

Zusammenfassung

Die vorliegende Dissertation befasst sich mit den Herausforderungen und dem Nutzen von Interleaving-Techniken im Kontext von Wechselrichtern für Asynchronmaschinen. In diesem Zusammenhang werden Interleaving-Topologien vorgestellt und analysiert. Es wird eine detaillierte Modellierung der bevorzugten Topologie sowie der vorgesehenen Last durchgeführt. Die Entwicklungsschritte für einen modellprädiktiven Regler mit endlichem Kontrollsatz (finite control set model predictive control) werden mitsamt einer anschließenden simulativen Evaluierung präsentiert. Zu den Optimierungszielen des Reglers zählen dabei unter anderem eine minimale Regelabweichung, die Erhöhung des Wirkungsgrades, eine Verringerung der notwendigen Hardware-Ressourcen, sowie die Reduzierung von grundsätzlichen parasitären Effekten aufgrund der Wechselrichterspeisung. Die erreichbare Regelgüte wird mit konventionellen zwei-level Wechselrichtern verglichen. Eine echtzeitfähige Implementierung des Regelungsalgorithmus' wird auf einem Maschinenprüfstand ausgeführt, um die Korrektheit der Modellierung und des Regelungsdesigns zu verifizieren. Die Abweichungen zwischen Simulationsergebnissen und Messungen an diesem Prüfstand werden diskutiert. Ferner werden Richtlinien für zukünftige Verbesserungen des Reglers und der Hardware-Auslegung, sowie für weiterführende Forschungsschwerpunkte dargelegt.

Abstract

This thesis studies the challenges and benefits of interleaving in the context of drive inverter systems for induction machines. For this purpose, interleaved inverter topologies are introduced and analyzed. A detailed modeling of the favored interleaved inverter system in combination with the anticipated load is conducted. An optimal control strategy in form of finite control set model predictive control is developed and evaluated in simulation. Several optimization goals for the drive systems, such as control quality, efficiency in terms of losses and hardware effort, and reduction of undesirable side-effects owing to inverter-feeding are considered. The acquirable performance is compared to conventional two-level inverter realizations. A real-time controller implementation and hardware-based proof of concept is carried out. Deviations between simulation results and hardware measurements are discussed. Guidelines for optimized controller and hardware designs, as well as for future research topics are provided.

List of Symbols and Abbreviations

List of symbols

Symbol	unit	description
A, $\boldsymbol{A}$	mm^2,-	cross section, system matrix (state-space representation)
a	-	Steinmetz Equation parameter for frequency
$\boldsymbol{B}$	-	input matrix (state-space representation)
B	T	magnetic flux density
b	-	Steinmetz Equation parameter for flux density
$\boldsymbol{C}$	-	output matrix (state-space representation)
C	F	capacitance
c	-	conversion factor for equivalent torque tuning of MPCC and MPTFC
$\cos(\varphi)$	-	power factor
$\boldsymbol{D}$	-	feed-through matrix (state-space representation)
E	J	energy
f, $\boldsymbol{f}$	Hz, -	frequency, non-linear system function (state-space representation)
G, g, $\boldsymbol{g}$	-, - , -	transfer function, enumeration variable, arbitrary vector
$\boldsymbol{h}$	Hz	non-linear output function (state-space representation)
I, i, $\boldsymbol{i}$	A	current (Laplace domain), current, current vector
j	-	imaginary unit $\sqrt{-1}$
J, $\boldsymbol{J}$	-	cost function, set of cost functions
$\boldsymbol{K}$	-	substitution matrix
k	-, -, -	discrete time step / Steinmetz Equation parameter for scaling / coupling factor
L, l	H, - / mm	inductance, enumeration variable / length
M, m	H, -	mutual inductance, modulation factor
N, n	-, s^{-1} / -	filter length / prediction horizon / number of turns per winding, rotational speed
P	W	active power
Q	V A	reactive power
R, $\boldsymbol{R}$	Ω, -	resistance, rotation matrix
S, s, $\boldsymbol{s}$	V A, - , -	apparent power, slip, switch position
$\boldsymbol{sv}$	V	space vector
T, $\boldsymbol{T}$	N m	torque, set of predicted torques
$\boldsymbol{U}$	-	sequence of input variables (state-space representation)
u, $\boldsymbol{u}$	-	input variable, input vector (state-space representation)
V, v, $\boldsymbol{v}$	V	constant voltage / voltage (Laplace domain), voltage, voltage vector
$\boldsymbol{X}$	-	sequence of state variables (state-space representation)
x, $\boldsymbol{x}$	-	state variable, state vector (state-space representation)
$\boldsymbol{Y}$	-	sequence of output variables (state-space representation)
y, $\boldsymbol{y}$	-	output variable, output vector (state-space representation)
Z, z	Ω	impedance, pole pairs

Symbol	unit	description
α	-	α-component of orthogonal $\alpha\beta\gamma$-reference system
β	-, rad	β-component of orthogonal $\alpha\beta\gamma$-reference system / angle between reference frames
γ	-	γ-component of orthogonal $\alpha\beta\gamma$-reference system
δ	-	air gap
η	-	efficiency
θ	rad, $\mathrm{kg\,m^2}$	load angle, inertia
λ	-	weighting factor
μ	-, $\mathrm{kg\,m\,s^{-2}\,A^{-2}}$	relative electromagnetic permeability / vacuum permeability
ν	-	ordinal number of harmonics
ξ	-	enumeration variable
σ	-	leakage factor
τ	s	time constant / auxiliary variable for time integration
Φ, φ	Wb, rad	magnetic flux, phase angle between voltage and current
Ψ	V s	magnetic flux linkage
ω	$\mathrm{rad\,s^{-1}}$	angular frequency
$\boldsymbol{\mathcal{U}}$	-	one-step control set
$\boldsymbol{\mathcal{X}}$	-	one-step constraints set for state vector
$\boldsymbol{\mathcal{Y}}$	-	one-step constraints set for output vector

List of subscripts

Subscript (with exemplary variable, combinations occur frequently)	description
v_0	reference point
i_1	inverter 1
i_2	inverter 2
$i_{2\mathrm{L}}$	two-level
$i_{3\mathrm{L}}$	three-level
i_{a}	component of phase a
R_{ac}	ac quantity
i_{b}	component of phase b
v_{block}	quantity to be blocked
i_{c}, $\boldsymbol{A}_{\mathrm{c}}$	component of phase c, controller
L_{cable}	cable
i_{cap}	capacitor
T_{clk}	clock
R_{con}	connecting
P_{cu}	copper
i_{d}, Ψ_{d}	drawn inverter current, d-component of the dq-reference system
$i_{\mathrm{d}+}$	drawn inverter current for the upper dc-link rail
$i_{\mathrm{d}-}$	drawn inverter current for the lower dc-link rail
V_{dc}	dc quantity / quantitiy related to dc-link

Subscript (with exemplary variable, combinations occur frequently)	description
$J_{\mathrm{dv/dt}}$	$\mathrm{d}v/\mathrm{d}t$-effects
T_{e}	electromagnetic
l_{eff}	effective
$\boldsymbol{A}_{\mathrm{exact}}$	time discretization with Euler exact method
m_{f}	modulation factor
t_{fall}	fall
P_{fe}	iron
T_{hyst}	hysteresis
$G_{\mathrm{i}}(s)$	current
P_{im}	induction machine
P_{in}	input
P_{inv}	inverter
β_{k}	angle between stator ($\alpha\beta$) and field-aligned (dq) reference frame
R_{leg}	leg
P_{loss}	losses
R_{m}	magnetic
J_{magmode}	magnetization mode
v_{motor}	motor
P_{n}	rated or nominal
Ψ_{opt}	optimal
P_{out}	output
J_{ovv}	over-voltage
N_{p} / $\boldsymbol{f}_{\mathrm{p}}$	prediction / plant
R_{par}	equivalently in parallel
x_{partpred}	partial prediction
$\boldsymbol{A}_{\mathrm{plant}}$	real plant
i_{ph}	(arbitrary) phase
t_{prop}	propagation delay
Ψ_{q}	q-component of the dq-reference system
i_{r}, β_{r}	rotor, angle between stator ($\alpha\beta$) and rotor reference frame
t_{rise}	rise
i_{rms}	rms-value
i_{sat}	saturation
R_{ser}	equivalently in series
i_{s}, T_{s}	stator, sample time
f_{sw}	switching
i_{source}	source
J_{T}	torque
R_{w}	winding
B_{δ}	air gap
B_{ν}	ordinal number of harmonics
L_{σ}	stray value
J_{Ψ}	flux linkage
τ_{ω}	speed

List of superscripts

Superscript (with exemplary variable)	description
$\boldsymbol{s}^{\mathrm{abc}}$	vector in abc-reference system
$\boldsymbol{\Psi}^{\alpha\beta}$	vector in $\alpha\beta$-reference system
$\boldsymbol{\Psi}^{\mathrm{dq}}$	vector in dq-reference system
Ψ^*, τ^*	reference value, equivalent time constant
L'	value per unit of length / intermediate value for auxiliary calculations

List of abbreviations

Abbreviation	description
AC	**A**lternating **C**urrent
ADC	**A**nalogue to **D**igital **C**onversion
ANPC	**A**ctive **N**eutral **P**oint **C**lamped
ASIC	**Application S**pecific **I**ntegrated **C**ircuit
CCS	**C**ontinuous **C**ontrol **S**et
CPLD	**C**omplex **P**rogrammable **L**ogic **D**evice
CLB	**C**onfigurable **L**ogic **B**lock
DC	**Direct C**urrent
DSP	**D**igital **S**ignal **P**rocessor
EMI	**E**lectro**m**agnetic **I**nterference
FCS	**F**inite **C**ontrol **S**et
FFT	**F**ast **F**ourier **T**ransformation
FIFO	**F**irst **I**n **F**irst **O**ut
FPGA	**F**ield **P**rogrammable **G**ate **A**rray
FPU	**F**loating **P**oint **U**nit
GPU	**G**raphics **P**rocessing **U**nit
iGSE	**i**mproved **G**eneralized **M**odified **S**teinmetz **E**quation
IO	**I**nput **O**utput
IP	**Intellectual P**roperty
JTAG	**J**oint **T**est **A**ction **G**roup
LUT	**L**ook**u**p **T**able
MACC	**M**ultiply **Acc**umulate
MCU	**M**icro **C**ontroller **U**nit
MMPCC	**Modified M**odel **P**redictive **Current C**ontrol
MMPTFC	**M**odified **M**odel **P**redictive **Torque F**lux **C**ontrol
MOSFET	**M**etal **Oxide S**emiconductor **F**ield **E**ffect **T**ransistor
MPC	**M**odel **P**redictive **C**ontrol
MPCC	**M**odel **P**redictive **Current C**ontrol
MPTFC	**M**odel **P**redictive **Torque F**lux **C**ontrol
MSE	**M**odified **S**teinmetz **E**quation
NPC	**N**eutral **P**oint **C**lamped
PI	**P**roportional Integral
PWM	**P**ulse **W**idth **M**odulation

Abbreviation	description
RAM	**R**andom **A**ccess **M**emory
RMS	**R**oot **M**ean **S**quare
SoC	**S**ystem **o**n a **C**hip
TDD	**T**otal **D**emand **D**istortion
THD	**T**otal **H**armonic **D**istortion
UART	**U**niversal **A**synchronous **T**ransmitter **R**eceiver

Remarks for further notations

Notation	description
v	scalar variable or parameter
$\underline{v}$	complex variable or parameter
$\boldsymbol{v}$	vector variable or parameter
$\widetilde{\Psi}$	estimated variable
$\bar{\boldsymbol{A}}$	transformed matrix
$\|*\|$	absolute value of scalar / magnitude of complex value
$\|\|*\|\|_\infty$	ℓ_1-norm (or "taxicab metric")
$\|\|*\|\|_2$	ℓ_2-norm (or "Euclidean norm")

Contents

1. Introduction

1.1. Purpose of Thesis

Two-level DC/AC converters, otherwise referred to as two-level inverters, are an economical solution to implement variable speed drive systems for a wide range of consumer and industrial applications, such as electric vehicles, efficiency-driven pumps or compressors, machine tools, wind turbines etc. However, their suitability is limited by particular aspects, such as the chosen DC-link voltage and the power quality requirements of the load. In some cases, high DC-link voltages can be mastered by appropriate selection of power electronic components, i.e. high blocking voltage capability, or otherwise by a carefully designed voltage balancing via series connection of the power switches [1]. The improvement of output power quality can partially be achieved by certain modulation schemes [2] [3]. Further enhancements usually involve high switching frequencies and hence correlate with higher losses in the switching devices.

On the other hand, multilevel converters are an attractive solution to overcome these issues. By definition, they are able to provide $n > 2$ voltage levels for each of the implemented output terminals. The corresponding availability of a staircase waveform for its output voltage can, in the optimal case, exponentially decrease the distortions imposed on the load [4]. Further, $\mathrm{d}v/\mathrm{d}t$-stress on the load's insulation can be reduced substantially. Lastly, by choosing suitable topologies, the necessary blocking voltage of the power switches can be reduced by the factor of $1/(n-1)$ [5]. Popular multilevel inverter structures include diode clamped converters, flying capacitor converters and modular multilevel converters. Although all of these topologies have considerable advantages, they also entail specific drawbacks, e.g. the necessity of balancing the DC-link capacitors, the requirement of several isolated DC-sources, and generally the increasing control complexity with a rising number of voltage levels. It can therefore be a difficult task to select an optimal topology for the use case at hand.

In this work, the focus lies on low-voltage variable speed drive applications, consequently prioritizing high power quality, but also efficiency aspects over voltage withstand capabilities. Common multilevel topologies in this field are the I- or T-type three-level converters, which belong to the diode clamped category. They show a good trade-off between output quality, amount of components and computational control effort, making moderate to high switching frequencies feasible for control algorithms running in real-time.

Nevertheless, there is also another, less frequently encountered possibility of implementing three-level converters, namely interleaved converters. Generally speaking, a topology can be considered to be interleaved as soon as multiple functional units share a common DC-source or their output is provided to a common load, whereby the multiplicity of these units is not necessary for basic functionality. These interleaved structures appear many times in DC/DC converter applications. In this case, a multitude of inductors or filters are used to enhance the parallel, i.e. the interleaved operation, aiming for the minimization of output ripple and thereby also the load's harmonic losses by diligently tuned pulse patterns [6]–[8]. Similar features, including further benefits such as DC-link optimization, can also be achieved with interleaved three-phase DC/AC converters.

These introduced interleaved inverters are occasionally proposed in literature [9]–[16], but tend to be rather underrepresented in teaching and the scientific discussion, despite several advantages. The wider aim of this work therefore is to reiterate the benefits and to introduce modern control strategies, namely model predictive control, for this particular topology family. Concretely, the challenges and benefits are thereby to be analyzed in the context of low voltage variable speed drive applications.

1.2. Structure of Thesis

In order to establish a sound understanding for the family of interleaved inverter topologies, the main concepts and characteristics are provided in Chapter 2. Exemplary topology variations are discussed and evaluated by their suitability for drive inverter systems and under consideration of design effort.

A detailed modeling of the interleaved topology chosen for investigation is conducted in Chapter 3. The modeling is further expanded to the anticipated load for the inverter, which is a squirrel-cage induction machine. Any important aspects for controller design and its performance analysis are highlighted in preparation for the following chapters.

The optimal control principle of finite control set model predictive control (FCS-MPC) is introduced in Chapter 4. General terminology, design challenges and a short comparison with conventional control approaches for drive systems are addressed. Several FCS-MPC styles are developed and analyzed for induction machine control with a basic two-level inverter. The established principles are then transferred to the interleaved inverter system. Furthermore, several additional control aims such as the optimization of the DC-link, reduction of common-mode voltage, as well as minimization of inverter *and* machine efficiency are introduced, implemented and evaluated.

Concrete and verified approaches for the real-time implementation of the established control algorithm are provided in Chapter 5. Specifically, various techniques for computational resource efficiency are carried out for FPGA-based computational platforms.

In Chapter 6, the for verification purposes developed hardware setup is introduced. The collected experimental data is compared to simulation results, and reasons for deviations are discussed. The gained insights are formulated as guidelines for possible improvements of the hardware design.

Lastly, Chapter 7 gives a brief summary of the thesis and points out relevant aspects for future research.

2. Interleaved Topology

This chapter introduces the interleaved inverter topology that is being focused on in this work. It gives an overview of the system and describes the specific features of interleaved operation. Secondly, related topologies are presented, summarizing differences, advantages and drawbacks. It can be seen as compact guidelines for topology selection.

2.1. Overview of Investigated Interleaved Topology

The investigated topology consists of two two-level inverters that are fed by a common DC-source and DC-link capacitor bank. The electrical circuit in Figure 2.1 depicts the overall topology and introduces the nomenclature of the appearing electrical quantities within the system. The total number of unique switch positions amounts to $2^6 = 64$, as six half bridges with two switching states each can be combined. The capability of interleaving is achieved by a phase-wise parallelization via so-called interleaving chokes. In the following, a brief summary of the topology's properties is given.

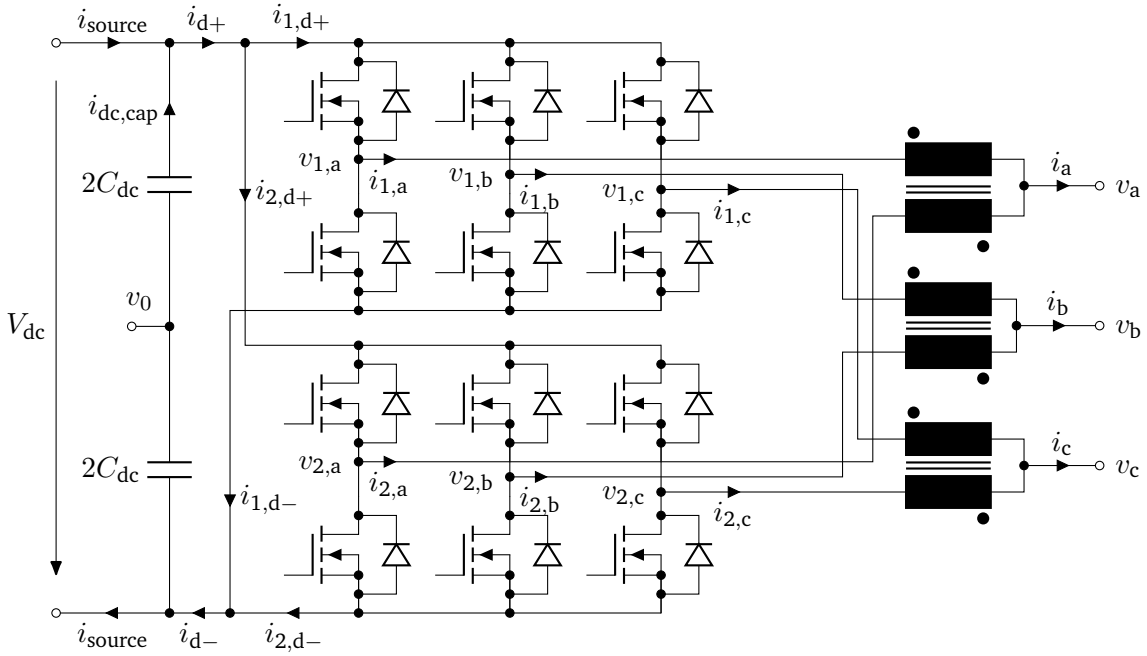


Figure 2.1.: Circuit diagram of interleaved inverter.

Effects on DC-link current and output current
The two two-level inverters in Figure 2.1 are in parallel operation. The currents drawn from the individual inverters are superimposed at the terminals of the DC-link capacitor bank. This gives the control designer the opportunity to realize compensating patterns for $i_{1,\mathrm{d}+}$, $i_{2,\mathrm{d}+}$ and $i_{1,\mathrm{d}-}$, $i_{2,\mathrm{d}-}$, securing a lowered stress on the DC-source and the DC-link. Secondly, the parallel inverters share a common output terminal for each phase. The leg currents at the respective junctions add up to the output phase currents. As shown in Chapter 4, the leg currents can be controlled toward a maintainable, arbitrary contribution of the output current. This enables features such as current sharing for minimal conduction losses in the power switches, as well as shifting losses between them.

Effects on inverter leg currents
The individual chokes of each phase are wound in a manner that the leg currents' flux contributions in the magnetic core are compensating each other. Equal current loading of the windings combined with an ideal coupling, i.e. the absence of any leakage, leads to a complete cancellation of magnetic flux. However, unequal leg currents imply an additional current flow from one inverter to the other, further referred to as the cross-currents $\boldsymbol{i}_1 - \boldsymbol{i}_2$ (or $i_{1,\mathrm{ph}} - i_{2,\mathrm{ph}}$ for a specific phase). These cross-currents experience a larger impedance, since they lead to an uncompensated magnetization of the core material.[1] Any interleaved states, i.e. switching states where at least one pair of the parallelized half bridges switch towards opposing DC-link potentials, will result in a change of the corresponding cross-current. As long as the chokes do not saturate, the rate of change is approximately proportional to the mutual inductance of the choke and the DC-link voltage. Regular switching states, where both two-level inverters have identical switch positions, will maintain the cross-currents' magnitudes. The cross-currents have to be monitored phase-wise in order to detect and prevent any saturation in the chokes. Lastly, it is noteworthy that the cross-currents $\boldsymbol{i}_1 - \boldsymbol{i}_2$ can have a significant common-mode component. It appears as circular current, flowing from one two-level inverter to the other via the interleaving chokes (cp. Section 3.1.3).

Effects on inverter output voltages
The interleaving chokes also affect the three-phase voltage output of the interleaved inverter.

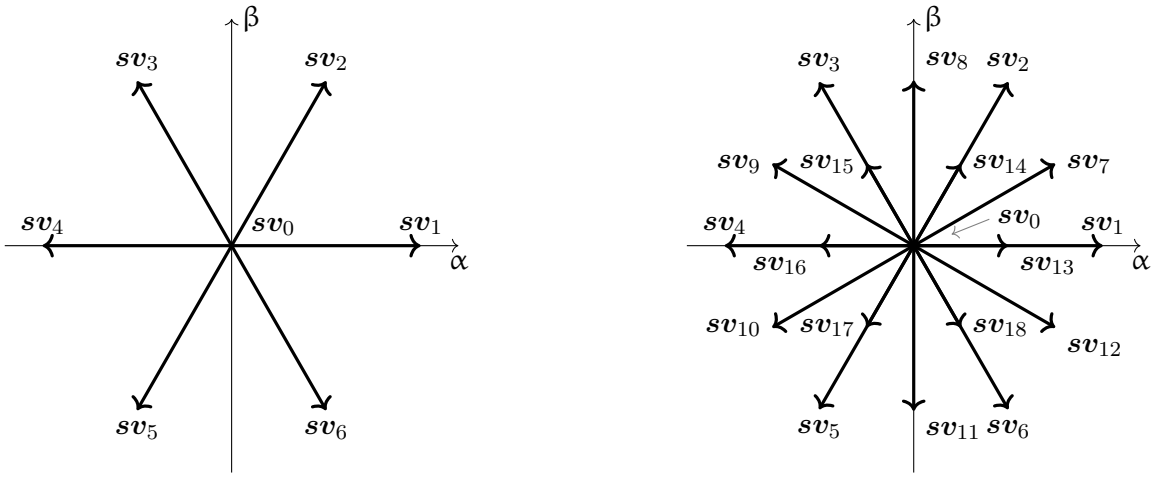


Figure 2.2.: Enumerated unique voltage space vectors of a two-level (left) and a three-level three-phase inverter (right) in the alpha-beta plane.

[1] The same effect is widely used in common-mode chokes for EMI suppression.

If identical switching states for both paralleled inverters are used, the achievable voltage space vectors are the same as for a simple two-level inverter. On the other hand, the chokes have an averaging effect if interleaving states are applied. This leads to $v_{\mathrm{ph0}} \approx {}^1/_2 \cdot \left(v_{1,\mathrm{ph0}} + v_{2,\mathrm{ph0}}\right)$. The overall system therefore essentially provides a three-level inverter with the (approximate) output-to-midpoint voltages $v_{\mathrm{a0}}\,,\ v_{\mathrm{b0}}\,,\ v_{\mathrm{c0}} \in \{-V_{\mathrm{dc}}/2\,,\ 0\,,\ V_{\mathrm{dc}}/2\}$. The resulting availability of output space vectors in the alpha-beta plane[2] is shown in Figure 2.2 and is identical to a three-phase, three-level topology. The entire set of these voltage space vectors is acquirable for load control, i.e. the set is unconstrained with respect to saturation prevention of the interleaving chokes. This conjuncture can be explained by the redundancy of switching state compositions that lead to identical space vectors, but with opposing impacts on the evolution of cross-currents (cp. Table A.1).

2.2. Related Interleaved Topologies

There are several other interleaved topologies described in the literature, which shall briefly be addressed here. The often minor, but distinct modifications alter at least one of the properties sketched in Section 2.1. The aim of this section is to deepen the understanding of interleaved topologies, to increase the knowledge of their capabilities and to ease a hypothetical decision making with respect to topology selection.

Uncoupled interleaving chokes with inverter parallelization
In contrast to the principle of coupled interleaving chokes, also uncoupled chokes can be realized for the parallelization of the respective halfbridges [17]. The main implication of this modification is the absence of compensation effects for leg current components that flow towards the load, as depicted in Figure 2.3.

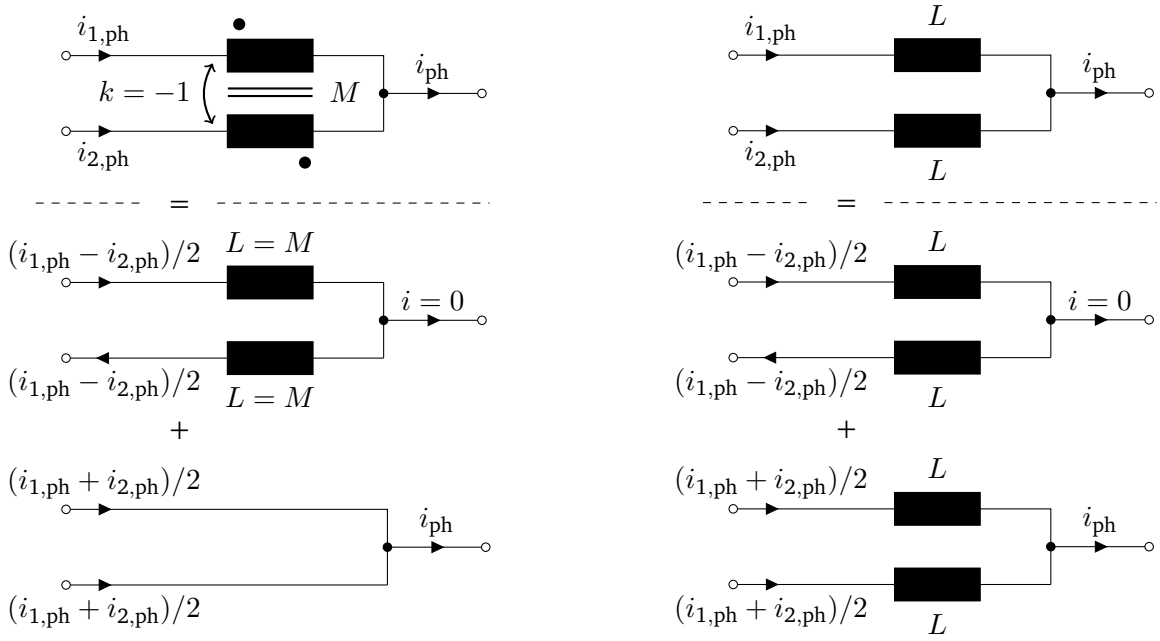


Figure 2.3.: Comparison of coupled and uncoupled interleaving choke (top), separated into cross-current (middle) and load current contribution (bottom).

[2]The alpha-beta plane is a commonly used reference system for symmetrical three-phase systems. It is helpful for the separation or (if negligible) elimination of common-mode or zero-sequence components and can be achieved by applying the so-called Clarke transformation (cp. Section 3.1.1).

In fact, this can be interpreted as a very positive influence, since the additional inductance usually leads to an attenuated total harmonic distortion (THD) of the load current. Nevertheless, the transient performance for load control may get strongly impaired for the same reason.

Regarding saturation constraints, the uncoupled choke has to be designed for the anticipated maximum leg currents $\left(B_{\text{sat}} \leftrightarrow L \cdot \max\left(|i_{1,\text{ph}}|, |i_{2,\text{ph}}|\right)\right)$. Therefore, under the assumption of shared load currents for the paralleled inverters, the chokes have to withstand a magnetization current of at least $i_{\text{ph}}/2$. On the other hand, for the coupled case the load-*independent* cross-currents should be considered $\left(B_{\text{sat}} \leftrightarrow 2M \cdot \max\left(|i_{1,\text{ph}} - i_{2,\text{ph}}|/2\right)\right)$. Hence, the coupled chokes can be designed with a higher degree of freedom.

Note that the modification of uncoupling the interleaving chokes can performed not only with the main topology of Section 2.1, but also to any of the following discussed topologies. In order to avoid repetition, this aspect is considered to be concluded and will not further be mentioned throughout this chapter.

Interleaving chokes with multiple inverter parallelization
In the previous sections, the number of parallel inverters was assumed to be specifically two. However, the amount of parallel branches is in principle not limited, i.e. may be increased to any arbitrary number n [17]. The phase output to midpoint voltages continue to follow the averaging effect of the chokes: $v_{\text{ph0}} \approx {}^{1}/_{n} \cdot \left(v_{1,\text{ph}} + v_{2,\text{ph}} + ... + v_{\text{n,ph}}\right)$. This implies $n+1$ voltage levels for n parallel inverters. Note that redundant switch positions exists for $|v_{\text{ph0}}| < |{}^{V_{\text{dc}}}/_{2}|$. If the overall converter shall be implemented with uncoupled chokes, the parallelization can be achieved straightforwardly by providing the individual chokes for each half bridge's output. Regarding coupled interleaving chokes, several variants exist.

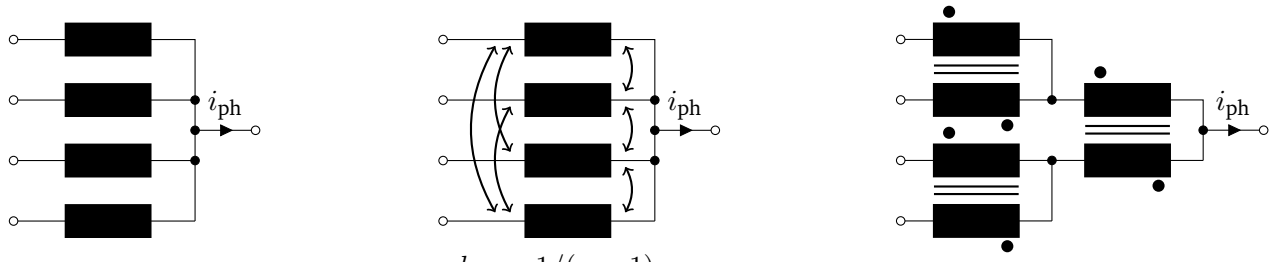


Figure 2.4.: Comparison of uncoupled inductors, multiple core leg coupling and "whiffletree" coupling [11] configuration for four parallel halfbridges.

An obvious solution are multiple core legs. However, while three-leg cores are widely and five-leg cores occasionally offered due to their usage for three-phase systems (e.g. transformers), higher-leg versions are typically not an "off the shelve" solution. Further, unwanted asymmetries between the legs may be increased because of unequal magnetization paths to neighboring legs. As a resolution, various configurations based on two-leg cores are proposed in [11]. One possible configuration, as well as the uncoupled and multiple core leg case are exemplarily sketched in Figure 2.4.

With respect to the DC-link optimization, a higher number of paralleled branches expand the amount of superimposed inverter currents that add up to the overall DC-link current i_{d}. This is a positive feature: The instantaneous values of i_{d} can be selected in a finer manner, allowing an enhanced minimization of the DC-link

capacitor current.

Interleaving chokes without inverter parallelization
The interleaving chokes do not necessarily have to be used for parallelization of two inverters. Instead, they can be placed between the top and bottom power switch of a single halfbridge [12]. Figure 2.5 shows an exemplary phase of such kind of inverter.

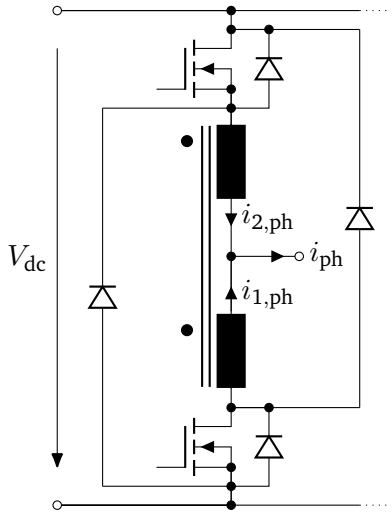


Figure 2.5.: Circuit diagram of coupled interleaving choke without inverter parallelization for one phase

Although intuitively expected, the component count of power semiconductor devices does not automatically decrease by the factor of two. This is due to the repositioning of the anti-parallel freewheeling diodes, which makes the inherent body diodes of MOSFETs superfluous. The same applies to the often integrated power diodes in IGBT modules. Consequently, the additional placement of power diodes is required.

Despite a lowered amount of actively controlled switches, the number of unique and allowed switch positions still adds up to $4^3 = 64$ for a three-phase system. The reason for this are two additional states for each of the phases, namely having both power switches in the on- or in the off-state simultaneously. While the concurrent on-state is normally not permitted (short circuit of the DC-link), it represents the magnetizing state for the chokes in this topology. Hence, a dead-time implementation is not needed here. Secondly, the usually undesirable case of simultaneous off-states (uncontrolled output voltage) leads to an active demagnetization of the chokes for this configuration.

Based on the constellation of switches in Figure 2.5, the magnetizing current in the choke can only have one polarity and always flows from the top winding to the bottom winding [18]. It can be translated to a magnetization bias $i_{\mathrm{bias,ph}} = i_{1,\mathrm{ph}} - i_{2,\mathrm{ph}} > 0$. In order to avoid any discontinuous operation within a switching cycle, this DC-magnetization current should have some specific margin to the completely demagnetized state. On the other hand, a large bias is unfavorable for the core design, e.g. increased saturation limits and anticipated magnetizing losses. To handle this issue, a trade-off has to be performed between additional hardware effort[3] or losses on the one side and higher controller and/or modulator complexity on the other side. Lastly, the currents for the magnetization bias of every phase add up to a circulating current, which may

[3] E.g. the placement of permanent magnets within the chokes to compensate the bias of current-induced magnetic flux.

increase the overall losses (cp. Section 3.1.3).

The property of a three-level output per phase is maintained. Therefore, also the available space vectors as shown in Figure 2.2 (right) are valid, including their inherent redundancy with respect to switch positions due to Clarke's transformation. However, the topology provides a limited optimization potential for the DC-link: In consideration of the required magnetization bias of the chokes, the potential is expected to be lower than for the parallel structure.

Interleaving chokes combined with other multilevel structures
The inverter's output power quality can be improved with an augmented number of voltage levels. This is achievable not only with interleaved inverter parallelization, but also with any other multilevel topology. In fact, both of these approaches can be combined with each other to achieve superior performance. As an example, two I-type multilevel converters can be interleaved with coupled inductors, as done in [13] and shown for one phase in Figure 2.6.

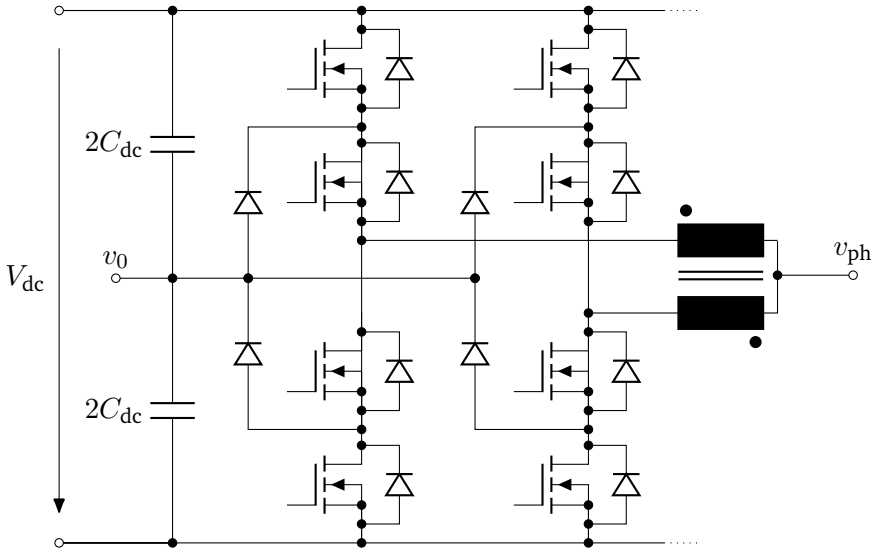


Figure 2.6.: Circuit diagram of coupled interleaving choke with I-type inverter parallelization for one phase

The three acquirable output voltages of the I-type halfbridges' are averaged via the interleaving chokes, resulting in the set $\{-V_{\mathrm{dc}}/2, -V_{\mathrm{dc}}/4, 0, V_{\mathrm{dc}}/4, V_{\mathrm{dc}}/2\}$ for the overall converter phase output. Similarly to the solely interleaved topology, redundancies regarding the switch positions exist for $|v_{\mathrm{ph0}}| < |V_{\mathrm{dc}}/2|$. On the other hand, next to the saturation limitations of the chokes this topology also requires a balancing of the DC-link. If the latter is not provided by appropriate voltage sources or an additional circuitry, the balancing has to be implemented in the controller or pulse-width modulation (PWM) scheme, which obviously adds to its complexity. Further, a PWM-based balancing decreases the redundancy of switch positions for additional optimization goals, e.g. presumably deteriorates the capability of DC-link current minimization.

Concluding thoughts
The previously addressed topologies or modifications are by far not the only possibilities to implement interleaving. Some papers propose a shared DC-link for two inverters which are connected to independent loads [19] [20], while in [21] [22] two-segmented, three-phase systems are considered. Secondly, the DC-link optimization can be improved also by other measures. For example, the number of phases can be risen

to any desired amount that is suitable for the load [14]. Similarly to an increased number of parallel converters, a higher count of phases provides better performance for minimizing the DC-link capacitor current [23].

In conclusion to the presented topologies, several configurations with unique advantages and drawbacks exist. Regarding the aspects of:

- Strong performance for load control (steady-state and transient)
- DC-link optimization potential
- Manageable hardware effort
- Real-time feasibility of non-linear, optimal controllers at high sampling rates

the main topology of Section 2.1 shows a good trade-off and is therefore going to be focused on for the remaining part of this thesis.

3. Mathematical Model

In this chapter, the mathematical model of the interleaved inverter system from Section 2.1 will be derived and analyzed. Moreover, the modeling of induction machines as anticipated load is recapitulated, paying special attention to effects associated with inverter-fed drives. The chapter in its whole is the basis for the design of optimal model predictive controllers, which will be introduced in Chapter 4.

3.1. Interleaved Inverter

The mathematical model of the four subsystems DC-link, two-level inverter, interleaving choke and load is provided in this section. In addition, the overall model is generated by appropriate substitutions across the subsystem models. It is given in the state-space representation, which can conveniently be used as prediction model for the model predictive controller.

3.1.1. Two-Level Inverter

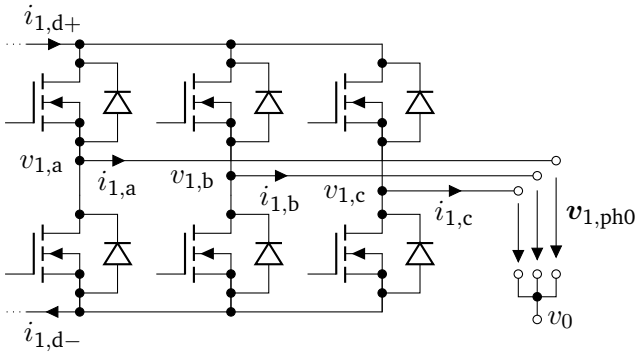


Figure 3.1.: Circuit of the (arbitrarly chosen) first two-level three-phase inverter.

Control signals
From a control point of view, the (arbitrarily chosen) first two-level inverter translates the logic signals $s_{1,\mathrm{ph}} \in \{0, 1\}$ for each half bridge (i.e. phase) into respective output potentials $v_{1,\mathrm{ph}}$. Each logic signal controls the half bridge in a complementary manner, e.g. $s_{1,\mathrm{ph}} = 1$ turns on the upper MOSFET and turns off the lower one. A turn-on delaying dead-time is implemented in order to avoid short circuits during current commutation. The output potentials are directly linked to the output voltages to DC-link midpoint, i.e. $v_{1,\mathrm{ph0}} \in \{-V_{\mathrm{dc}}/2, V_{\mathrm{dc}}/2\}$.[1]

[1] Under negligence of any voltage losses in the switches.

Voltage space vectors

Going through all $2^3 = 8$ possible switch positions and by applying the Clarke transformation given in Equation (3.1), the available voltage space vectors in the $\alpha\beta$-plane can be derived.

$$\boldsymbol{T}_{\mathrm{c},3} = {}^2\!/_3 \cdot \begin{pmatrix} 1 & -{}^1\!/_2 & -{}^1\!/_2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ {}^1\!/_2 & {}^1\!/_2 & {}^1\!/_2 \end{pmatrix} \tag{3.1}$$

$$\boldsymbol{v}_1^{\alpha\beta\gamma} = T_{\mathrm{c},3} \cdot \boldsymbol{v}_1^{\mathrm{abc}} \tag{3.2}$$

$$\boldsymbol{T}_{\mathrm{c},2} = {}^2\!/_3 \cdot \begin{pmatrix} 1 & -{}^1\!/_2 & -{}^1\!/_2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{pmatrix} \tag{3.3}$$

$$\boldsymbol{v}_1^{\alpha\beta} = T_{\mathrm{c},2} \cdot \boldsymbol{v}_1^{\mathrm{abc}} \tag{3.4}$$

In Eq. (3.2), the inverter voltages are transformed to the orthogonal $\alpha\beta\gamma$-reference system[2]. The advantage of this transformation is the fact that $v_{1,\gamma}$ represents the zero-sequence or common-mode component. The separation of the common-mode share can often be helpful for analysis, as shown in the DC-link modeling in Section 3.1.3. In many cases, the zero-sequence can even be neglected completely. An example is the common-mode current of orderly operated multi-phase systems with unconnected star point (i.e. electrical machines, transformers etc.), where $\sum_{\mathrm{ph}} i_{\mathrm{ph}} = 0$ holds. If the common-mode current remains zero at any given time, the common-mode voltage does not have to be considered for load control either[3]. The reduced transform $\boldsymbol{T}_{\mathrm{c},2}$ can then be applied, decreasing the later on defined control problem by one dimension.

Figure 3.2 depicts the space vectors in the orthogonal $\alpha\beta$-plane for two-level inverters, giving also the size of the spanning hexagon in terms of the DC-link voltage V_{dc}. Any reference space vector within this hexagon can be reproduced by appropriate PWM methods.

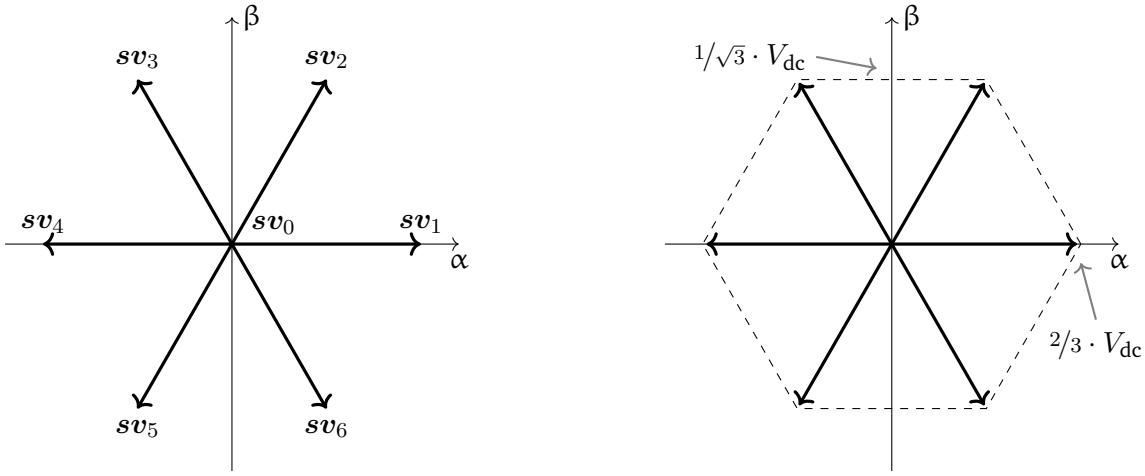


Figure 3.2.: Enumerated unique space vectors of a two-level three-phase inverter in the alpha-beta plane (left) and the size of the spanning hexagon (right).

[2]The superscripts identify the reference system of the respective vector

[3]Due to parasitic paths, a comparably small common-mode current in fact can circulate between the load and inverter whenever the common-mode voltage is of a non-zero waveform. The according implications are discussed in more detail in Section 3.2.4.

If $\boldsymbol{T}_{\mathrm{c},2}$ can be applied to the respective system, the resulting vectors are often interpreted as complex variables, e.g. $\boldsymbol{v}_1^{\alpha\beta} = \underline{\boldsymbol{v}}_1^{\alpha\beta} = (v_{\alpha,1} \quad \mathrm{j}v_{\beta,1})^{\mathrm{T}}$. This interpretation is generally valid and can be very valuable for future derivations that contain derivatives (cp. Section 3.2.1).

Operation modes of inverter

The magnitudes of the inverter's output voltage and current, $\boldsymbol{v}_1^{\mathrm{abc}}$ and $\boldsymbol{i}_1^{\mathrm{abc}}$, as well as the phase difference φ between these quantities,[4] define the inverter's active and reactive output power P and Q at a given frequency (e.g. fundamental frequency or harmonics). The apparent power $|S|$ is the magnitude of the complex power $S = P + \mathrm{j} \cdot Q = \sum_{m \in \{\mathrm{a,b,c},\}} v_{1,m} \cdot i_{1,m}$. Due to the relation $|S| \cdot \cos(\varphi) = P$, the factor $\cos(\varphi)$ is often referred to as *power factor* when investigating the fundamental power.

While the inverter's output current is often specified by the operation mode of the load (e.g. in the case of ohmic-inductive loads, such as induction machines), the magnitude and phase of the output voltage is influenced directly by the switching actions of the inverter. For this reason, the operating conditions of the inverter are considered to be dependent on the factors $\cos(\varphi)$ or φ, and m_{f}, the latter being the modulation factor. It describes the relation $m_{\mathrm{f}} = {}^{v_{\mathrm{ph0}}}/_{(V_{\mathrm{dc}}/2)}$, i.e. the amplitude of the phase output voltage to half of the DC-link's voltage level. It is an element of the interval $m_{\mathrm{f}} \in \{0, {}^{2}/_{\sqrt{3}}\}$ in case of linear modulation. High modulation factors therefore imply high output voltage and in tendency higher apparent power. On the other hand, the power factor gives the relation between active and reactive power. For example, a power factor of $\cos(\varphi) = -1$, $\cos(\varphi) = 0$, $\cos(\varphi) = 1$ describes the inverter is supplying active power towards the DC-link, supplying / consuming solely reactive power, supplying active power towards the output, respectively.

Transistor model

The equivalent MOSFET and body diode circuit of Figure 3.3 represent the static on- and off-behavior of the device. While high conductivity is ensured in the on-state due to a low R_{on}, the power switch's (voltage-dependent) output capacitance C_{oes} allows (strongly reduced) current flow during the static off-state. Irregardless of the MOSFET's state, the body diode generally remains available for potential current flow.

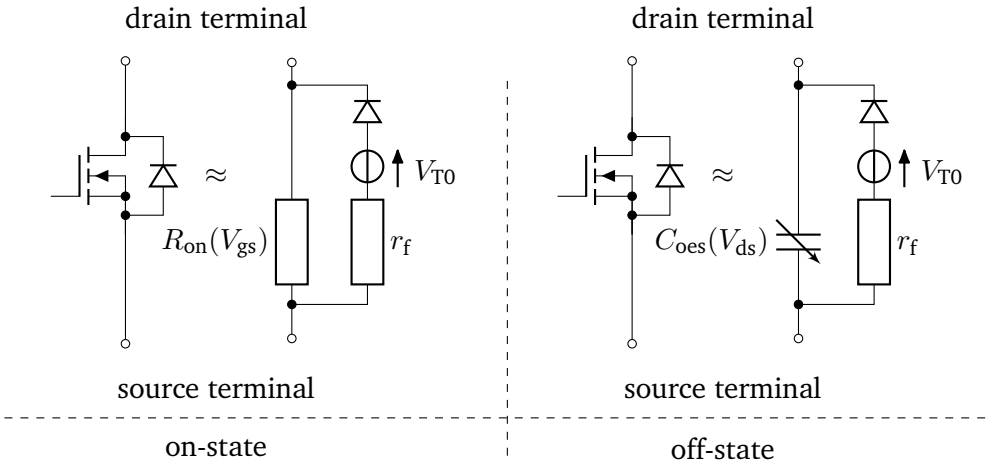


Figure 3.3.: Typical MOSFET model in the on-state (left) and in the off-state (right).

[4] The definition of the phase difference relies on harmonic signals. If multiple harmonics are present, the consideration of all the appearing frequencies has to take place. Alternatively, definitions for the active and reactive power exist also in the time domain, e.g. $P_{\mathrm{av}} = \frac{1}{T} \int_0^T \boldsymbol{v}_1^{\mathrm{abc}}(t) \cdot \boldsymbol{i}_1^{\mathrm{abc}}(t)\,\mathrm{d}t$.

Being a unipolar device, the MOSFET is capable of conducting current in forward (drain to source) and backward direction (source to drain) when turned on. Under regular operating conditions, the conductivity of the on-state MOSFET can be assumed to be substantially larger than of the body diode, i.e. the current will almost entirely flow through the closed transistor channel. This property is going to be exploited by the control algorithm, hence the body diode will merely be used for the short dead-time interval during commutation and can be neglected for the remaining switching cycle.

Commutation model
Depending on the switching signals $s_{1,\text{ph}} \in \{0, 1\}$, either the top or the bottom MOSFET of a halfbridge is active. The transition – further referred to as commutation – between these states usually implies switching losses, since the MOSFETs turn on or turn off within a finite time, being exposed to a respective current and voltage drop. These losses are roughly proportional to the DC-link voltage V_{dc} (switched voltage) and the drain-source current (switched current) [24]. Two exemplary commutations are given in Figure 3.4. As it can be seen in the figure, the state of the active MOSFET (forward conducting or backward conducting) also determines whether turn-off or turn-on losses are occurring when it is being switched[5]. This aspect is important for precise loss models, since the dissipated energy generally differs for turn-on and turn-off activity. Concretely, the commutation from the diode towards the forward-conducting MOSFET (bottom-right in Figure 3.4) has to be considered as a ”hard” commutation that dissipates more energy, and even more so includes reverse-recovery losses of the diode.

The specific transient turn-on and turn-off behavior of the semiconductors is explicitly not considered by Figure 3.4. More accurate models that resemble the transient characteristics[6] are given in [5]. They can be specifically helpful for the hardware design, e.g. for carrying out trade-offs with respect to fall and rise time (tunable via external gate resistors), output current capability of the gate driver, necessary blocking voltage of the switches etc. However, the integration of the concrete transient behavior in the system model does not bring any significant benefit for a predictive controller design: Its outputs are the switch positions per se, therefore their characteristics cannot be optimized by the control algorithm. Nevertheless, it is possible and further also expedient to implement look-up tables or curve fitting functions for the turn-on and turn-off losses of the switching devices, e.g. $E_{\text{on}}(i_{\text{drain}}, V_{\text{dc}})$ and $E_{\text{off}}(i_{\text{drain}}, V_{\text{dc}})$. With this information, the control actions of the model predictive controller can be suited to purposes such as minimizing inverter losses [25] or loss balancing among the switches (cp. Chapter 4).

[5]The case distinction in Figure 3.4 in fact lacks in generality, since the turn-off commutation during the dead-time (top-left of the figure) only applies for sufficiently high currents and/or dead-times. In any other case, the charges of the parasitic capacitances of the MOSFETs are not relocated to enable the conduction of the anti-parallel diode. The subsequent turn-on commutation is then not happening lossless anymore, but however still with strongly reduced losses.

[6]These models usually include all of the (voltage-dependent) junction capacitances of the MOSFETs, revers-recovery characteristics of the diode and the properties of the gate driving circuitry.

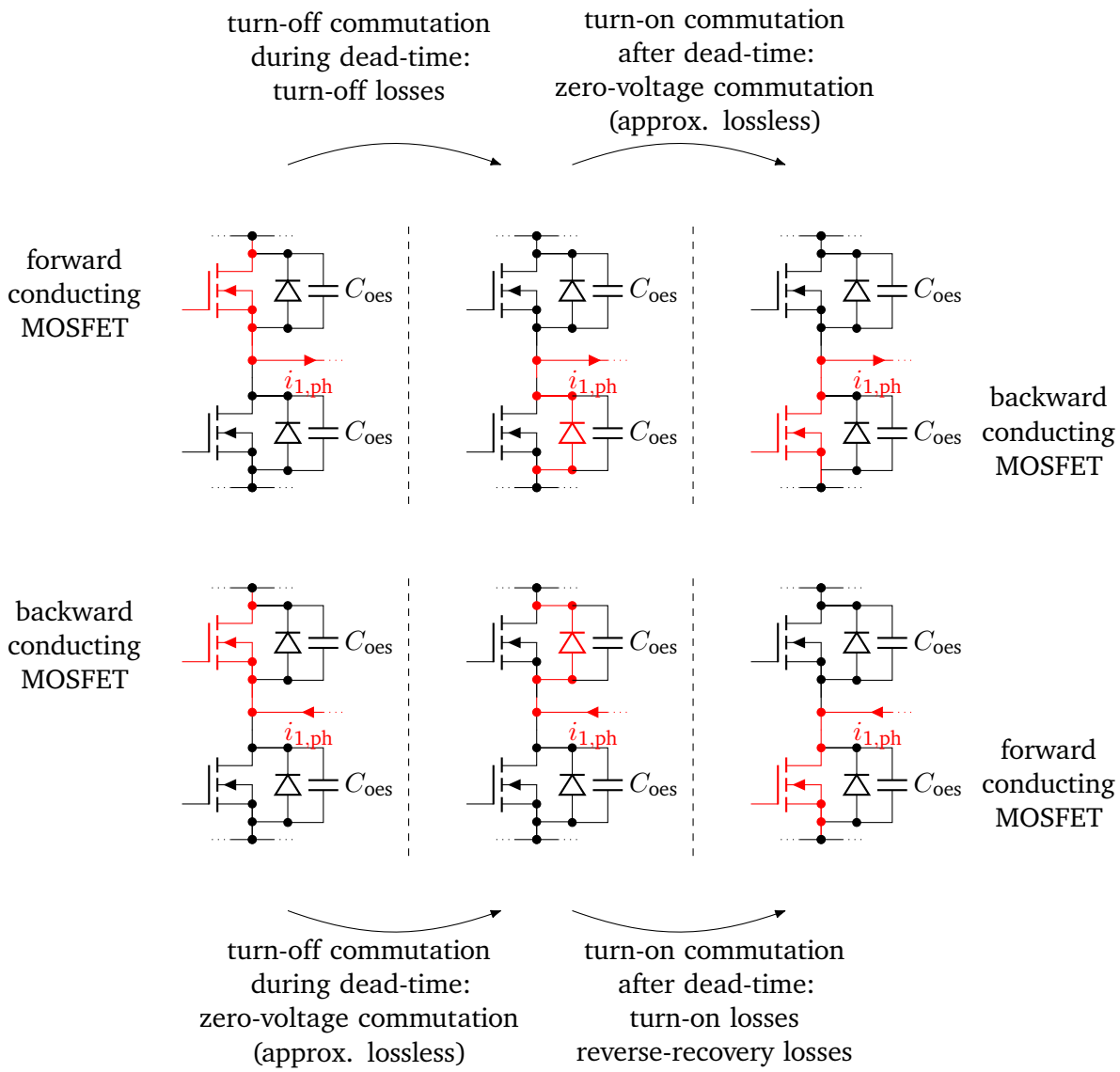


Figure 3.4.: Sequence of commutations within a halfbridge, depending on output current direction and the according current path (marked in red).

Drawn inverter current

The logic signals determine the contribution of the half bridges' leg currents $i_{1,\mathrm{ph}}$ to the respective inverter current $i_{1,\mathrm{d}+}$ and $i_{1,\mathrm{d}-}$.

$$v_{1,\mathrm{ph0}} = \begin{cases} +V_{\mathrm{dc}}/2 & \text{if} \quad s_{1,\mathrm{ph}} = 1 \\ -V_{\mathrm{dc}}/2 & \text{if} \quad s_{1,\mathrm{ph}} = 0 \end{cases} \tag{3.5}$$

$$i_{1,\mathrm{d}+} = +\sum_{\mathrm{ph}} s_{1,\mathrm{ph}} \cdot i_{1,\mathrm{ph}} = i_{1,\mathrm{d}-} \tag{3.6}$$

$$i_{1,\mathrm{d}-} = -\sum_{\mathrm{ph}} \bar{s}_{1,\mathrm{ph}} \cdot i_{1,\mathrm{ph}} = i_{1,\mathrm{d}+} \tag{3.7}$$

In the case of partly inductive loads (e.g. induction machines), the currents $i_{1,\mathrm{d}+}$, $i_{1,\mathrm{d}-}$ are highly dependent on the inverters' switch positions, as they modulate the rather sluggishly behaving output currents. It is noteworthy that Eq. (3.7) holds for every given switch position if, and only if, the output currents are common-mode free. This can be explained by interpreting the inverter (including its output terminals that add up to the common-mode component) as a large junction for currents. The conjuncture can also be proven formally as follows:

$$\begin{aligned} &s_{1,\mathrm{a}} i_{1,\mathrm{a}} + s_{1,\mathrm{b}} i_{1,\mathrm{b}} + s_{1,\mathrm{c}} i_{1,\mathrm{c}} = -\bar{s}_{1,\mathrm{a}} i_{1,\mathrm{a}} - \bar{s}_{1,\mathrm{b}} i_{1,\mathrm{b}} - \bar{s}_{1,\mathrm{c}} i_{1,\mathrm{c}} \\ &\big(s_{1,\mathrm{a}} + \bar{s}_{1,\mathrm{a}}\big) i_{1,\mathrm{a}} + \big(s_{1,\mathrm{b}} + \bar{s}_{1,\mathrm{b}}\big) i_{1,\mathrm{b}} + \big(s_{1,\mathrm{c}} + \bar{s}_{1,\mathrm{c}}\big) i_{1,\mathrm{c}} = 0 \\ &i_{1,\mathrm{a}} + i_{1,\mathrm{b}} + i_{1,\mathrm{c}} = 0 \quad \blacksquare \end{aligned} \tag{3.8}$$

3.1.2. Interleaving Chokes

General equivalent circuit of a real inductance
Like any other real component, inductors have certain parasitics that can be taken account of in an equivalent circuit. For such purpose, a basic model is given in Figure 3.5. The parameters introduced within this figure shall be described briefly in the following. The explanations are based on [26]. Exemplary ferrite core material properties can be extracted from [27].

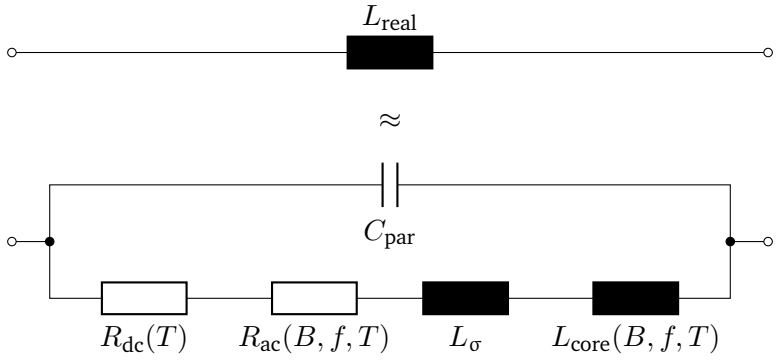


Figure 3.5.: Typical equivalent circuit of a real inductor.

- $L_{\mathrm{core}}(B,f,T)$: Actual inductance of the inductor. If magnetic cores are used, its value and its impedance can be approximated by (3.9) and (3.10), respectively:

$$L_{\mathrm{core}}(B,f,T) \approx \frac{\mu_0 \cdot \mu_{\mathrm{r}}'(B,f,T) \cdot A_{\mathrm{eff}} \cdot N^2}{l_{\mathrm{eff}}} = \frac{N^2}{R_{\mathrm{m,core}}(B,f,T)} \tag{3.9}$$

$$X_{\mathrm{core}}(B,f,T) \approx \omega \cdot L_{\mathrm{core}}(B,f,T) \tag{3.10}$$

  where A_{eff} and l_{eff} is the effective cross-section and path length of the core, N is the number of windings and μ is the permeability. The latter is split up into the permeability of free space (μ_0) and the real part of the complex relative permeability ($\underline{\mu}_{\mathrm{r}} = \mu_{\mathrm{r}}' - j \cdot \mu_{\mathrm{r}}''$). The parameter μ_{r} is dependent on several factors,

such as temperature of the core, the present magnetic flux and frequency of the magnetizing current. All of the geometric and material specific parameters can be summed up to the magnetic resistance / so-called reluctance $R_{\text{m,core}}$, as done in (3.9).

- $R_{\text{ac}}(B, f, T)$: AC-resistance of the inductance. It can be split up in two categories:
  1. AC-resistance of windings ($R_{\text{ac,w}}$): It generally increases with higher frequencies because of the Skin and the Proximity effect.
  2. AC-resistance of core ($R_{\text{ac,m}}$): This equivalent resistance corresponds to the core losses appearing due to eddy currents and magnetic hysteresis. The value for this component of R_{ac} can be determined in analogy to (3.10), but with the replacement $\mu_{\text{r}}' \rightarrow \mu_{\text{r}}''$. Note that the frequency dependency of $R_{\text{ac}}(B, f, T)$ does not only result from μ_{r}'', but also due to the factor ω in (3.10). It takes into account the occurrence of performed hystersis cycles per time unit.

     Alternatively, the core losses are often approximated with the Steinmetz equation $P_{\text{core}} = k \cdot f^a \cdot B^b$, where the factor / exponents are dependent on the core material[7]. The equation can also be modified to take into account the core's temperature as well as non-sinusoidal excitations (Modified Steinmetz Equation (MSE), or improved Generalized Modified Steinmetz Equation (iGSE)) [28].

  The frequency dependencies of R_{ac}, L_{core} can usually not simply be expressed in the time domain by multiplying with a correction factor such as f_0^a (i.e. a linearization for an explicit frequency f_0), since the excitation's frequency can generally have a wide range. This particularly applies to transient or non-sinusoidal signals, e.g. inrush or triangular-shaped currents. As a solution, adjustments in the model of Figure 3.5 have to be carried out, e.g. by implementing ladder models for the specific components [29].

- L_σ: Leakage inductance of windings and air gap (if implemented).
- $R_{\text{dc}}(T)$: DC-resistance of the windings.
- C_{par}: Capacitive coupling between the inductor's windings. It plays a crucial role for very high frequencies, as it forms a resonant circuit with the other components. The resonance frequency is assumed to be in the range of several MHz. Hence, the influence of C_{par} can be neglected[8] with respect to creating a model valid for inverter switching frequencies of $f_{\text{sw}} \leq 100\,\text{kHz}$.

Equivalent magnetic circuit of a two-leg interleaving choke

Figure 3.6 depicts the exemplary structure of a interleaving choke based on a two-leg core, as well as its equivalent magnetic circuit. The parameters $R_{\text{m,leg}}$, $R_{\text{m,con}}$, $R_{\text{m,}\sigma}$ represent the magnetic resistances of the core legs, the leg-connecting parts of the yoke, and the parasitic stray paths. The coupling flux[9] $\Phi_{12,\text{ph}}$, total magnetic core resistance $R_{\text{m,core}}$ and mutual inductance M_{12} is calculated according to (3.11) - (3.13).

$$R_{\text{m,core}} = 2R_{\text{m,con}} + 2R_{\text{m,leg}} \tag{3.11}$$

$$\Phi_{12,\text{ph}} = \frac{N \cdot i_{1,\text{ph}}}{R_{\text{m,core}} \;||\; R_{\text{m,}\sigma}} \cdot \frac{R_{\text{m,}\sigma}}{R_{\text{m,core}} + R_{\text{m,}\sigma}} = \frac{N \cdot i_{1,\text{ph}}}{R_{\text{m,core}}} \tag{3.12}$$

$$M_{12} = \frac{\Psi_{12,\text{ph}}}{i_{1,\text{ph}}} = \frac{N \cdot \Phi_{12,\text{ph}}}{i_{1,\text{ph}}} = \frac{N^2}{R_{\text{m,core}}} = M_{21} \tag{3.13}$$

[7] For ferrite materials, such as the one used in the experimental setup of this thesis, common intervals are $a \in [1.1, 1.9]$ and $b \in [1.6, 3.0]$.

[8] Parasitic winding capacitances can play a larger role in more sophisticated models that aim for reproducing the behavior of parasitic common-mode currents etc.

[9] The subscript 12 expresses the flux present in winding 2, produced solely by winding 1.

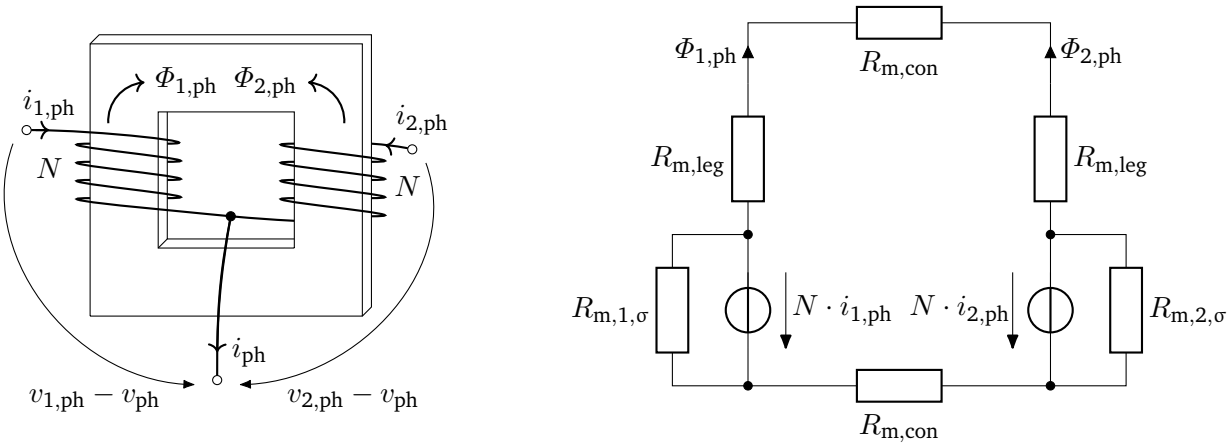


Figure 3.6.: Exemplary physical structure of an interleaving choke with two legs (left) and its equivalent magnetic circuit (right).

For the sake of completeness, it should be mentioned that also other configurations are possible for implementing the interleaving chokes. For example, the two windings of each phase can be placed on the respective legs of a three-leg or five-leg core [10]. However, due to the resulting cross-coupling between the phases, these variants are limited (five-leg core) or even not capable at all (three-leg core) of suppressing the common-mode component of the cross currents. This current component appears as circulating current and generally is undesirable (cp. Section 3.1.3).

Equivalent electrical circuit of the interleaving choke

The equivalent electrical circuit of the choke is given in Figure 3.7. Note that the parasitics, i.e. leakage inductance and DC-ohmic winding resistance, as well as the equivalent AC-resistance (e.g. iron losses) of the choke are included here.

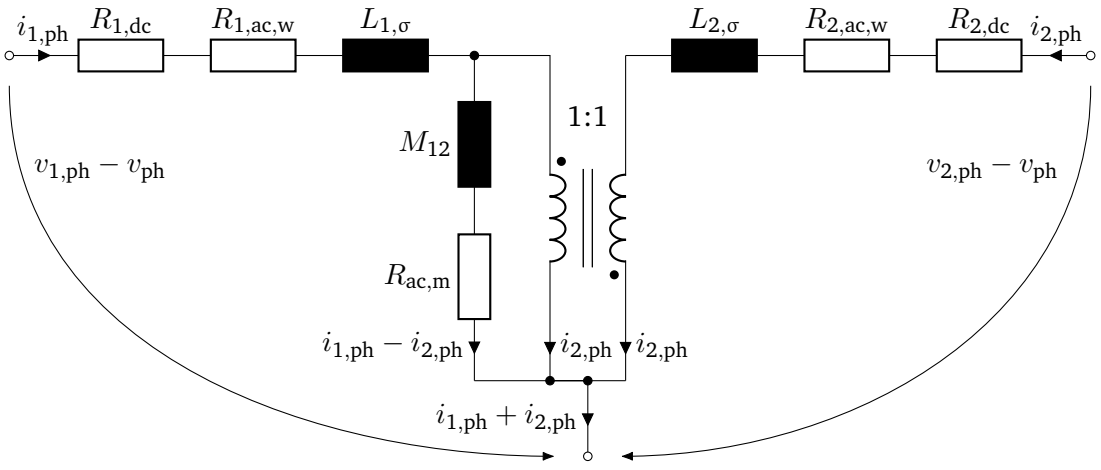


Figure 3.7.: Equivalent electrical circuit of interleaving choke.

The individual voltage loop equations and Kirchhoff's junction rule then give the expressions (3.14) - (3.16), forming a system of equations.

$$v_{1,\mathrm{ph}} - v_{\mathrm{ph}} = \left(R_{1,\mathrm{dc}} + R_{1,\mathrm{ac,w}}\right) \cdot i_{1,\mathrm{ph}} + \left(L_{1,\sigma} + M_{12}\right) \cdot \frac{\mathrm{d}}{\mathrm{d}t} i_{1,\mathrm{ph}} - M_{12} \cdot \frac{\mathrm{d}}{\mathrm{d}t} i_{2,\mathrm{ph}} + R_{\mathrm{ac,m}} \cdot \left(i_{1,\mathrm{ph}} - i_{2,\mathrm{ph}}\right) \quad (3.14)$$

$$v_{2,\mathrm{ph}} - v_{\mathrm{ph}} = \left(R_{2,\mathrm{dc}} + R_{2,\mathrm{ac,w}}\right) \cdot i_{2,\mathrm{ph}} + \left(L_{2,\sigma} + M_{12}\right) \cdot \frac{\mathrm{d}}{\mathrm{d}t} i_{2,\mathrm{ph}} - M_{12} \cdot \frac{\mathrm{d}}{\mathrm{d}t} i_{1,\mathrm{ph}} + R_{\mathrm{ac,m}} \cdot \left(i_{2,\mathrm{ph}} - i_{1,\mathrm{ph}}\right) \quad (3.15)$$

$$i_{1,\mathrm{ph}} + i_{2,\mathrm{ph}} = i_{\mathrm{ph}} \quad (3.16)$$

For the sake of simplicity, the following equations are set up under the assumption of a constant equivalent resistance $R_{\mathrm{ac,m}}$ for magnetization losses and of perfectly matched windings with $R_{\mathrm{ac,w}} = 0$. These measures shorten the equations considerably, but however also hinder an analysis regarding unmatched parameters. As will be shown in Section 4.3.11, the corresponding deviations are mostly negligible. Nevertheless, in order to perform an analysis with the complete mathematical model, an unsimplified derivation for the choke's equations is provided in Appendix A.2.

By applying elementary row operations to the simplified versions of Eqn. (3.14) - (3.16), Eqn. (3.17) - (3.19) can be derived. As previously noted, the parameters M_{12} and $R_{\mathrm{ac,m}}$ can show a high frequency dependency.

$$v_{\mathrm{ph}} = \frac{1}{2}\left(v_{1,\mathrm{ph}} + v_{2,\mathrm{ph}}\right) - \frac{1}{2} R_{\mathrm{dc}} \cdot \left(i_{1,\mathrm{ph}} + i_{2,\mathrm{ph}}\right) - \frac{1}{2} L_{\sigma} \cdot \frac{\mathrm{d}}{\mathrm{d}t}\left(i_{1,\mathrm{ph}} + i_{2,\mathrm{ph}}\right) \quad (3.17)$$

$$\frac{\mathrm{d}}{\mathrm{d}t} i_{1,\mathrm{ph}} = \frac{v_{1,\mathrm{ph}} - v_{2,\mathrm{ph}} + R_{\mathrm{dc}} \cdot \left(i_{\mathrm{ph}} - 2 i_{1,\mathrm{ph}}\right) + 2 R_{\mathrm{ac,m}} \cdot \left(i_{\mathrm{ph}} - 2 i_{1,\mathrm{ph}}\right)}{2 L_{\sigma} + 4 M_{12}} + \frac{1}{2} \cdot \frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{ph}} \quad (3.18)$$

$$\frac{\mathrm{d}}{\mathrm{d}t} i_{2,\mathrm{ph}} = \frac{v_{2,\mathrm{ph}} - v_{1,\mathrm{ph}} + R_{\mathrm{dc}} \cdot \left(i_{\mathrm{ph}} - 2 i_{2,\mathrm{ph}}\right) + 2 R_{\mathrm{ac,m}} \cdot \left(i_{\mathrm{ph}} - 2 i_{2,\mathrm{ph}}\right)}{2 L_{\sigma} + 4 M_{12}} + \frac{1}{2} \cdot \frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{ph}} \quad (3.19)$$

Finally, the negligence of all parasitic parameters yields the approximations given in Eqn. (3.20) - (3.22).

$$v_{\mathrm{ph}} \approx \frac{1}{2}\left(v_{1,\mathrm{ph}} + v_{2,\mathrm{ph}}\right) \quad (3.20)$$

$$\frac{\mathrm{d}}{\mathrm{d}t} i_{1,\mathrm{ph}} \approx \frac{v_{1,\mathrm{ph}} - v_{2,\mathrm{ph}}}{4 M_{12}} + \frac{1}{2} \cdot \frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{ph}} \quad (3.21)$$

$$\frac{\mathrm{d}}{\mathrm{d}t} i_{2,\mathrm{ph}} \approx \frac{v_{2,\mathrm{ph}} - v_{1,\mathrm{ph}}}{4 M_{12}} + \frac{1}{2} \cdot \frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{ph}} \quad (3.22)$$

Interpretation of equations
Equation (3.20) emphasizes the averaging effect of the interleaving choke with respect to the output voltage, which leads to a greater availability of voltage space vectors (cp. Figure 2.2). The second and third term of complete voltage equation of Eq. (3.17) correspond to parasitic voltage drops at the ohmic resistance and leakage inductance of the windings etc. Note that voltage drops due to magnetization (parameters $R_{\mathrm{ac,m}}$ and M_{12}) do not appear in the equation for the phase voltage.

The implications of Eq. (3.18) and Eq. (3.19) are best visible if transformed to the Laplace domain, as given in Eq. (3.23) and Eq. (3.24).

$$I_{1,\mathrm{ph}}(s) = \frac{1}{2} \cdot \frac{\left(V_{1,\mathrm{ph}}(s) - V_{2,\mathrm{ph}}(s)\right) + \left(R_{\mathrm{dc}} + 2R_{\mathrm{ac,m}} + s(L_\sigma + 2 \cdot M_{12})\right) \cdot I_{\mathrm{ph}}(s)}{R_{\mathrm{dc}} + 2R_{\mathrm{ac,m}} + s\left(L_\sigma + 2M_{12}\right)} \tag{3.23}$$

$$I_{2,\mathrm{ph}}(s) = \frac{1}{2} \cdot \frac{\left(V_{2,\mathrm{ph}}(s) - V_{1,\mathrm{ph}}(s)\right) + \left(R_{\mathrm{dc}} + 2R_{\mathrm{ac,m}} + s(L_\sigma + 2 \cdot M_{12})\right) \cdot I_{\mathrm{ph}}(s)}{R_{\mathrm{dc}} + 2R_{\mathrm{ac,m}} + s\left(L_\sigma + 2M_{12}\right)} \tag{3.24}$$

The first term describes the strong impact of interleaving vectors on the cross-currents, i.e. switch positions where $v_{1,\mathrm{ph}} - v_{2,\mathrm{ph}} \neq 0$ holds. In this case, $i_{1,\mathrm{ph}}$ is strongly increasing and $i_{2,\mathrm{ph}}$ is strongly decreasing, or vice versa. The magnitude of the cross-current's change is approximately $\Delta|i_{1,\mathrm{ph}} - i_{2,\mathrm{ph}}| \approx {}^{2V_{\mathrm{dc}}}/_{(4M_{12})} \cdot \Delta t$, where Δt is an arbitrary duration of the applied interleaving vector. The influence of the interleaving vectors decays over time, if they are not applied any longer (first order lag element).

Moreover, the current sharing behavior reveals itself in the respective second term: In consideration of perfectly matched windings and abstinent interleaving vectors, the output current is shared equally. The impact of an interleaving vector, including the decaying properties, as well as the current sharing behavior is exemplarily illustrated in Figure 3.8.

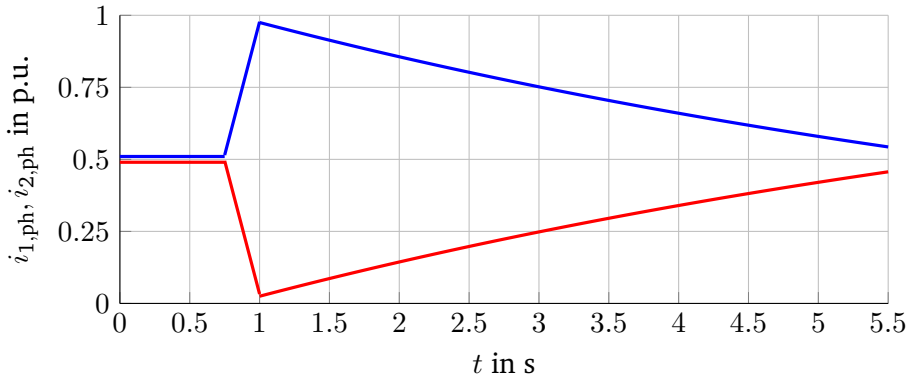


Figure 3.8.: Impact of an interleaving vector on $i_{1,\mathrm{ph}}, i_{2,\mathrm{ph}}$ applied from $t = 0.75\,\mathrm{s}$ to $t = 1.00\,\mathrm{s}$, as well as the decaying characteristics and the tendency towards equally shared currents.

3.1.3. DC-link

The DC-link is already present in the overall system circuit of Figure 2.1. However, before the actual derivation of the mathematical model is conducted, two assumptions for the DC-link shall be established.

1. The supplying current i_{source} is assumed to be equal to the averaged drawn inverter current $i_{\mathrm{d,av}}$. Firstly, this implies that the AC-components of $i_{1,\mathrm{d}+}, i_{1,\mathrm{d}}$,...,$\mathrm{i_{d-}}$ appear completely in $i_{\mathrm{dc,cap}}$. Secondly, it suggests that all of the averaged real power consumed by the load is directly supplied by the source.

2. The overall capacitance value of the DC-link C_{dc} is assumed to be large enough that neither the switching frequency-related voltage ripple, nor the ripple due to reactive power has to be considered.

These simplifications offer the possibility to analyze the topology's properties independently of the feeding circuit, e.g. uncontrolled or controlled six-pulse bridge, batteries, or others.

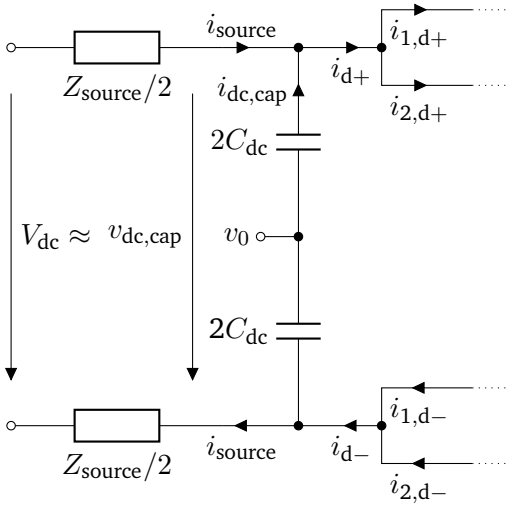


Figure 3.9.: Equivalent circuit of the DC-link for nodal equations.

Nodal Equations

The essential equations can be obtained by the nodal rule of the involved junctions in Figure 3.9. As given in Eq. (3.27) and Eq. (3.28), the overall inverter current i_{d} is identical for the positive and negative rail.

$$i_{\text{source}} = i_{\text{d}+} + i_{\text{dc,cap}} \tag{3.25}$$
$$i_{\text{source}} = i_{\text{d}-} - i_{\text{dc,cap}} \tag{3.26}$$
$$i_{\text{d}-} = i_{1,\text{d}-} + i_{2,\text{d}-} = i_{\text{d}} \tag{3.27}$$
$$i_{\text{d}+} = i_{1,\text{d}+} + i_{2,\text{d}+} = i_{\text{d}} \tag{3.28}$$

Circulating choke current

In contrast to i_{d}, the input and output currents of the individual inverters ($i_{1,\text{d}+}$, $i_{1,\text{d}-}$ and $i_{2,\text{d}+}$, $i_{2,\text{d}-}$), are not necessarily equal. In fact, they are unequal as soon as non-zero common-mode components in $\boldsymbol{i}_1$, $\boldsymbol{i}_2$ exists, as it was already proven in Section 3.1.1. The difference between the respective input and output inverter current is therefore identical to this common-mode component:

$$i_{1,\text{d}+} = i_{1,\text{d}-} + i_{1,\gamma} \tag{3.29}$$
$$i_{2,\text{d}+} = i_{2,\text{d}-} + i_{2,\gamma} \tag{3.30}$$

The occurence of $i_{1,\gamma}$, $i_{2,\gamma}$ is linked to the finite impedance path for common-mode currents via the interleaving chokes. This path is identified easily in Figure 2.1, but can also be proven formally as followed: Take simplified three-phase versions[10] of Eq. (3.18) and Eq. (3.19), which yields the equation below.

$$\frac{\text{d}}{\text{d}t}(\boldsymbol{i}_{\text{out}}/2) + \frac{\text{d}}{\text{d}t}\boldsymbol{i}_1 \approx \frac{\text{d}}{\text{d}t}(\boldsymbol{i}_{\text{out}}/2) - \frac{\text{d}}{\text{d}t}\boldsymbol{i}_2 \approx \frac{1}{4M} \cdot (\boldsymbol{v}_1 - \boldsymbol{v}_2) \tag{3.31}$$

If interpreted in the alpha-beta-gamma domain, Eq. (3.31) clearly shows an impact on $i_{1,\gamma}$, $i_{2,\gamma}$ if the common-mode voltages of the paralleled inverters are unequal ($v_{1,\gamma} - v_{2,\gamma} \neq 0$). Since Eq. (3.27) and Eq. (3.28) at

[10] simplified by assuming equal parameters for each phase and under negligence of leakage and losses

the common junction of the inverters continue to hold, the identity $i_{1,\gamma} = -i_{2,\gamma}$ can be derived. The current $i_{1,\gamma}$ is circulating from one inverter to the other via the interleaving chokes, as depicted in Figure 3.10. It occurs independently of the inverters' switch positions. The circulation does not flow through the DC-link capacitor, nor does it contribute to the load current. i.e. it does not provide any optimization potential for either subsystem. On the other hand, it superimposes to the remaining current components of $\boldsymbol{i}_1$, $\boldsymbol{i}_2$, i.e. a higher circulating current correlates with increased conduction losses within the chokes and semiconductors.

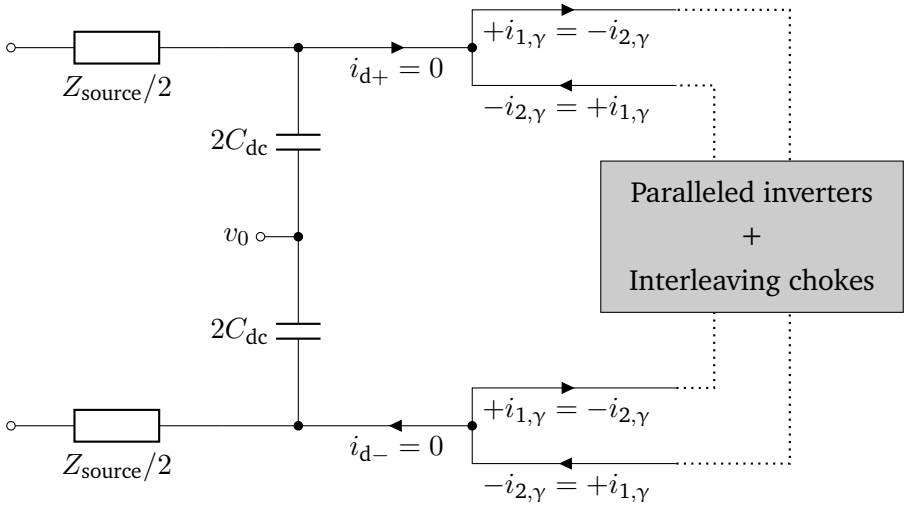


Figure 3.10.: Isolated view of gamma component for interleaved inverter system: The current component $i_{1,\gamma}$ circulates from one inverter to the other via the interleaving chokes.

DC-link capacitor current of a two-level inverter

As stated in the beginning of this section, the DC-link capacitor current $i_{\text{dc,cap}}$ is assumed to be equal to the ac-component of the drawn inverter current. In case of a two-level inverter controlled with typical modulation schemes,[11] the rms-value of the DC-link capacitor current $i_{\text{dc,cap,rms}}$ can be calculated analytically with Eq. (3.32) [30]. For the respective derivation, a symmetrical three-phase system as load is presumed and load-related ripple is neglected.

$$i_{\text{dc,cap,rms}} = i_{\text{ph,rms}} \cdot \sqrt{2m_{\text{f}} \left(\frac{\sqrt{3}}{4\pi} + \cos^2(\varphi) \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} m_{\text{f}} \right) \right)} \tag{3.32}$$

The value $i_{\text{ph,rms}}$ denotes the rms-value of the inverter's phase output current. Note that Eq. (3.32) only has a dependency on the modulation factor m_{f} and the power factor $\cos(\varphi)$, but holds for any of the above-mentioned modulation methods. In brevity, the cause is the independency of $i_{\text{dc,cap,rms}}$ on the two-level inverter's common-mode voltage component, which is the only difference among the modulation schemes with respect to rms-values over a complete switching cycle. The DC-link current in dependency of the inverter's operating point is visualized in Figure 3.11.

DC-link capacitor current of an interleaved inverter

The advantage of an interleaved inverter with respect to the DC-link capacitor current is that the drawn inverter currents $i_{1,\text{d}}, i_{2,\text{d}}$ can be superimposed in a compensating manner. The aim is to bring $i_{1,\text{d}} + i_{2,\text{d}}$ as

[11] For example sine triangle modulation, third harmonic injection, space vector modulation, discontinuous pulse width modulation [3].

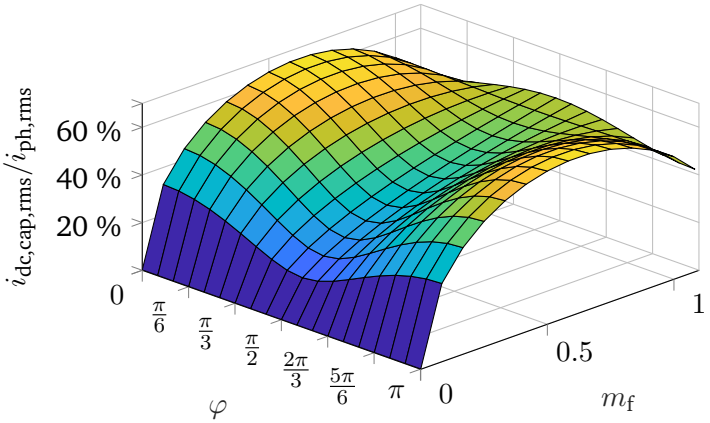


Figure 3.11.: DC-link capacitor current for a two-level inverter in dependency of the modulation factor m_{f} and phase angle φ (power factor $\rightarrow \cos(\varphi)$).

close as possible to the averaged load current, since only the difference of these currents will flow through the DC-link capacitor under the given assumptions. For example, if a larger power factor is present, a lowered $i_{\text{dc,cap,rms}}$ can be achieved if the zero-voltage space vector of one inverter (leading to $i_{1,\text{d}} = 0$) and an active space vector of the other inverter (leading to $i_{2,\text{d}} \neq 0$) are present simultaneously. This can be achieved by a specific carrier shift between the modulations for the interleaved inverters. An example[12] is given in Figure 3.12. It clearly shows that the modulation method and chosen carrier shift have a strong impact on the resulting $i_{\text{dc,cap,rms}}$. However, the optimal combination of modulation and carrier shift depends on the specific operating point of the inverter. A thorough investigation of this aspect is provided in [19].

An even better solution for $i_{\text{dc,cap,rms}}$ can be found by optimizing the pulse patterns for every upcoming switching cycle[13] by means of a linear program [31]. In analogy to Figure 3.11, the optimized $i_{\text{dc,cap,rms}}$ for the interleaved inverter is presented in Figure 3.13. The simplification of large output and interleaving inductances, i.e. negligence of any output current ripples remains.

It is visible that $i_{\text{dc,cap,rms}}$ can be reduced by 35 % to 80 % by using the interleaved inverter with optimized pulse patterns. Over all possible operation points, the relative reduction is in the area of 50 %. Current-related losses, which depend quadratically on $i_{\text{dc,cap,rms}}$, can therefore be reduced significantly with appropriate switching patterns. Lastly, please note that due to dependency of $i_{\text{dc,cap,rms}}/i_{\text{ph,rms}}$ on m_{f} and $\cos(\varphi)$, there generally is the possibility to define optimal machine magnetization values for a given reference torque. The attained optimal reference values $\Psi^*_{\text{s,opt}}(T^*_{\text{e}})$ may however differ from the optimal machine magnetization with respect to machine losses (cp. Section 3.2.4).

[12] For the sake of simplicity, the output and interleaving inductances are assumed to be very large for this example, i.e. the currents $i_{\text{d},1}, i_{\text{d},2}$ remain constant for the respective voltage space vectors. The consideration of changing $i_{\text{d},1}, i_{\text{d},2}$ due to machine ripple and cross-current evolution through the interleaving chokes is provided the model predictive controller design of Section 4.3.8.

[13] This optimization includes constraints for balancing the choke magnetization over one switching period T_{sw}.

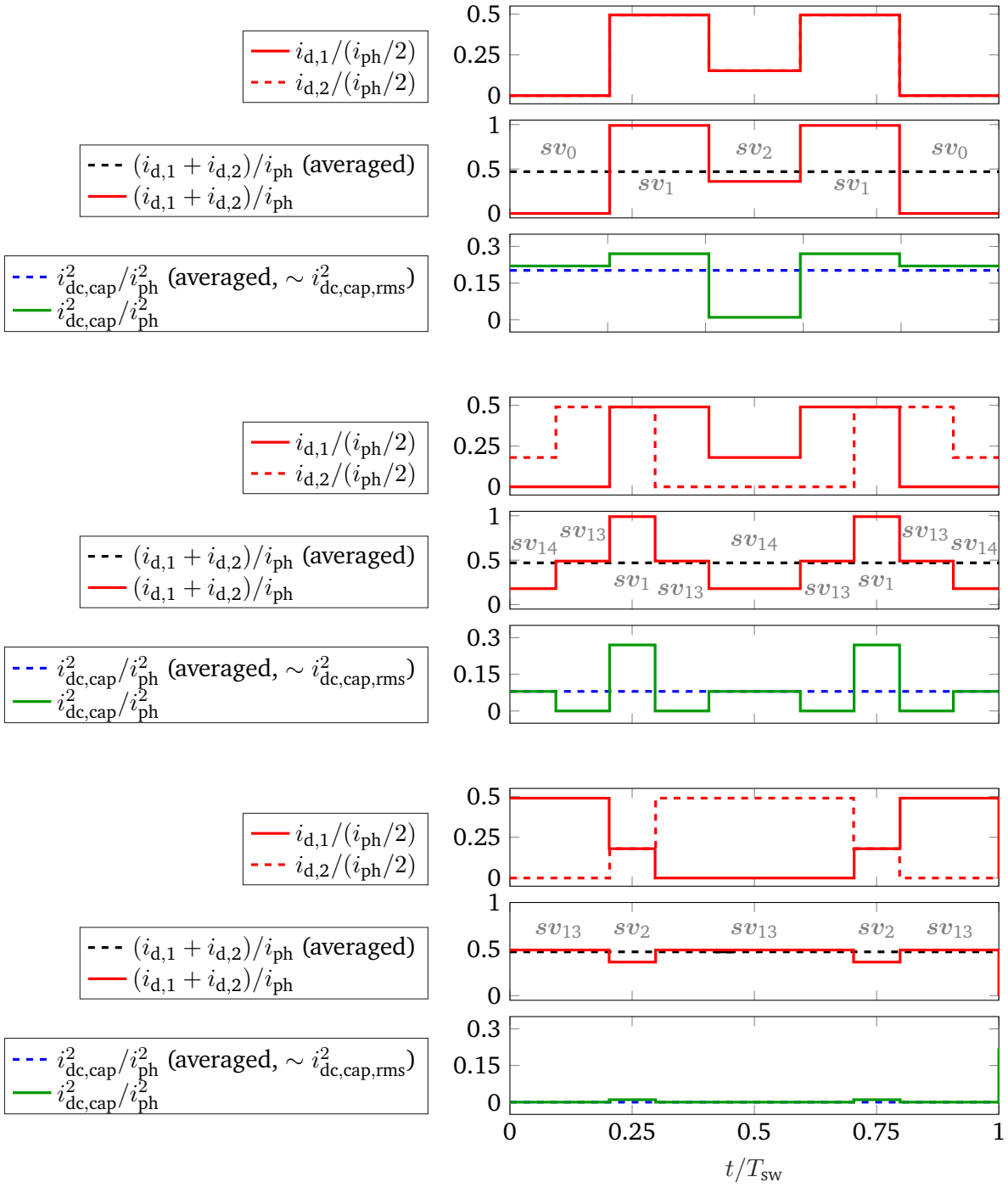


Figure 3.12.: Example of modulation scheme impact on i_d over one switching period T_{sw} at operating point $m_f = 0.7, \cos(\varphi) = 0.3 \cdot \pi/2, \arg(\underline{v}_{out}) = 0.3 \cdot \pi/3$ of interleaved inverter. Upper three panels: flat-bottom modulation without carrier shift. Middle three panels: flat-bottom modulation with 50% carrier shift between inverters. Lower three panels: flat-top modulation with 50% carrier shift between inverters.

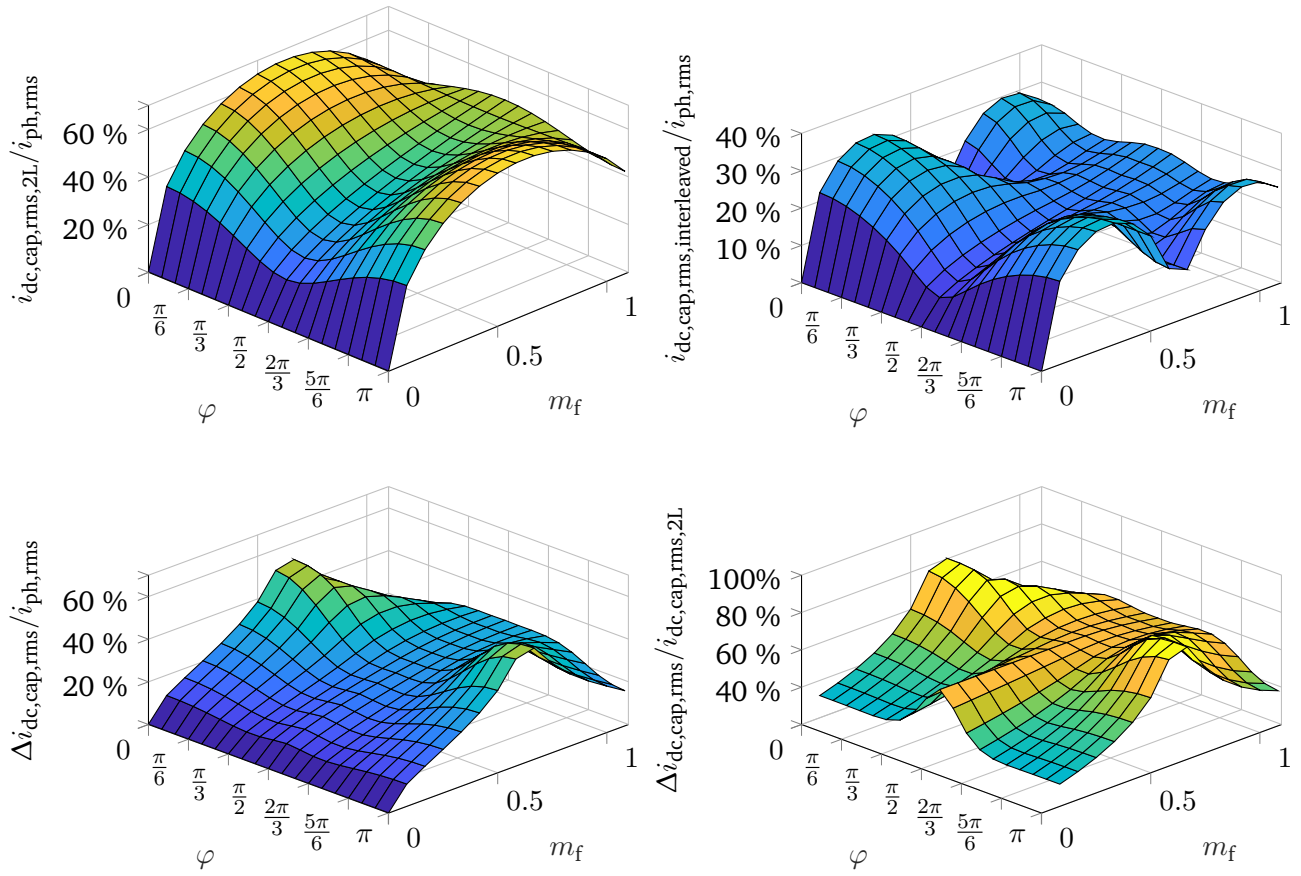


Figure 3.13.: DC-link capacitor current in dependency of the modulation factor m_{f} and phase angle φ (power factor $\rightarrow \cos(\varphi)$) for a two-level inverter (top left) and interleaved inverter with optimized pulse pattern (top right). Absolute (bottom left) and relative (bottom right) difference of DC-link capacitor current between two-level inverter and interleaved inverter with optimized pulse pattern.

Supply line leakage

The supply lines between DC-link capacitors and the inverter module inputs can show inductive properties with respect to a high frequency excitation. The values of these parasitics $L_{\mathrm{dc},\sigma}$ depend on the concrete wiring, but can reach up to $100\,\mathrm{nH}$ and beyond[14]. Figure 3.14 shows the corresponding placement of the parasitics for separate and shared supply lines to the two-level inverters. Unquestionably, this leakage inductance is much smaller than the load and the interleaving chokes, hence can be neglected for setting up the system matrix of the overall system. Yet, the quantities can influence the resonance frequency of the DC-link and further can also cause critical over-voltages at the switching devices during their turn-off of forward conduction, where high values of $|{}^{\mathrm{d}}/_{\mathrm{d}t} \cdot i_{\mathrm{d},1}|$, $|{}^{\mathrm{d}}/_{\mathrm{d}t} \cdot i_{\mathrm{d},2}|$ occur. The mechanism for these over-voltages is sketched in Figure 3.15.

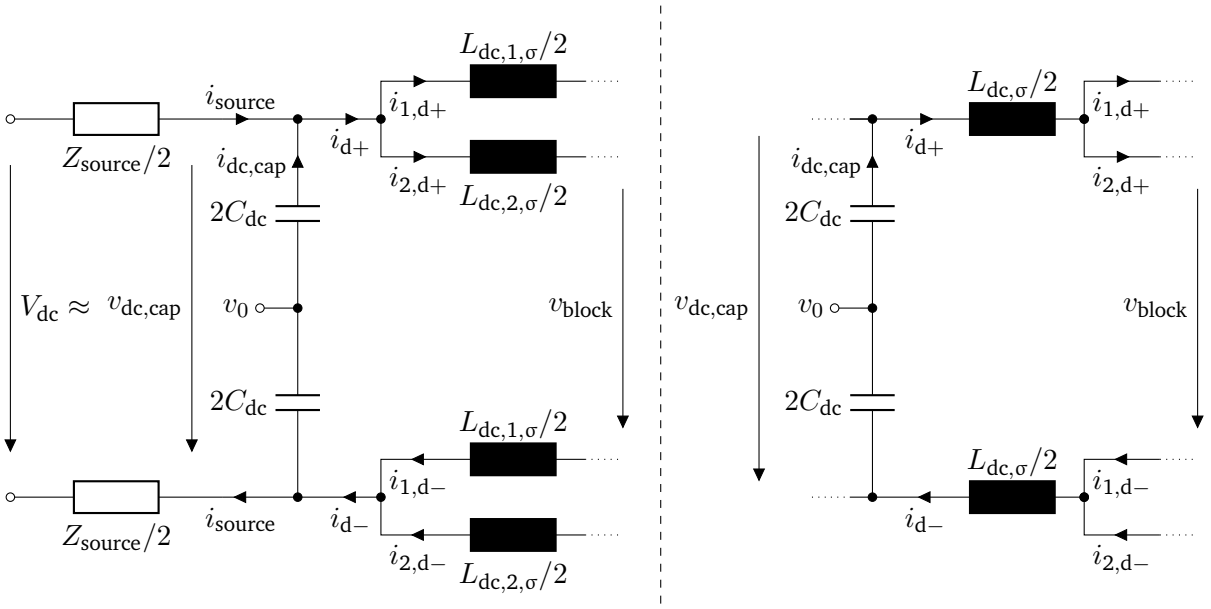


Figure 3.14.: Equivalent circuit of the DC-link including inverter supply line leakage with separate (left) and shared wiring (right) of the two-level inverters.

High rates of current change lead to a voltage drop at the inductances. It adds up with the DC-link voltage to the overall blocking voltage v_{block} at the half bridges. It is important to note that while turn-offs of forward conduction *increase* the voltage to be blocked by the transistors (due to ${}^{\mathrm{d}}/_{\mathrm{d}t}\, i_{\mathrm{d}} < 0$), the turn-on activities for forward conduction in fact *decrease* the values of v_{block}. This brings upon potential to decrease the over-voltages by choosing appropriately compensating switching activity.[15]

This effect is particularly of interest for fast switching devices. For instance, silicon carbide MOSFETs (which are used for the experimental setup of this thesis [24]) can experience over-voltages of $100\,\mathrm{nH} \cdot 2\,\mathrm{A\,ns^{-1}} = 200\,\mathrm{V}$ during *regular* operation. Fault conditions that require an immediate turn-off during short circuits obviously produce even more strenuous situations. In order to prevent irreversible damage to the transistors by exceeding their maximum break-down voltage, these fault conditions necessitate special techniques, e.g.

[14] A fair approximation is $50\,\mathrm{nH}$ to $200\,\mathrm{nH}$ per $10\,\mathrm{cm}$ of parallel conductors. The spacing of the conductors should be between twice and 100-fold larger than their diameter to make the approximation valid [32].

[15] Note that this kind of compensation requires close attention to timing of the switching activities, since the ${}^{\mathrm{d}i}/_{\mathrm{d}t}$-effects have to appear at the same time. This may necessitate variable dead-time adjustment due to varying delay as well as fall and rise times for turn-on and turn-off, which generally are dependent on the current to be switched.

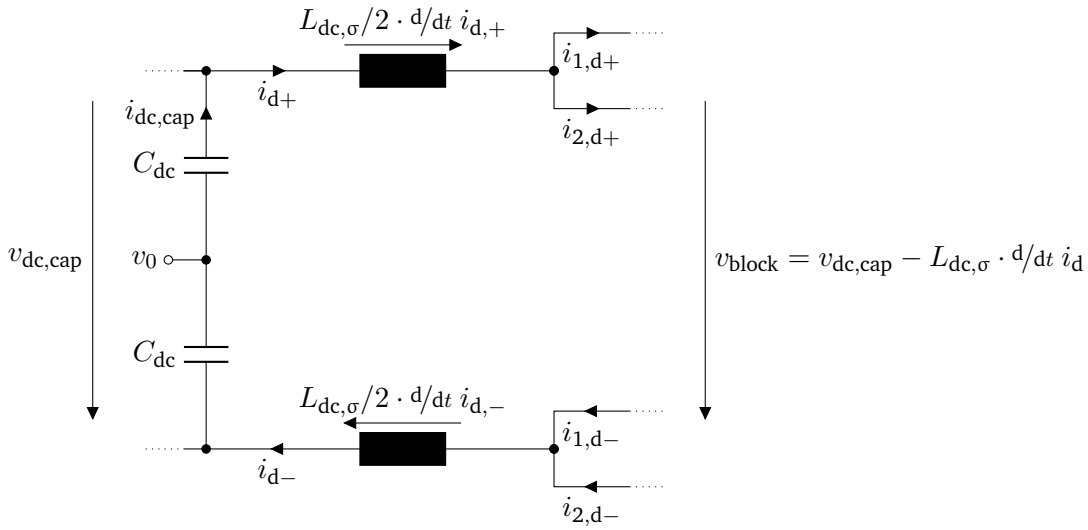


Figure 3.15.: Sketched mechanism of transient over-voltages during switching activities.

active-clamping [33]. They usually lead to higher conduction losses and therefore should preferably take effect solely for fault conditions. In order to do so, it is crucial to keep an appropriate margin between the over-voltages due to regular operation and due to short circuits etc.

DC-link capacitors

The DC-link capacitors in the detailed equivalent circuit of Figure 3.14 do not consider the characteristics of a real capacitor. In order to model losses and other non-ideal behavior, particularly at higher frequencies, the capacitances should be replaced by a proper equivalent circuit model that resembles these properties. A common replacement circuit for real capacitors is the consideration of the equivalent insulation resistance R_{par}, series resistance R_{ser} and series inductance L_{ser}, as given in Figure 3.16.

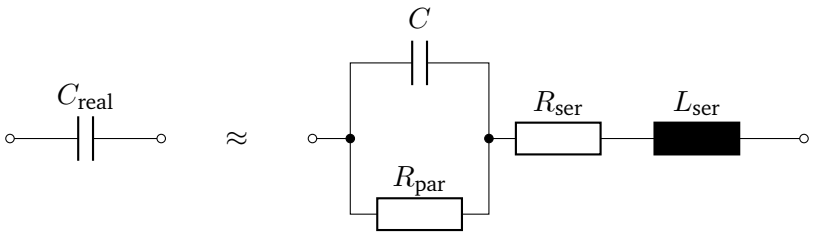


Figure 3.16.: Typical equivalent circuit of a real capacitor.

Depending on the capacitor technology and required accuracy of its model, also more complex approaches exist. For example, models with compensations for frequency, temperature and DC bias are proposed for several capacitor technologies in [34].

Traditionally, aluminum electrolytic capacitors (Al-caps) are often used for DC-link stabilization purposes. They feature a high energy density and low costs, but also unfavorable characteristics for higher frequencies. Owing

to the commissioning of modern, faster switching devices such as silicon carbide (SiC) MOSFETs, the demands towards the DC-link capacitors are steadily increasing. For this reason, Al-caps are being progressively replaced by specialized DC-link capacitors, e.g. metallized polypropylene film capacitors (MKP-caps) [35]. Next to the film capacitors, another promising alternative is given by multi-layer ceramic capacitors (MLC-caps) [36]. Table 3.1 compares the three capacitor technologies. Note that obviously only tendencies can be captured, i.e. the table does not spare the comparison of specifics products that come into question for designing the DC-link. However, two crucial aspects shall be discussed in more detail: The inferior performance of Al-caps with respect to high switching frequencies and fast switching transients, as well as minimization of losses.

Table 3.1.: Performance comparison of three main types of capacitors for DC-link applications. [36]

	Al-cap	MKP-cap	MLC-cap
Nominal capacitance	$+$	o	$-$
Maximum voltage	o	$+$	$-$
Energy density	$+$	$-$	$-$
Cost per stored energy	$+$	o	$-$
Series resistance	$-$	$+$	o
Ripple current	$-$	$+$	o
Voltage derating	o	$+$	$-$
Operating frequency	$-$	$+$	$+$
Operating temperature	o	$-$	$+$
Capacitance stability	o	$+$	$-$
Reliability	$-$	o	$+$

Legend: relative performance is superior $(+)$, intermediate $(\ \mathrm{o}\ )$, inferior $(-)$

Regarding the first aspect, Al-caps generally show a larger equivalent series inductance L_{ser}. This is critical due to two reasons: Firstly, it implies elevated overvoltages during transistor turn-off, impairing the possibility of utilizing fast switching semiconductors. Secondly, a high L_{ser} leads to a lowered resonance frequency f_{res} of the DC-link capacitors, which limits the deployable switching frequency of the inverter[16].

In consideration of the DC-link's losses, the substantially larger equivalent series resistance R_{ser} of Al-caps is adverse to an efficient inverter design. Moreover, high values of dissipated power in the capacitors may even lead to offended operating temperature constraints. In the worst case, this would necessitate either improved cooling, or the installation of additional capacitors, even if voltage ripple constraints had already been met.

Despite the superiority[17] of foil and muli-player ceramic capacitors, in any case some trade-off has to be carried out regarding the required energy storage, anticipated voltage ripple, component costs, available space etc. In order to overcome the specific drawbacks of the chosen capacitor technology, several design-related solutions are presented in [36] and elaborated in [37]–[39]. Proposed are hybrid DC-link banks (Al-caps combined with foil caps) or additional active circuitry. An alternative to these physical adjustments are adaptions in the control scheme, which can also alleviate the difficulties associated with the DC-link. As regularly mentioned in Chapter 2, it is this concept, in combination with the interleaved topology, that is dealt within this thesis.

[16] For obvious reasons, a strong excitation of this parasitic resonant circuit has to be avoided at all costs.

[17] Please note that further important aspects (that are not discussed in this thesis) exist, such as expected life time, dominant failure modes and their most severe stressors [36].

3.2. Induction Machine

The basic equations for modeling induction machines are recapitulated here. In this context, the principle and advantages of field oriented modeling will also be reviewed. Moreover, peculiarities of inverter-fed drive systems are discussed in order to properly consider them in the controller design of the following chapter.

Note that friction and stray losses are not considered in this thesis. Consequently, space harmonics due to the winding arrangements and saturation effects are disregarded, unless explicitly stated otherwise. This means that an ideal sinusoidal distribution of current loading and flux density is assumed. Lastly, the magnetization losses of the machine are neglected for the derivation of the machine's dynamics, i.e. are only examined for investigations with respect to the fundamental frequency behavior.

3.2.1. Basic System Equations

Basic principle
Induction machines consist of an electrical stator and rotor circuit. They are magnetically coupled via a small airgap in between them. With an appropriate voltage or current feeding of the stator circuit, a rotating magnetic field in the airgap is built up. The rotor circuit is exposed to this field, leading to an induced voltage there as long as it is not rotating mechanically with identical speed of the airgap field, i.e. as long as there is a slip between the rotor and the stator. This slip is defined as $s = 1 - \omega_\mathrm{r}/\omega_\mathrm{k}$, where ω_r and ω_k are the rotational electrical speeds of the rotor and the airgap field, respectively.

According to Lenz's law, the induced rotor current will flow in a manner that it opposes any changes of the initial field. Therefore, it will lead to the production of electromagnetic torque that pulls the rotor mechanically, following the motion of the field excited by the stator.

Dynamic model of electrical quantities
The basic system equations for the dynamics of squirrel cage induction machines can be derived based on the stator and rotor voltage loop [40], which are given in Eqn. (3.33) - (3.34). Note that the equations are written in the respective stator and rotor reference frame (superscripts $\alpha\beta$ and dq, both orthogonal systems). The equations are not subject to any physical rotation in this case, meaning that the time derivatives do not include any motionally induced electromotive force. The rotor voltage equation is equaled to zero, as the rotor bars are establishing a short circuit in squirrel cage machines.

$$\boldsymbol{v}_\mathrm{s}^{\alpha\beta} = R_\mathrm{s}\boldsymbol{i}_\mathrm{s}^{\alpha\beta} + \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{\Psi}_\mathrm{s}^{\alpha\beta} \tag{3.33}$$

$$\boldsymbol{v}_\mathrm{r}^{\mathrm{dq}} = R_\mathrm{r}\boldsymbol{i}_\mathrm{r}^{\mathrm{dq}} + \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{\Psi}_\mathrm{r}^{\mathrm{dq}} = 0 \tag{3.34}$$

where $R_\mathrm{s}, R_\mathrm{r}$ are the stator and rotor winding resistance

In the next step, the two equations have to be transformed / rotated into the same reference system. Within this section, the stator reference frame is chosen. In consideration of the time derivatives within the equations, it further is beneficial to interpret the variables as complex for the transformation (cp. Section 3.1.1). In this case, the rotation can be achieved via an appropriate substitution of the variables, as exemplarily given in Eq. (3.51) (for the regular vectorial form, also the rotational matrix in Eq. (3.36) can be used).

$$\underline{\boldsymbol{g}}^{\alpha\beta} = \underline{\boldsymbol{g}}^{\mathrm{dq}} \cdot e^{\mathrm{j}\beta_\mathrm{r}} \tag{3.35}$$

$$\boldsymbol{g}^{\alpha\beta} = \begin{pmatrix} \cos(\beta_\mathrm{r}) & -\sin(\beta_\mathrm{r}) \\ \sin(\beta_\mathrm{r}) & \cos(\beta_\mathrm{r}) \end{pmatrix} \cdot \boldsymbol{g}^{\mathrm{dq}} = \boldsymbol{R}(\beta_\mathrm{r}) \cdot \boldsymbol{g}^{\mathrm{dq}} \tag{3.36}$$

where β_r is the angle from the stator to the rotor reference frame

When applying the substitution of Eq. (3.51) to Eqn. (3.33) - (3.34), the time dependency of β_r has to be taken into account. This leads to the appearance of its time derivative ω_r, i.e. the angular speed of the rotor. The resulting system equations are:

$$\underline{\boldsymbol{v}}_\mathrm{s}^{\alpha\beta} = R_\mathrm{s}\underline{\boldsymbol{i}}_\mathrm{s}^{\alpha\beta} + \frac{\mathrm{d}}{\mathrm{d}t}\underline{\boldsymbol{\Psi}}_\mathrm{s}^{\alpha\beta} \tag{3.37}$$

$$\underline{\boldsymbol{v}}_\mathrm{r}^{\alpha\beta} = R_\mathrm{r}\underline{\boldsymbol{i}}_\mathrm{r}^{\alpha\beta} + \frac{\mathrm{d}}{\mathrm{d}t}\underline{\boldsymbol{\Psi}}_\mathrm{r}^{\alpha\beta} - \mathrm{j}\omega_\mathrm{r}\underline{\boldsymbol{\Psi}}_\mathrm{r}^{\alpha\beta} = 0 \tag{3.38}$$

Lastly, the stator and rotor equations can be combined with each other by taking into account the relation according to Eqn. (3.39) - (3.40).

$$\begin{pmatrix} \underline{\boldsymbol{\Psi}}_\mathrm{s} \\ \underline{\boldsymbol{\Psi}}_\mathrm{r} \end{pmatrix} = \begin{pmatrix} L_\mathrm{s} & M_\mathrm{sr} \\ M_\mathrm{sr} & L_\mathrm{r} \end{pmatrix} \begin{pmatrix} \underline{\boldsymbol{i}}_\mathrm{s} \\ \underline{\boldsymbol{i}}_\mathrm{r} \end{pmatrix} \tag{3.39}$$

$$\begin{pmatrix} \underline{\boldsymbol{i}}_\mathrm{s} \\ \underline{\boldsymbol{i}}_\mathrm{r} \end{pmatrix} = \frac{1}{\sigma} \begin{pmatrix} 1/L_\mathrm{s} & (\sigma-1)/M_\mathrm{sr} \\ (\sigma-1)/M_\mathrm{sr} & 1/L_\mathrm{r} \end{pmatrix} \begin{pmatrix} \underline{\boldsymbol{\Psi}}_\mathrm{s} \\ \underline{\boldsymbol{\Psi}}_\mathrm{r} \end{pmatrix} \tag{3.40}$$

where M_sr is the mutual inductance between stator and rotor
and $L_\mathrm{s}, L_\mathrm{r}$ are the self inductances of the stator and rotor
and $\sigma = 1 - M_\mathrm{sr}^2/(L_\mathrm{s}L_\mathrm{r})$

Equations (3.33) - (3.40) are suitable to set up an equivalent circuit model of the machine, as it is shown in Figure 3.17. The final state-space representation of the induction machine can be formulated with two arbitrarily chosen vectors of $\{\underline{\boldsymbol{\Psi}}_\mathrm{s}^{\alpha\beta}, \underline{\boldsymbol{\Psi}}_\mathrm{r}^{\alpha\beta}, \underline{\boldsymbol{i}}_\mathrm{s}^{\alpha\beta}, \underline{\boldsymbol{i}}_\mathrm{r}^{\alpha\beta}\}$. A good representation for control purposes is the usage of the easily measurable stator current $\underline{\boldsymbol{i}}_\mathrm{s}^{\alpha\beta}$ and the rather sluggishly behaving rotor flux linkage $\underline{\boldsymbol{\Psi}}_\mathrm{r}^{\alpha\beta}$. It is given in Eq. (3.41) in its complex notation and in Eq. (3.42) in its regular vectorial form.

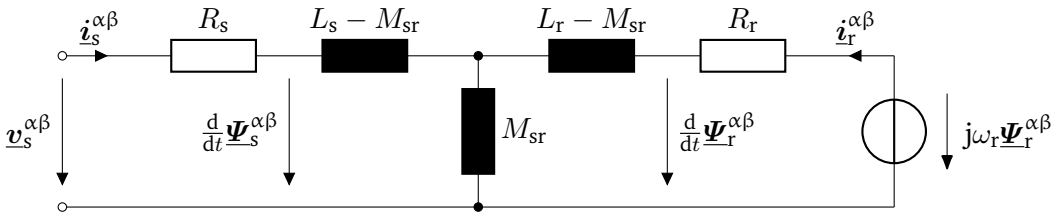


Figure 3.17.: Equivalent circuit model of the induction machine for the alpha-beta reference frame, based on mutual inductance.

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{pmatrix}\underline{\boldsymbol{i}}_{\mathrm{s}}^{\alpha\beta}\\ \underline{\boldsymbol{\Psi}}_{\mathrm{r}}^{\alpha\beta}\end{pmatrix}=\frac{1}{\sigma L_{\mathrm{s}}}\begin{pmatrix}-R_{\mathrm{s}}-M_{\mathrm{sr}}^2R_{\mathrm{r}}/L_{\mathrm{r}}^2 & M_{\mathrm{sr}}R_{\mathrm{r}}/L_{\mathrm{r}}^2\\ \sigma L_{\mathrm{s}}\cdot M_{\mathrm{sr}}R_{\mathrm{r}}/L_{\mathrm{r}} & -\sigma L_{\mathrm{s}}\cdot R_{\mathrm{r}}/L_{\mathrm{r}}\end{pmatrix}\begin{pmatrix}\underline{\boldsymbol{i}}_{\mathrm{s}}^{\alpha\beta}\\ \underline{\boldsymbol{\Psi}}_{\mathrm{r}}^{\alpha\beta}\end{pmatrix}+\ldots$$
$$\begin{pmatrix}0 & -\mathrm{j}\omega_{\mathrm{r}}\cdot M_{\mathrm{sr}}/(\sigma L_{\mathrm{s}}\cdot L_{\mathrm{r}})\\ 0 & \mathrm{j}\omega_{\mathrm{r}}\end{pmatrix}\begin{pmatrix}\underline{\boldsymbol{i}}_{\mathrm{s}}^{\alpha\beta}\\ \underline{\boldsymbol{\Psi}}_{\mathrm{r}}^{\alpha\beta}\end{pmatrix}+\frac{1}{\sigma L_{\mathrm{s}}}\begin{pmatrix}\underline{\boldsymbol{v}}_{\mathrm{s}}^{\alpha\beta}\\ \mathbf{0}\end{pmatrix} \tag{3.41}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{pmatrix}\boldsymbol{i}_{\mathrm{s}}^{\alpha\beta}\\ \boldsymbol{\Psi}_{\mathrm{r}}^{\alpha\beta}\end{pmatrix}=\boldsymbol{K}_{11}\cdot\begin{pmatrix}\boldsymbol{i}_{\mathrm{s}}^{\alpha\beta}\\ \boldsymbol{\Psi}_{\mathrm{r}}^{\alpha\beta}\end{pmatrix}+\omega_{\mathrm{r}}\cdot\boldsymbol{K}_{12}\cdot\begin{pmatrix}\boldsymbol{i}_{\mathrm{s}}^{\alpha\beta}\\ \boldsymbol{\Psi}_{\mathrm{r}}^{\alpha\beta}\end{pmatrix}+K_{13}\cdot\begin{pmatrix}\boldsymbol{v}_{\mathrm{s}}^{\alpha\beta}\\ \mathbf{0}\end{pmatrix} \tag{3.42}$$

where $\boldsymbol{K}_{11}=\frac{1}{\sigma L_{\mathrm{s}}}\begin{pmatrix}-R_{\mathrm{s}}-M_{\mathrm{sr}}^2R_{\mathrm{r}}/L_{\mathrm{r}}^2 & 0 & M_{\mathrm{sr}}R_{\mathrm{r}}/L_{\mathrm{r}}^2 & 0\\ 0 & -R_{\mathrm{s}}-M_{\mathrm{sr}}^2R_{\mathrm{r}}/L_{\mathrm{r}}^2 & 0 & M_{\mathrm{sr}}R_{\mathrm{r}}/L_{\mathrm{r}}^2\\ \sigma L_{\mathrm{s}}\cdot M_{\mathrm{sr}}R_{\mathrm{r}}/L_{\mathrm{r}} & 0 & -\sigma L_{\mathrm{s}}\cdot R_{\mathrm{r}}/L_{\mathrm{r}} & 0\\ 0 & \sigma L_{\mathrm{s}}\cdot M_{\mathrm{sr}}R_{\mathrm{r}}/L_{\mathrm{r}} & 0 & -\sigma L_{\mathrm{s}}\cdot R_{\mathrm{r}}/L_{\mathrm{r}}\end{pmatrix}$

and $\boldsymbol{K}_{12}=\begin{pmatrix}0 & 0 & 0 & M_{\mathrm{sr}}/(\sigma L_{\mathrm{s}}\cdot L_{\mathrm{r}})\\ 0 & 0 & -M_{\mathrm{sr}}/(\sigma L_{\mathrm{s}}\cdot L_{\mathrm{r}}) & 0\\ 0 & 0 & 0 & -1\\ 0 & 0 & 1 & 0\end{pmatrix}$

and $K_{13}=\frac{1}{\sigma L_{\mathrm{s}}}$

Dynamical model of electromagnetic torque

The production of electromagnetic torque is based on the interaction between the magnetic air gap flux density and the current loading in the machine [40]. Its calculation can be transferred to the stator flux and current, leading to the following equation:

$$T_{\mathrm{e}}=\frac{3}{2}z_{\mathrm{p}}\cdot\boldsymbol{\Psi}_{\mathrm{s}}^{\alpha\beta}\times\boldsymbol{i}_{\mathrm{s}}^{\alpha\beta}=\frac{3}{2}z_{\mathrm{p}}\cdot|\boldsymbol{\Psi}_{\mathrm{s}}^{\alpha\beta}|\cdot|\boldsymbol{i}_{\mathrm{s}}^{\alpha\beta}|\cdot\sin(\theta_{\Psi\rightarrow\mathrm{i}}) \tag{3.43}$$

where z_{p} is the machine's number of pole pairs

The torque equation also holds in any other reference frame. Secondly, Eqn. (3.39) and (3.40) can be utilized to express the electromagnetic torque in terms of other quantities that describe the machine's electrical state, i.e. a combination of two vectors from $\{\boldsymbol{\Psi}_{\mathrm{s}},\boldsymbol{\Psi}_{\mathrm{r}},\boldsymbol{i}_{\mathrm{s}},\boldsymbol{i}_{\mathrm{r}}\}$. Examples for alternative torque equations are given in Eqn. (3.44) - (3.45).

$$T_{\mathrm{e}}=\frac{3}{2}z_{\mathrm{p}}\cdot\frac{M_{\mathrm{sr}}}{L_{\mathrm{r}}}\cdot\boldsymbol{\Psi}_{\mathrm{r}}^{\alpha\beta}\times\boldsymbol{i}_{\mathrm{s}}^{\alpha\beta}=\frac{3}{2}z_{\mathrm{p}}\cdot\frac{M_{\mathrm{sr}}}{L_{\mathrm{r}}}\cdot|\boldsymbol{\Psi}_{\mathrm{r}}^{\alpha\beta}|\cdot|\boldsymbol{i}_{\mathrm{s}}^{\alpha\beta}|\cdot\sin(\theta_{\Psi\rightarrow\mathrm{i}}) \tag{3.44}$$

$$T_{\mathrm{e}}=\frac{3}{2}z_{\mathrm{p}}\cdot\frac{M_{\mathrm{sr}}}{\sigma L_{\mathrm{s}}L_{\mathrm{r}}}\cdot\boldsymbol{\Psi}_{\mathrm{r}}^{\alpha\beta}\times\boldsymbol{\Psi}_{\mathrm{s}}^{\alpha\beta}=\frac{3}{2}z_{\mathrm{p}}\cdot\frac{M_{\mathrm{sr}}}{\sigma L_{\mathrm{s}}L_{\mathrm{r}}}\cdot|\boldsymbol{\Psi}_{\mathrm{r}}^{\alpha\beta}|\cdot|\boldsymbol{\Psi}_{\mathrm{s}}^{\alpha\beta}|\cdot\sin(\theta_{\Psi\mathrm{r}\rightarrow}\Psi\mathrm{s}) \tag{3.45}$$

Dynamic model of rotor speed

The mechanical angular speed of the rotor ω_{m} results from the time integral of net torque available at the machine shaft. Compared to the dynamics of the electrical quantities, it usually reacts very sluggish to the applied torque due to large values of rotational inertia θ_{m}.

$$\omega_{\mathrm{m}}(t)=\int_0^t\frac{1}{\theta_{\mathrm{m}}}\cdot\big(T_{\mathrm{e}}(\tau)-T_{\mathrm{load}}(\tau)\big)\mathrm{d}\tau \tag{3.46}$$

The mechanical angular speed ω_m relates to the electrical angular speed of the rotor via $\omega_\mathrm{r} = z_\mathrm{p} \cdot \omega_\mathrm{m}$, where z_p is the number of pole pairs of the respective machine.

Flux estimators
Under negligence of special measurement instrumentation, only the stator currents of the induction machine can be measured directly. On the other hand (and as previously noted), at least one additional quantity is needed to completely describe the dynamics of the machine, including its electromechanical torque. As will be shown in Chapter 4, this likewise applies to the implementation of a performant current, torque or flux controller. There are several possibilities to acquire this additional quantity.

The derived state-space model of the induction machine can be utilized to estimate the missing quantity, if the stators currents are measured and the applied stator voltages are known[18]. For example, an iteratively executed calculation of Eq. (3.41) provides an estimate for $\underline{\boldsymbol{\Psi}}_\mathrm{r}^{\alpha\beta}$. However, due to parameter uncertainties between the model and plant (e.g. temperature dependency etc.), significant errors can occur in the estimation. Two typical estimators are given in the following:

$$\text{according to Eq. (3.37):} \quad \underline{\boldsymbol{\Psi}}_\mathrm{s}^{\alpha\beta}(t) = \int_0^t \left(\underline{\boldsymbol{v}}_\mathrm{s}^{\alpha\beta}(\tau) - R_s \underline{\boldsymbol{i}}_\mathrm{s}^{\alpha\beta}(\tau) \right) \mathrm{d}\tau \tag{3.47}$$

$$\text{...in Laplace domain:} \quad \underline{\boldsymbol{\Psi}}_\mathrm{s}^{\alpha\beta}(s) = \frac{\underline{\boldsymbol{v}}_\mathrm{s}^{\alpha\beta}(s) - R_\mathrm{s} \underline{\boldsymbol{i}}_\mathrm{s}^{\alpha\beta}(s)}{s} \tag{3.48}$$

$$\text{extracted from Eq. (3.41):} \quad \underline{\boldsymbol{\Psi}}_\mathrm{r}^{\alpha\beta}(t) = \int_0^t \frac{-(1 - j\omega_\mathrm{r} \cdot \tau_\mathrm{r}^*) \cdot \underline{\boldsymbol{\Psi}}_\mathrm{r}^{\alpha\beta}(\tau) + M_\mathrm{sr} \cdot \underline{\boldsymbol{i}}_\mathrm{s}^{\alpha\beta}}{\tau_\mathrm{r}^*} \mathrm{d}\tau \tag{3.49}$$

$$\text{...in Laplace domain:} \quad \underline{\boldsymbol{\Psi}}_\mathrm{r}^{\alpha\beta}(s) = \frac{M_\mathrm{sr}}{1 - j\omega_\mathrm{r}\tau_\mathrm{r}^* + s\tau_\mathrm{r}^*} \cdot \underline{\boldsymbol{i}}_\mathrm{s}^{\alpha\beta}(s) \tag{3.50}$$

$$\text{where} \quad \tau_\mathrm{r}^* = L_\mathrm{r}/R_\mathrm{r}$$

Equation (3.48) is also known as the *voltage model* and Eq. (3.50) as the *current model* for flux linkage estimation. Note that with the help of Eq. (3.40) the voltage model can also be expressed in terms of $\boldsymbol{\Psi}_\mathrm{r}^{\alpha\beta}$, $\boldsymbol{i}_\mathrm{s}^{\alpha\beta}$, $\boldsymbol{v}_\mathrm{s}^{\alpha\beta}$ and the current model in terms of $\boldsymbol{\Psi}_\mathrm{s}^{\alpha\beta}$, $\boldsymbol{i}_\mathrm{s}^{\alpha\beta}$.

The open-loop integrator makes the voltage model susceptible for offset errors in the current measurement. On the other hand, the current model is dependent on the rotor resistance R_r, which is more difficult to determine and tends to have higher temperature variations. The quality of the estimation can be improved by using more sophisticated estimators, such as a Luenberger observer [42] or Kalman filter [43], which themselves come in several variations more or less suitable for induction machines [44]. The main idea of these kind of observers is to enhance the estimation performed by the plant model by measurement feedbacks of the actual plant.

Speed estimation
As can be seen in the system equations of the induction machine and in the current model for flux estimation, the rotor speed is an essential quantity for the machine modeling. The availability of ω_r is even more so important, if a speed control loop is supposed to be implemented.

[18] The stator voltages do not necessarily have to be measured. For instance, in the case of an inverter-fed machine, the applied voltage vectors are known, as they correspond the respective controller output. Moreover, a more sophisticated model with the consideration of the inverter's nonlinearities can further improve the accuracy [41].

In this thesis, the rotor speed is assumed to be available through encoder measurements. However, the methods mentioned for flux estimators and observers can generally also be applied for speed estimation. In literature, a wide variety of different techniques are described for sensorless control, which shall not be further discussed here.

3.2.2. Influence of Spatial Harmonics

As mentioned in the beginning of this chapter, this thesis does not cover the influence of spatial harmonics within the induction machine in detail. Nonetheless, their cause, effects and justification for their negligence shall be briefly provided here. Many of the following explanations as well as any underived equations are based on the fundamental work provided in [45].

Spatial harmonics within the air gap's flux density B_δ of the machine usually appear for two reasons: Firstly, due to the distributed placement of coil windings in slots, and secondly due to iron saturation. The latter occurs as a third harmonic, being in phase with the respective fundamental wave. The resulting distortion leads to a flattening top of the overall flux density, which resembles the saturation effects well. On the other hand, the spatial harmonics due to slotting results in an overall step-like shaped field. The appearing harmonics have several ordinal numbers ν that follow the scheme $\nu = 1 + 2m_\mathrm{s} \cdot g$, where $m_\mathrm{s} \in \mathbb{N}$ is the number of stator phases and $g \in \mathbb{Z}$ is used for the enumeration. Similarly, ordinal numbers μ for spatial harmonics that result from the rotor slots can be calculated[19]. The harmonics' wave lengths and speeds decrease with $\sim {}^1\!/_\nu$ or $\sim {}^1\!/_\mu$, respectively. Further, the sign of the ordinal number indicates the direction of the harmonic wave's propagation.

Depending on the actual winding type (e.g. single layer or double layer winding with respective pitching) and the number of slots, the amplitude of the spatial harmonics can vary strongly with respect to the ordinal number. An example of spatial harmonics for a two-layer stator winding with $5/6$ pitch and two slots per pole and phase is given in Figure 3.18. Although the spatial harmonics have a much lower amplitude than the fundamental wave (e.g. $8\,\%$ for the harmonic with poorest damping by pitching etc.), they can have some noticeable and unfavorable effects:

1. Harmonic rotor bar currents that are induced by spatial field harmonics of the stator. They entail additional losses.
2. Harmonic stator currents that are induced by spatial field harmonics of the rotor. They cause additional losses and may lead to EMI issues (if the machine is used as a generator).
3. Asynchronous harmonic torque that results from spatial stator harmonics of ordinal number ν and the corresponding induced rotor currents. Analogously to the torque of the fundamental wave, it can be calculated with the well known Kloss function, but under consideration of the harmonic quantities (modified inductance values, slip etc.).
4. Synchronous harmonic torque that occurs for particular harmonics of ν, μ (spatial stator harmonics together with spatial rotor harmonics). This synchronous torque appears if the harmonic stator and rotor waves have identical speed and length.

[19] Note that in case of a squirrel cage induction machine, the number of rotor phases m_r is equal to ${}^{Q_\mathrm{r}}\!/_{z_\mathrm{p}}$, where Q_r is the number of rotor bars / rotor slots and z_p is the number of pole pairs. This is the case since each rotor bar per pole pair can be interpreted as a rotor phase consisting of ${}^1\!/_2$ turns. As usually m_r and ${}^{Q_\mathrm{r}}\!/_{z_\mathrm{p}} > 3$ holds, equal ordinal numbers $\nu = \mu$ can exists, while their overall enumeration can however differ quite largely.

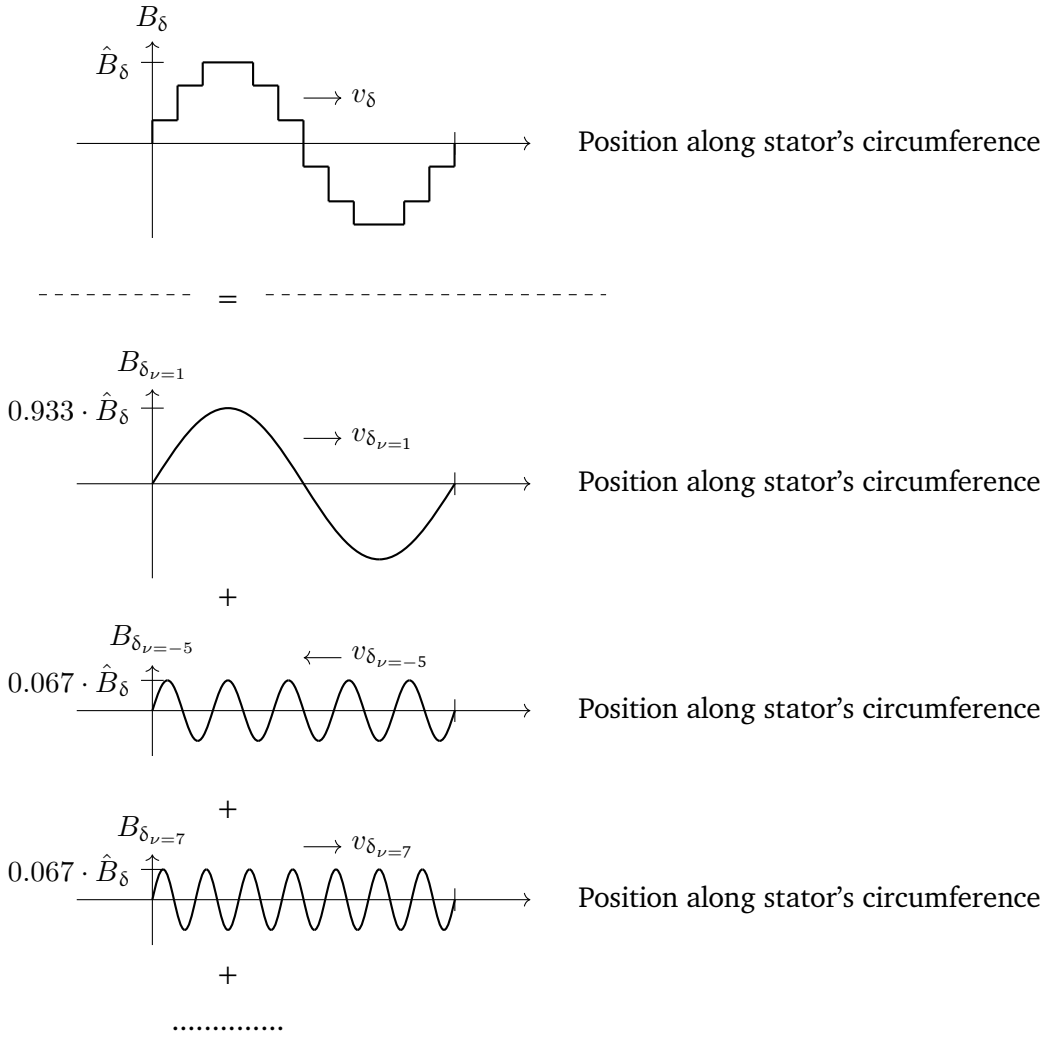


Figure 3.18.: Example of a step-like shaped air gap field B_δ and its separation into fundamental (index 1) and fifth, seventh (indexes -5, 7) harmonic wave along the stator's circumference.

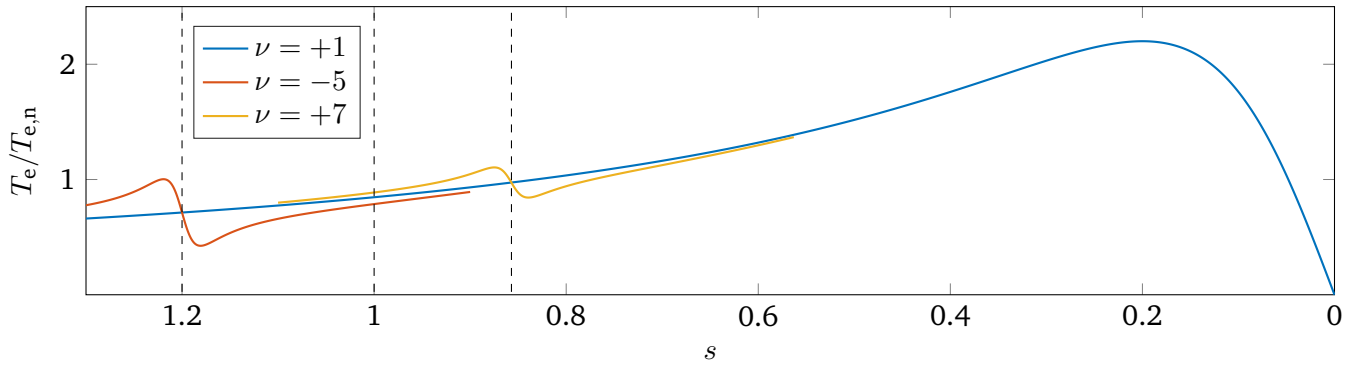


Figure 3.19.: Example for asynchronous harmonic torque for the ordinal numbers $\nu = -5$ and $\nu = +7$, together with the fundamental asynchronous torque ($\nu = +1$).

While the stator current harmonics can be kept at bay via fast current control, the harmonic torque distortions can usually not be compensated due to missing direct measurements of flux density and/or electromagnetic torque. However, it can be shown that the harmonic torque components appear at higher slips. The reason for this is the decreased speed of the harmonic waves, shifting and compressing the respective torque contributions towards $s = 1$. Such high slips can largely be avoided with variable-frequency drives, i.e. the harmonic torque components can be mostly averted.

For the sake of completeness, it should be mentioned that a thorough modeling of spatial harmonics usually requires FEM-based analysis [46] or detailed measurements for parameterization [47]. Lastly, an alternative approach is given in [48], where the system matrix of the induction machine is expanded in order to take into account a definable spatial resolution for the (analytically described) discrete slotting. This method maintains the possibility of utilizing environments for ordinary differential equations, such as Matlab. The approach can further be extended with nonlinear saturation curves. However, it only shows a modest performance when compared to the generally more accurate results that can be acquired via FEM-analysis.

3.2.3. Field-Oriented Model of Induction Machine

Transformation to field-aligned reference system
The field-oriented modeling is a very effective method to simplify the analysis and control complexity for electrical drives. As the name suggests, this modeling can be achieved by transforming the state-space representation and torque equation of the induction machine to a reference frame aligned with the rotor flux (axis d and q, superscript dq). The placement of the axis for this reference frame, which is rotating with the speed of the rotor flux ω_k, is shown in Figure 3.20. Note that the q-component of $\boldsymbol{\Psi_\mathrm{r}}$ vanishes in this chosen alignment.

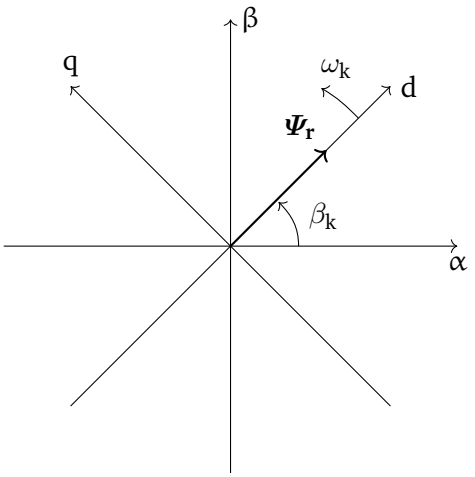


Figure 3.20.: Rotor flux aligned reference frame (dq-reference frame) in relation to alpha-beta reference frame.

The rotation of Eq. (3.51) can be applied to the state-space representation of the induction machine in the $\alpha\beta$-frame (Eq. (3.41) and Eq. (3.44)) to acquire the field-oriented representation. Figure 3.21 depicts the equivalent circuit of the induction machine in the respective dq-reference frame.

$$\underline{\boldsymbol{g}}^{\alpha\beta} = \underline{\boldsymbol{g}}^{\mathrm{dq}} \cdot e^{\mathrm{j}\beta_\mathrm{k}} \tag{3.51}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{pmatrix}\underline{\boldsymbol{i}}_\mathrm{s}^\mathrm{dq}\\ \underline{\boldsymbol{\Psi}}_\mathrm{r}^\mathrm{dq}\end{pmatrix} = \frac{1}{\sigma L_\mathrm{s}}\begin{pmatrix}-R_\mathrm{s}-M_\mathrm{sr}^2R_\mathrm{r}/L_\mathrm{r}^2 & M_\mathrm{sr}R_\mathrm{r}/L_\mathrm{r}^2\\ \sigma L_\mathrm{s}\cdot M_\mathrm{sr}R_\mathrm{r}/L_\mathrm{r} & -\sigma L_\mathrm{s}\cdot R_\mathrm{r}/L_\mathrm{r}\end{pmatrix}\begin{pmatrix}\underline{\boldsymbol{i}}_\mathrm{s}^\mathrm{dq}\\ \underline{\boldsymbol{\Psi}}_\mathrm{r}^\mathrm{dq}\end{pmatrix} + \ldots$$
$$\begin{pmatrix}-\mathrm{j}\omega_\mathrm{k} & -\mathrm{j}\omega_\mathrm{r}\cdot M_\mathrm{sr}/(\sigma L_\mathrm{s}\cdot L_\mathrm{r})\\ 0 & \mathrm{j}(\omega_\mathrm{r}-\omega_\mathrm{k})\end{pmatrix}\begin{pmatrix}\underline{\boldsymbol{i}}_\mathrm{s}^\mathrm{dq}\\ \underline{\boldsymbol{\Psi}}_\mathrm{r}^\mathrm{dq}\end{pmatrix} + \frac{1}{\sigma L_\mathrm{s}}\begin{pmatrix}\underline{\boldsymbol{v}}_\mathrm{s}^\mathrm{dq}\\ \mathbf{0}\end{pmatrix} \tag{3.52}$$

$$T_\mathrm{e} = \frac{3}{2}z_\mathrm{p}\cdot\frac{M_\mathrm{sr}}{L_\mathrm{r}}\cdot\boldsymbol{\Psi}_\mathrm{r}^\mathrm{dq}\times\boldsymbol{i}_\mathrm{s}^\mathrm{dq} = \frac{3}{2}z_\mathrm{p}\cdot\frac{M_\mathrm{sr}}{L_\mathrm{r}}\cdot|\boldsymbol{\Psi}_\mathrm{r}^\mathrm{dq}|\cdot|\boldsymbol{i}_\mathrm{s}^\mathrm{dq}|\cdot\sin(\theta_{\Psi\to\mathrm{i}}) \tag{3.53}$$

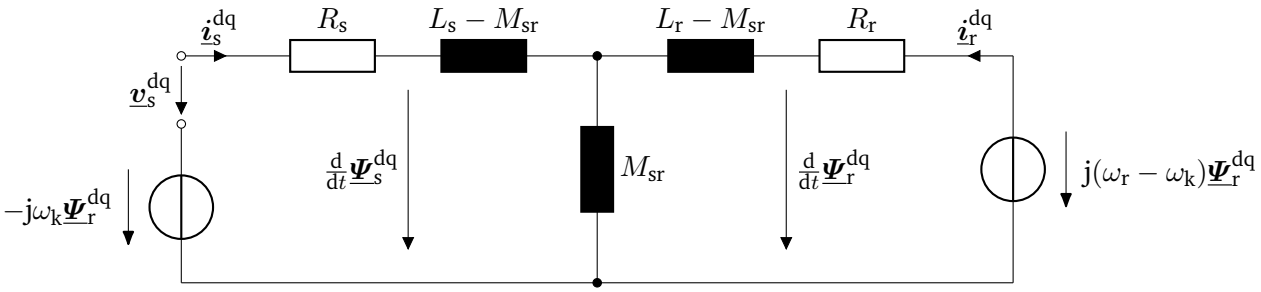


Figure 3.21.: Equivalent circuit model of the induction machine for the dq-reference frame, based on mutual inductance.

The dynamics of the machine can also be illustrated as block diagrams. Figure A.2 and Figure A.3 in the appendix provide these diagrams for the stator and rotor in the field-oriented reference frame, respectively. They are expressed in the Laplace domain.

Derivation of control law and other implications
If field orientation is assumed to be acquired and also to be maintained, $\Psi_\mathrm{r,q} = {}^\mathrm{d}/_{\mathrm{d}t}\,\Psi_\mathrm{r,q} = 0$ has to hold. This has implications on the the rotor flux and torque equations, as given and further elaborated in the following.

$$\frac{\mathrm{d}}{\mathrm{d}t}\Psi_\mathrm{r,d} = -\frac{R_\mathrm{r}}{L_\mathrm{r}}\cdot\Psi_\mathrm{r,d} + \frac{M_\mathrm{sr}R_\mathrm{r}}{L_\mathrm{r}}\cdot i_\mathrm{s,d} \tag{3.54}$$
$$\frac{\mathrm{d}}{\mathrm{d}t}\Psi_\mathrm{r,q} = (\omega_\mathrm{r}-\omega_\mathrm{k})\cdot\Psi_\mathrm{r,d} + \frac{M_\mathrm{sr}R_\mathrm{r}}{L_\mathrm{r}}\cdot i_\mathrm{s,q} = 0 \tag{3.55}$$
$$T_\mathrm{e} = \frac{3}{2}z_\mathrm{p}\cdot\frac{M_\mathrm{sr}}{L_\mathrm{r}}\cdot\Psi_\mathrm{r,d}\cdot i_\mathrm{s,q} \tag{3.56}$$

- Equation (3.55): It can be rewritten to $\omega_\mathrm{k}-\omega_\mathrm{r} = ({}^{M_\mathrm{sr}R_\mathrm{r}}/_{L_\mathrm{r}})\cdot({}^{i_\mathrm{1,q}}/_{\Psi_\mathrm{r,d}})$, which can be interpreted as the field-oriented control law. It imposes a specific rotor slip[20] $s = 1-{}^{\omega_\mathrm{r}}/_{\omega_\mathrm{k}}$ on the machine and depends on its magnetization and electromagnetic torque.
- Equation (3.54): Due to the alignment with the d-axis, the complete rotor magnetization appears in $\Psi_\mathrm{r,d}$. It can be controlled solely by the d-component of the stator current.
- Equation (3.56): The torque can be manipulated dynamically with the q-component of the stator current, while the rather sluggishly behaving rotor flux maintains the machine's magnetization.

[20] with respect to *electrical* revolutions

The advantage of the field orientation is that the originally nonlinear torque control problem is reduced to a linear control problem for the two separated current components $i_{1,\mathrm{d}}, i_{1,\mathrm{q}}$. It should be noted that the principle is based on the assumption that the stator currents can be controlled accurately and in a fast manner. Specifically, if the use of linear controllers is anticipated, the feedback of $\Psi_{\mathrm{r,d}}$ on the stator currents should be treatable as a disturbance. In fact, this is the case due to the generally sluggish behavior of the rotor flux.

Attainment of field-orientation
The purpose and benefits of the field-orientation have been discussed. However, the question remains how field-orientation can actually be attained. For this reason, the two main methods shall shortly be explained in the following [49].

1. Indirect field-orientation: The reference values (indicated with an asterisk) for the stator currents and the slip follow directly from the reference values for the rotor flux and the electromagnetic torque.

$$\text{according to Eq. (3.54):}\quad i^*_{\mathrm{s,d}} = \frac{L_r}{M_{\mathrm{sr}} R_{\mathrm{r}}} \cdot \frac{\mathrm{d}}{\mathrm{d}t}\Psi^*_{\mathrm{r,d}} + \frac{1}{M_{\mathrm{sr}}} \cdot \Psi^*_{\mathrm{r,d}} \tag{3.57}$$

$$\text{...in Laplace domain:}\quad i^*_{\mathrm{s,d}}(s) = \left(s \cdot \frac{L_{\mathrm{r}}}{M_{\mathrm{sr}} R_{\mathrm{r}}} + \frac{1}{M_{\mathrm{sr}}}\right) \cdot \Psi^*_{\mathrm{r,d}}(s) \tag{3.58}$$

$$\text{according to Eq. (3.56):}\quad i^*_{\mathrm{s,q}} = \frac{2}{3 z_{\mathrm{p}}} \cdot \frac{L_{\mathrm{r}}}{M_{\mathrm{sr}}} \cdot \frac{T^*_{\mathrm{e}}}{\Psi^*_{\mathrm{r,d}}} \tag{3.59}$$

$$\text{according to Eq. (3.55):}\quad \omega^*_{\mathrm{k}} - \omega_{\mathrm{r}} = \frac{M_{\mathrm{sr}} R_{\mathrm{r}}}{L_{\mathrm{r}}} \cdot \frac{i^*_{\mathrm{s,q}}}{\Psi^*_{\mathrm{r,d}}} \tag{3.60}$$

   By integrating ω^*_{k}, the reference value for the field alignment β^*_{k} can be determined. This angle is used for transforming the stator current reference values to the stator-fixed alpha-beta reference frame, which is the natural reference frame for the inverter and its modulator.

   The indirect field-orientation can be interpreted as choosing the appropriate slip for the reference torque on a precalculated Kloss curve, which itself is dependent on the current rotor speed and desired machine magnetization. Conversely, no *direct* field-orientation (e.g. via a flux measurement or estimation) is performed. The entire flux alignment and reference value determination is therefore an open-loop process.

2. Direct field-orientation: In contrast to the previously explained principle of indirect field-orientation, the direct-field orientation relies on the measurement / estimation of the rotor flux. Estimators or observers as introduced in Section 3.2.1, e.g. Eq. (3.49), can be used to obtain the estimated rotor flux in the $\alpha\beta$-reference system $\underline{\widetilde{\boldsymbol{\Psi}}}_{\mathrm{r}}^{\alpha\beta}$. The argument of $\underline{\widetilde{\boldsymbol{\Psi}}}_{\mathrm{r}}^{\alpha\beta}$ corresponds by definition with the estimated angle for the field-oriented reference frame. Analogously to the method for the indirect field-orientation, this angle is used to transform the stator currents and controller outputs between the dq-reference and alpha-beta reference frame, respectively.

   The utilization of the estimated rotor flux closes a feedback loop for the field-alignment. For this reason, it can be assumed to be more accurate than the indirect field orientation. Nevertheless, due to parameter mismatches within the estimator model, deviations between the estimated field orientation $\widetilde{\beta}_{\mathrm{k}}$ and actual field orientation β_{k} should be anticipated. The estimated rotor flux can further be used for an improved determination of the stator current reference values. Firstly, the reference value of the rotor flux in Eq. (3.59) can be replaced with the magnitude of the estimated rotor flux. Secondly, instead

of using the transfer function in Eq. (3.58), a closed feedback loop can be implemented for achieving faster flux control.

The overall controller structures for indirect and direct field-oriented control are shown in Figure 3.22. For the sake of simplicity, it is given entirely in the Laplace domain, i.e. does not consider any sample and hold or sampling characteristics.

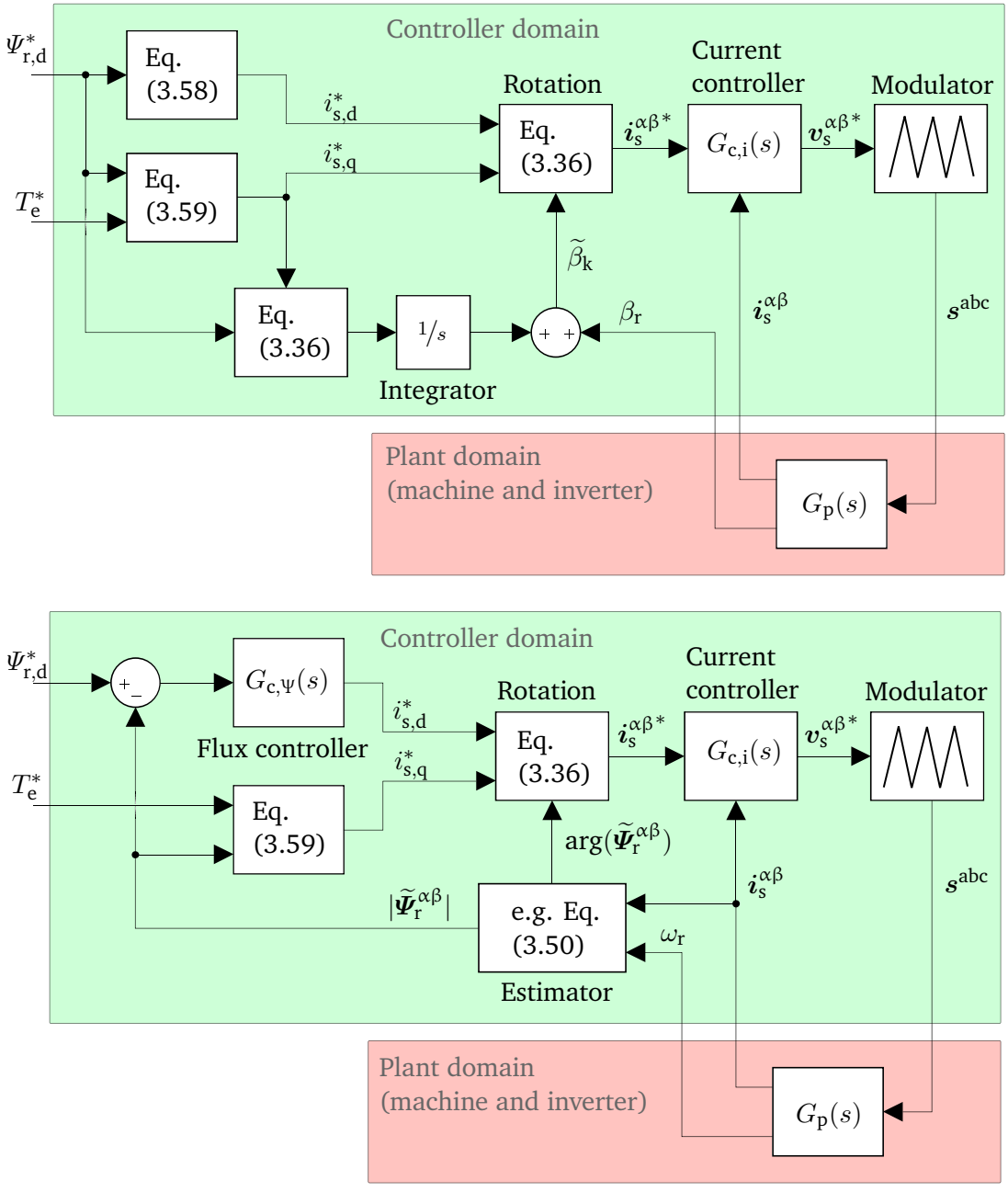


Figure 3.22.: Control loop structure for indirect (top) and direct (bottom) field-oriented control.

Sluggishness of rotor flux linkage
The relative sluggishness of the rotor flux linkage $\underline{\boldsymbol{\Psi}}_{\mathrm{r}}^{\mathrm{dq}}$ already becomes visible due to the missing *direct* impact of the stator voltage $\underline{\boldsymbol{v}}_{\mathrm{s}}^{\mathrm{dq}}$ in Eq. (3.52) and block diagrams given in Figure A.2 and A.3. Nevertheless, it can be also identified easily when transforming Eq. (3.52) into the Laplace domain:

$$\underline{\boldsymbol{i}}_{\mathrm{s}}^{\mathrm{dq}}(s) = \frac{1}{\sigma L_{\mathrm{s}}} \cdot \frac{\tau_{\mathrm{s}}^*}{1 + \mathrm{j}\omega_{\mathrm{k}} \cdot \sigma L_{\mathrm{s}} + s\tau_{\mathrm{s}}^*} \cdot \left(\underline{\boldsymbol{v}}_{\mathrm{s}}^{\mathrm{dq}}(s) + \left(\frac{M_{\mathrm{sr}} R_{\mathrm{r}}}{L_{\mathrm{r}}^2} + \mathrm{j}(\omega_{\mathrm{k}} - \omega_{\mathrm{r}}) \frac{M_{\mathrm{sr}}}{L_{\mathrm{r}}^2} \right) \underline{\boldsymbol{\Psi}}_{\mathrm{r}}^{\mathrm{dq}}(s) \right) \tag{3.61}$$

$$\underline{\boldsymbol{\Psi}}_{\mathrm{r}}^{\mathrm{dq}}(s) = \frac{M}{1 + \mathrm{j}(\omega_{\mathrm{k}} - \omega_{\mathrm{r}}) \cdot \tau_{\mathrm{r}}^* + s\tau_{\mathrm{r}}^*} \cdot \underline{i}_{\mathrm{s}}^{\mathrm{dq}}(s) \tag{3.62}$$

$$\text{where } \tau_{\mathrm{s}}^* = \frac{\sigma L_{\mathrm{s}}}{R_{\mathrm{s}} + (R_{\mathrm{r}} M_{\mathrm{sr}}^2)/L_{\mathrm{r}}^2}$$

$$\text{and} \quad \tau_{\mathrm{r}}^* = L_{\mathrm{r}}/R_{\mathrm{r}}$$

Clearly, the transfer functions $\underline{\boldsymbol{i}}_{\mathrm{s}}^{\mathrm{dq}}(s)$ and $\underline{\boldsymbol{\Psi}}_{\mathrm{r}}^{\mathrm{dq}}(s)$ include a first order lag behavior with the respective time constants τ_{s}^* and τ_{r}^*, where $\tau_{\mathrm{r}}^* \gg \tau_{\mathrm{s}}^*$ holds. While the input for $\underline{\boldsymbol{i}}_{\mathrm{s}}^{\mathrm{dq}}(s)$ is the stator voltage (including some distortions from the rotor flux), the input for $\underline{\boldsymbol{\Psi}}_{\mathrm{r}}^{\mathrm{dq}}(s)$ is the stator current itself. Therefore, the influence of the stator voltage on the rotor flux will have a prolonged time constant (combination of τ_{s}^* and τ_{r}^*) and a stronger attenuation for high frequencies (two first order lag elements $\rightarrow$ second order lag element, i.e. -40 dB/decade).

3.2.4. Inverter-Fed Induction Machines

Feeding electrical machines with an inverter brings upon the possibility of realizing variable-speed drives, and more specifically also the control of electromagnetic torque and flux (cp. e.g. Section 3.2.3 and Chapter 4). While the control of electromagnetic torque correlates with the speed and consumed or generated power of the machine, the control of magnetization allows special operating modes. These include field-weakening mode for speeds beyond the nominal value or machine operation low DC-link voltages. Furthermore, optimal values for machine magnetization can be determined to minimize its anticipated losses. The theory of this optimal reference magnetization for induction machines is provided in this section.

Secondly, inverter-fed induction machines experience specific parasitic effects due to the time-modulated input voltage, which further usually also includes a non-zero common-mode component. Several modulation techniques exist, such as sinusoidal pulse width modulation, space vector modulation, discontinuous pulse width modulations [3] etc. They each have a step-like shaped input voltage in common, though the severity of unfavorable impacts can differ. However, the step-like shape of the voltage implies time harmonics that are superimposed to the desired fundamental or reference signal of the modulation. There are three main effects that can be linked to these time harmonics: An additional current ripple and torque ripple and $\mathrm{d}v/\mathrm{d}t$-effects[21]. Moreover, the non-zero common-mode component of the input voltage can trigger parasitic common-mode currents. All of these aspects are discussed in this section.

Optimal reference magnetization
A straightforward way to decrease the anticipated machine losses is the application of optimal magnetization. In the case of induction machines, it utilizes an offline optimization to acquire setpoints for the reference flux at given torque and speed, leading to the least amount of copper and iron losses within the machine. In order to derive the optimal relation $\Psi_{\mathrm{s,opt}}^*(\omega_{\mathrm{r}}, T_{\mathrm{e}}^*)$, the equivalent circuit of the induction machine can be

[21] Although another effect of the time harmonics, the emergence of accoustic noise is not considered in this thesis

extended with an equivalent resistance that represents the magnetization losses of the machine, as provided in Figure 3.23.

If a constant input voltage $\underline{\boldsymbol{v}}_{\mathrm{s}}^{\mathrm{dq}}$ and machine speed ω_{r} is assumed, all of the quantities in the figure are dc values.[22] The voltage drops at the inductances can therefore be omitted. Any quantity can now be calculated in dependence of the machine parameters $R_{\mathrm{s}}, R_{\mathrm{r}}$,.., the machine's speed ω_{r} and the input voltage $\underline{\boldsymbol{v}}_{\mathrm{s}}^{\mathrm{dq}}$. Note that this might require substitutions via Eq. (3.39), which brings back the dependency on the parameters L_{s} etc.

The equivalent resistance $R_{\mathrm{fe,ser}}$ is multiplied with ω_{k} to represent the dependency on performed hysteresis cycles. The linear dependency shows that a constant imaginary component of $\underline{\mu}_{\mathrm{r}}$ is assumed (cp. Section 3.1.2). The equivalent resistance R_{fe} is labeled with the subscript *ser* to point out the placement of it in the schematic. Very often the component is also placed in parallel to M_{sr}. However, the values for either position can be acquired by solving the equation $X_{\mathrm{sr}} + R_{\mathrm{fe,ser}} = X_{\mathrm{sr}} || R_{\mathrm{fe,par}}$ for the desired quantity.[23]

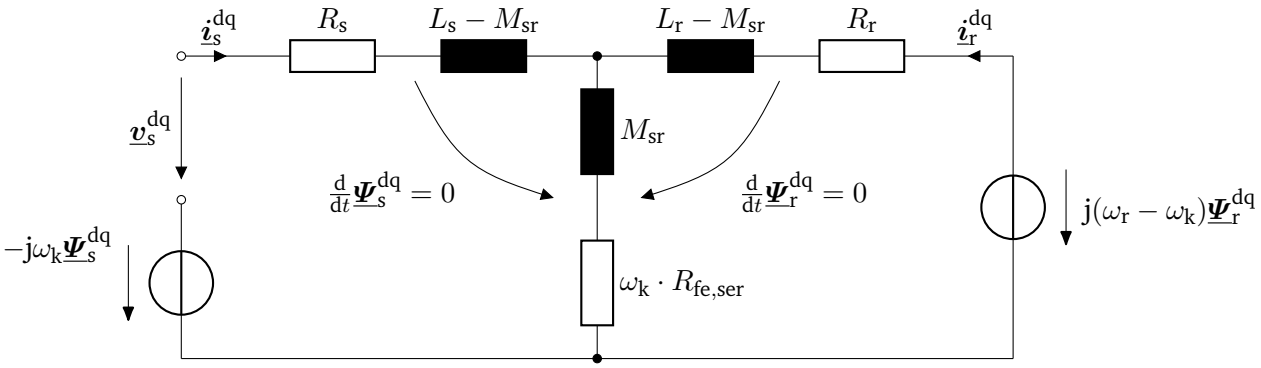


Figure 3.23.: Equivalent circuit model of the induction machine for the dq-reference frame including magnetization losses, based on mutual inductance and for a constant excitation $\underline{\boldsymbol{v}}_{\mathrm{s}}^{\mathrm{dq}}$.

In the next step, the parameter ω_{k} can be replaced in terms of $\Psi_{\mathrm{r,d}}$, T_{e} and ω_{r} by applying Eqn. (3.55) - (3.56), i.e. considering the corresponding slip. Eventually, equations that represent losses, input power and output power[24] can be expressed with the quantities $\omega_{\mathrm{r}}, T_{\mathrm{e}}, \Psi_{\mathrm{s}}$ or $\omega_{\mathrm{r}}, T_{\mathrm{e}}, \Psi_{\mathrm{r}}$, as well as the machine parameters. Performing a numerical analysis that minimizes $\eta = P_{\mathrm{im,out}}/P_{\mathrm{im,in}}$, the optimal stator or rotor flux magnitude can be acquired for various torque and speeds. An exemplary result is given in Figure 3.24, which is based on the parameters of the induction machine used for this thesis (cp. Table B.1).

It can be identified that the optimal stator flux magnitude has the tendency to decrease for lower speeds and torque, while it even increases beyond the rated flux for high values of requested torque. In order to avoid saturation and ensure proper controllability, the flux reference should be limited with upper and lower boundaries, e.g. $\Psi_{\mathrm{s,opt}} \in [1/3 \cdot \Psi_{\mathrm{s,n}}\ ,\ \Psi_{\mathrm{s,n}}]$.

[22] This is the case for an ideal stationary operating condition. Note that a constant $\underline{\boldsymbol{v}}_{\mathrm{s}}^{\mathrm{dq}}$ does imply that all quantities represented in the $\alpha\beta$-reference frame are rotating with a constant speed ω_{k}.

[23] It is crucial to consider that this transformation is only valid for the specific chosen value of ω_{k}, which however does not impair the analysis provided here.

[24] Losses (copper and magnetization): $P_{\mathrm{IM,cu}} = R_{\mathrm{s}} \cdot i_{\mathrm{s}}^2 + R_{\mathrm{r}} \cdot i_{\mathrm{r}}^2$, $P_{\mathrm{im,fe}} = R_{\mathrm{fe,ser}} \cdot (i_{\mathrm{s}} + i_{\mathrm{r}})^2$, input power: $P_{\mathrm{im,in}} = 3 \cdot v_{\mathrm{s}} \cdot i_{\mathrm{s}}$, output power: $P_{\mathrm{im,out}} = T_{\mathrm{e}} \cdot \omega_{\mathrm{r}}$

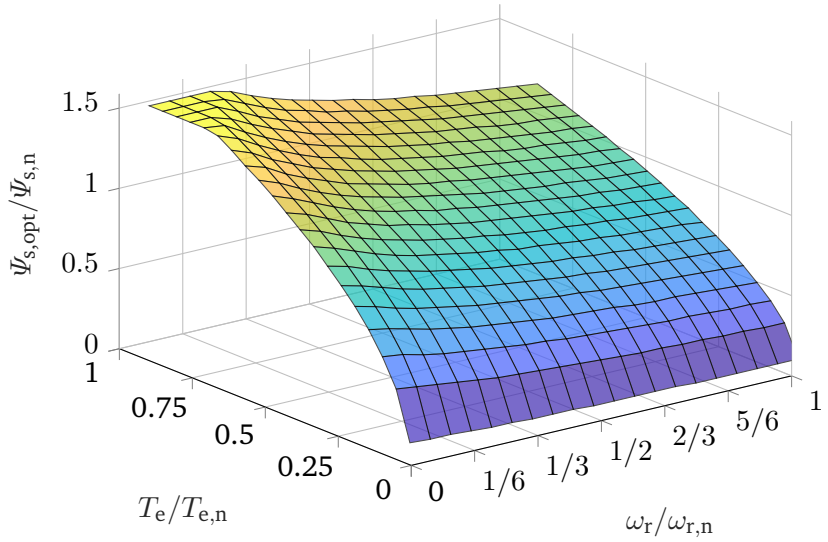


Figure 3.24.: Exemplary data of optimal stator flux for minimizing machine losses [50], based on machine parameters used for this thesis (cp. Table B.1).

For the sake of completeness, it has to be mentioned that the discussed method of optimal reference magnetization only brings advantages at stationary operating points: The derivation for the optimal flux was based on the assumption of subsided transients, which cannot be guaranteed for dynamic machine operation (particularly due to the slugghish rotor flux). Larger changes in the torque reference therefore may not be reproduced properly by the controller and machine. Secondly, a frequently changing T_{e}^{*} may lead to very large losses, if the setpoint adjustment of machine magnetization fails to follow in a sufficiently dynamic manner and hence leads to blatantly unfavorable flux values.

Additional current ripple

Since the voltage time harmonics induced by the inverter can be interpreted as additional voltage input components, the induction machine will react to these excitations as well. A harmonic analysis can be performed by transferring the equivalent circuit model of Figure 3.17 to the Fourier domain, as given in Figure 3.25. Note that this model is further based on the leakage representation, which relies on the transformed rotor quantities[25] $L'_{\mathrm{r}\sigma}, R'_{\mathrm{r}}, i'_{\mathrm{r}}$. Due to the introduction of the harmonic's slip s_l, the entire circuit can be formulated in terms of the specifiable harmonic input frequency $\nu\omega_{\mathrm{k}}$ [45].

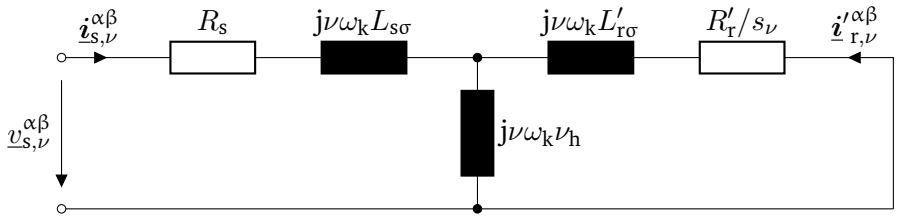


Figure 3.25.: Equivalent circuit model of the induction machine for the alpha-beta reference frame with harmonic input frequencies $\nu\omega_{\mathrm{s}}$, based on leakage inductances.

[25]The transformed rotor quantities take the turns ratio of the stator and rotor circuit into account, allowing the separation of magnetizing inductance L_{h} and pure stray inductances $L_{\mathrm{s}\sigma}, L'_{\mathrm{r}\sigma}$.

High input frequencies $\nu\omega_s$ lead to a very large magnetizing reactance $\nu\omega_\mathrm{k}L_\mathrm{h}$. On the other hand, the slip for harmonics can be approximated to $s_\nu = {}^{(\nu\omega_\mathrm{k}-\omega_\mathrm{r})}/_{\nu\omega_\mathrm{k}} \approx 1$, since their rotating fields move much faster than the rotor, which rotates approximately with the speed of the fundamental. This suggests independence of the respective load condition, which otherwise varies strongly with the slip. In summary, the following approximation for the ν-th harmonic and the corresponding harmonic current losses can be made:

$$i_{\mathrm{s},\nu} \approx \frac{v_{\mathrm{s},\nu}}{\sqrt{\nu\omega_\mathrm{k} \cdot \left(R_\mathrm{s}/\omega_{\mathrm{k,n}} + R'_\mathrm{r}/(2\pi\ \sqrt{\mathrm{Hz}} \cdot s_\nu)\right)^2 + (\nu\omega_\mathrm{s})^2 \cdot (L_{\mathrm{s}\sigma} + L'_{\mathrm{r}\sigma})^2}} \tag{3.63}$$

$$P_{\mathrm{im,ripple}} \approx 3 \sum_\nu \sqrt{\nu\omega_\mathrm{k}} \cdot \left(R_\mathrm{s}/\omega_{\mathrm{k,n}} + R'_\mathrm{r}/(2\pi\ \sqrt{\mathrm{Hz}} \cdot s_\nu)\right) \cdot i^2_{\mathrm{s},\nu} \tag{3.64}$$

Note that the increase of $R'_\mathrm{r}, R_\mathrm{s}$ due to current displacement effects is considered by the factors $\sqrt{\nu\omega_\mathrm{k}/(2\pi\ \mathrm{Hz})}$ and $\sqrt{\nu\omega_\mathrm{k}/\omega_{\mathrm{k,n}}}$ [51], which assumes that the nominal measured resistance values are acquired at $\omega_{\mathrm{k,n}}$ and a slip of $s = 2\%$. If the voltage harmonics have a sufficiently high frequency, i.e. the relation $(\nu\omega_\mathrm{k})^2(L_{\mathrm{s}\sigma} + L'_{\mathrm{r}\sigma})^2 \gg \nu\omega_\mathrm{k} \cdot (R_\mathrm{s}/\omega_{\mathrm{k,n}} + R'_\mathrm{r}/(2\pi\ \sqrt{\mathrm{Hz}} \cdot s_\nu))^2$ holds, the harmonic currents are mainly limited by the leakage inductances and decrease with ${}^1/_{\nu\omega_\mathrm{k}}$. The harmonic ohmic losses $P_{\mathrm{IM,ripple}}$ therefore tend to decrease with $\nu^{-3/2}$.

Additional torque ripple

In analogy to the synchronous and asynchronous torque due to spatial harmonics (cp. Section 3.2.1), the time harmonics can induce a pulsating torque, i.e. a torque ripple. The main contribution comes from the combination of time harmonics with the fundamental wave, as the product of two harmonics obviously leads to very small amplitudes. In comparison to the harmonic torque due to spatial harmonics, the frequency of the time harmonics can vary with the speed of the machine. This is due to their derivation of the fundamental wave, which obviously covers a large frequency range for different rotor speeds. Although the time harmonics with low ordinal numbers, e.g. $-5, 7$, have low amplitudes (assuming sufficiently high switching frequencies), they might lead to torque ripple in the frequency range where torsion resonance may occur [45].

Insulation stress due to $\mathrm{d}v/\mathrm{d}t$-effects

Fast changes of the machine's stator voltage, i.e. high values of $|{}^{\mathrm{d}v_\mathrm{s}}/_{\mathrm{d}t}|$ can be problematic because of the resulting voltage stress on the stator windings' insulation. Repetitive voltage surges may cause partial discharges that can finally lead to its break down. Particularly, adjacent phases within the winding overhangs and adjacent wires of coil windings are considered to be the most critical cases [52]. Usually it is the phase-to-phase and not the phase-to-midpoint voltage that is being considered. The reason is that the phase-to-phase voltage is either directly involved (insulation of adjacent phases) or it is the voltage that is of larger amplitude, therefore also involving higher $|{}^{\mathrm{d}v_\mathrm{s}}/_{\mathrm{d}t}|$. As an example, the IEC standard IEC 60034-25 specifies allowable voltage rates of $13\,\mathrm{kV}$ and $19\,\mathrm{kV}$ for machines with nominal stator voltages of up to $500\,\mathrm{V}$ and $690\,\mathrm{V}$, respectively.

Fast switching devices inherently lead to high values of $|{}^{\mathrm{d}v_\mathrm{s}}/_{\mathrm{d}t}|$. Next to this, another effect tends to even further increase these potentially problematic values due to transient voltage overshoots: The cable between inverter and motor terminals acts as transmission line, transmitting pulses generated by the converter. As for any wave propagations, the cable ends are subject to reflection phenomena. The reflection at the motor and inverter terminals can be calculated according to the following two equations:

$$r_\mathrm{motor} = \frac{Z_\mathrm{motor} - Z_\mathrm{cable}}{Z_\mathrm{motor} + Z_\mathrm{cable}} \tag{3.65}$$

$$r_\mathrm{inv} = \frac{Z_\mathrm{inv} - Z_\mathrm{cable}}{Z_\mathrm{inv} + Z_\mathrm{cable}} \tag{3.66}$$

The impedances Z_{motor}, Z_{inv} and Z_{cable} are the high-frequency wave impedances of the according systems. Exemplary values are $r_{\text{inv}} \approx -1$, $r_{\text{motor}} \approx 0.75$ for large and $r_{\text{motor}} \approx 0.95$ for small electrical machines, respectively [45]. The propagation time t_{prop}, i.e. the duration for the wave traveling from the inverter to the motor terminals or vice versa, is directly dependent on the cable length l_{cable} and the wave's velocity v_{cable}, which is determined via the following equations [26].

$$v_{\text{cable}} = \frac{1}{\sqrt{L'_{\text{cable}} C'_{\text{cable}}}} \tag{3.67}$$

$$t_{\text{prop}} = \frac{l_{\text{cable}}}{v_{\text{cable}}} \tag{3.68}$$

where L', C' indicates the values per unit length

Voltage overshoots at the machine terminals occur if the rise time t_{rise} of an applied voltage step is in the range of or even significantly smaller than t_{prop}. For example, if $t_{\text{rise}} = 0$ holds, the full amplitude of the voltage step reaches the motor terminals at $t = t_{\text{prop}}$ and is superimposed to its immediate reflection, increasing the voltage stress on the local winding insulation. The reflected wave reaches the inverter at $2t_{\text{prop}}$ and gets reflected there again, in turn traveling towards the motor terminals. Overall, an oscillation with the frequency $f_{\text{prop}} = 1/4t_{\text{prop}}$ with specific damping correlated to the reflection factors is built up. An exemplary pattern of the voltage at the motor terminals is shown in Figure 3.26.

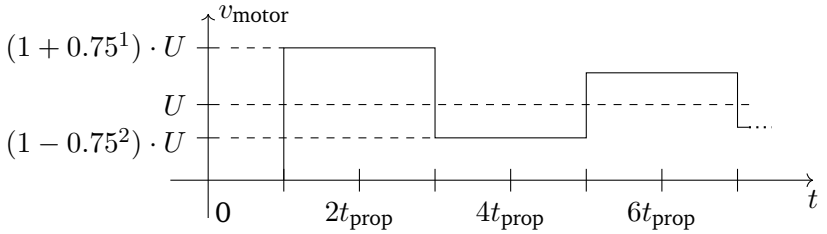


Figure 3.26.: Time characteristic of motor terminal voltage v_{motor} after an applied voltage step U from the inverter at $t = 0$ ($t_{\text{rise}} = 0$, $r_{\text{inv}} = -1$, $r_{\text{motor}} = 0.75$).

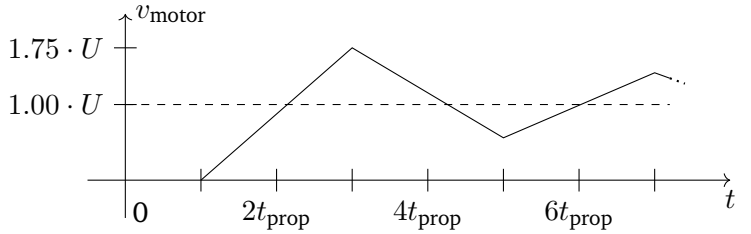


Figure 3.27.: Time characteristic of motor terminal voltage v_{motor} analogous to Figure 3.26, but with $t_{\text{rise}} = 2t_{\text{prop}}$.

The stress on the insulation is alleviated for $t_{\text{rise}} > 2t_{\text{prop}}$, as this implies that the full amplitude of the voltage step is not entirely built up at $t = 3t_{\text{prop}}$, while the inverter reflections already start to decrease the motor terminal voltage. The transitional case for $t_{\text{rise}} = 2t_{\text{prop}}$ is depicted in Figure 3.27.

[26] for this investigation, lossless cables are assumed.

In order to ensure an actual alleviation, several possibilities exist. As proposed in [52], measures include high quality motor insulation, output filters and combined "inverter motors" that secure short motor cables (aspiring $t_{\text{rise}} \gg 2t_{\text{prop}}$). Lastly, carefully designed PWMs or controller implementations can also decrease the stress on the insulation system by generally reducing the appearing $|\mathrm{d}v_{\text{s}}/\mathrm{d}t|$ (cp. Section 4.3.4).

Parasitic common-mode currents
Most commonly, the star point of induction machines is floating, i.e. is not connected to any DC-link potential or the ground. Under negligence of any parasitics, this means that there is an infinite common-mode impedance between the load and the inverter and a common-mode current cannot flow. However, the machine windings not only constitute an inductive behavior, but also a capacitive one among each other and towards neighboring components [53]. These couplings close a circuit with the DC-link of the inverter and can therefore generally allow a (small) common-mode current to flow. The parasitic capacitances are normally small enough to keep this current bounded to an unharmful level. Nonetheless, if sufficiently high common-mode voltages are applied, electric-discharge-machining currents can appear at the lubricant of the machine's bearing. During the time of the discharge, the bearing acts as a low-impedance component. This leads to a short-term increase of the common-mode current, which can significantly damage the motor bearing and generally decreases its lifetime expectancy in a substantial manner[27].

Remedies for the parasitic common-mode currents are described in the IEC standard 60034-17. Specifically, filters such as common-mode chokes can be applied between the motor and inverter, which can however be bulky, expensive and increase the system's losses. Another approach is the careful design of PWM methods that reduce the common-mode voltage applied to the machine terminals [54]. Similarly to the latter, special controller implementations are presented in Section 4.3.5.

3.3. Mathematical Model of Overall System

The mathematical model of the overall system is acquired by inserting the subsystem equations into each other, eliminating as many variables as possible. Eventually, the desired linear and time-variant state-space representation[28] should have a form according to Eqn. (3.69) and (3.70).

$$\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{x}(t) = \boldsymbol{A}(t)\boldsymbol{x}(t) + \boldsymbol{B}(t)\boldsymbol{u}(t) \tag{3.69}$$

$$\boldsymbol{y}(t) = \boldsymbol{C}(t)\boldsymbol{x}(t) + \boldsymbol{D}(t)\boldsymbol{u}(t) \tag{3.70}$$

Nonetheless, before this procedure is conducted, it stands to reason to make a case distinction between plant models (mimicking the real systems behavior) and controller models (for controller implementation).

Plant model
Regarding the plant model, it should be possible to consider asymmetries and parameter deviations in order to investigate their respective performance impacts. For this reason, the matrix forms of the subsystem equations have to be used, which are derived and provided in their final form in Appendix A. Exemplary steps for the derivation of the overall plant model are also provided there. The resulting plant model representation is given in Eq. (3.71).

[27] Also other mechanisms that damage the motor bearings and are directly linked to parasitic common-mode current exist [53]. For the sake of simplicity, they are not further discussed in this thesis.

[28] The linearity is given only if the non-linearities of Section 3.1.2 etc. are neglected. The machine's speed ω_{r} is treated as a merely slowly changing, time-variant parameter that is measurable via an encoder.

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\\ \boldsymbol{i}_1\end{pmatrix} = \left(\boldsymbol{A}_{\text{plant}'} + \omega_\mathrm{r}(t)\cdot\boldsymbol{A}_{\text{plant}''}\right)\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\\ \boldsymbol{i}_1\end{pmatrix} + \boldsymbol{B}_\text{plant}\begin{pmatrix}\boldsymbol{v}_1\\ \boldsymbol{v}_2\end{pmatrix} \tag{3.71}$$

Note that the system matrix $\boldsymbol{A}(t)$ can be split up into a constant and a time-variant part, namely $\boldsymbol{A}_{\text{plant}'}$ and $\omega_\mathrm{r}(t)\cdot\boldsymbol{A}_{\text{plant}''}$. The output states $\boldsymbol{y}(t)$ are omitted here, since the variables of interest are yet to be defined (cp. Chapter 4). The rank of the system of equations is 7.

Controller model

The main simplification that can be applied to the controller model is the assumption of symmetric parameters for the interleaving chokes. This assumption is based on the premise that deviations and asymmetries are related to changes during operation, such as temperature dependencies etc., which are not known to the control designer. Further, deviations *between* the windings etc. are expected to be low due to similar ambient conditions. This presumption allows to preserve the scalar values of Eqn. (3.17) - (3.19) instead of expanding them to matrices. The system of equations is defined as given in Eq. (3.72).

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\\ \boldsymbol{i}_1\end{pmatrix} = \left(\boldsymbol{A}_{\mathrm{c}'} + \omega_\mathrm{r}(t)\cdot\boldsymbol{A}_{\mathrm{c}''}\right)\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\\ \boldsymbol{i}_1\end{pmatrix} + \boldsymbol{B}_\mathrm{c}\begin{pmatrix}\boldsymbol{v}_1\\ \boldsymbol{v}_2\end{pmatrix} \tag{3.72}$$

Further simplifications, which may lead to more 0-entries in $\boldsymbol{A}_{\mathrm{c}'}$, $\boldsymbol{A}_{\mathrm{c}''}$, $\boldsymbol{B}_\mathrm{c}$ and therefore potentially reduces the computational effort for the controller, are analyzed in Section 4.3.11.

4. Finite Control Set Model Predictive Control

Model predictive control (MPC) is a powerful control principle that receives increasing attention in the power electronics community, beginning approximately in the early 2000s [55]. However, it was originally developed already in the 1960s as an application of optimal control theory and has been successfully applied in the chemical process industry since then [56]. The progressing adaption of MPC for power electronic applications is strongly linked to the improved computational capabilities of control platforms. Nowadays, it is possible to implement model predictive controllers with sample rates in the range of $100\,\mathrm{kHz}$ and higher while using "cost-optimized" configurable logic systems (cp. Chapter 5). Particularly, finite control set model predictive controllers (FCS-MPC) show an outstanding suitability for power electronics applications, since this control principle further takes advantage of the discrete nature of the power switches [57].

This chapter provides the basic terms, principles and advantages of (FCS-)MPC, its application for induction machine control, and finally its implementation and simulation results for the investigated system of this thesis. The hardware implementation and experimental results are provided in Chapter 5 and Chapter 6.

4.1. Basics of Model Predictive Control

Before the aspects of MPC are discussed in more detail, its suitability for the control of induction machines shall be pointed out briefly in the following section. In order to do so, a short introduction of the classical approaches and a comparison with their respective alternatives is performed. Please be aware that this comparison should not be interpreted as a complete review of every available control technique, but rather as a rough guideline or motivation for the utilization of FCS-MPC.

4.1.1. Overview of Classical Controller Types and possible Alternatives for Machine Control

In the domain of torque controlled induction machines, there are two well-known concepts that can be considered to be the classical approaches: Field-oriented control (FOC) and direct torque control (DTC). It is possible to combine these concepts with rather simple PI and hysteresis controllers, respectively, which demand very low computational effort.

Field-oriented control with PI controllers
The field-oriented principle for induction machines was already introduced in Section 3.2.3. It was shown that as soon as field-orientation is attained, the torque and flux control problem can be simplified to the control of the two stator current components $i_{\mathrm{s,d}}$ and $i_{\mathrm{s,q}}$. The plant transfer functions for these currents ($G_{\mathrm{i_A}}(s) = {i_{\mathrm{s,d}}(s)}/{v_{\mathrm{s,d}}(s)}$ and $G_{\mathrm{i_B}}(s) = {i_{\mathrm{s,q}}(s)}/{v_{\mathrm{s,q}}(s)}$) are first order lag elements. They further include additional distortions due to cross-coupling of the stator currents, as well as the rotor flux (cp. for example Eq. (3.61) or Figure A.2).

The current controllers can be implemented as PI controllers and tuned according to the magnitude optimum [58]. The design of the controller is performed in the Laplace domain and subsequently transformed to

the Z-domain (e.g. via the bilinear transform / Tustin's method)[1]. PI controllers are usually robust enough to withstand the inflicting distortions, i.e. the previously mentioned cross-couplings. However, their performance can be improved with an appropriate feedforward structure.

The method of field-oriented control with PI controllers certainly is a control principle that was widely adopted for many industrial processes, and it has been proven to work well. On the other hand, it also brings some disadvantages, which are shortly summarized in the following:

1. Since the feed-forward structure only approximates the actual plant dynamics, a perfect decoupling cannot be achieved. This entails reactions of the controlled torque during reference steps for the machine's magnetization and vice versa[2].

2. The dynamics of the controlled stator currents and therefore of the torque is only poor. The tuned (magnitude optimum) closed loop transfer function of the stator current (arbitrary component / phase) can usually be approximated with a first order lag element, having the time constant $2\tau_\Sigma$. This time constant is the summation of all uncompensated time constants of the plant [58]. Conversely, the dominant time constant τ_s^* for the stator current is compensated by the controller and does not appear in the closed loop transfer function.

$$G_{\text{FOC,closed}}(s) = \frac{i_s(s)}{i_{s,\text{ref}}(s)} \approx \frac{1}{1 + s \cdot 2\tau_\Sigma}$$

$$\text{with} \qquad f_g = \frac{1}{2\pi \cdot 2\tau_\Sigma} \qquad \text{(cut-off frequency of closed control loop)}$$

   The time constant τ_Σ is often outweighed by the bandwidth of the current sensor, or the time lag introduced by the modulation of the inverter. In the latter case, τ_Σ can be approximated with the switching period $T_{sw} = 1/f_{sw}$. Therefore, a switching frequency of $f_{sw} = 10\,\text{kHz}$ leads to a cut-off frequency of $f_g = \frac{f_{sw}}{2\pi \cdot 2} \approx 800\,\text{Hz}$ and a controller bandwidth of $[0\,\text{Hz}, 800\,\text{Hz}]$.

3. The use of PI controllers, which are linear controllers, do not consider any constraints of the system, such as the limited voltage amplitude related to the inverter's DC-link. Therefore, the closed loop performance of the tuned controllers only applies for the small signal behavior, i.e. small reference steps, and can be substantially worse otherwise. For the same reason, the implementation of anti-windup techniques should be considered.

Field-oriented control with full state feedback via pole placement

If an outer field-oriented loop is implemented (cp. e.g. Figure 3.22), a current control is sufficient to acquire torque and flux control for the induction machine. The current control does not necessarily have to implemented with PI controllers, but can also be implemented via a full state feedback with pole placement. As its name suggests, the peculiarity of such method is that not only the output quantities, but also other system variables are fed back, eventually allowing a (in theory) arbitrary pole placement for the controlled system [59]. Particularly, this is possible due to the consideration of all of the system's variables, allowing an effective decoupling etc.

[1] It is assumed that the time discretization that is introduced via a digital controller implementation has only a negligible impact on the overall performance, if the sampling time is significantly higher than the dominant time constant of the system.

[2] This drawback is in fact inherent to the dynamics of the induction machine. Nevertheless, a prioritization or a constraining of the cross-coupling related errors is not possible with this technique.

Nevertheless, the full state feedback with pole placement can only be implemented straight-forwardly for linear systems. This is problematic for two reasons: Firstly and predominantly, very small values for the placed poles (corresponding with high dynamics) require large controller gains, which may lead to leaving the linear region of the system. This is largely due to the finite DC-link voltage available for the inverter and can lead to a distortion of the tuned poles. Secondly, the state-space representation of induction machines contains the rotational speed of the machine ω_r, which is dependent on load conditions and the produced electromagnetic torque of the machine. Even if ω_r changes comparably slow with respect to the electrical time constants, allowing to treat the system as a time-variant system rather than a nonlinear one, considerable adaptions such as gain scheduling have to be made.

Field-oriented control with full state feedback as linear-quadratic regulator
Another popular method for designing controllers for linear systems are linear-quadratic regulators. In this case, a cost function is defined that describes the error between the state variables and their respective reference values. The error terms can be expressed quadratically in terms of the state variables, explaining the name of this controller concept [60]. Similarly, the control effort can be included in the cost function. Eventually, a (constant) full state feedback which minimizes the cost function can be determined numerically. This is performed by solving the so-called algebraic Riccati equation, which follows from the cost function and system description. Note that identically to the pole placement controller, this approach only works properly in the case of linear systems. Hence, its application for the control of induction machines needs specific adaptions and its anticipated performance can be impaired, as already described above.

Direct torque control
The method of direct torque control (DTC) utilizes the equations of the induction machine, but does not aim at the design or tuning of a linear torque controller. In contrast, it relies on the division of the $\alpha\beta$-reference frame in six distinct sectors[3]. Based on the current sector the stator flux is positioned in, a look-up table provides the information which voltage space vectors can be applied for an increase, decrease or approximate conservation of the machine's electromagnetic torque. Similarly, the look-up table is augmented with the appropriate voltage space vectors for manipulating the stator flux's magnitude [58]. Two hysteresis controllers can finally be implemented to keep the desired torque and machine magnetization within a predefined band.

Next to its extraordinary simplicity, the advantage of the DTC method is a highly dynamic performance. However, it comes at the disadvantage of a variable switching frequency and the lack of steady-state accuracy. The latter can be improved by including predictive elements within the control algorithm. For example, predicted slopes of the torque can be utilized to determine optimal switching instants to match the mean of the electromagnetic torque with its reference value.

4.1.2. General Formulation for Model Predictive Control

The fundamental concept of model predictive control is the following: A time-discrete mathematical model of the plant is used in order to predict future system states $\boldsymbol{x}$ and system outputs $\boldsymbol{y}$. The number of predicted states and outputs corresponds to the prediction horizon N_p. The inputs for the predictions consist of the control vector $\boldsymbol{u}$ and the current (measured) version of the state vector. Each of the predicted states and system outputs are evaluated by a cost function J and restricted by the constraints $\boldsymbol{\mathcal{X}}$ and $\boldsymbol{\mathcal{Y}}$, respectively. The cost function often expresses the tracking error to reference signals, which is then minimized. The control vector corresponds to the optimization variables of this minimization problem, with $\boldsymbol{u}^*$ being the optimum.

[3]These sectors are bounded by the voltage limit and two respectively neighboring voltage space vectors, cp. e.g. Figure 3.2.

Several future states $\boldsymbol{X}$ and system outputs $\boldsymbol{Y}$ can be taken into account within the cost function J. In this case, the total costs are a summation of all of the predicted stage costs, computed by J', respectively. Moreover, the consideration of several future states leads to a sequence of optimal control vectors $\boldsymbol{U}^*$ that is found for every executed step of the algorithm. However, only the imminent control vector of this sequence will be applied to the plant, while the rest of the acquired sequence is discarded.

In summary, the MPC works as an iterative optimization with receding horizon. Figure 4.1 illustrates the basic structure of the MPC within a control loop. The optimization problem is formulated as given in Eqn. (4.1). The set $\boldsymbol{\mathcal{U}}^{N_\mathrm{p}}$ is the control set that the MPC can utilize. If it is restricted to the discrete switching states ($N_\mathrm{p} = 1$) or sequence of switching states ($N_\mathrm{p} > 1$) of the inverter, the resulting structure is a FCS-MPC. On the other hand, a control set without these restrictions corresponds to a CCS-MPC (continuous control set). Note that neither the controller's system model functions $\boldsymbol{f}_\mathrm{c}$ and $\boldsymbol{h}_\mathrm{c}$, nor the cost function of Eqn. (4.1) necessarily have to be linear.

$$
\begin{aligned}
\underset{\boldsymbol{U}(k)}{\text{minimize}} \quad & J\left(\boldsymbol{X}(k+1), \boldsymbol{Y}(k+1), \boldsymbol{U}(k)\right) = \sum_{l=k}^{k+N_\mathrm{p}-1} J'\left(\boldsymbol{x}(l+1), \boldsymbol{y}(l+1), \boldsymbol{u}(l)\right) \\
\text{subject to} \quad & \boldsymbol{X}(k+1) = \left(\boldsymbol{x}^\mathrm{T}(k+1), \boldsymbol{x}^\mathrm{T}(k+2), ..., \boldsymbol{x}^\mathrm{T}(k+N_\mathrm{p})\right)^\mathrm{T} \\
& \boldsymbol{Y}(k+1) = \left(\boldsymbol{y}^\mathrm{T}(k+1), \boldsymbol{y}^\mathrm{T}(k+2), ..., \boldsymbol{y}^\mathrm{T}(k+N_\mathrm{p})\right)^\mathrm{T} \\
& \boldsymbol{U}(k) = \left(\boldsymbol{u}^\mathrm{T}(k), \boldsymbol{u}^\mathrm{T}(k+1), ..., \boldsymbol{u}^\mathrm{T}(k+N_\mathrm{p}-1)\right)^\mathrm{T} \\
& \boldsymbol{x}(l+1) \in \boldsymbol{\mathcal{X}} \; \forall \; l = k, ..., k+N_\mathrm{p}-1 \\
& \boldsymbol{y}(l+1) \in \boldsymbol{\mathcal{Y}} \; \forall \; l = k, ..., k+N_\mathrm{p}-1 \\
& \boldsymbol{u}(l) \qquad \in \boldsymbol{\mathcal{U}} \; \forall \; l = k, ..., k+N_\mathrm{p}-1 \\
& \boldsymbol{x}(l+1) = \boldsymbol{f}_\mathrm{c}\left(\boldsymbol{x}(l), \boldsymbol{u}(l)\right) \; \forall \; l = k, ..., k+N_\mathrm{p}-1 \\
& \boldsymbol{y}(l+1) = \boldsymbol{h}_\mathrm{c}\left(\boldsymbol{x}(l), \boldsymbol{u}(l)\right) \; \forall \; l = k, ..., k+N_\mathrm{p}-1
\end{aligned}
\tag{4.1}
$$

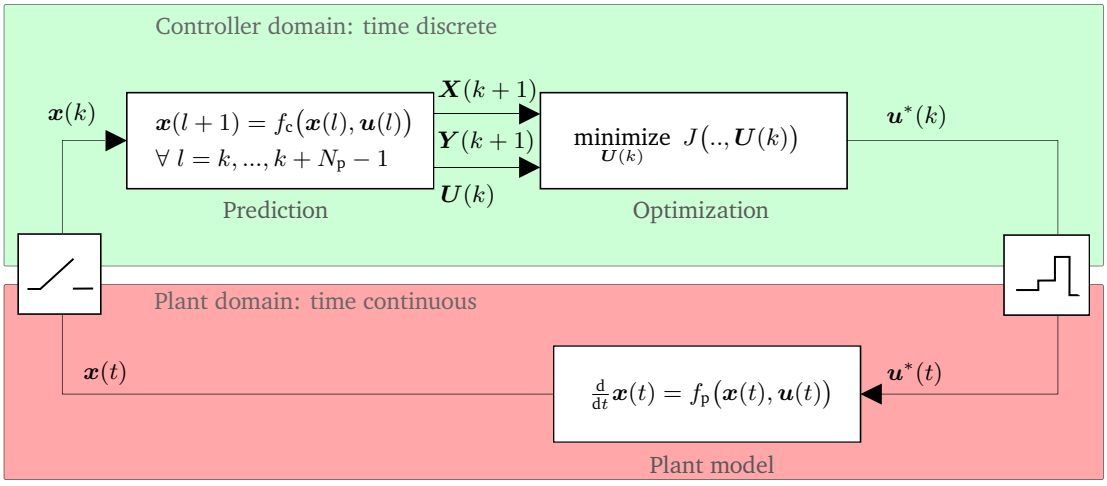


Figure 4.1.: Basic structure of model predictive control loop.

4.1.3. Time Discretization

Since MPC implementations rely on a time-discrete plant model, but the true characteristics of an induction machine however are described in the time-continuous domain, a respective discretization has to be applied to its mathematical model. Generally speaking, there are many methods for performing such discretization, allowing a numerical approximation of the plant's time characteristics and therefore also the state predictions. These methods can be divided into implicit and explicit methods, as well as single-step or multi-step methods, e.g:

1. Single-step, explicit: Euler forward method
2. Single-step, implicit: Euler backward method
3. Single/multi-step (using intermediate steps), explicit or implicit: Runge-Kutta methods
4. Multi-step (using past values), explicit: Adams-Bashforth methods

The decision on which discretization to use is dependent on the available computational power, acceptable tolerance for anticipated errors, and the general stability of the respective method [61]. For example, the Euler forward method can be implemented very easily by the following approximation:

$$\frac{\mathrm{d}}{\mathrm{d}t}x(t) \approx \frac{x(k+1)-x(k)}{T_\mathrm{s}}$$

$$\rightarrow \quad \boldsymbol{x}(k+1) = (\boldsymbol{A}\cdot T_\mathrm{s} + \boldsymbol{I})\cdot \boldsymbol{x}(k) + \boldsymbol{B}\cdot T_\mathrm{s}\cdot \boldsymbol{u}(k) \qquad \text{(for linear, time-invariant systems)} \tag{4.2}$$

$$\rightarrow \quad \boldsymbol{x}(k+1) = (\boldsymbol{A}(k)\cdot T_\mathrm{s} + \boldsymbol{I})\cdot \boldsymbol{x}(k) + \boldsymbol{B}(k)\cdot T_\mathrm{s}\cdot \boldsymbol{u}(k) \qquad \text{(for linear, time-variant systems)} \tag{4.3}$$

where T_s is the respective sample time and $\boldsymbol{I}$ is the identity matrix of appropriate dimension. Note that the system is assumed to be either inherently linear or linearized for the current sampling. While the Euler forward is strikingly easy to implement, it does converge rather slowly towards the solution of the original, time-continuous differential equations, and can even become unstable if too large sample times are chosen. For this reason, usually enhanced versions of the Euler forward method are used, e.g. Heun's method, representing the transition towards higher-order, explicit Runge-Kutta methods.

However, MPC implementations ensure that the system input $\boldsymbol{u}$ remains constant throughout the sampling time interval of the controller. This provides the possibility of solving the time-continuous differential equation for a discrete time step, yielding the exact solution for time-discretized systems (Euler exact):

$$\boldsymbol{x}(k+1) = \boldsymbol{A}_\text{exact}\cdot \boldsymbol{x}(k) + \boldsymbol{B}_\text{exact}\cdot \boldsymbol{u}(k) \tag{4.4}$$

$$\text{where } \boldsymbol{A}_\text{exact} = \mathrm{e}^{\boldsymbol{A}\cdot T_\mathrm{s}} \tag{4.5}$$

$$\text{and} \quad \boldsymbol{B}_\text{exact} = \boldsymbol{A}^{-1}\cdot\left(\mathrm{e}^{\boldsymbol{A}\cdot T_\mathrm{s}} - \boldsymbol{I}\right)\cdot \boldsymbol{B} \tag{4.6}$$

In the given equations, $\mathrm{e}^{(*)}$ represents the matrix potential. The Euler forward method can therefore be seen as first-order approximation of the Euler exact solution. Note that $\boldsymbol{B}_\text{exact}$ can only be determined if $\boldsymbol{A}$ is invertible.

In order to prevent distortions for any simulation results, the Euler exact method is consistently utilized in Chapter 4 of this thesis[4]. Nevertheless, the method becomes impractical for real-time implementations, since

[4] Exempt the discretization of the flux estimator; it relies on the input $\boldsymbol{i}_\mathrm{s}$, which is not piece-wise constant. Therefore, the estimator equations are solved with Adams-Bashforth method instead [62].

a time-variant[5] system matrix $\boldsymbol{A}$ would necessitate repetitive calculations of the matrix potential appearing in Eq. (4.6). For this reason, the real-time controller implementation is based on the Euler forward method. An analysis of the respective impact is provided in Section 4.3.12.

4.1.4. Time Compensation

In comparison to controller implementations in purely simulational environments, any hardware based real-time implementation of control algorithms will introduce some sort of computational time delay. This delay is linked to the control algorithm's run time, i.e. the time necessary to sample and condition measurement signals, calculate the controller's outputs etc. If this time delay appears in the real system, but remains unconsidered in the control algorithm, it can substantially impair the controller performance. This is particularly the case for measured signals, i.e. quantities within the feedback loop, that are of high dynamics.

Figure 4.2 illustrates the impact of a computational delay on an arbitrary controlled quantity x for a one-step FCS-MPC. For the sake of simplicity, the delay is considered to have an overall duration of one controller time step $T_{\mathrm{s,c}}$. Moreover, the FCS-MPC is assumed to have a control set of merely two elements.

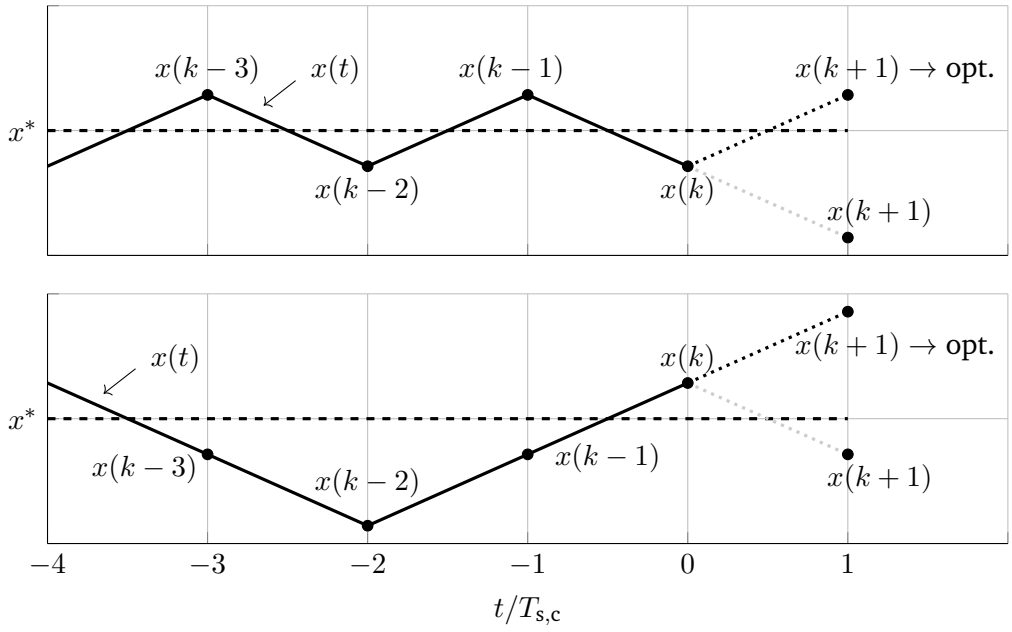


Figure 4.2.: Exemplary trajectory of an arbitrary quantity x controlled by a one-step FCS-MPC: Idealized behavior without appearing time delay (top) and impaired controller behavior due to uncompensated time delay (bottom).

In the case of the idealized behavior (Figure 4.2, top), i.e. no appearing computational delay, the optimal predicted state $x(k+1)$ is identified correctly, establishing a trajectory for $x(t)$ with low ripple around the reference value x^*. On the other hand, if the controlled system includes a time delay that is not being compensated (Figure 4.2, bottom), the optimal predicted state $x(k+1)$ is based on the sampled value $x(k-1)$ instead of $x(k)$. It can easily be seen that the resulting ripple of $x(t)$ increases largely, underpinning the benefit

[5] A time-variant system matrix indeed is present for the control of induction machines due to the dependency on the machine's rotational speed ω_{r}.

of implementing a time delay compensation. In analogy to Figure 4.1, the necessary modifications of the MPC principle for a properly functioning time compensation[6] are depicted in Figure 4.3.

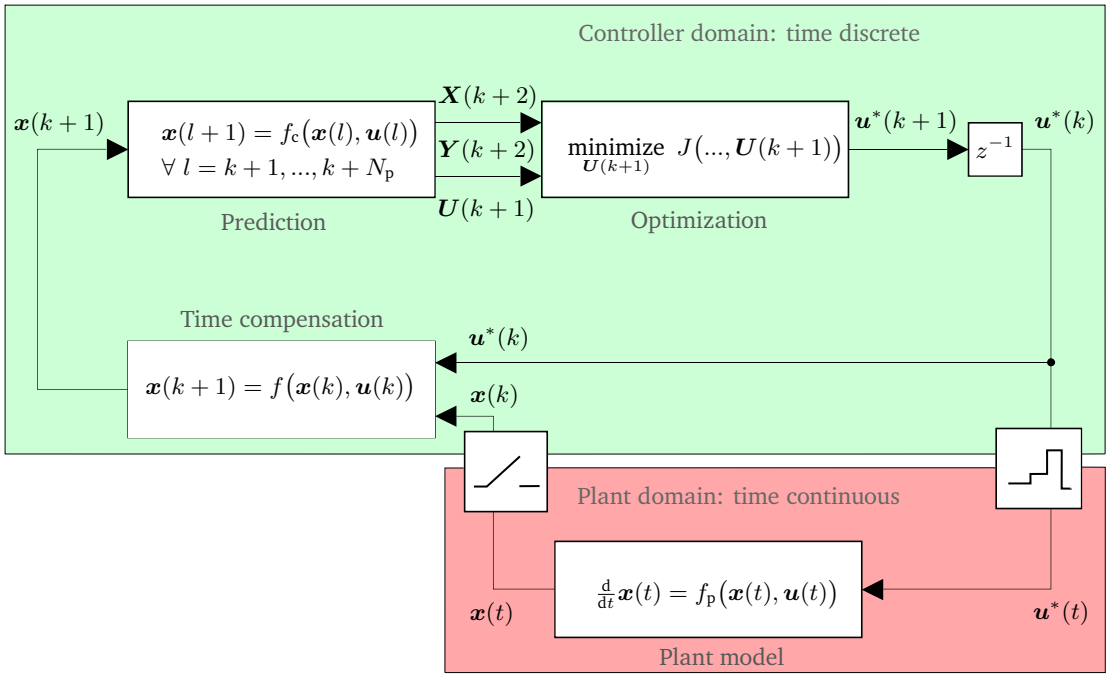


Figure 4.3.: Structure of model predictive control loop with time compensation.

4.1.5. Definition and Choice of Norm

Since it is necessary to define a cost function to perform an optimization of the control aims defined in the MPC, e.g. the minimization of reference tracking errors, it is required to make a decision on the respective norm that is to be utilized. A comparably easy way of performing reference tracking is the minimization of the absolute error. A simple cost function of a system then becomes:

$$\underset{\boldsymbol{U}(k)}{\text{minimize}} \quad J\left(\boldsymbol{x}(k)\right) = \sum_{l=k}^{k+N_\mathrm{p}-1} ||\boldsymbol{x}(l+1) - \boldsymbol{x}^*||_\infty = \sum_{l=k}^{k+N_\mathrm{p}-1} \sum_{\xi} |x_\xi(l+1) - {x_\xi}^*| \tag{4.7}$$

where the index ξ addresses the individual elements of $\boldsymbol{x}$. The norm $||*||_\infty$ is often referred to as ℓ_1-norm. However, there are two distinct reasons for utilizing the computational more demanding ℓ_2-norm $||*||_2^2$ for the reference tracking instead, which takes into account the squared error terms:

$$\underset{\boldsymbol{U}(k)}{\text{minimize}} \quad J\left(\boldsymbol{x}(k)\right) = \sum_{l=k}^{k+N_\mathrm{p}-1} ||\boldsymbol{x}(l+1) - \boldsymbol{x}^*||_2^2 = \sum_{l=k}^{k+N_\mathrm{p}-1} \sum_{\xi} \left(x_\xi(l+1) - {x_\xi}^*\right)^2 \tag{4.8}$$

[6] Note that neither the delay, nor the time compensation block are required to have a length of exactly one controller time step. The prediction interval for the time compensation can easily be matched with the true time delay appearing in the system, including measurement delays etc., via the factor T_s (cp. e.g. Eq. (4.3)), given that this value is known.

One benefit of the ℓ_2-norm addresses the closed-loop stability. It gains relevance as soon as the control effort is included in the cost function. In the case of a FCS-MPC, this implies the penalization of switching activity:

$$\underset{\boldsymbol{U}(k)}{\text{minimize}} \quad J\left(\boldsymbol{x}(k)\right) = \sum_{l=k}^{k+N_\mathrm{p}-1} ||\boldsymbol{x}(l+1) - \boldsymbol{x}^*||_2^2 + \lambda_\mathrm{sw} \cdot \left(\sum_{l=k}^{k+N_\mathrm{p}-1} ||\boldsymbol{u}(l) - \boldsymbol{u}(l-1)||_\infty \right) \tag{4.9}$$

Note that the applied ℓ_1-norm for the control effort is plausible, since the inverter's switching losses rise linearly with the amount of switching actions[7]. The priority of minimizing the control effort can be shifted via the weighting term λ_sw. Next, an operating point is considered that has very large deviations between $\boldsymbol{x}$ and $\boldsymbol{x}^*$, which further also requires switching actions to decrease these deviations. If the ℓ_1-norm is used for the reference tracking, the deviations will only be reduced if the acquirable decrease of the tracking error outweighs the costs for control effort. Conversely, if the control effort's costs outweigh the possible decrease of the tracking error, no switching occurs and the tracking error may become even larger. The control performance deteriorates and stability issues arise [63]. In comparison, the ℓ_2-norm encourages any switching activity that reduces large deviations between $\boldsymbol{x}$ and $\boldsymbol{x}^*$. Due to the quadratic consideration of the tracking error, even smaller reductions of the tracking error can outweigh the control effort's cost, if the operating point is far away from its reference. This characteristic supports closed-loop stability.

A second benefit of the ℓ_2-norm is its relevance for error rms-value reduction. Consider for example the reference tracking of the stator current for induction machines, which can represent torque and flux control within a field-oriented control loop. A stator current reference tracking, which further ensures low error rms-values, is of extraordinary interest, since it implies proper machine control and simultaneously low harmonic losses (cp. Section 3.2.3 and Section 3.2.4). By comparing the ℓ_2-norm with the time-discrete version for a error rms-value calculation, it can be identified that the former is proportional to the square of the latter.

$$\ell_2\text{-norm in cost function of MPC for quantity } x: \quad \sum_{l=k}^{k+N_\mathrm{p}-1} \left(x(l+1) - x^*\right)^2 \tag{4.10}$$

$$\text{Time-discrete error rms calculation for quantity } x: \quad \frac{1}{N} \cdot \sqrt{\sum_{l=k}^{k+N-1} \left(x(l+1) - x^*\right)^2} \tag{4.11}$$

Since the MPC minimizes the costs, and the minimal squared rms-value corresponds to the minimal rms-value itself, the ℓ_2-norm can be seen as the desired reference tracking with an included coarse (time-discrete) minimization of error rms-value. Note that in the case of a two-dimensional $\boldsymbol{x}$, e.g. α and β-component of the stator current, the ℓ_2-norm leads to circular contour lines[8] around the reference value $\boldsymbol{x}^*$.

Due to the given reasons, the ℓ_2-norm will be used for reference tracking in this thesis.

4.1.6. Solvers for the MPC's Optimization Problem

In order to realize model predictive controllers as real-time implementations, the included optimization problem has to solved efficiently. In this context, it is reasonable to distinguish between the principles of CCS-MPC and FCS-MPC.

[7] Disregarding the influence of the current loading during switching, cp. Section 4.3.6.
[8] The contour lines imply predicted values of equivalent costs attained by the cost function.

Solvers for CCS-MPC
In case of CCS-MPC implementations for linear, time-invariant or time-variant systems, the optimization problem of the controller is solvable by linear or quadratic[9] programming [64]. In comparison to a full state feedback as linear-quadratic regulator, the formulation of linear or quadratic programming allows certain constraints, such as the limitation of the system's input variable due to a finite DC-link voltage. Therefore, large reference steps do not lead to sub-optimal controller outputs, providing a clear advantage over the linear-quadratic regulator.

Generally, the linear or quadratic programming has to be performed for every sample time of the controller, since the optimization problem encounters new conditions, i.e. the newly sampled state variables or changed system parameters in case of a time-variant system. Methods such as the Simplex algorithm or Cutting-plane method allow to solve the optimization problem in polynomial time, i.e. usually efficiently. The polynomial time however can not be ensured anymore if non-linear systems or non-convex cost functions are to be evaluated, which is for example the case with respect to minimizing the DC-link current (multiplication of state variable with system input variable).

On the other hand, if linear time-invariant systems can be assumed, the approach of multi-parametric linear or quadratic programming can be applied. The multi-parametric methods interpret the state variables as parameters, allowing to determine a solution in terms of the current state of the system. By means of these measures, a piece-wise linear feedback control law can be defined [65] [66]. Although this method appears very promising due to the low computational online demand it implies, it is not properly applicable for induction machines with variable speed, which either have to be treated as nonlinear or at least time-variant systems.

Since the output of CCS-MPCs is a (constrained) continuous value, its application in the domain of power electronics normally requires an additional PWM module.

Solvers for FCS-MPC
In comparison to the CCS-MPC, the peculiarity of a FCS-MPC is the restriction of the control set for possible input variables to a finite number of values. In case of power electronics, this restriction usually is identical to the reduction of the control set to the available switch positions $\boldsymbol{\mathcal{U}}$ (or sequences of switch positions $\boldsymbol{\mathcal{U}}^{N_\mathrm{p}}$ for $N_\mathrm{p} > 1$). This leads to a so-called mixed-integer linear or quadratic optimization problem. Although these kind of problems appear to be solvable in an easier way than in case of the continuous control set, the opposite is true: They are considered to be NP-hard, meaning that they cannot be solved in polynomial time, i.e. not efficiently.

Nevertheless, the finite elements of the control set bring upon the possibility of performing a total enumeration of predicted costs, making the optimization problem trivial. Regarding this approach, all of the possible switch positions or sequences of switch positions can individually be applied to the plant model and cost function. A simple comparison among the predicted values then provides the optimal controller output. Following this principle, non-linearities within the system or cost function do not impair or constrain the search for the global optimal solution.

The approach of total enumeration can be computational low demanding, if a prediction horizon of merely $N_\mathrm{p} = 1$ is chosen. On the other hand, higher prediction horizons lead to an exponentially increasing computa-

[9] The difference between linear and quadratic programming is in this case the chosen norm of the cost function, namely the usage of the ℓ_1-norm or the ℓ_2-norm (cp. Section 4.1.5).

tional effort. For this reason, methods such as branch-and-bound [67] or sphere-decoding [68] techniques should be applied to keep the necessary hardware resources at bay.

Note that the FCS-MPC inherently includes a modulator, since the controller outputs are directly matched with the optimal switch positions of an inverter. This provides the possibility of including an optimization of the inverter's switching activity in the FCS-MPC, as already hinted at in Section 4.1.5. Due to this advantage, its convenient implementation and the unrestricted definition of the cost function, the FCS-MPC is chosen to be focused on in this thesis.

4.2. Design and Evaluation of Finite Control Set Model Predictive Control for Induction Machines

In this section, the application of FCS-MPC to an inverter-fed induction machine is described. In this context, four controller types will be introduced, analyzed and compared. This discussion was originally provided in [15], hence the following sections are strongly based on this source and include direct quotations. In comparison to Section 4.3, an ideal two-level inverter is assumed here, i.e. interleaving is not considered.

Note that for the sake of simplicity, the system and control matrices $\boldsymbol{A}_\mathrm{c}$, $\boldsymbol{B}_\mathrm{c}$ are not marked uniquely for the introduced controller types. Instead, it is assumed that the appropriate matrices for the respectively demanded state vector compositions are chosen. Likewise, only constant reference values of torque and flux are presumed. Lastly, the computational delay of the control algorithm is neglected, therefore the implementation of a time compensation does not have to be taken into account.

As for any other controller type, the main objectives for the FCS-MPC shall be the control of electromagnetic torque and the machine's magnetization. The secondary control objective is to decrease the total demand distortion (TDD) of the stator current and torque for a given average switching frequency. This ensures high control quality while at the same time lowering the anticipated inverter losses (switching frequency) and machine losses (TDD of current, cp. Section 3.2.4).

Because the cost function does not have to be restricted to a summation of linear or quadratic expressions, but instead can also contain non-linear terms, a direct prediction and control of the machine's torque and flux is generally possible. This concept will be referred to as Model Predictive Torque and Flux Control (MPTFC). As an alternative, a field-oriented approach that relies on the model predictive control of the stator currents can be considered. This is the concept of Model Predictive Current Control (MPCC). Other principles, such as the combined approach of MPC and optimized pulse patterns (MPPPC) [69], are out of the scope of this thesis and are therefore not considered.

4.2.1. Model Predictive Torque and Flux Controller (MPTFC)

With this principle, the torque and stator flux magnitude are directly controlled by making according predictions with the system matrix[10] and torque equations of Section 3.2.

Formulation of the Control Problem
The MPTFC with $N_\mathrm{p} = 1$ can be formulated as given in the following.

$$
\begin{aligned}
\underset{\boldsymbol{u}(k)}{\text{minimize}} \quad & J_{\mathrm{T},1}(k) + J_{\Psi,1}(k) + J_{\mathrm{sw}}(k) \\
\text{subject to} \quad & \begin{pmatrix} \boldsymbol{i}_\mathrm{s}^{\alpha\beta}(k+1) \\ \boldsymbol{\Psi}_\mathrm{s}^{\alpha\beta}(k+1) \end{pmatrix} = \boldsymbol{A}_\mathrm{c}(\omega_\mathrm{r}) \cdot \begin{pmatrix} \boldsymbol{i}_\mathrm{s}^{\alpha\beta}(k) \\ \widetilde{\boldsymbol{\Psi}}_\mathrm{s}^{\alpha\beta}(k) \end{pmatrix} + \boldsymbol{B}_\mathrm{c}\, \boldsymbol{T}_{\mathrm{c},2} \cdot (V_\mathrm{dc}/2) \cdot \boldsymbol{u}(k) \\
& \boldsymbol{u}(k) \in \boldsymbol{\mathcal{U}}_\mathrm{FCS} \\
& T_\mathrm{e}(k+1) = \frac{3}{2} z_\mathrm{p} \cdot \boldsymbol{\Psi}_\mathrm{s}^{\alpha\beta}(k+1) \times \boldsymbol{i}_\mathrm{s}^{\alpha\beta}(k+1) \\
& J_{\mathrm{T},1}(k) = \lambda_{\mathrm{T},1} \cdot \left(T_\mathrm{e}(k+1) - T_\mathrm{e}^* \right)^2 \\
& J_{\Psi,1}(k) = \left(1 - \lambda_{\mathrm{T},1}\right) \cdot \left(||\boldsymbol{\Psi}_\mathrm{s}^{\alpha\beta}(k+1)||_2 - \Psi_\mathrm{s}^* \right)^2 \\
& J_{\mathrm{sw}}(k) = \lambda_{\mathrm{sw}} \cdot ||\boldsymbol{u}(k) - \boldsymbol{u}(k-1)||_1
\end{aligned}
\tag{4.12}
$$

The factor $\lambda_{\mathrm{T},1} \in [0, 1]$ is a dimensionless weighting factor that is used to shift the prioritization between torque and magnetization control quality, whereas λ_sw weights the penalization of switching activities. A lowered switching activity results in a reduced average switching frequency of the converter.[11]

Please note that unlike the field-oriented principle, the machine's magnetization is controlled via the stator flux in the MPTFC principle. The reason is the missing direct impact of the stator voltage on the rotor flux (second-order transfer function, cp. Section 3.2.3), i.e. the rotor flux remains unaffected by the imminent control vector of the calculated optimal control sequence. Therefore, a prediction horizon of $N_\mathrm{p} > 1$ would strictly be necessary to acquire any closed-loop control of the machine magnetization [70]. This is however an undesired and unnecessary limitation regarding real-time feasible controller implementations with fast sampling rates.

The overall controller structure of the MPTFC is shown in Figure 4.4.

Algebraic Performance Analysis
The torque costs shall be expressed in terms of merely the stator flux error. In order to derive such expression, the field-oriented reference frame shall be utilized. For a more thorough derivation, please also refer to [71].

If interpreted in the dq-reference frame, T_e can be rewritten as given in Eq. (4.13). Rearranging this equation, $\Psi_{\mathrm{s,q}}^*$ can be derived from $T_\mathrm{e}^*, \Psi_{\mathrm{r,d}}^*$. Lastly, assuming a negligible rotor flux error, the term $J_{\mathrm{T},1}$ can be expressed with Eq. (4.15). The assumption of a negligible rotor flux error is usually valid for a constant reference magnetization. The reason is the sluggish behavior of $\boldsymbol{\Psi}_\mathrm{r}$ and therefore easy steady-state controllability.

[10] The system matrix used for the MPTFC has to match a state vector composition that was not explicitly derived previously. Please see Appendix A.3 on how to transform the system matrix to any desired composition.
[11] More sophisticated methods for penalizing switching activity with respect to anticipated inverter losses are presented in Section 4.3.6.

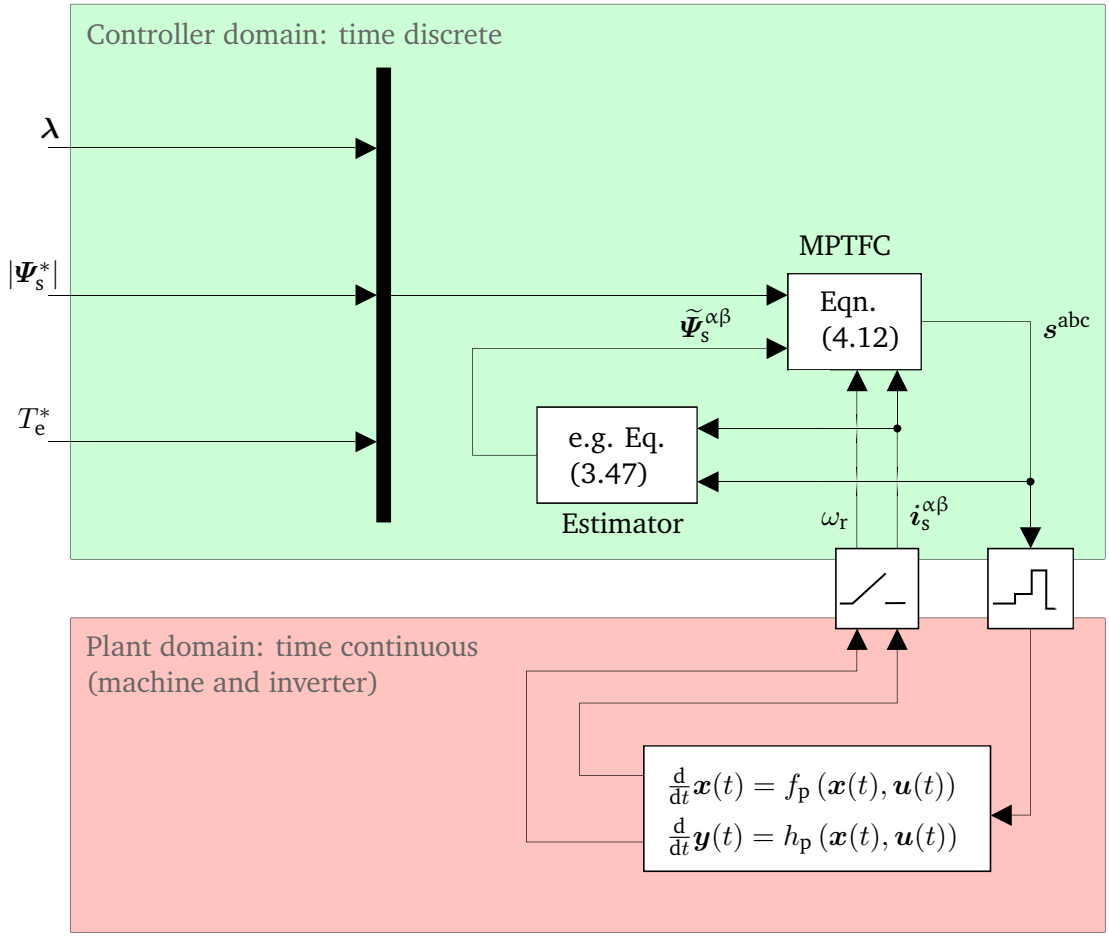


Figure 4.4.: Control loop structure of MPTFC.

$$T_\mathrm{e} = \frac{3}{2} z_\mathrm{p} \cdot \frac{M_\mathrm{sr}}{L_\mathrm{s} L_\mathrm{r} - M_\mathrm{sr}^2} \cdot \Psi_\mathrm{s,q} \Psi_\mathrm{r,d} \tag{4.13}$$

$$\Psi_\mathrm{s,q}^* = \frac{2}{3 z_\mathrm{p}} \cdot \frac{L_\mathrm{s} L_\mathrm{r} - M_\mathrm{sr}^2}{M_\mathrm{sr}} \cdot \frac{T_\mathrm{e}^*}{\Psi_\mathrm{r,d}^*} \tag{4.14}$$

$$J_{\mathrm{T},1}(k) \approx c \cdot \lambda_{\mathrm{T},1} \cdot \left(\Psi_\mathrm{s,q}(k+1) - \Psi_\mathrm{s,q}^*\right)^2 \tag{4.15}$$

$$\text{where } \; c = \left(\frac{3}{2} z_\mathrm{p} \cdot \frac{M_\mathrm{sr}}{L_\mathrm{s} L_\mathrm{r} - M_\mathrm{sr}^2} \cdot \Psi_\mathrm{r,d}^*\right)^2 \gg 1 \tag{4.16}$$

The contour lines (i.e. lines of equivalent costs for the predicted error) for $J_{\mathrm{T},1}$, $J_{\Psi,1}$ and $J_{\mathrm{T},1} + J_{\Psi,1}$ can now be illustrated in terms of $\boldsymbol{\Psi}_\mathrm{s}$ within the dq-reference frame, which is depicted in Figure 4.5. It can easily be identified that $J_{\Psi,1} = 0$ describes a circle with the radius of the reference stator flux magnitude Ψ_s^*, while $J_{\mathrm{T},1} = 0$ is represented by a horizontal line at $\Psi_\mathrm{s,q}^*$. If the weighting for the torque is chosen according to $c \cdot \lambda_{\mathrm{T},1,\mathrm{circ}} = (1 - \lambda_{\mathrm{T},1,\mathrm{circ}})$, i.e. $\lambda_{\mathrm{T},1,\mathrm{circ}} = {}^1/_{(c+1)}$, the predicted errors of $\Psi_\mathrm{s,d}$ and $\Psi_\mathrm{s,q}$ are approximately weighted equally, leading to circular-like contour lines around the coordinate $J_{\mathrm{T},1} + J_{\Psi,1} = 0$.

Circular contour lines for the predicted stator flux error are of special interest, as they imply likewise circular contours for the anticipated stator current error[12]. As it was already shown in Section 4.1.5, the circular contour lines resulting from MPC cost functions can be interpreted as a (coarse) minimization of TDD. Hence, a main contributor for machine losses can be minimized by a suitable tuning of the MPTFC.

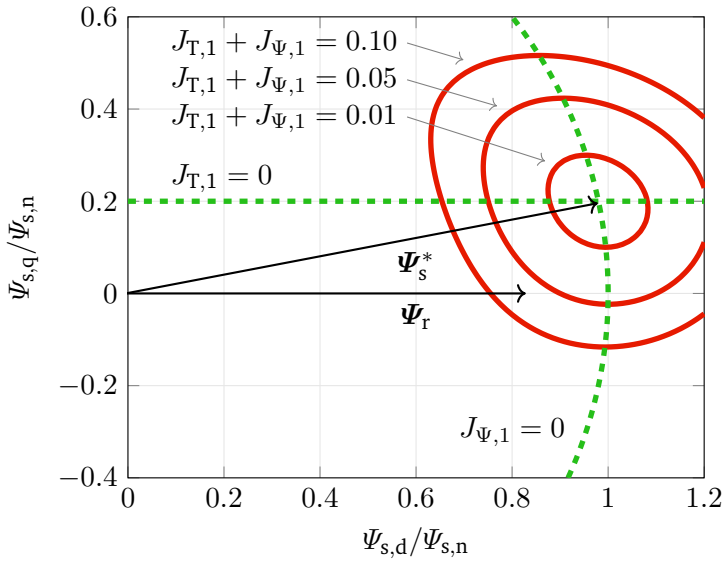


Figure 4.5.: Contour lines for $J_{T,1}$, $J_{\Psi,1}$, and $J_{T,1} + J_{\Psi,1}$ in the dq-reference frame, expressed in terms of $\boldsymbol{\Psi}_s$. The weighting factors are tuned to $\lambda_{T,1} = \lambda_{T,1,circ}$, $\lambda_{sw} = 0$, and the reference values are set to $\Psi_{s,q}^* = 0.2 \cdot \Psi_{s,n}, \Psi_s^* = \Psi_{s,n}$.

Note that the calculation of c depends on the the *rotor* flux magnitude's reference, whereas the control of machine magnetization itself is based on the stator flux in case of the MPTFC. Due to the relation $\Psi_{r,d} = {}^{M_{sr}}/_{L_s} \cdot \Psi_s \cdot \cos(\theta_{\Psi_{sr}})$ and the load angle $\theta_{\Psi_{sr}}$ being within the boundaries of $\pm 15°$, the substitution $\Psi_{r,d}^* \rightarrow \Psi_s^*$ in Eq. (4.16) however only produces minor deviations [69] and may therefore be applied. Alternatively, the rotor flux magnitude can be estimated, which can then be used for the computation of Eq. (4.16).

Conclusion
The MPTFC is a straightforward implementation for torque and flux control of IMs. A prioritization between torque or stator flux magnitude control quality can be shifted online by adapting the weighting factor $\lambda_{T,1}$. Further, a specific tuning of $\lambda_{T,1}$ can be utilized for a (slightly distorted) minimization of stator current TDD.

A disadvantage of the MPTFC is the square root operation for predicting the flux magnitude, which tends to be more demanding with respect to the necessary computational effort.

[12]This can be shown by appropriate substitutions via Eqn. (3.39) - (3.40) and under the remaining assumption of a negligible rotor flux error.

4.2.2. Modified Model Predictive Torque and Flux Controller (MMPTFC)

The modification of the MPTFC aims at the exclusion of the computational demanding square root operation, which is originally needed for the flux magnitude prediction.

Formulation of Control Problem
The formulation of the MMPTFC is almost identical to the MPTFC, with the only difference to be found in the cost function terms J_T, J_Ψ:

$$\begin{aligned} J_{\mathrm{T},2}(k) &= \lambda_{\mathrm{T},2} \cdot \left(T_\mathrm{e}(k+1) - T_\mathrm{e}^*\right)^2 \\ J_{\Psi,2}(k) &= (1-\lambda_{\mathrm{T},2}) \cdot \left(||\boldsymbol{\Psi}_\mathrm{s}^{\alpha\beta}(k+1)||_2^2 - (\Psi_\mathrm{s}{}^*)^2\right)^2 \end{aligned} \tag{4.17}$$

As the comparison between Eqn. (4.12) and Eqn. (4.17) shows, the square root operation is simply omitted for the MMPTFC.

Algebraic Performance Analysis
Although the term $J_{\Psi,2}$ appears to loose its physical meaning, i.e. expressing costs of the predicted error in stator flux magnitude, $J_{\Psi,2} = 0$ in fact still describes the same circular contour line as $J_{\Psi,1} = 0$. However, since the costs of $J_{\Psi,2}$ tend to increase faster than of $J_{\Psi,1}$ for the same stator flux errors, the tuning of $\lambda_{\mathrm{T},2}$ has to be adapted to maintain the approximately circular-shaped contour lines.

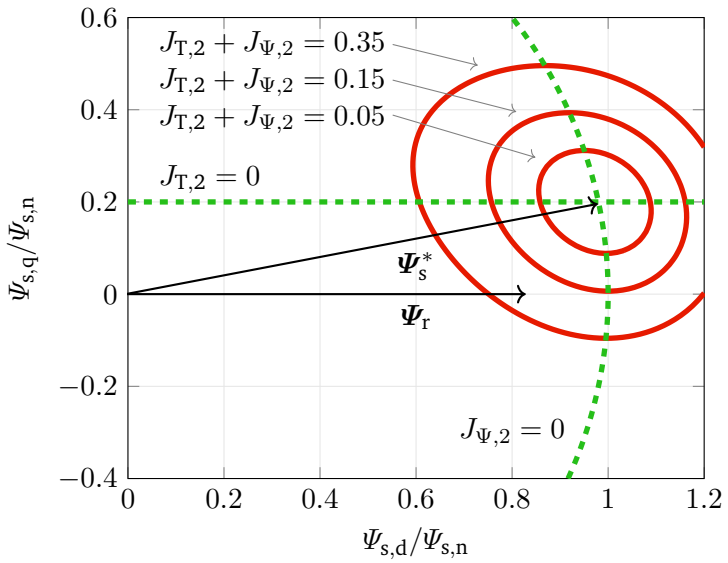


Figure 4.6.: Contour lines for $J_{\mathrm{T},2}$, $J_{\Psi,2}$, and $J_{\mathrm{T},2} + J_{\Psi,2}$ in the dq-reference frame, expressed in terms of $\boldsymbol{\Psi}_\mathrm{s}$. The weighting factors are tuned to $\lambda_{\mathrm{T},2} = \lambda_{\mathrm{T},2,\mathrm{circ}} = \frac{1}{(c/4+1)}$, $\lambda_\mathrm{sw} = 0$. The demanded torque and machine magnetization is identically chosen to Fig. 4.5.

The optimal weighting $\lambda_{\mathrm{T},2}$ is dependent on the reference value Ψ_s^*. It can be expressed by $\lambda_{\mathrm{T},2,\mathrm{circ}} = g(c, \Psi_\mathrm{s}^*)$, where g is an unknown function. In this thesis, g was approximated by the following procedure:

1. Find the true circular contour lines fitted to the cost function $J_{\mathrm{T},2} + J_{\Psi,2}$ for specific values of cost and $\lambda_{\mathrm{T},2}$. This can be performed by the least-squares method as described in [72].

2. Sweep $\lambda_{\mathrm{T},2}$ in terms of c, Ψ_s^* and iteratively perform step 1 to determine the respective areas between the true circles and the contour lines of $J_{\mathrm{T},2} + J_{\Psi,2}$ (normalized to the area of the respective true circles).

3. Pick $\lambda_{\mathrm{T},2} = \lambda_{\mathrm{T},2,\mathrm{circle}}$ that led to the minimal normalized area between the true circle and $J_{\mathrm{T},2} + J_{\Psi,2}$.

4. Create a lookup table for $\lambda_{\mathrm{T},2,\mathrm{circ}}$ for several values of Ψ_s^*.

5. Utilize an interpolation method, e.g. splines, between the values of the lookup table to acquire continuous values for $\lambda_{\mathrm{T},2,\mathrm{circ}}$.

With the method described above, the contour lines of $J_{\mathrm{T},2} + J_{\Psi,2}$ can often be fitted closer to the true circle than it is possible for the $\lambda_{\mathrm{T},1}$-tuned MPTFC. Hence, the current TDD minimization of the MMPTFC may in some cases even be less distorted than in the case of the MPTFC, even though its computational effort is less.

As a rule of thumb, a good approximation of circular contour lines for the MMPTFC can also be determined by:

$$\begin{aligned} & c \cdot \lambda_{\mathrm{T},2,\mathrm{circ}} = 4 \cdot (1 - \lambda_{\mathrm{T},2,\mathrm{circ}}) \\ \rightarrow \quad & \lambda_{\mathrm{T},2,\mathrm{circ}} = \frac{1}{c/4 + 1} \end{aligned} \tag{4.18}$$

Conclusion
The MMPTFC saves the computational expenses of square root operations. Otherwise, its properties are similar to the MPTFC, i.e. the capability of torque error minimization and (slightly distorted) current TDD minimization is preserved.

4.2.3. Model Predictive Current Control (MPCC)

The MPCC implementation utilizes the field-oriented principle to acquire reference values for the stator currents, which represent the desired electromagnetic torque and rotor flux magnitude. Therefore, an outer control loop as described in Section 3.2.3 with rotor flux estimation is required. The task of the MPCC itself is then to minimize the tracking error of the stator currents.

Formulation of Control Problem
The MPCC with $N_\mathrm{p} = 1$ can be formulated in a compact manner as given in the following.

$$\begin{aligned} \underset{\boldsymbol{u}(k)}{\text{minimize}} \quad & J_\mathrm{i}(k) + J_\mathrm{sw}(k) \\ \text{subject to} \quad & \begin{pmatrix} \boldsymbol{i}_\mathrm{s}^{\alpha\beta}(k+1) \\ \boldsymbol{\Psi}_\mathrm{r}^{\alpha\beta}(k+1) \end{pmatrix} = \boldsymbol{A}_\mathrm{c}(\omega_\mathrm{r}) \cdot \begin{pmatrix} \boldsymbol{i}_\mathrm{s}^{\alpha\beta}(k) \\ \widetilde{\boldsymbol{\Psi}}_\mathrm{r}^{\alpha\beta}(k) \end{pmatrix} + \boldsymbol{B}_\mathrm{c}\, \boldsymbol{T}_{\mathrm{c},2} \cdot (V_\mathrm{dc}/2) \cdot \boldsymbol{u}(k) \\ & \boldsymbol{u}(k) \in \boldsymbol{\mathcal{U}}_\mathrm{FCS} \\ & \boldsymbol{i}_\mathrm{s}^{\alpha\beta\,*}(k+1) = \boldsymbol{R}\big(\widetilde{\beta}_\mathrm{k}(k+1)\big) \cdot \boldsymbol{i}_\mathrm{s}^{\mathrm{dq}^*} \\ & \widetilde{\beta}_\mathrm{k}(k+1) = \mathrm{atan2}\big(\widetilde{\Psi}_{\beta,\mathrm{r}}(k+1) / \widetilde{\Psi}_{\alpha,\mathrm{r}}(k+1)\big) \\ & J_\mathrm{i}(k) = ||\boldsymbol{i}_\mathrm{s}^{\alpha\beta}(k+1) - \boldsymbol{i}_\mathrm{s}^{\alpha\beta\,*}(k+1)||_2^2 \\ & J_\mathrm{sw}(k) = \lambda_\mathrm{sw} \cdot ||\boldsymbol{u}(k) - \boldsymbol{u}(k-1)||_1 \end{aligned} \tag{4.19}$$

The state vector $\boldsymbol{x} = (\boldsymbol{i}_\mathrm{s}^{\alpha\beta}\ \boldsymbol{\Psi}_\mathrm{r}^{\alpha\beta})^\mathrm{T}$ is chosen, for it provides simplified predictions due to more zero-entries in $\boldsymbol{B}_\mathrm{c}$ (owing to the missing direct impact of the stator voltage on the rotor flux). Note that the reference values $\boldsymbol{i}_\mathrm{s}^{\alpha\beta *}$ generally are time-variant for $T_\mathrm{e}^* = \text{const}, \Psi_\mathrm{r,d}^* = \text{const}$, due to the continuously rotating field of the machine. For $N_\mathrm{p} = 1$ they in fact will remain constant for the concurrent prediction. Higher prediction horizons do however lead to an additional computational burden: The values $\widetilde{\beta}_\mathrm{k}, \sin(\widetilde{\beta}_\mathrm{k}), \cos(\widetilde{\beta}_\mathrm{k})$ have to be determined for every uniquely predicted value of the rotor flux, since it gains a dependency on the input vector $\boldsymbol{u}$. Eventually, this also entails that the reference values $\boldsymbol{i}_\mathrm{s}^{\alpha\beta *}$ have to be predicted for $N_\mathrm{p} > 1$.

The overall controller structure of the MPCC is shown in Figure 4.7.

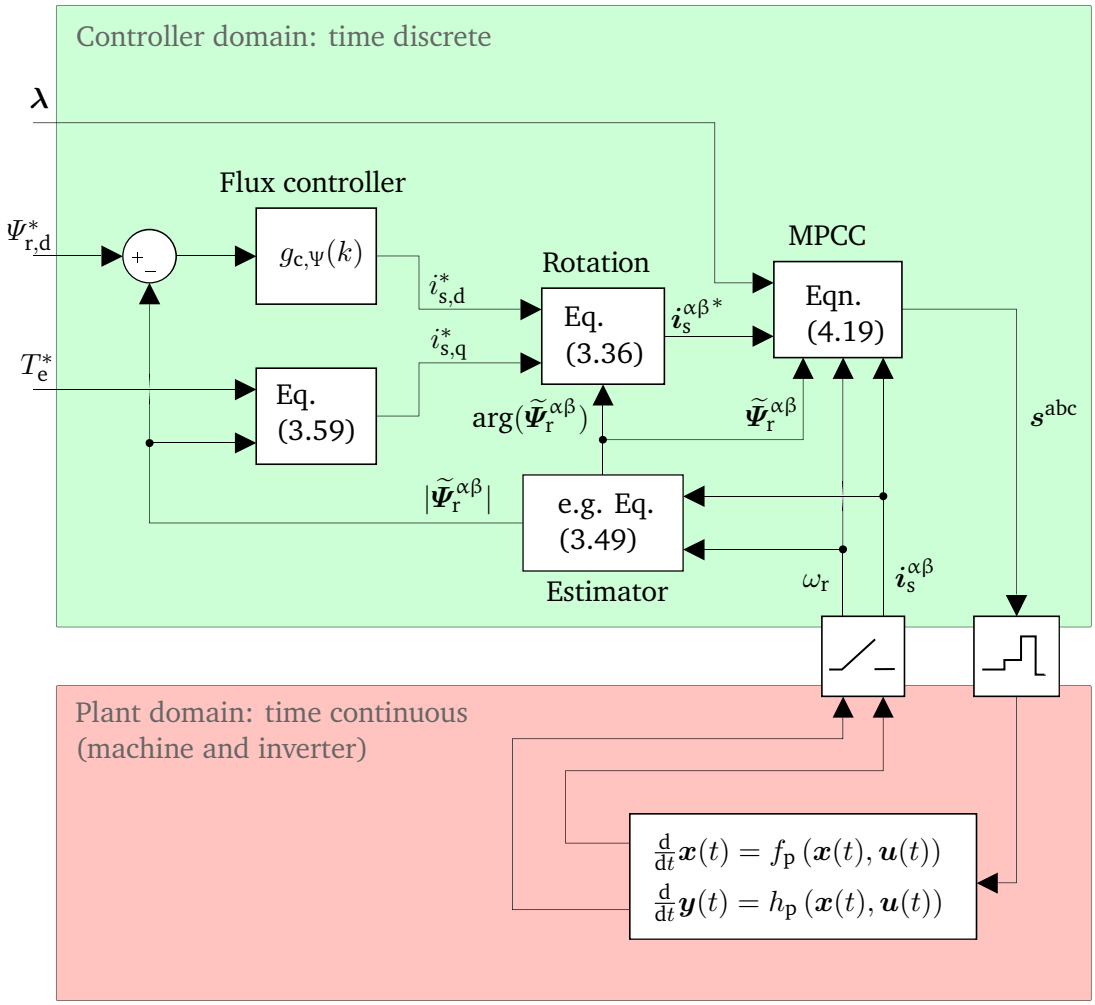


Figure 4.7.: Control loop structure of MPCC.

Algebraic Performance Analysis

The cost function term J_i obviously leads to circular contour lines for the predicted stator current errors, being centered around $\boldsymbol{i}_\mathrm{s}^*$. As already mentioned in the analysis for the MPTFC, this likewise applies to the predicted stator flux errors. In order to allow an easier comparison, the contour lines of the MPCC are therefore also expressed in terms of the stator flux, as given in Figure 4.8. Clearly, the circular shapes are not distorted here.

The outer control loop for flux control can either be implemented with the transfer function Eq. (3.58), or with an additional controller. In the first case, fairly low dynamics for reference changes of $\Psi^*_{\mathrm{r,d}}$ have to be anticipated. In the case of an outer-loop flux controller, additional tuning is needed. If a linear controller such as a PI controller is used, a trade-off between dynamic and overshoot behavior for the controlled machine magnetization has to be made. Moreover, an anti-windup structure should be implemented.

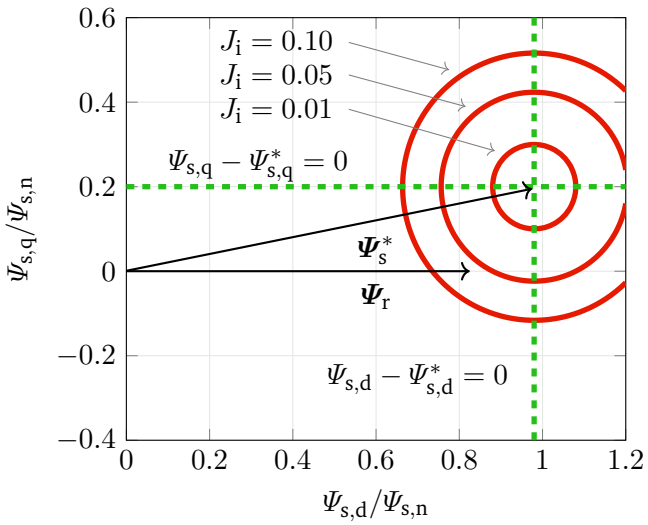


Figure 4.8.: Contour lines for J_i in the dq-reference frame, expressed in terms of $\boldsymbol{\Psi}_\mathrm{s}$. The demanded torque and machine magnetization is identically chosen to Fig. 4.5.

Conclusion
The MPCC is computational low demanding with respect to the necessary predictions and its cost function, if $N_\mathrm{p} = 1$ is set or β_k is assumed to change only negligible. It is capable of minimizing the stator current TDD without the (slight) distortions encountered for the MPTFC.

The main disadvantage of the MPCC is the required outer loop for field orientation that impairs the dynamic behavior for changes in the demanded machine magnetization. Secondly, another disadvantage in its proposed form is that the MPCC is not capable of prioritizing torque control quality.

4.2.4. Modified Model Predictive Current Controller (MMPCC)

The MPCC can be modified to allow a heavier penalization of the torque error. In order to acquire this property, the cost function has to evaluate the stator currents in the dq-reference frame, allowing an increase of error weighting $\lambda_\mathrm{q} \in [0, 1]$ for the q-axis. This can either be achieved via predictions in the dq-reference frame, or the transformation of the predicted values of $i_\mathrm{s}^{\alpha\beta}$ before being passed on to J_i. Depending on the implementation style, either the input vector $\boldsymbol{u}$ or the predicted currents are subject to the time-variant transformation $\boldsymbol{R}(-\widetilde{\beta}_\mathrm{k})$. The latter case is chosen here.

Formulation of Control Problem
The MMPCC with $N_\mathrm{p} = 1$ can be formulated in a compact manner as given in the following.

$$
\begin{aligned}
&\underset{\boldsymbol{u}(k)}{\text{minimize}} \quad J_\mathrm{i}(k) + J_\mathrm{sw}(k) \\
&\text{subject to} \begin{pmatrix} \boldsymbol{i}_\mathrm{s}^{\alpha\beta}(k+1) \\ \boldsymbol{\Psi}_\mathrm{r}^{\alpha\beta}(k+1) \end{pmatrix} = \boldsymbol{A}_\mathrm{c}(\omega_\mathrm{r}) \cdot \begin{pmatrix} \boldsymbol{i}_\mathrm{s}^{\alpha\beta}(k) \\ \widetilde{\boldsymbol{\Psi}}_\mathrm{r}^{\alpha\beta}(k) \end{pmatrix} + \boldsymbol{B}_\mathrm{c}\, \boldsymbol{T}_{\mathrm{c},2} \cdot (V_\mathrm{dc}/2) \cdot \boldsymbol{u}(k) \\
&\qquad \boldsymbol{u}(k) \in \boldsymbol{\mathcal{U}}_\mathrm{FCS} \\
&\qquad \boldsymbol{i}_\mathrm{s}^{\mathrm{dq}}(k+1) = \boldsymbol{R}\big(-\widetilde{\beta}_\mathrm{k}(k+1)\big) \cdot \boldsymbol{i}_\mathrm{s}^{\alpha\beta}(k+1) \\
&\qquad \widetilde{\beta}_\mathrm{k}(k+1) = \mathrm{atan2}\big(\widetilde{\Psi}_{\beta,\mathrm{r}}(k+1)/\widetilde{\Psi}_{\alpha,\mathrm{r}}(k+1)\big) \\
&\qquad J_\mathrm{i}(k) = \big(\lambda_\mathrm{q} - 1\big) \cdot \big(i_{\mathrm{s,d}}(k+1) - i_{\mathrm{s,d}}^*\big)^2 + \lambda_\mathrm{q} \cdot \big(i_{\mathrm{s,q}}(k+1) - i_{\mathrm{s,q}}^*\big)^2 \\
&\qquad J_\mathrm{sw}(k) = \lambda_\mathrm{sw} \cdot ||\boldsymbol{u}(k) - \boldsymbol{u}(k-1)||_1
\end{aligned}
\tag{4.20}
$$

Conclusion
The MMPCC almost has the identical properties as the MPCC. The difference is its capability of shifting the prioritization between torque and stator current TDD minimization during its operation.

The disadvantage of the MMPCC is the additional computational effort required for transforming the predicted stator currents (or input vector). Furthermore, if prediction horizons of $N_\mathrm{p} > 1$ are aspired, the predictions of $\widetilde{\beta}_\mathrm{k}, \sin(\widetilde{\beta}_\mathrm{k}), \cos(\widetilde{\beta}_\mathrm{k})$ have to be performed additionally, as already described for the MPCC.

4.2.5. Stationary Controller Performance

The simulated performance of torque and stator current TDD minimization is provided in Figure 4.9. The respective TDDs are measured against the switching frequency, which is tunable via λ_sw. The simulated machine is a standard IE1 $5.5\,\mathrm{kW}$, $400\,\mathrm{V}$ squirrel cage induction motor. The simulation is run with $V_\mathrm{dc} = 800\,\mathrm{V}$, rated torque and rated speed. The FCS-MPC implementations are each sampled with $100\,\mathrm{kHz}$, have a prediction horizon of $N_\mathrm{p} = 1$ and are discretized with the exact Euler forward method. A complete overview of the simulation parameters is provided in Appendix B.

A simulational comparison with other control principles, e.g. field-oriented control with PI controllers and space vector modulation, is not performed in this thesis. Case studies can be found in literature with respect to machine TDD vs. average switching frequency [55] or inverter losses vs. machine losses [73]. In essence, FCS-MPC usually is superior, if the MPC is being sampled appropriately fast (see also Section 4.3.13).

Figure 4.9 clearly shows that there is a distinct trade-off between torque and current TDD minimization. Supplementary simulation results beyond Figure 4.9 are provided in Appendix C.1. Further key take-aways of the figure are:

- Torque: The achieved TDD of the MPCC is already fairly low, yet it underperforms when compared with implementations with highly penalized errors in the q-axis.
- Current: The TDD is minimized best for the MPCC and MMPCC with $\lambda_\mathrm{q} = 0.5$, but also for the MPTFC

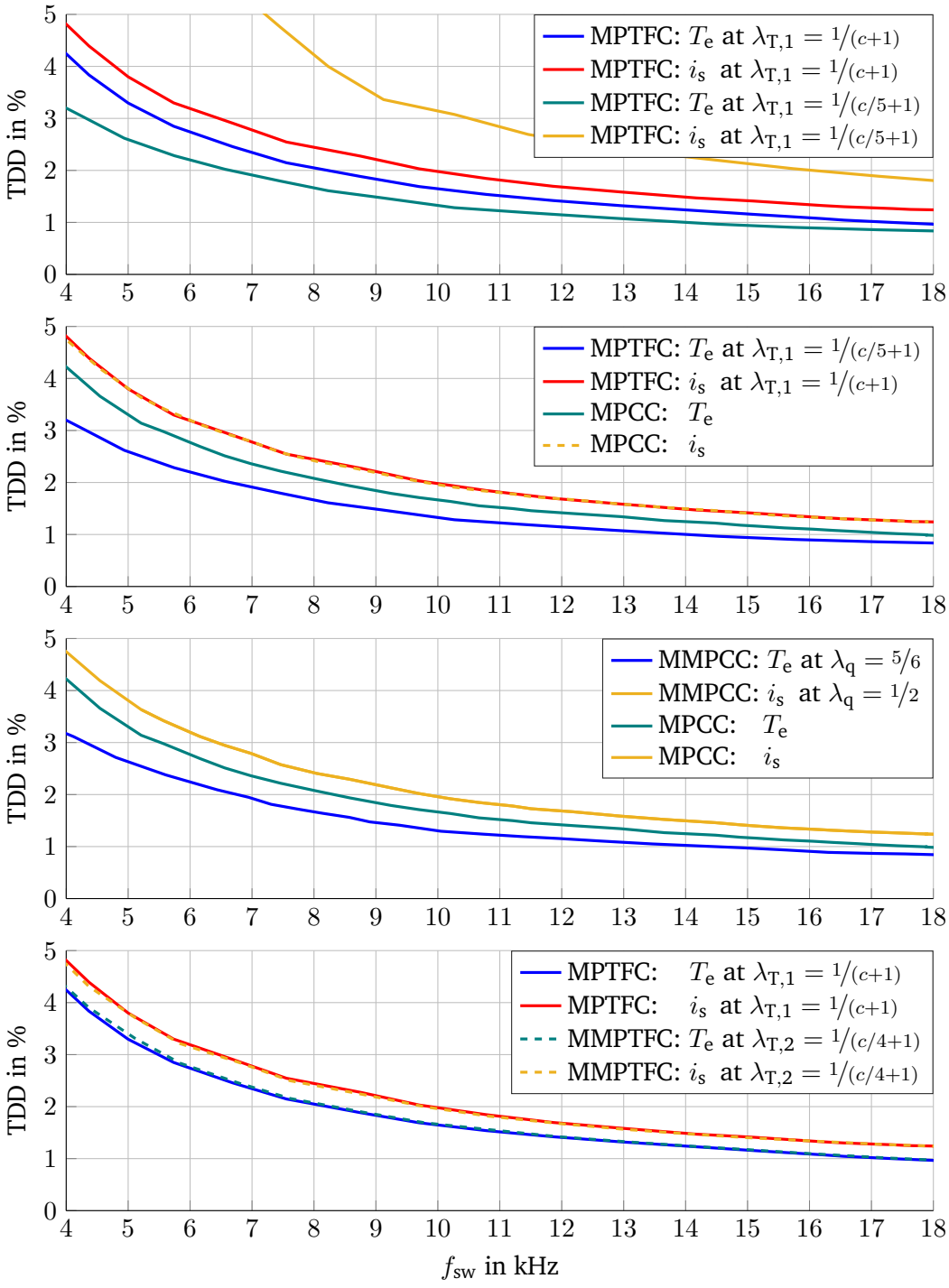


Figure 4.9.: Performance of respective torque and stator current TDD minimization vs. average switching frequency.

and MMPTFC, if their respective $\lambda_{T,circ}$-tuning is commissioned. Hence, the discussed distortions of the MPTFC and MMPTFC are negligible.

- Current: An applied curve-fitting shows that the current TDD approximately decreases with a propor-

tionality of $1/f_{\mathrm{sw}}$. This supports the theory established in Section 3.2.4 (cp. for instance Eq. (3.63)) and underpins the minimization capability of harmonic conduction losses in the machine.

- Equivalency: The performance of the MPCC, MMPCC, MPTFC and MMPTFC is almost identical, if their respective $\lambda_{\mathrm{T,circ}}$-tuning and $\lambda_{\mathrm{q}} = 0.5$ is set.

Spectral analysis
As the average switching frequency increases with a lower penalization of switching activity, the spectrum of the machine quantities likely are subject to a shift. Figure 4.10 illustrates this shift by comparing the spectrum of an arbitrary phase current for $\lambda_{\mathrm{sw}} = 0$ with the results for $\lambda_{\mathrm{sw}} = 2 \cdot \mathrm{e}^{-2}$. These weightings can be associated with average switching frequencies of approximately $18\,\mathrm{kHz}$ and $10\,\mathrm{kHz}$, respectively.

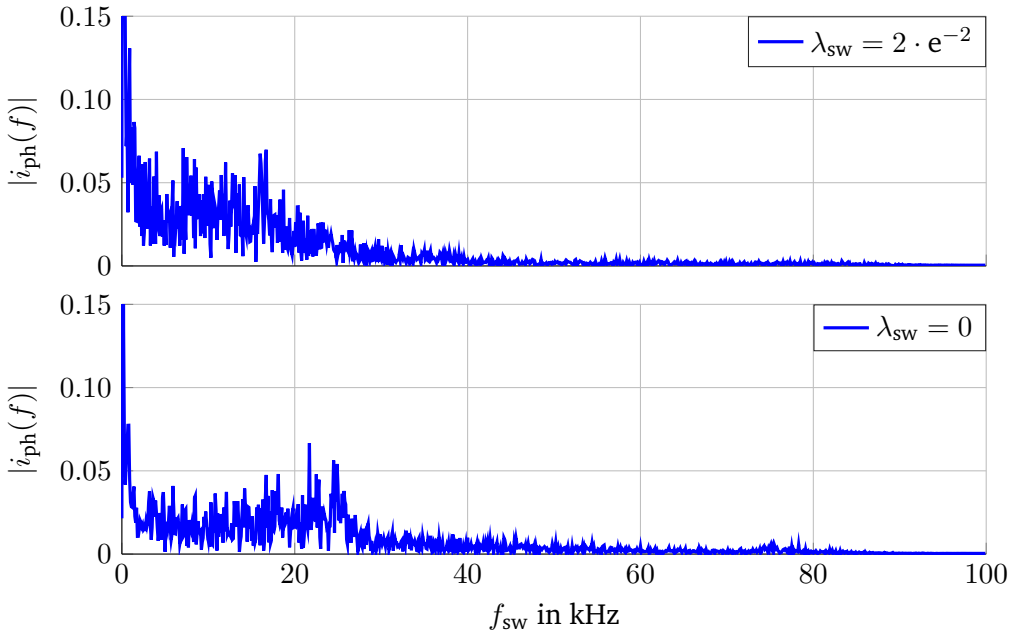


Figure 4.10.: Spectra of an arbitrary phase current for a high (top) and low (bottom) penalization of switching activity.

Firstly, the figure points out the relatively broad spectrum of the phase current, which is typical for FCS-MPC implementations. Secondly, it can be identified that the spectrum is shifted towards higher frequencies in the case of $\lambda_{\mathrm{sw}} = 0$. In addition, the amplitudes of the appearing frequencies overall decrease for this case, which suits the already identified decrease of current TDD for lowered values of λ_{sw}.

4.2.6. Transient Controller Performance

Since the transient controller performance of the MPCC and MMPCC is highly depend on the outer FOC-loop and the tuning of the flux controller, only the MMPTFC's (equivalently to the MPTFC's) performance is discussed in this section.

Performance for changes in reference torque
Figure 4.11 shows the step response of torque and stator flux magnitude for $T_{\mathrm{e}}^{*} = 0 \rightarrow T_{\mathrm{e}}^{*} = T_{\mathrm{e,n}}$, $\lambda_{\mathrm{T,2}} = {}^{1}/_{(c/4+1)}$ and otherwise nominal operating conditions. It can be seen that the torque is quickly following the reference change without any overshoot, while the stator flux magnitude is kept fairly steady at the desired value.

The latter property slightly impairs the dynamics of the torque reference tracking, i.e. the step response is not happening at the fastest speed possible. This can also be identified by the slightly lessening gradient of T_e during the tracking of the large reference step. A second reason for suboptimal torque reference tracking is obviously the limited capability of predicting the optimal trajectory for larger time horizons due to $N_\mathrm{p} = 1$.

Conversely, in Figure 4.12 the simulation results are shown for $\lambda_{\mathrm{T},2} = 0.01 \cdot {}^{1}/_{(c/4+1)}$, i.e. for a high prioritization of torque control quality. Clearly, the torque reference tracking is happening at a faster rate, which however comes at the cost of larger deviations of the desired machine magnetization and stator current TDD.

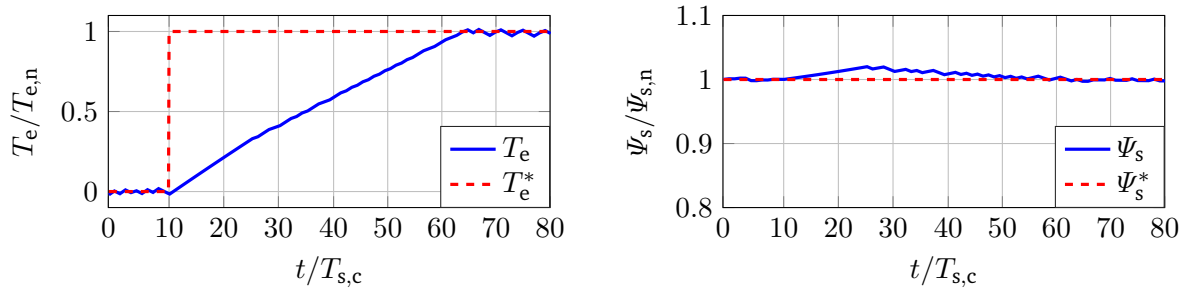


Figure 4.11.: Step response of torque and stator flux magnitude for $T_\mathrm{e}^* = 0 \rightarrow T_\mathrm{e}^* = T_\mathrm{e,n}$ and $\lambda_{\mathrm{T},2} = {}^{1}/_{(c/4+1)}$

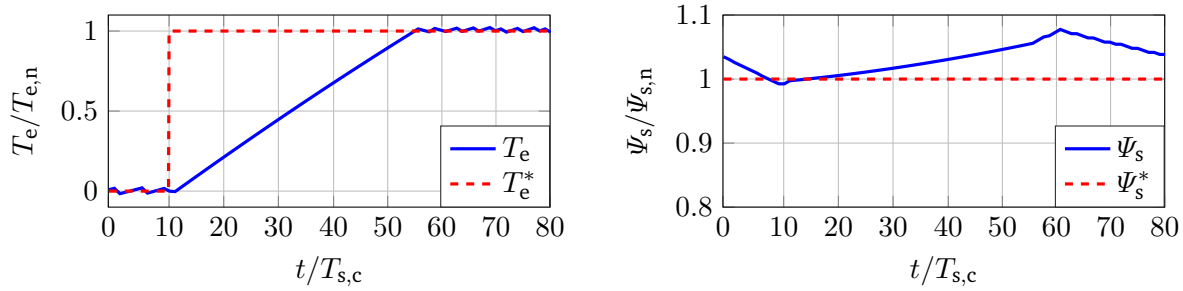


Figure 4.12.: Step response of torque and stator flux magnitude for $T_\mathrm{e}^* = 0 \rightarrow T_\mathrm{e}^* = T_\mathrm{e,n}$ and $\lambda_{\mathrm{T},2} = 0.01 \cdot {}^{1}/_{(c/4+1)}$.

Performance for changes in reference magnetization

Figure 4.13 shows the step response of an arbitrary phase current and the stator flux magnitude for $\Psi_\mathrm{s}^* = 0 \rightarrow \Psi_\mathrm{s}^* = \Psi_\mathrm{s,n}$ and $T_\mathrm{e}^* = 0, \lambda_{\mathrm{T},2} = {}^{1}/_{(c/4+1)}$. It represents the situation of an initial machine magnetization before regular operation modes are acquired.

As expected, the machine magnetization quickly follows the reference step. Furthermore, the the large step of Ψ_s^* imposes a very large overshoot of the stator current, which decays only slowly to its stationary value. The high values of $i_\mathrm{s,ph}$ can cause elevated power dissipation and therefore a large temperature rise in the respective power switches, which should be avoided. A straightforward way to avert the overshoots is to limit the dynamics and/or step sizes of the reference magnetization. Although this measure appears to be a crucial restriction, high dynamics with respect to the machine magnetization are usually not demanded: The value of Ψ_s^* normally changes only for new steady-state operating conditions with optimal reference magnetization (cp. Section 3.2.4) or for operating conditions in the field-weakening range. Regarding the latter, the necessity of

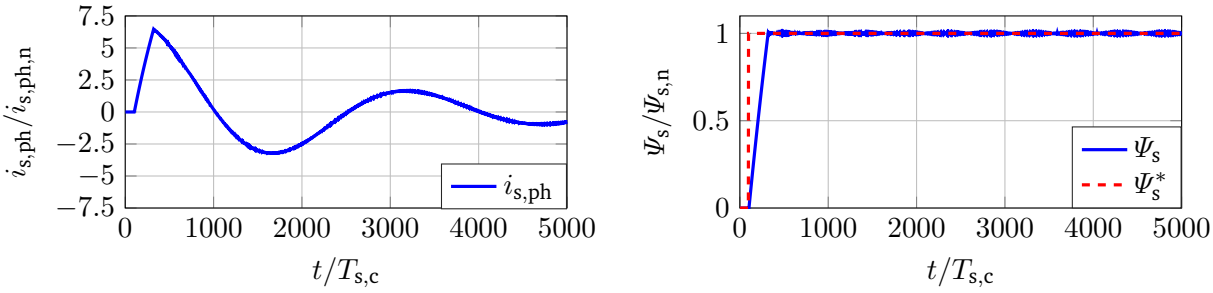


Figure 4.13.: Step response of stator flux magnitude and stator current for $\Psi_{\mathrm{s}}^* = 0 \rightarrow \Psi_{\mathrm{s}}^* = \Psi_{\mathrm{s,n}}$

dynamic magnetization follows from changes in the rotor speed, which inherently have a large time constant due to the rotational inertia at the machine shaft.

4.2.7. Comparison of Estimated Computational Resources

A summary of the discussed FCS-MPC implementations regarding their advantages, disadvantages and necessary computational resources for the respective cost functions is given in Table 4.1 (mathematical operations of the state-space model, the outer FOC loop as well as computations for determining weighting factors are not considered). The factors 7_{p}^N, 8_{p}^N etc. indicate operations linked to the FCS. This is due to the seven unique space-vectors in the alpha-beta plane and eight unique switch positions of the three-phase two-level inverter.

The condensed message of Table 4.1 is that the MPCC requires the least computational resources, but is also limited in its capabilities. The MMPCC necessitates less additions than the MMPTFC for its cost function, but needs more trigonometric functions for rotating the predicted stator currents. The most computational resources are required by the MPTFC.

For many applications, an online transition between torque and current TDD minimization is not required, and the torque TDD does not have to be minimized perfectly (disregarding fatigue-related effects). For example, this is usually the case for speed-controlled drives. For this particular application, the features of the MPCC are sufficient. However, the low demand of computational resources for the MPCC is only valid for $N_{\mathrm{p}} = 1$, as otherwise the future rotor alignments have to be considered for the prediction of the MPCC's *reference values*. On the other hand, higher prediction horizons usually allow a better overall performance, i.e. TDD minimization capability at a particular average switching frequency [55] [74], which is also shown in Section 4.3. Therefore, $N_{\mathrm{p}} > 1$ should be considered, if for instance machine *and* inverter loss minimization is of greater interest. In this case, the lowest demanding FCS-MPC implementation is not obvious. In fact, a trade-off between multiplications and trigonometric functions has to be performed in order to evaluate if the MPCC or the MMPTFC should be the controller of choice.

In many cases, the approximation of trigonometric functions such as $\mathrm{atan2}(*), \sin(*), \cos(*)$ rely on iterative methods, such as CORDIC algorithms [75]. Although this keeps the necessary multiplications and additions at bay, it leads to an increased computational delay of the overall controller algorithm, which is a converse property to fast sampling FCS-MPCs. Therefore, the MMPTFC appears to be a very promising implementation style with good performance and managable computational effort. For this reason, it is this variant that will be used for machine control in the sections to follow.

Table 4.1.: Summary of the advantages, disadvantages and computational effort of the discussed FCS-MPC implementations.

	MPTFC	MMPTFC
benefits	torque TDD minimization	torque TDD minimization
	current TDD minimization (distorted)	current TDD minimization (distorted)
drawbacks	square root operations	none
multiplications (#)	$8 \cdot 7^{N_\mathrm{p}} + 1 \cdot 8^{N_\mathrm{p}}$	$8 \cdot 7^{N_\mathrm{p}} + 1 \cdot 8^{N_\mathrm{p}}$
additions (#)	$4 \cdot 7^{N_\mathrm{p}} + 3 \cdot 8^{N_\mathrm{p}}$	$4 \cdot 7^{N_\mathrm{p}} + 3 \cdot 8^{N_\mathrm{p}}$
special operations	square root in $J_{\Psi,1}$: 7^{N_p}	none

	MPCC	MMPCC
benefits	current TDD minimization	current TDD minimization torque TDD minimization
drawbacks	requires FOC loop no torque TDD minimization	requires FOC loop rotation of predictions / FCS
multiplications (#)	$2 \cdot 7^{N_\mathrm{p}} + 1 \cdot 8^{N_\mathrm{p}} + 2 \cdot 7^{N_\mathrm{p}-1}$	$8 \cdot 7^{N_\mathrm{p}} + 1 \cdot 8^{N_\mathrm{p}}$
additions (#)	$3 \cdot 7^{N_\mathrm{p}} + 2 \cdot 8^{N_\mathrm{p}} + 2 \cdot 7^{N_\mathrm{p}-1}$	$3 \cdot 7^{N_\mathrm{p}} + 2 \cdot 8^{N_\mathrm{p}}$
special operations	trig. functions: $3 \cdot 7^{N_\mathrm{p}-1}$	trig. functions: $3 \cdot 7^{N_\mathrm{p}-1}$

4.3. Design and Evaluation of Finite Control Set Model Predictive Control for Interleaved Inverter System

In this section, the previously described and analyzed FCS-MPC is augmented by the capability of controlling the interleaved inverter structure that is discussed in Chapter 2 (cp. for instance Figure 2.1). The machine control itself will be based on the previously introduced MMPTFC with $N_\mathrm{p} = 1$, while the flux estimator is based on the current model (cp. Section 3.2.1). However, instead of merely considering the torque TDD, current TDD and average switching frequency, additional secondary control aims will be integrated in the control algorithm. These secondary control aims are meant to find solutions for problematic peculiarities of inverter-fed induction machines, but also for loss minimization of the overall drive inverter system. Secondary control aims that are focused on are:

- Restraining turn-off related over-voltages at the power switches,
- reduction of large voltage steps at the machine terminals ($\mathrm{d}v/\mathrm{d}t$-effects),
- minimization of common-mode voltage,
- minimization, symmetrization and shift of losses among semiconductors,
- minimization of losses appearing in the DC-link.

The implementation, algebraic analysis and simulation results are presented separately for each of these optimization goals. A complete overview of the respective simulation parameters is provided in Appendix B. Moreover, the benefits of prolonged prediction horizons, as well as the impacts of asymmetries, parameter mismatch and chosen discretization method are discussed. Lastly, a short outlook regarding further improvements to the approach of this thesis are addressed.

4.3.1. Initial Adaptions for Interleaved Inverter System

In order to transfer the previously introduced control algorithm to the interleaved inverter structure, the following adjustments have to be made.

Expansion of state vector
The state vector has to be expanded, since the rank of the system matrix for the interleaved system increases from $\mathrm{rank}(\boldsymbol{A}_\mathrm{c}) = 4$ to $\mathrm{rank}(\boldsymbol{A}_\mathrm{c}) = 7$ (cp. Appendix A.2). For this matter, the current share of one of the paralleled two-level inverters $\boldsymbol{i}_1^{\alpha\beta\gamma}$ is included in the state vector $\boldsymbol{x}$. This choice for the state vector is arbitrary, e.g. $\boldsymbol{x}$ can also be expanded with the current share of the other two-level inverter instead. Alternatively, the state vector can be chosen as $\boldsymbol{x} = (\boldsymbol{i}_1^{\alpha\beta\gamma}\ \boldsymbol{i}_2^{\alpha\beta\gamma}\ \boldsymbol{\Psi}_\mathrm{r}^{\alpha\beta})^\mathrm{T}$, or in fact any other combination that is capable of maintaining $\mathrm{rank}(\boldsymbol{A}_\mathrm{c}) = 7$ within the state-space representation. Note that the inclusion of $\boldsymbol{i}_1^{\alpha\beta\gamma}, \boldsymbol{i}_2^{\alpha\beta\gamma}$ increases the size of the resulting system matrix beyond 7×7 (and likewise the size of $\boldsymbol{B}_\mathrm{c}$), but leads to a higher degree of symmetry. The latter may be helpful for tuning observers such as a Kalman filter, but shall not be further considered in this thesis.

Augmentation of finite control set
The FCS for the interleaved inverter is expanded to a set of $2^6 = 64$ possible switch positions, i.e. $\boldsymbol{\mathcal{U}}_\mathrm{FCS} = \{-1, 1\}^6$. However, since the stator voltage's common-mode component $v_{\mathrm{s},\gamma}$ may be neglected for mere purposes of machine control, the Clarke transformation $\boldsymbol{T}_{\mathrm{c},2}$ can be applied. This results in 19 unique voltage space vectors. These space vectors and the size of the spanning hexagons are depicted in Figure 4.14. As can be seen, there

are 6 large space vectors (length $^2/_3 \cdot V_{\mathrm{dc}}$), 6 medium space vectors (length $^1/\sqrt{3} \cdot V_{\mathrm{dc}}$), 6 small space vectors (length $^1/_3 \cdot V_{\mathrm{dc}}$) as well as the zero-voltage space vector. The relation of switch positions and the resulting voltage space vector is given in Table A.2, which can be found in the appendix.

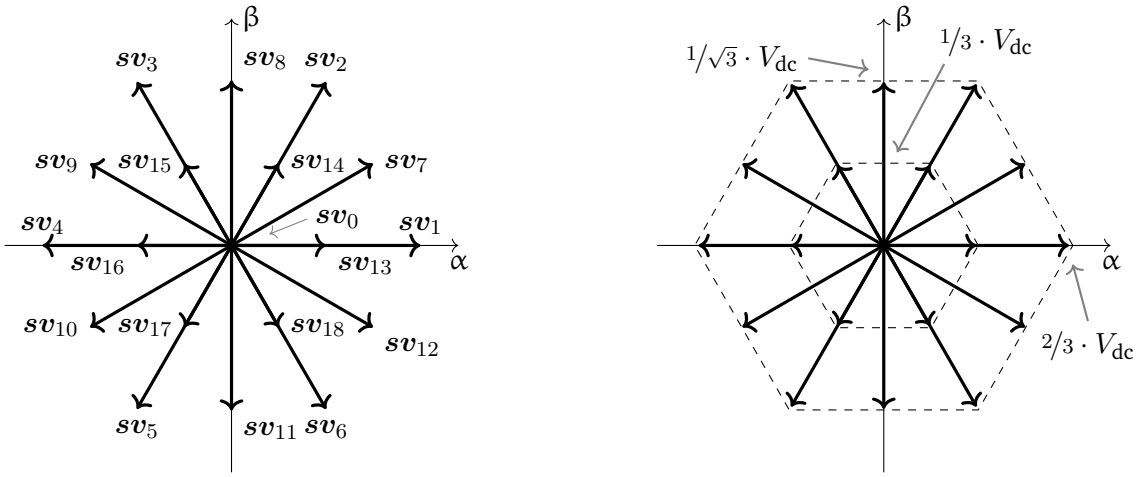


Figure 4.14.: Enumerated unique space vectors of a three-level three-phase inverter in the alpha-beta plane (left) and the size of the spanning hexagons (right).

Similarly to the redundancy of voltage space vectors with respect to the available switch positions, there also is a quasi-redundancy of interleaved states that lead to similar evolutions[13] of the cross-currents $\boldsymbol{i}_1 - \boldsymbol{i}_2$. This is summarized in Table A.1. Nevertheless, these redundancies are not congruent, i.e. the entire FCS has to be considered if machine control *and* the control of cross-currents is aspired.

Additional constraints for preventing saturation in interleaving chokes
As discussed in Chapter 2, the cross-currents have to be monitored phase-wise to detect and prevent any saturation in the chokes. This feature can be implemented by an according constraint $\boldsymbol{\mathcal{Y}}$ that limits the magnitude of cross-currents for each phase to a respective value i_{sat}, e.g.:

$$\boldsymbol{y}(k+1) \in \boldsymbol{\mathcal{Y}} = [0, i_{\mathrm{sat}}]^3$$

$$\text{where } \boldsymbol{y} = \begin{pmatrix} |i_{\mathrm{a},1} - i_{\mathrm{a},2}| & |i_{\mathrm{b},1} - i_{\mathrm{b},2}| & |i_{\mathrm{c},1} - i_{\mathrm{c},2}| \end{pmatrix}^{\mathrm{T}}$$

However, constraints such as the one defined above may lead to stability problems under certain conditions. For instance, if $\boldsymbol{y}(k)$ already is outside of the constraining set $\boldsymbol{\mathcal{Y}}$ as initial condition of the concurrent control algorithm step and further cannot meet the constraints within the prediction horizon, no valid solution or optimal switching sequence can be determined. In other words, an inherent tendency to decrease the violation of constraints is missing. Therefore, it is rather advised to implement such constraints as additional part of the cost function. For such implementation, the costs associated with the violation of constraints should increase monotonically and strongly, e.g. at least quadratically with respect to the deviation (see also Section 4.1.5).

[13] Switch positions that lead to identical values of $\boldsymbol{v}_1 - \boldsymbol{v}_2$ will not automatically lead to identical evolutions of the cross-currents, since the inverter's output voltage (being approximately proportional to $v_1 + v_2$) may differ. Since the overall stator current reacts to different stator voltages, the cross-currents may evolve slightly differently → quasi-redundancy.

4.3.2. Basic Machine Control

The machine control is implemented analogously to the MMPTFC of Section 4.2.2. In addition, the prevention of saturation for the interleaving chokes is implemented via the introduction of the term J_{sat}.

Formulation of Control Problem
This basic machine control (including saturation protection) is given in Eqn. (4.21).

$$
\begin{aligned}
&\underset{\boldsymbol{u}(k)}{\text{minimize}} \quad J_{\text{T},2}(k) + J_{\Psi,2}(k) + J_{\text{sw}}(k) + J_{\text{sat}}(k) \\
&\text{subject to} \begin{pmatrix} \boldsymbol{i}_{\text{s}}^{\alpha\beta}\,(k+1) \\ \boldsymbol{\Psi}_{\text{s}}^{\alpha\beta}(k+1) \\ \boldsymbol{i}_{1}^{\text{abc}}(k+1) \end{pmatrix} = \boldsymbol{A}_{\text{c}}(\omega_{\text{r}}) \cdot \begin{pmatrix} \boldsymbol{i}_{\text{s}}^{\alpha\beta}\,(k) \\ \widetilde{\boldsymbol{\Psi}}_{\text{s}}^{\alpha\beta}(k) \\ \boldsymbol{i}_{1}^{\text{abc}}(k) \end{pmatrix} + \boldsymbol{B}_{\text{c}}\, \boldsymbol{T}_{\text{c},2} \cdot (V_{\text{dc}}/2) \cdot \boldsymbol{u}(k) \\
&\qquad \boldsymbol{u}(k) \in \boldsymbol{\mathcal{U}}_{\text{FCS}} \\
&\qquad T_{\text{e}}(k+1) = \frac{3}{2} z_{\text{p}} \cdot \boldsymbol{\Psi}_{\text{s}}^{\alpha\beta}(k+1) \times \boldsymbol{i}_{\text{s}}^{\alpha\beta}(k+1) \\
&\qquad \boldsymbol{i}_{2}^{\text{abc}}(k+1) = \boldsymbol{T}_{\text{c},2}^{-1} \cdot \boldsymbol{i}_{\text{s}}^{\alpha\beta}(k+1) - \boldsymbol{i}_{1}^{\text{abc}}(k+1) \\
&\qquad J_{\text{T},2}(k) \;= \lambda_{\text{T},2} \cdot \left(T_{\text{e}}(k+1) - T_{\text{e}}^{*}\right)^2 \\
&\qquad J_{\Psi,2}(k) = (1 - \lambda_{\text{T},2}) \cdot ||\boldsymbol{\Psi}_{\text{s}}^{\alpha\beta}(k+1)||_2^2 - ({\Psi_{\text{s}}}^{*})^2 \\
&\qquad J_{\text{sw}}(k) = \lambda_{\text{sw}} \cdot ||\boldsymbol{u}(k) - \boldsymbol{u}(k-1)||_1 \\
&\qquad J_{\text{sat}}(k) = \begin{cases} \sum_{m \in \{\text{a,b,c}\}} \lambda_{\text{sat}} \cdot \left(|i_{1,m}(k+1) - i_{2,m}(k+1)| - i_{\text{sat,c}}\right)^2 & \text{if } |i_{1,m}(k+1) - i_{2,m}(k+1)| > i_{\text{sat,c}} \\ 0 & \text{else} \end{cases}
\end{aligned}
\tag{4.21}
$$

Note that the chosen state vector composition requires a transformation to the abc-reference system in order to acquire the second inverter's current share $\boldsymbol{i}_2$.[14]

The cost term J_{sat} penalizes parts of the predicted cross-currents' amplitudes when exceeding the value $i_{\text{sat,c}}$. In comparison to the implementation of a hard constraint $\boldsymbol{\mathcal{Y}}$ for avoidance of saturation in the interleaving chokes, the realization via J_{sat} comes at the price of setting $i_{\text{sat,c}} < i_{\text{sat}}$, i.e. below the actual saturation limit. In any other case, a true prevention of saturation cannot be achieved for obvious reasons. However, keeping the magnetizing current well below its physical limit may also be advantageous with respect to magnetization losses, which rise rapidly for higher flux density (cp. Section 6.1). The actual costs of J_{sat} are scaled by the factor λ_{sat}, if the limit $i_{\text{sat,c}}$ is reached. It should be chosen in a manner that the prevention of reaching $i_{\text{sat,c}}$ is still attained for large steps in the machine's reference magnetization or torque, which may also lead to large cost terms. For instance, with respect to the torque error, this can be fulfilled by $\lambda_{\text{sat}} \cdot \left(|i_{1,\text{ph,n}} + i_{2,\text{ph,n}}| - i_{\text{sat,c}}\right)^2 \gg \lambda_{\text{T},2} \cdot T_{\text{e,n}}^2$, where the index n indicates the rated values for the respective quantities. For the upcoming analyses, the weighting factor is set to $\lambda_{\text{sat}} = 5 \cdot 10^4$, yielding the following inequality:

$$
\lambda_{\text{sat}} \cdot \left(|i_{1,\text{ph,n}} + i_{2,\text{ph,n}}| - i_{\text{sat}}\right)^2 > 10 \cdot {}^{1}\!/_{(c/4+1)} \cdot T_{\text{e,n}}^2 \tag{4.22}
$$

[14] Since the interleaving chokes are implemented phase-wise, the abc-reference system is most suitable to observe the cross-currents and check for saturation constraints.

The controller's limit for the interleaving choke saturation is set to:

$$i_{\mathrm{sat,c}} = 1.2 \cdot {}^{2V_{\mathrm{dc}}}/_{(4M_{12})} \cdot T_{\mathrm{s,c}} \approx {}^{1}/_{4} \cdot i_{\mathrm{ph,n}} \tag{4.23}$$

The chosen $i_{\mathrm{sat,c}}$ allows the magnetization of a respective interleaving choke for one controller time step (including an additional margin of 20%), if a prior symmetrical current loading is assumed.

Analysis of switching patterns

As indicated above, the interleaved switch positions[15] cannot be held for several controller time steps without having any switching activity. This is due to the inherent magnetization of the interleaving chokes during interleaved states. Hence, at some point the switch positions have to be altered to initiate a corresponding demagnetization in order to prevent saturation. Nevertheless, all of the interleaving space vectors have a redundancy with respect to their switch positions. This redundancy in fact always allows a magnetization and demagnetization of the participating chokes (cp. Table A.1 and Table A.2). Therefore, any interleaved voltage space vector in the $\alpha\beta$-plane can be held for an arbitrary duration.

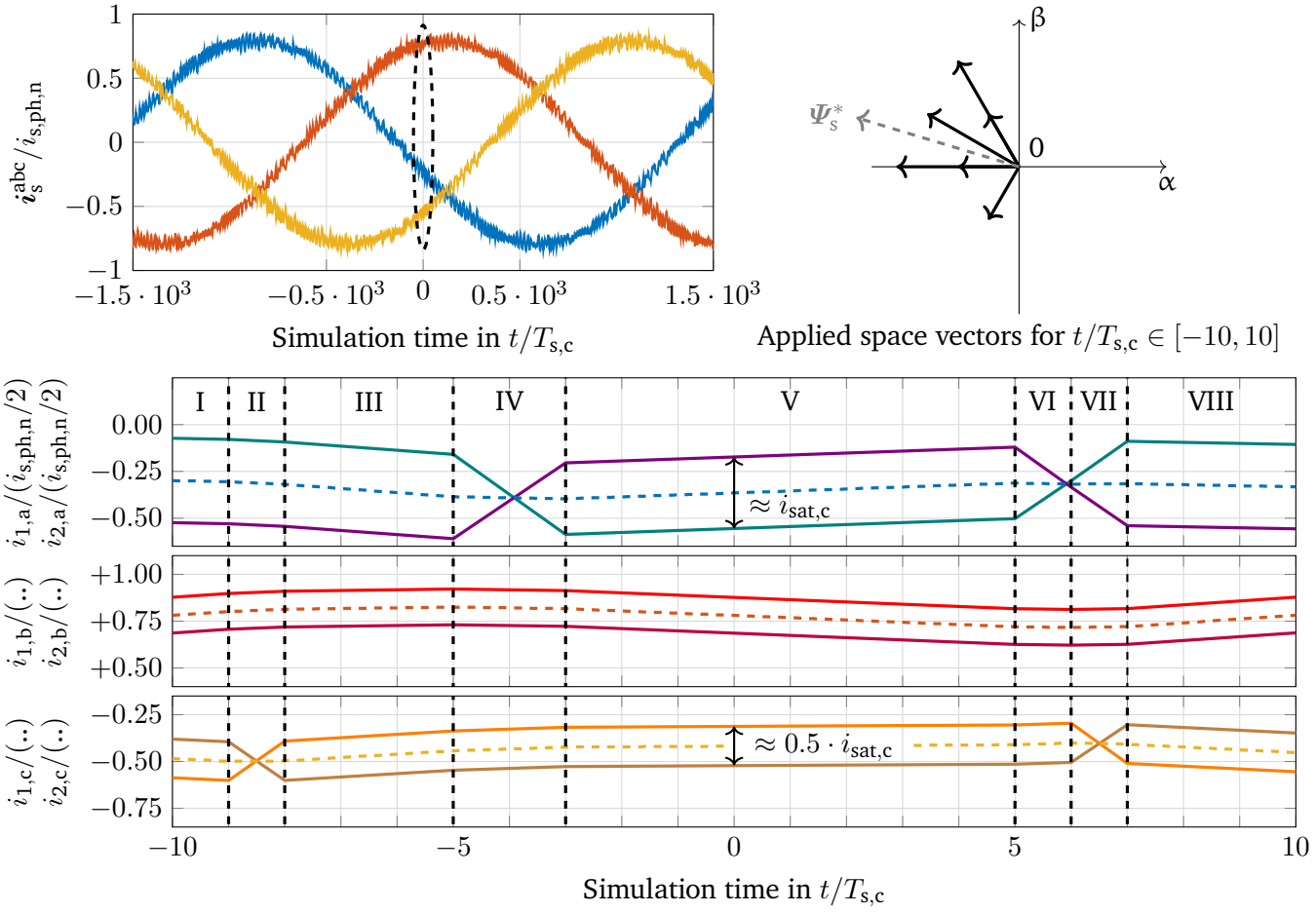


Figure 4.15.: Exemplary pattern of applied switching states $(s_1^{\mathrm{abc}} s_2^{\mathrm{abc}})$ and their impact on i_1^{abc} and i_2^{abc}. The respective states are: I $\rightarrow (010010)$, II $\rightarrow (010011)$, III $\rightarrow (011011)$, IV $\rightarrow (011111)$, V $\rightarrow (111111)$, VI $\rightarrow (111011)$, VII $\rightarrow (111010)$, VIII $\rightarrow (010010)$.

[15] Space vectors enumerated as 7 - 18 in Figure 4.14, as well as some of the zero-voltage space vectors (cp. Table A.2)

In spite of this capability, a more frequently encountered pattern is the usage of various voltage space vectors for machine control and balancing the chokes' magnetization. This can even be observed for very short time frames, e.g. $\Delta t = 20 \cdot T_{\mathrm{s,c}}$. Exemplary simulated time characteristics of this behavior are given in Figure 4.15. It is noteworthy that the established pattern often, but not always switches only one transistor for each controller time step, as it is also depicted in Figure 4.15. No concurrent switching is a very positive feature, since simultaneous turn-offs can lead to large transient over-voltages at the power switches and should therefore be avoided (cp. Section 3.1.3). Nevertheless, this property cannot be ensured with the provided controller implementation, particularly for low values of λ_{sw}. Hence, further adaptions of the cost function should be considered (cp. Section 4.3.3).

Analysis of interleaving chokes' magnetization modes

Figure 4.15 also shows that the appearing magnitude of the cross-currents $i_{1,\mathrm{ph}} - i_{2,\mathrm{ph}}$ can follow from two general magnetization modes:

- Mode 1: An interleaved state for the duration of $2 \cdot T_{\mathrm{s,c}}$ leads to a symmetrical polarization in phase a. The maximum magnitude of the cross-current in this phase is approximately ${}^{2V_{\mathrm{dc}}}/_{(4M_{12})} \cdot T_{\mathrm{s,c}}$ $(\approx i_{\mathrm{sat,c}})$.
- Mode 2: An interleaved state for the duration of $T_{\mathrm{s,c}}$ leads to a symmetrical polarization in phase c. The maximum magnitude of the cross-current in this phase is approximately ${}^{V_{\mathrm{dc}}}/_{(4M_{12})} \cdot T_{\mathrm{s,c}}$ $(\approx 0.5 \cdot i_{\mathrm{sat,c}})$.

The reason that both of these choke magnetization modes can exist is linked to the decaying influence of an applied interleaving vector on the cross-currents (cp. Section 3.1.2 / Figure 3.8). If the polarity of a respective cross-current is changed regularly and in time spans considerably shorter than the time constant of the choke (i.e. the time constant of the decay), Mode 1 is established. The direction of decay is alternating together with the polarity of the cross-current. Overall, the partial decays compensate each other (cp. Figure 4.16, left).

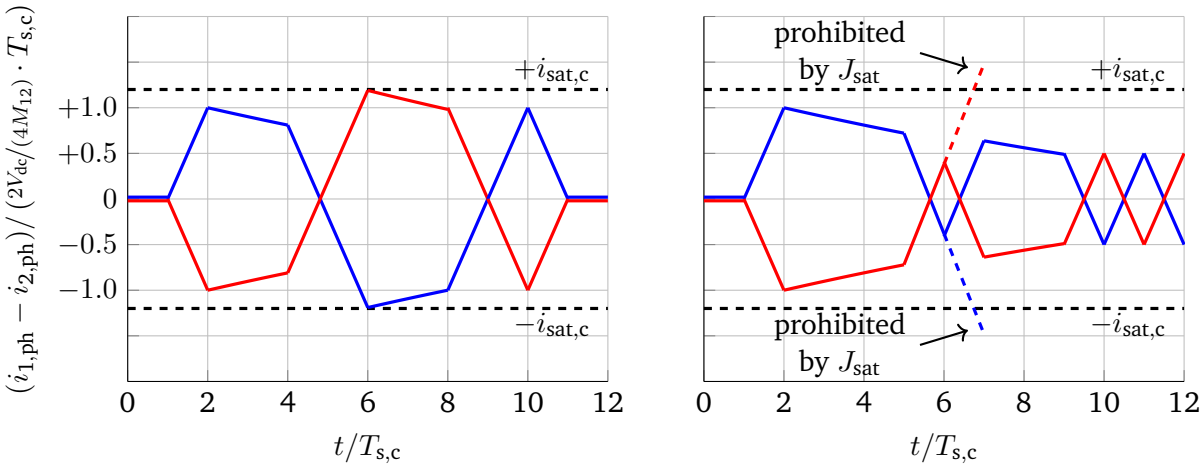


Figure 4.16.: Explanatory switching pattern for origin of magnetization modes for cross-currents.

On the other hand, if the polarity of the cross-currents is not changed regularly, the decay is not being compensated. Over time, the cross-current's magnitude decreases. As soon as the decay advances to the point that a respective interleaving state cannot be held for $2 \cdot T_{\mathrm{s,c}}$ anymore, the magnetization slides[16] into an unfixed mode. The polarization is unsymmetrical in this operating mode until an alternating polarity pattern is re-initiated at the level $|i_{1,\mathrm{ph}} - i_{2,\mathrm{ph}}| = {}^{2V_{\mathrm{dc}}}/_{(4M_{12})} \cdot T_{\mathrm{s,c}}$, leading to Mode 2. (cp. Figure 4.16, right).

[16] Please note that the decaying characteristics of the cross-current are usually not as pronounced as depicted in Figure 4.16, i.e. it can take several thousand controller samplings $T_{\mathrm{s,c}}$ before the choke magnetization slides into Mode 2.

Mode 1 clearly is the preferable magnetization mode, since it takes advantage of the full *intended* interleaving capability of the chokes, which is defined by $i_{\text{sat,c}}$. Particularly, it requires less switching activity for keeping the interleaving chokes' magnetization within the imposed saturation limits while using interleaved states. Nonetheless, the conservation of Mode 1 cannot be ensured by the control problem formulation of Eqn. (4.21). In fact, it can be observed that the two magnetization modes alternate in the time span of several seconds.

In order to overcome this issue, a Mealy machine can be designed that guarantees the necessary alternating polarity pattern of the cross-currents, as given in Figure 4.17. Depending on the previous control actions, either a future neutral/negative evolution ($J'_{\text{magmode},m} = -1$) or a neutral/positive evolution ($J'_{\text{magmode},m} = +1$) is imposed on the respective cross-current $i_{1,\text{ph}} - i_{2,\text{m}}$. Together with the additional cost term J_{magmode} defined in Eq. (4.24), the state machine establishes the repeating state sequence $\{... \rightarrow q3 \rightarrow q4 \rightarrow q5 \rightarrow q6 \rightarrow q3 \rightarrow ...\}$, which is equivalent of maintaining Mode 1 for the chokes' magnetization[17].

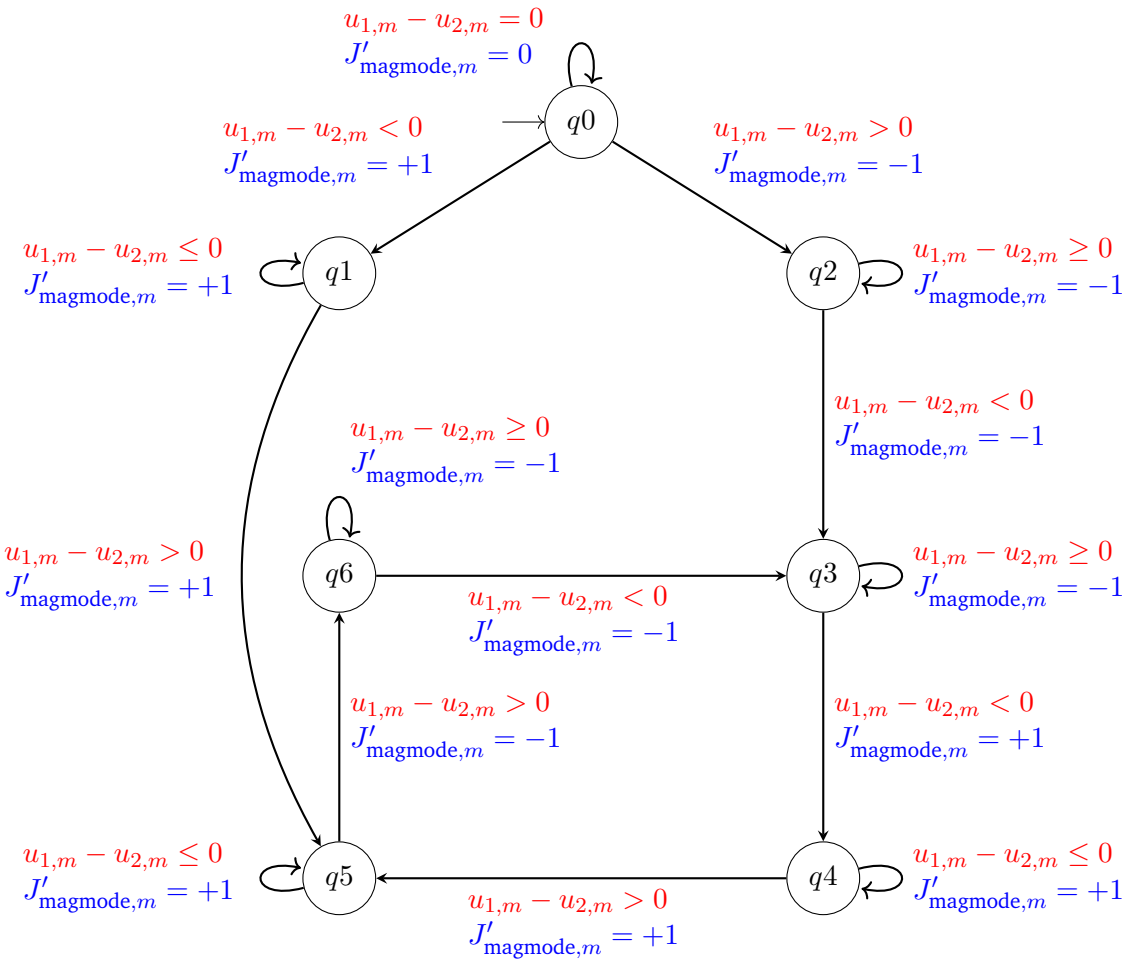


Figure 4.17.: Mealy machine with inputs of time instant $(k-1)$ and outputs of time instant (k) for maintaining Mode 1 for choke magnetization.

[17] A similar finite state machine can also be defined to hold the chokes' magnetization in Mode 2. Due to its similarity to the Mealy machine in Figure 4.17, it is not explicitly depicted in this thesis.

$$J_{\text{magmode}}(k) = \lambda_{\text{magmode}} \cdot \left(\sum_{m \in \{\text{a,b,c}\}} J''_{\text{magmode},m}(k) \right)$$

$$J''_{\text{magmode},m}(k) = \begin{cases} 1 & \text{if } J'_{\text{magmode},m}(k) < 0 \wedge u_{1,m}(k) - u_{2,m}(k) > 0 \\ 1 & \text{if } J'_{\text{magmode},m}(k) > 0 \wedge u_{1,m}(k) - u_{2,m}(k) < 0 \\ 0 & \text{else} \end{cases} \tag{4.24}$$

The weighting term can be chosen to $\lambda_{\text{magmode}} = \lambda_{\text{sat},1}/10$, i.e. the penalization for violating the switching scheme is less weighted than the costs for exceeding the choke saturation limit, but still leads to a larger costs than reference changes of torque and flux (even if their changes are in the range of the rated values).

Note that the activation of J_{magmode} can also be seen as saturation protection for the interleaving chokes. However, unmatched winding parameters or adverse starting conditions (cp. Section 4.3.11) make it reasonable to retain the cost term J_{sat}, which implements the saturation protection based on current measurement feedback.

Analysis of stationary performance

The trade-off between torque and flux control quality, including the tuning for minimized stator current TDD, is accomplished identically to the MMPTFC design of Section 4.2.2 with $\lambda_{\text{T},2} = 1/(c/4+1)$. However, due to the additional voltage space vectors that are available for machine control, generally a more performant TDD minimization can be anticipated. The explicit reason for the performance boost lies in the smaller angles between the available space vectors of the interleaved converter ($\Delta\theta_{\text{sv}} = \pi/6$) when compared to the two-level inverter ($\Delta\theta_{\text{sv}} = \pi/3$). These smaller angles correspond to a lowered granularity, i.e. higher resolution of the finite control set. Likewise, the space vectors of smaller amplitude[18] enhance the resolution of the FCS. Overall, this brings the determined optimal switch positions of the FCS-MPC closer to the optimal output voltage of a continuous control set, which can be seen as true optimum for the respective prediction horizon.

In Figure 4.18 the basic performance of current and torque TDD minimization vs. the average switching frequency is given. The interleaved system's performance (3L) is compared to the regular two-level inverter[19] (2L). The simulation parameters are identical to the ones provided in Section 4.2.5. The magnetization of the interleaving chokes is kept strictly at Mode 1, i.e. the cost term J_{magmode} is active.

Figure 4.18 clearly shows that the capability of the interleaved inverter system strongly outperforms the one of a simple two-level inverter for $f_{\text{sw}} > 5\,\text{kHz}$. The achievable minimum of TDD is reached at $f_{\text{sw}} \approx 14\,\text{kHz}$, and a further increase of λ_{sw} does not increase the switching frequency anymore[20]. However, the interleaved inverter's outperformance lessens for high values of λ_{sw}, which lead to $f_{\text{sw}} < 5\,\text{kHz}$. For very low switching frequencies, the interleaved inverter can even perform worse than the regular two-level inverter. The performance deficit can be explained by the circumstance that the enforced lessening of switching activity conflicts with the usage of interleaved switching states, which cannot be held for several time steps without switching activity. The controller holds the interleaved states as long as possible to avoid switching, but eventually has to initiate a demagnetization with a then impaired set of allowed switch positions. The selection of $N_{\text{p}} = 1$ does not enable the controller to predict these incompatibilities. For this reason, unfavorable optima are regularly determined for the low ranges of f_{sw}.

[18] Enumerated with indexes 13 - 18 in Figure 4.14

[19] The two-level inverter is synthesized by disabling the interleaving capability of the interleaved inverter topology.

[20] The TDDs are depicted as horizontal lines from this point on to facilitate the comparisons. A further minimization of TDD is only possible with a lowered controller sampling time $T_{\text{s,c}}$, which decreases the granularity / increases the time resolution of the FCS-MPC.

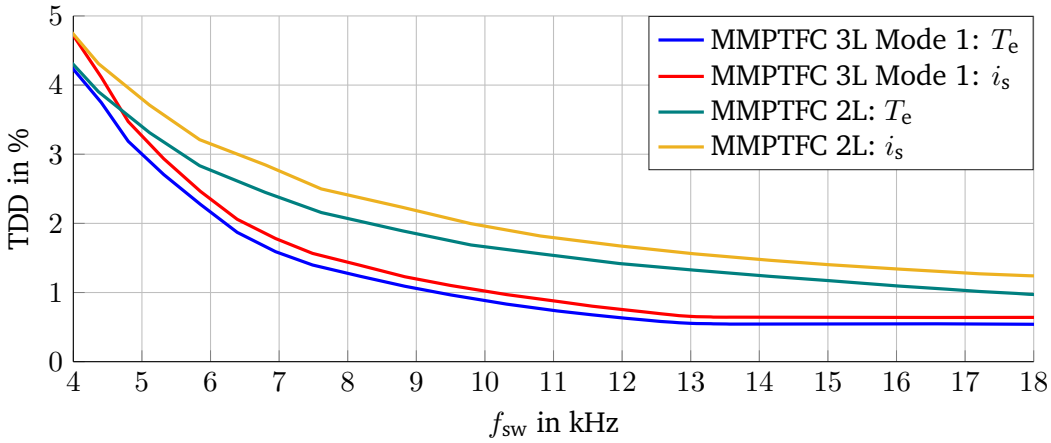


Figure 4.18.: Performance of respective torque and stator current TDD minimization vs. average switching frequency. Comparing the MMPTFC principle for the regular two-level inverter with the interleaved inverter system with choke magnetization in Mode 1.

For the sake of completeness, the performance of the interleaved inverter system in Mode 1 is compared to the results of an implementation with Mode 2 and without any fixed choke magnetization mode, i.e. an inactive cost term J_{magmode}. The corresponding results in Figure 4.19 underpin that Mode 1 is the preferable one, which however also tends to brings upon higher magnetization losses. The performance of Mode 2 approaches the TDD of Mode 1 for very low and very high switching frequencies, whereas it is considerably worse otherwise. The unfixed mode may perform similar to Mode 1 or Mode 2, depending on the appearing magnetization mode during the signal capturing. Due to the superiority of Mode 1, it is to be maintained for the remaining analyses, unless mentioned otherwise.

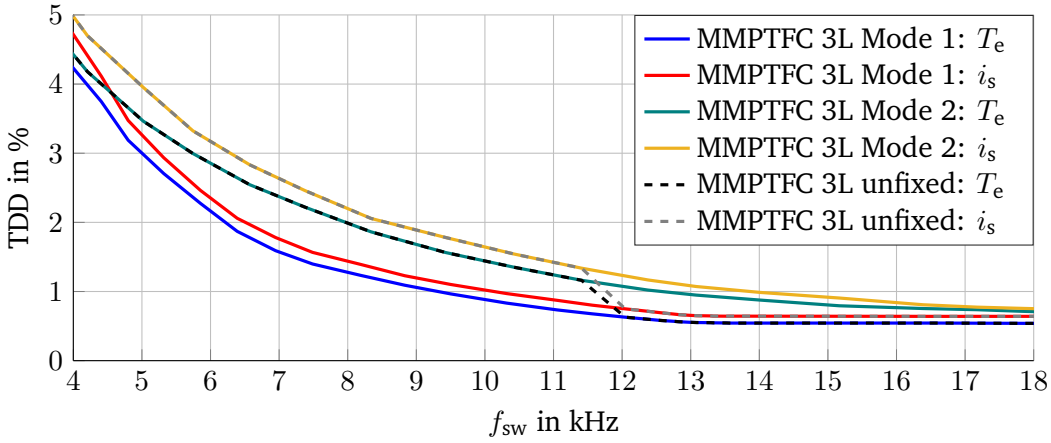


Figure 4.19.: Performance of respective torque and stator current TDD minimization vs. average switching frequency. Comparing the choke magnetizations Mode 1, Mode 2 and without fixed choke magnetization mode.

Supplementary simulation results are provided in Appendix C.2.

4.3.3. Restraining of Over-Voltages during Transistor Turn-Off

Section 3.1.3 already provided the explanation for the mechanism of increased transient voltages at the power switches during their respective turn-off, and the reasoning for keeping these over-voltages appropriately bounded during regular operation. The usual approach for restraining the voltage transients is found in the implementation of PWM methods (e.g. sinusoidal PWM, space vector modulation etc.): The sequence of applied space vectors is chosen in a manner that only one switch at a time is changing. However, in case of a FCS-MPC respective constraints have to be defined. In the previous section it was shown that the general penalization of switching activity does not necessarily prevent concurrent turn-offs. Hence, modifications of the cost term J_{sw} are required.

Limitation of concurrent turn-offs for each two-level inverter
A straightforward fix can be implemented by explicitly increasing the costs of multiple switching actions for *each* of the two-level inverters:

$$\begin{aligned} J_{\text{sw,ovv1}}(k) &= \begin{cases} \lambda_{\text{sw,ovv1}} & \text{if } J''_{\text{sw,ovv1,1}}(k) > 1 \vee J''_{\text{sw,ovv1,2}}(k) > 1 \\ 0 & \text{else} \end{cases} \\ J''_{\text{sw,ovv1},l}(k) &= \sum_{m \in \{\text{a,b,c}\}} J'_{\text{sw,ovv1},l,m}(k) \\ J'_{\text{sw,ovv1},l,m}(k) &= \begin{cases} 1 & \text{if } |u_{l,m}(k) - u_{l,m}(k-1)| \neq 0 \\ 0 & \text{else} \end{cases} \end{aligned} \tag{4.25}$$

The usage of $J_{\text{sw,ovv1}}$ can be helpful for constraining the switching-related over-voltages in case of separate or shared supply line leakages for the two-level inverters (cp. Figure 3.14). Note that a concurrent switching is allowed as long as it is distributed on both of the two-level inverters, i.e. $J_{\text{sw,ovv1}} = 0$ for $J''_{\text{sw,ovv1,1}}(k) = J''_{\text{sw,ovv1,2}}(k) = 1$.

Limitation of concurrent turn-offs for combined two-level inverters
If a common leakage inductance is assumed[21], an improved term $J_{\text{sw,ovv,2}}$ can be defined:

$$\begin{aligned} J_{\text{sw,ovv2}}(k) &= \begin{cases} \lambda_{\text{sw,ovv2}} & \text{if } J''_{\text{sw,ovv2}}(k) > 2 \\ 0 & \text{else} \end{cases} \\ J''_{\text{sw,ovv2}}(k) &= \sum_{l \in \{1,2\}} \sum_{m \in \{\text{a,b,c}\}} J'_{\text{sw,ovv2},l,m}(k) \\ J'_{\text{sw,ovv2},l,m}(k) &= \begin{cases} 1 & \text{if } |u_{l,m}(k) - u_{l,m}(k-1)| \neq 0 \\ 0 & \text{else} \end{cases} \end{aligned} \tag{4.26}$$

The term $J_{\text{sw,ovv2}}$ penalizes any cases of more than two concurrent switching actions. Due to the common supply line leakage, a distinction between the two two-level inverters then does not have to be made, i.e. it does not matter in which half bridges the transistors are switched. This provides overall more flexibility for the FCS-MPC.

[21] This assumption is based on the circumstance that good hardware designs either indeed have a common supply line leakage, or they have very low supply line leakage and the over-voltage is primarily linked to the equivalent series inductance $L_{\text{dc,ser}}$ of the DC-link capacitors. The latter is inherently shared by both two-level inverters.

Limitation of expected transient over-voltage

The previously described methods reliably prevent multiple switching activities, but also restrict the allowed set of upcoming switch positions of the FCS-MPC more than actually necessary. A presumably better solution can be found by directly predicting costs associated with the expected over-voltages. Respective values can then be determined by taking into account the actual transistor currents that have to be switched.

$$J_{\mathrm{sw,ovv3}}(k) = \begin{cases} \lambda_{\mathrm{sw,ovv3}} \cdot J'_{\mathrm{sw,ovv3}}(k) & \text{if } J'_{\mathrm{sw,ovv3}}(k) > u_{\mathrm{ovv,off}} \\ 0 & \text{else} \end{cases}$$

$$J'_{\mathrm{sw,ovv3}}(k) = \frac{1}{\hat{i}_{1,\mathrm{ph,n}}} \cdot \left(\sum_{l=\{1,2\}} \sum_{m\in\{\mathrm{a,b,c}\}} |u_{l,m}(k) - u_{l,m}(k-1)| \cdot i_{l,m}(k) \right) \tag{4.27}$$

Note that the cost term described by Eqn. (4.27) allows a compensation of turn-on and turn-off activities, as the respective current polarity is considered. This compensation in fact also applies to the transient over-voltages owing to a common leakage inductance. It generally provides the possibility of allowing multiple turn-offs, if simultaneous turn-ons are keeping the resulting over-voltage appropriately low.[22] The value $u_{\mathrm{ovv,off}}$ describes the boundary at which the concurrent switching activities lead to an expected over-voltage that is no longer tolerable for the specific hardware design.

Performance analysis

Figure 4.20 shows the controller performance of the various implementations at rated machine operation. The weighting terms can be chosen to $\lambda_{\mathrm{sw,ovv1}} = \lambda_{\mathrm{sw,ovv2}} = \lambda_{\mathrm{sw,ovv3}} = \lambda_{\mathrm{sat}}/10$, i.e. concurrent switching is less weighted than the costs for exceeding the choke saturation limit, but still lead to a larger penalization than reference changes of torque and flux (even if their changes are in the range of the rated values). In order to ensure a fair comparison between the three methods, $u_{\mathrm{ovv,off}} = 2$ is chosen. This ensures that over-voltages corresponding to two concurrent turn-offs at rated current are avoided in any case.

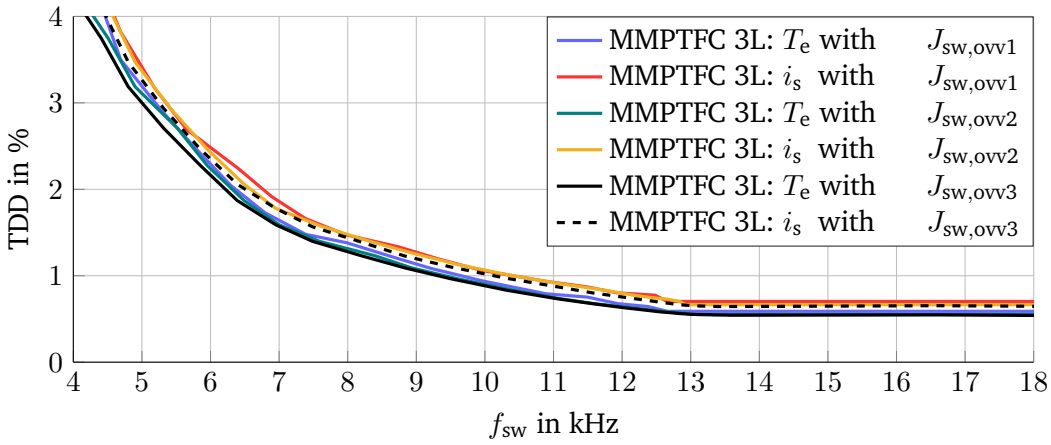


Figure 4.20.: Performance of respective torque and stator current TDD minimization vs. average switching frequency for various methods of restraining transient over-voltages at rated machine operation.

Clearly, the advantage of replacing $J_{\mathrm{sw,ovv1}}$ with $J_{\mathrm{sw,ovv2}}$ or $J_{\mathrm{sw,ovv3}}$ is only modest, as shown in Figure 4.20, pointing out that the restriction of the FCS with respect to concurrent switching is mainly negligible. On the

[22] Note that this kind of compensation between turn-on and turn-off related voltage drops at the common leakage inductance may require additional adaptive measures such as variable dead-time, as mentioned in Section 3.1.3.

other hand, the implementation of $J_{\text{sw,ovv2}}$ or $J_{\text{sw,ovv3}}$ only requires little additional computational burden[23] and might outperform $J_{\text{sw,ovv1}}$ for other operating conditions of the machine. In summary, a strong recommendation on which implementation should be chosen cannot be provided. Nevertheless, method $J_{\text{sw,ovv3}}$ will be used henceforth, since it is capable of providing identical results when compared to a completely deactivated $J_{\text{sw,ovv}}$ while ensuring the over-voltage limitations (cp. Figure 4.21 with $u_{\text{ovv,off}} = 1.5$).

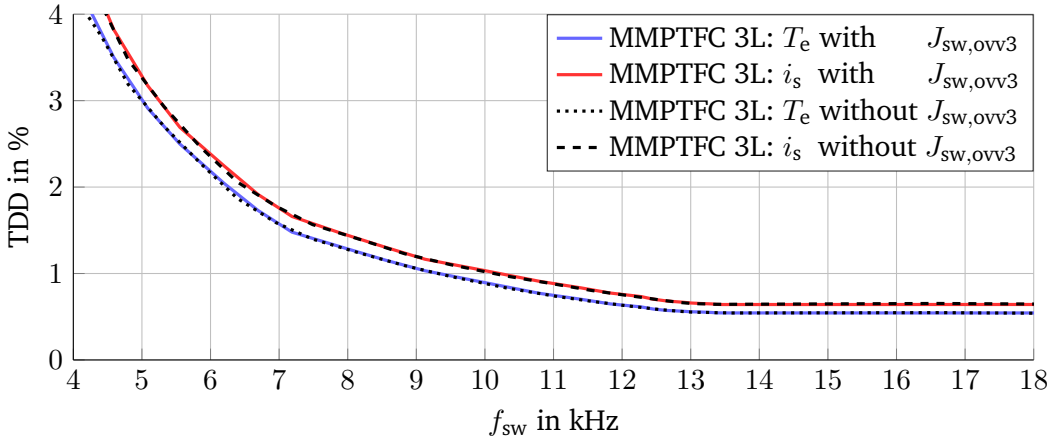


Figure 4.21.: Performance of respective torque and stator current TDD minimization vs. average switching frequency without and with $J_{\text{sw,ovv3}}$ for restraining transient over-voltages at rated machine operation.

Supplementary simulation results are provided in Appendix C.3.

4.3.4. Reduction of Large Voltage Steps at the Machine Terminals

As discussed in Section 3.2.4, high rates of change of the machine's stator voltage cause stress on the motor's insulation and therefore should be limited. The high values of $|\mathrm{d}v_s/\mathrm{d}t|$ are caused by fast switching semiconductors and can even increase further in the case of long motor cables due to reflection phenomena. However, the usage of long motor cables may be a necessity of the particular hardware setup and fast switching semiconductors are essential for implementing designs with high switching frequency. On the other hand, remedies such as the usage of specialized filters inherently increase the costs of the system and come at the expense of additional losses. However, the rate of stator voltage change can also be manipulated by the control algorithm, e.g. by restraining the switching activity to avoid large voltage steps. This measure is discussed in the following.

Restraining of large phase-to-phase voltage steps

The easiest method for reducing large phase-to-phase voltage steps[24] by the controller is to dynamically restrict the FCS in a respective manner. In the previous section, a similar restriction has been introduced to limit concurrent turn-offs of the power switches. For the purpose of restraining large voltage steps, another cost function term can be defined analogously. As it can be seen, the partial terms (e.g. $J'_{\text{sw,dv/dt,ab}}$) impose costs for any switching activity that yields a phase-to-phase voltage change larger than $V_{\text{dc}}/2$. The overall term $J_{\text{sw,dv/dt}}$ then simply sums up the restrictions for all of the phase-to-phase combinations.

[23] The multiplication $(u_{l,m}(k) - u_{l,m}(k-1)) \cdot i_{l,m}(k)$ appears to be computational demanding, but in fact only represents a masking of the the inverter leg currents with 1 or -1, which requires very little computational resources.

[24] As discussed in Section 3.2.4, primarily fast changes of the phase-to-phase voltages are of interest with respect to the issue of machine insulation stress.

$$
\begin{aligned}
J_{\text{sw,dv/dt}}(k) &= \lambda_{\text{sw,dv/dt}} \cdot \left(\sum_{m \in \{\text{ab,ac,bc}\}} J'_{\text{sw,dv/dt},m}(k) \right) \\
J'_{\text{sw,dv/dt,ab}}(k) &= \begin{cases} 1 & \text{if } |u_{\text{ab}}(k) - u_{\text{ab}}(k-1)| > 2 \\ 0 & \text{else} \end{cases} \\
J'_{\text{sw,dv/dt,ac}}(k) &= \begin{cases} 1 & \text{if } |u_{\text{ac}}(k) - u_{\text{ac}}(k-1)| > 2 \\ 0 & \text{else} \end{cases} \\
J'_{\text{sw,dv/dt,bc}}(k) &= \begin{cases} 1 & \text{if } |u_{\text{bc}}(k) - u_{\text{bc}}(k-1)| > 2 \\ 0 & \text{else} \end{cases} \\
u_{\text{ab}} &= u_{1,\text{a}} + u_{2,\text{a}} - u_{1,\text{b}} - u_{1,\text{b}} \\
u_{\text{bc}} &= u_{1,\text{b}} + u_{2,\text{b}} - u_{1,\text{c}} - u_{1,\text{c}} \\
u_{\text{ac}} &= u_{1,\text{a}} + u_{2,\text{a}} - u_{1,\text{c}} - u_{1,\text{c}}
\end{aligned} \tag{4.28}
$$

Since the phase-to-phase voltages naturally are common-mode free, they can also be interpreted as voltage space vectors in the $\alpha\beta$-plane. The various phase-to-phase voltage space vectors that result from different switch positions stand in the same relation to each other as found for the regular phase voltage. Hence, large voltage steps with respect to the phase-to-phase voltage are equivalent to large differences within sequencing phase voltage space vectors. The cost term in Eq. (4.28) dynamically restrains the available voltage space vectors to the *direct* neighbors of the current one. Exemplary sequences are (cp. Figure A.1):

$$
\begin{aligned}
\boldsymbol{v}_{\text{s,sv1}}(k-1) &\rightarrow \{\boldsymbol{v}_{\text{s,sv1}}(k), \boldsymbol{v}_{\text{s,sv12}}(k), \boldsymbol{v}_{\text{s,sv13}}(k), \boldsymbol{v}_{\text{s,sv7}}(k)\} \\
\boldsymbol{v}_{\text{s,sv13}}(k-1) &\rightarrow \{\boldsymbol{v}_{\text{s,sv13}}(k), \boldsymbol{v}_{\text{s,sv0}}(k), \boldsymbol{v}_{\text{s,sv14}}(k), \boldsymbol{v}_{\text{s,sv18}}(k), \boldsymbol{v}_{\text{s,sv7}}(k), \boldsymbol{v}_{\text{s,sv12}}(k), \boldsymbol{v}_{\text{s,sv1}}(k)\}
\end{aligned}
$$

Overall, the cost term reduces the maximum appearing phase-to-phase voltage steps to half of the amplitude that regularly occurs in case of a two-level inverter (e.g. for the transition $\boldsymbol{v}_{\text{s,sv1}}(k-1) \rightarrow \boldsymbol{v}_{\text{s,sv2}}(k)$). Note that the restrictions are however not interfering with the crucial aspect of bounding the cross-currents, as there are always switch combinations available that prevent a further magnetization of any of the chokes, namely $\boldsymbol{v}_{\text{s,sv0}}$,..,$\boldsymbol{v}_{\text{s,sv6}}$.

Performance analysis

The impact of the introduced cost term $J_{\text{sw,dv/dt}}$ is visualized in Figure 4.22. The costs terms of the previous sections are maintained ($J_{\text{sat}}, J_{\text{sw}}, J_{\text{sw,ovv}}$) and the weighting is set to $\lambda_{\text{sw,dv/dt}} = \lambda_{\text{sat,1}}/10$. The figure shows that – analogously to constraining concurrent turn-offs – a prevention of large voltage steps does not have a significant impact on the TDD minimization potential over the average switching frequency. Hence, the MPC tends to use neighboring voltage space vectors independently of the cost term $J_{\text{sw,dv/dt}}$. This behavior in fact is expected, since a sequence of neighboring vectors usually implies lowest possible TDD.

Supplementary simulation results are provided in Appendix C.4.

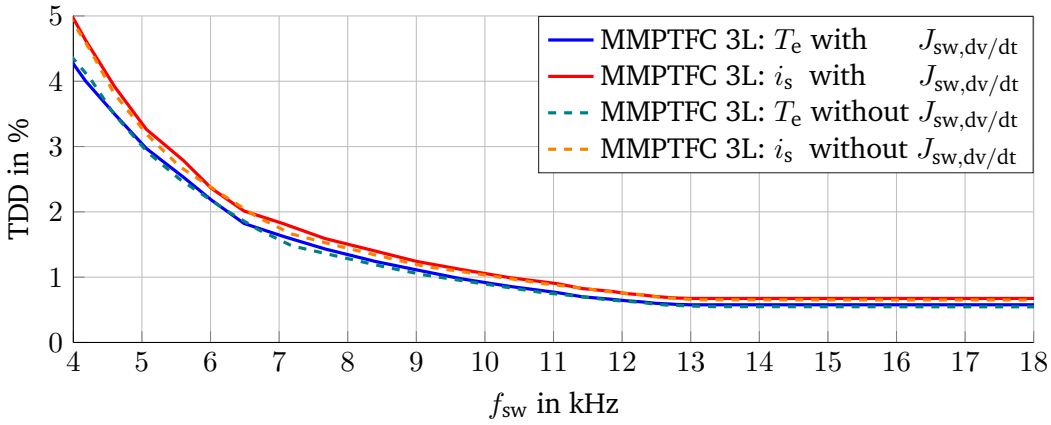


Figure 4.22.: Performance of respective torque and stator current TDD minimization vs. average switching frequency for restraining transient phase-to-phase $^{dv}/_{dt}$ at rated machine operation.

4.3.5. Minimization of Common-Mode Voltage

In order to ensure a high lifetime expectancy of the motor bearings, it is advised to keep parasitic electric discharges and the resulting common-mode current through this component at bay (cp. Section 3.2.4). Next to physical filters placed between the machine and inverter, this can be achieved by decreasing the common-mode voltage at the motor terminals. The common-mode voltage levels at the machine terminal are dependent on the inverter's output voltage / switch positions and can be calculated by the following equation:

$$v_{s,cm} = \frac{1}{3} \cdot \left(\sum_{m \in \{a,b,c\}} v_{s,m} \right) \approx \frac{1}{6} \cdot \left(\sum_{l=\{1,2\}} \sum_{m \in \{a,b,c\}} v_{l,m} \right) \tag{4.29}$$

$$\rightarrow \text{for two-level inverter:} \quad v_{cm} \in \{-V_{dc}/2, -V_{dc}/6, +V_{dc}/6, +V_{dc}/2\}$$

$$\rightarrow \text{for interleaved inverter:} \quad v_{cm} \in \{-V_{dc}/2, -V_{dc}/3, -V_{dc}/6, 0, +V_{dc}/6, +V_{dc}/3, +V_{dc}/2\}$$

The greater availability of lowered absolute values for $v_{s,cm}$ in case of the interleaved inverter system generally is a positive feature. Nevertheless, the switching states where $v_{cm} = 0$ holds are of particular interest ("common-mode free"). The respective common-mode free voltage space vectors can quickly be identified in Table A.2. Fortunately, all of the medium length voltage space vectors $\boldsymbol{v}_{s,sv7},\ldots,\boldsymbol{v}_{s,sv12}$ as well as most of the zero-voltage space vectors fulfill this attribute. Hence, it is possible to implement a fully functional machine control based solely on common-mode free space vectors, which is also established in [76] for PWM-based methods. The following cost term can be utilized:

$$J_{cm}(k) = \begin{cases} \lambda_{cm} & \text{if } |J'_{cm}(k)| > 0 \\ 0 & \text{else} \end{cases}$$

$$J'_{cm}(k) = {}^1/_6 \cdot \left(\sum_{l=\{1,2\}} \sum_{m \in \{a,b,c\}} u_{l,m}(k) \right) \tag{4.30}$$

If λ_{cm} is chosen to be very large, it can be assumed that indeed only common-mode free space vectors will be used for machine control. On the other side, a weighting factor λ_{cm} in the range of λ_{sw} will rather establish a switching pattern with a merely lowered average value of the common-mode voltage.

Performance analysis
It can directly be anticipated that the activation of J_{cm} significantly reduces the capability of minimizing TDD over the average switching frequency. The restriction to medium voltage space vectors practically increases the FCS-MPC's granularity back to the one of a regular two-level inverter. This expectation is supported by the simulation results depicted in Figure 4.23. For the respectively given simulations, the costs terms of the previous sections are mostly maintained ($J_{\mathrm{sat}}, J_{\mathrm{sw}}, J_{\mathrm{sw,ovv3}}$) and the weighting is set to $\lambda_{\mathrm{cm}} = \lambda_{\mathrm{sat},1}/10$. Note that the cost term $J_{\mathrm{sw,dv/dt}}$ has to be inactive for an activated J_{cm}, since larger voltage steps are mandatory to allow switching between the medium space vectors and the zero-voltage space vector.

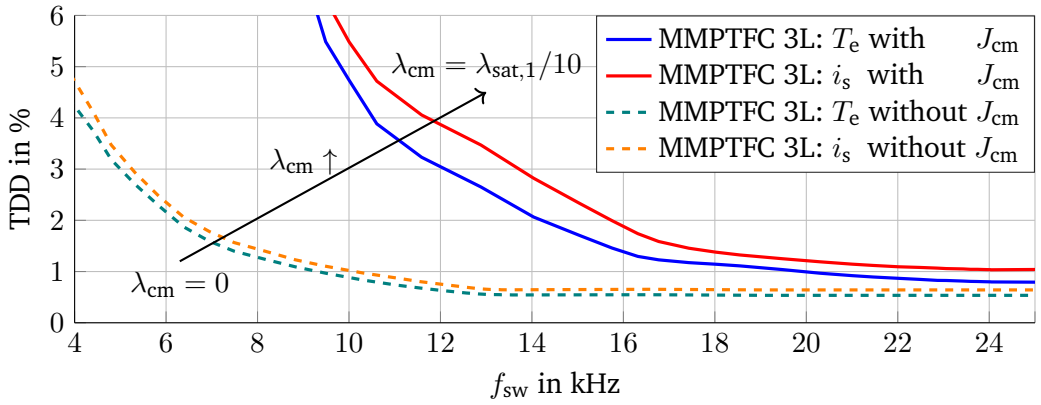


Figure 4.23.: Performance of respective torque and stator current TDD minimization vs. average switching frequency for zero-voltage common-mode space vectors at rated machine operation.

Figure 4.23 further reveals that the activation of J_{cm} approximately leads to a doubling of the average switching frequency due to the increased granularity. Very low switching frequencies cannot be achieved, since the common-mode free voltage space vectors always impose a magnetization of the interleaving chokes and therefore necessitate a respectively controlled balancing. The minimized TDDs at $25\,\mathrm{kHz}$, which are the achievable minima for this operation mode, still are approximately 1.5-fold higher than without the restriction to common-mode free space vectors. It is noteworthy that the DC-link capacitor current $i_{\mathrm{dc,cap,rms}}$ is not deteriorated, if the machine TDDs with and without activated J_{cm} are approximately equivalent.

Lastly, it has to be considered that the utilized space vectors are indeed common-mode free, but the inverter's output transients *during* switching activity are usually not. This aspect does not only include delay, fall and rise times of the transistors themselves, but also output voltage distortions due to the implemented dead-time (cp. Figure 3.4). This means that the issue of damaging the machine bearings due to electric-discharge-machining currents cannot be ruled out entirely, and may require further attention.

Supplementary simulation results are provided in Appendix C.5.

4.3.6. Minimization of Inverter Losses

In the previously presented performance analyses, the average switching frequency of the inverter was used as measure for the reduction of the inverter losses P_{inv}. This generally is a good approximation, since the switching losses are the primary loss group of the semiconductors that can be directly influenced by the control algorithm.

On the other hand, the reduction of conduction losses $P_{\text{inv,cond}}$ implies a necessary decrease of conducted currents. This however conflicts with the requested current for machine control ($\rightarrow$ manipulation of the stator current $\boldsymbol{i}_{\text{s}}$) or the usage of interleaved states ($\rightarrow$ current distribution between the paralleled inverters). Regarding the first aspect, a better solution for minimizing $P_{\text{inv,cond}}$ was already provided with the method of optimal machine magnetization (cp. Section 3.2.4). Regarding the latter, the minimization of $P_{\text{inv,cond}}$ is in fact trivial, as the conduction losses are lowest for an equal current loading among the respective paralleled half bridges. This however is a direct incompatibility with the aspiration of utilizing interleaved states for improved machine control etc., and therefore it will not be regarded as a direct optimization goal.

In conclusion, the minimization of inverter losses is approached by the minimization of the inverter's switching losses $P_{\text{inv,sw}}$.

Minimization of switching losses
As discussed, the average switching frequency can be used as measure for the reduction of inverter switching losses $P_{\text{inv,sw}}$. Nevertheless, the true switching losses are in fact dependent not only on the amount of switching activity, but also on the implemented driver circuitry[25] as well as on the voltage and drain-source currents at which the respective switching is occurring [77]. While it is an admissible assumption that the voltage to be switched is approximately equal to V_{dc}, the current-weighted switching activities are indeed a measure that can be considered in the control algorithm.

According to the datasheet of the SiC MOSFETs that are used for this thesis [24], the turn-on and turn-off losses approximately have a linear dependency on the drain-source current[26]. This attribute can be used to construct an enhanced cost function, which includes the current weighting for the switching activity.

$$J_{\text{sw,loss}}(k) \;= \frac{\lambda_{\text{sw,loss}}}{\hat{i}_{1,\text{ph,n}}} \cdot \left(\sum_{l=\{1,2\}} \sum_{m\in\{\text{a,b,c}\}} |u_{l,m}(k) - u_{l,m}(k-1)| \cdot |i_{l,m}(k)| \right) \tag{4.31}$$

Performance analysis of switching loss minimization
In order to evaluate the anticipated benefits of replacing the original cost term for switching activity J_{sw} with $J_{\text{sw,loss}}$, an inverter loss model has to be included in the simulation. It is set up identically to Eqn. (4.32). Note that the turn-on and turn-off losses of the power switches generally differ. Nevertheless, the separated view on the switching losses for the top and bottom MOSFET of each respective half bridges is not necessary for the overall switching loss minimization via $J_{\text{sw,loss}}$, since turn-on and turn-off activity have to appear in an equal amount over time.

$$E_{\text{inv,sw}}(k) = \sum_{l=\{1,2\}} \sum_{m\in\{\text{a,b,c}\}} E'_{\text{inv,sw},l,m}(k)$$

$$E'_{\text{inv,sw},l,m}(k) = \frac{1}{\hat{i}_{1,\text{ph,n}}} \cdot \left(E'_{\text{inv,sw,top},l,m}(k) + E'_{\text{inv,sw,top},l,m}(k) \right) \cdot |i_{l,m}|$$

[25] For instance the gate resistance, amplitude of gate-source voltage, maximum gate current etc.
[26] The special case for very low drain-source currents (discussed in Section 3.1.1), where the commutation is not completed during the dead-time interval, are not considered.

$$E'_{\text{inv,sw,top},l,m}(k) = \begin{cases} E'_{\text{inv,sw,on}} & \text{if } u_{l,m}(k) - u_{l,m}(k-1) > 0 \\ E'_{\text{inv,sw,off}} & \text{if } u_{l,m}(k) - u_{l,m}(k-1) < 0 \\ 0 & \text{else} \end{cases}$$

$$E'_{\text{inv,sw,bot},l,m}(k) = \begin{cases} E'_{\text{inv,sw,on}} & \text{if } u_{l,m}(k) - u_{l,m}(k-1) < 0 \\ E'_{\text{inv,sw,off}} & \text{if } u_{l,m}(k) - u_{l,m}(k-1) > 0 \\ 0 & \text{else} \end{cases} \tag{4.32}$$

The parameters $E'_{\text{inv,sw,on}}$, $E'_{\text{inv,sw,off}}$ are linearized slopes that represent the switching losses per drain-source current and can be derived from the curves given in the MOSFET's datasheet.

Figure 4.24 illustrates the performance of the respective cost functions in terms of torque and current TDD vs. average switching losses at rated machine operation. The switching losses are all normalized with respect to the average losses occurring for J_{sw} at an average switching frequency of $f_{\text{sw}} = 10\,\text{kHz}$. Please note that the cost term J_{cm} is not active for this analysis to prevent any strong deterioration of the results. On the other hand, the cost term linked to concurrent turn-off $J_{\text{sw,ovv3}}$, as well as for large voltage steps $J_{\text{sw,dv/dt}}$ initially remain active.

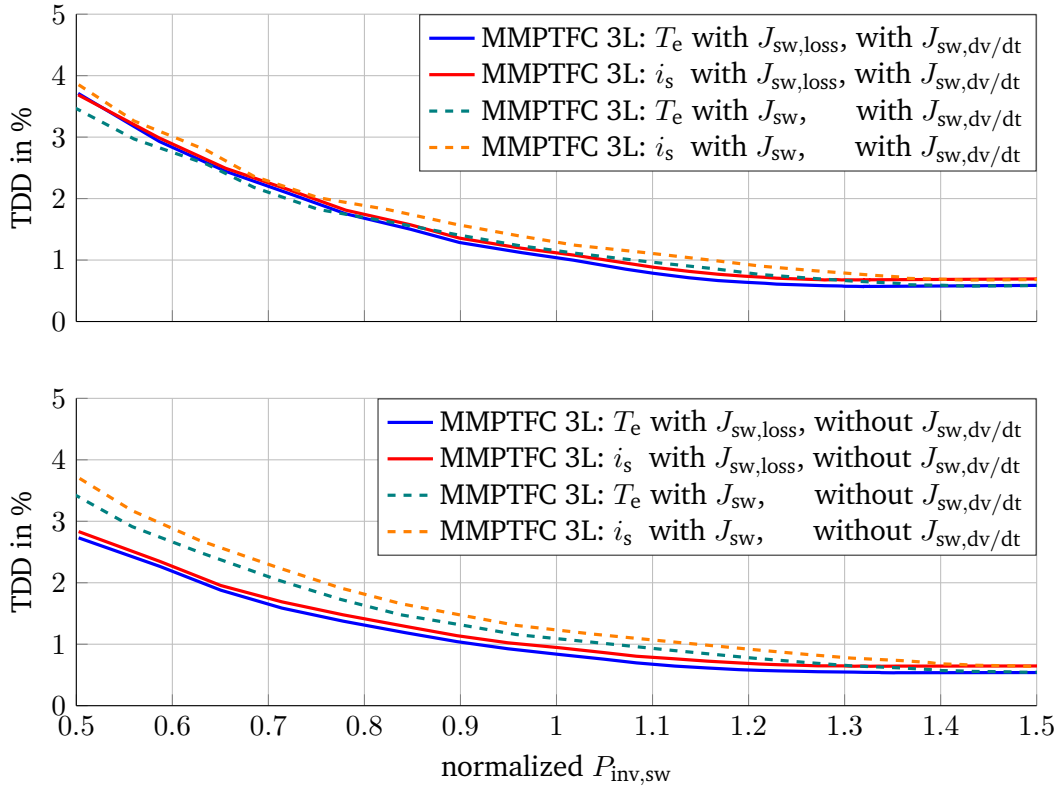


Figure 4.24.: Performance of respective torque and stator current TDD minimization vs. average switching losses for respective cost terms J_{sw}, $J_{\text{sw,loss}}$ with activated (top) and deactivated $J_{\text{sw,dv/dt}}$ (bottom) at rated machine operation.

Contrary to expectations, the enhanced, current-weighted switching loss minimization $J_{\text{sw,loss}}$ performs only better at medium switching frequencies when compared with the original method of mere switching frequency

reduction J_{sw}. Nonetheless, a more consistent performance boost for low and medium frequencies can be identified if the cost term $J_{\text{sw,dv/dt}}$ is deactivated for the respective comparison. This observation shows that switching actions beyond neighboring voltage space vectors can have a favorable constellation of current loading, particularly at low switching frequencies. The favorable current loading can reduce the switching losses, even though the performed switching actions increase. Overall, the necessity of a trade-off between the minimization of switching losses and the restraining of large voltage steps at the machine terminals is implied.

Implications on inverter conduction losses
Lastly, the impact of a decreased average switching frequency / averaged switching losses on the inverter's conduction losses $P_{\text{inv,cond}}$ shall be discussed briefly. For this purpose, the normalized average conduction losses[27] are provided in Figure 4.25 in dependency of the averaged switching losses. The cost term $J_{\text{sw,loss}}$ (without $J_{\text{sw,dv/dt}}$) is used for this analysis.

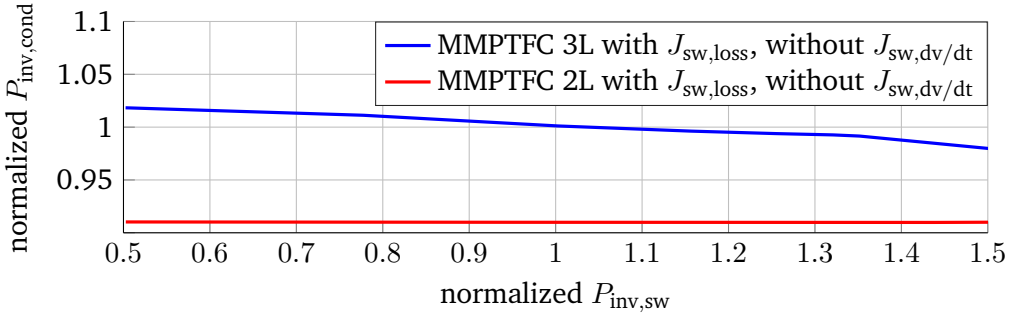


Figure 4.25.: Averaged and normalized conduction losses $P_{\text{inv,cond}}$ of the inverter vs. average switching losses for cost term $J_{\text{sw,loss}}$ at rated machine operation.

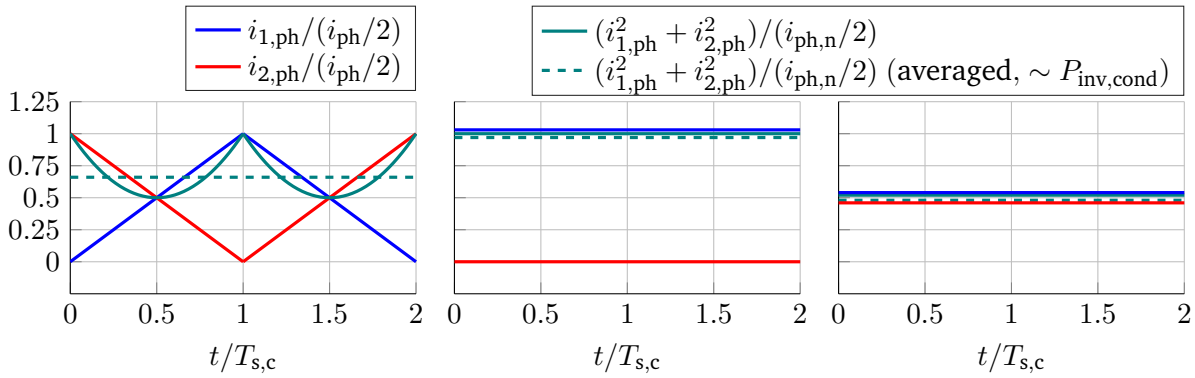


Figure 4.26.: Example of a strong magnetization and demagnetization (left), constantly magnetized (middle) and constantly unmagnetized state (right) of an arbitrary phase.

It can be seen that increased switching losses (being strongly correlated with higher values of f_{sw}) lead to a *slight* reduction of inverter conduction losses. This conjuncture is mainly linked to the more frequently appearing magnetization and demagnetization of the interleaving chokes: Assuming a symmetrical magnetization around the unmagnetized state of a respective interleaving choke and under consideration of time-averaged

[27]The relative conduction losses are calculated by the summation of rms-values for the drain-source currents. The normalization of $P_{\text{inv,cond}}$ then is performed analogously to the normalization of $P_{\text{inv,sw}}$ for Figure 4.24.

values, the magnetizing process results in a more evenly distributed current sharing of the participating half bridges than a constantly magnetized state. Nevertheless, the lowest conduction losses will usually[28] be achieved for the completely balanced case (cp. Figure 4.26).

4.3.7. Shift and Symmetrization of Losses Among Semiconductors

The property of symmetrical loss distribution among semiconductors is an important issue with respect to thermal management of the commissioned power switch modules. An unbalanced power loss distribution and consecutively high temperature gradients within the module represent significant stress on the devices and decrease the lifetime expectancy etc. For example, it is for this reason that neutral point clamped three-level inverters (NPC) are often implemented as active neutral point clamped inverters (ANPC) with symmetrizing PWM methods, despite the entailing additional gate driver circuitry and controller complexity.

In case of the FCS-MPC investigated in this thesis, the switching actions up to now were optimized for machine control, switching frequency, switching losses, concurrent turn-offs and $^{\mathrm{d}v}/_{\mathrm{d}t}$-effects. However, none of these aims inherently impose a symmetrical distribution of switching activity[29] (and even more so losses). Although the idealized switching and conduction losses of the semiconductors *tend* to average out over a electrical revolution in the $\alpha\beta$-plane, the possibility of symmetrizing losses should nevertheless be added as a further control aim by means of a cost function term. As motivation for this measure, consider for instance a parameter mismatch of the on-resistance of respective paralleled halfbridges. By fulfilling the chokes' saturation constraints, it can be assumed that (over time) the control algorithm indirectly enforces a balanced current sharing. Hence, the losses of the paralleled branch with higher values of R_{on} encounters proportionally higher conduction losses and therefore increases in temperature. The positive temperature coefficient of the MOSFET's R_{on} [24] reinforces this effect even further.

Methods for shifting losses among halfbridges
Both major loss groups of the inverter, $P_{\mathrm{inv,sw}}$ and $P_{\mathrm{inv,cond}}$, are generally suitable for actively shifting the losses among the six half bridges of the interleaved inverter. The following enumeration shall give an overview of the available methods with their respective implications:

- Method 1: Prevention of interleaving in respective phase. This measure specifically reduces the switching losses (less activity necessary for balancing the magnetization current of the choke) and conduction losses (cp. Figure 4.26) for both of the respective paralleled half bridges. The method can be achieved by manipulating a phase-specific $i_{\mathrm{sat,c}}$ of Eqn. (4.21) towards zero. The other phases remain mainly unaffected. Thus, this method can be used for shifting losses among the three phases, but however not among the six halfbridges. Another disadvantage of this measure is the static, unsymmetrical truncation of the FCS, which may lead to asymmetries in machine control.

- Method 2: Offset in respective interleaving choke magnetization. This strategy aims at higher conduction losses in one of the paralleled half bridges by increasing the current share of it. This can be acquired by including the desired offset i_{shift} in the cost term J_{sat}. This method has little impact on the distribution of switching activity and can therefore be used to selectively shift losses among the halfbridges. Nevertheless, under the consideration of fast changing cross-currents during interleaved states, the offset can only be achieved in a very granular manner, which weakens the suitability of this method for accurate loss shifting.

[28] Under the assumption of matched resistances.
[29] This attribute is not solely linked to FCS-MPC implementations, but is also present for other control algorithms managing larger sets of possible switching states of multilevel topologies, e.g. with sorting algorithms [17].

- Method 3: Reducing switching actions of respective halfbridges. This measure imposes a higher penalization of switching activity on one or multiple halfbridges. It can be implemented by modifying the cost function for inverter switching loss minimization (Section 4.3.6, Eq. (4.31)), as provided below.

$$J_{\text{sw,shift}}(k) = \frac{\lambda_{\text{sw,loss}}}{i_{\text{ph,n}}/2} \cdot \left(\sum_{l=\{1,2\}} \sum_{m\in\{\text{a,b,c}\}} \lambda_{\text{sw,shift},l,m} \cdot |u_{l,m}(k) - u_{l,m}(k-1)| \cdot |i_{l,m}(k)| \right) \tag{4.33}$$

  The halfbridge-specific weighting $\lambda_{\text{sw,shift},l,m}$ can accordingly be set to equal or larger values than unity.

  If both paralleled halfbridges of a respective phase are tuned to an increased penalization, their switching losses are shifted towards the other phases. The switching activity is reduced most at the maxima and minima of the sine waves, as higher current loadings imply higher costs. Although an unsymmetrical current loading appears at these extrema (the constellation being dependent on the last applied interleaving state, which can be seen as quasi-random), the conduction losses tend to equal out over several periods. They therefore remain approximately symmetrical. If on the other hand only one halfbridge is tuned for increased switching costs, both paralleled halfbridges still encounter decreased switching losses, but the penalized halfbridge takes over a bigger portion of conduction losses. The reason is the elevated switching cost for the penalized halfbridge, especially at high current magnitudes. This creates a probability bias for the respective interleaving state that is applied before reaching the extrema of the sine waves: The result is a larger amplitude for the penalized halfbridge's current, and a lower one for its counterpart of the same phase.

  In summary, this method can be used to shift losses between phases and also between the respective paralleled halfbridges. The time characteristics of the currents, as well as the normalized average $P_{\text{inv,cond}}$ and $P_{\text{inv,sw}}$ of the individual halfbridges are depicted in Figure 4.27 and Figure 4.28 for different compositions of $\lambda_{\text{sw,shift},l,m}$.

Methods for symmetrizing losses among halfbridges

As the simulation results of Figure 4.27 and Figure 4.28 show, a loss shift between the halfbridges is certainly possible. However, while the tendencies of the loss shifts are clear, the specific outcome is very hard to predict. For instance, both illustrated cases show an over-proportional loss shift from phase a to phase b, while losses in phase c are less. It can be shown that this result is somewhat random and can easily be conversed with slightly different operation points of the machine or with different time instants for activating $J_{\text{sw,shift}}$. Therefore, a true symmetrization of losses, or even more preferable of the temperature in the power switches, necessitates an outer control loop with appropriate feedback. The latter can be implemented via an actual temperature measurement or with a precise thermal model. With respect to the outer loop, the controller should be robust (capability of handling the above-mentioned cross-couplings) and with rather low dynamics (in order to to avoid instabilities). However, the design of such outer control loop is out of the scope of this thesis and is therefore not further considered.

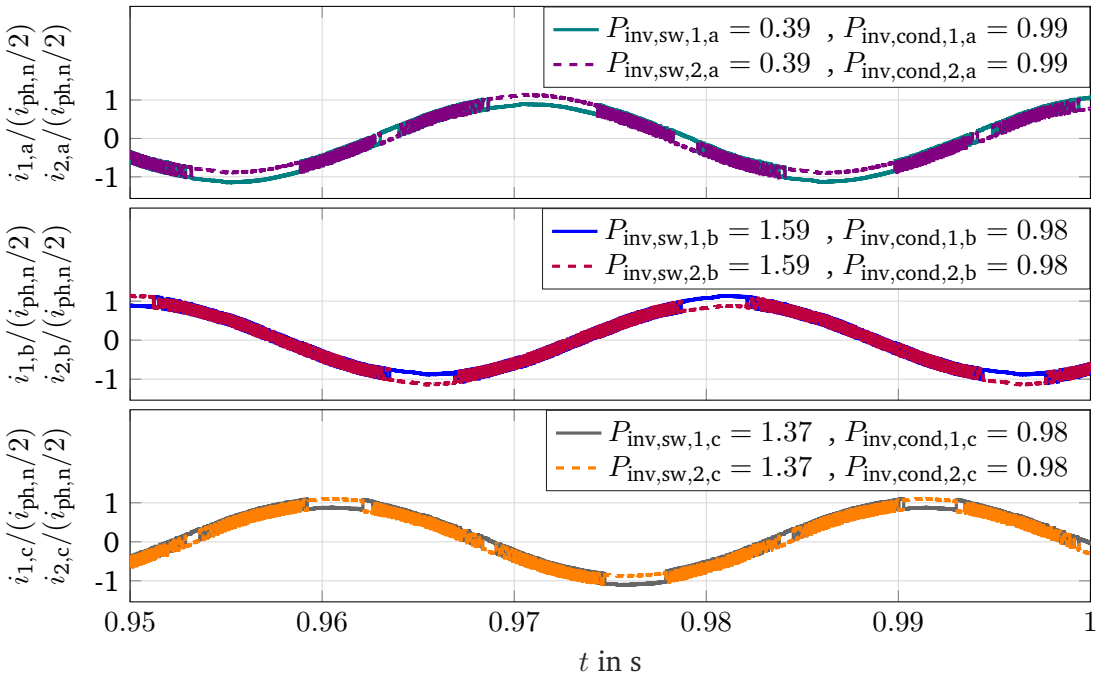


Figure 4.27.: Method 3 for shifting losses. Leg currents and normalized average $P_{\text{inv,cond}}$, $P_{\text{inv,sw}}$ for $\lambda_{\text{sw,shift,1,a}} = \lambda_{\text{sw,shift,2,a}} = 2$, others unity: The amplitudes alternate between the leg currents at each extremum, yielding the trend towards equal conduction losses over several periods.

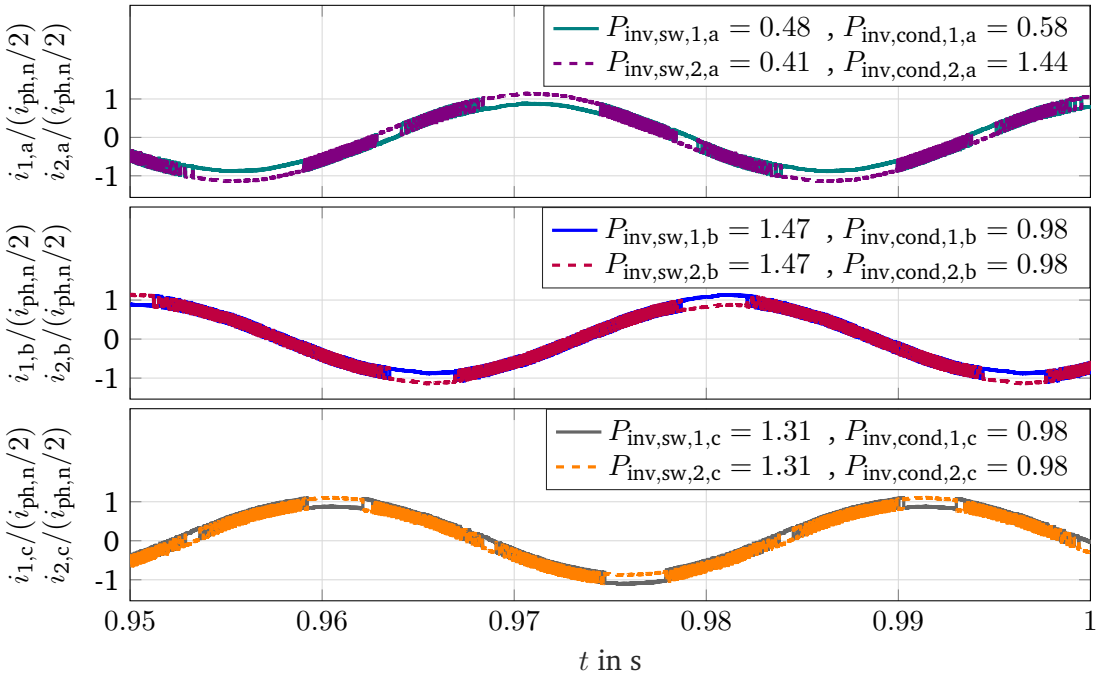


Figure 4.28.: As Figure 4.27, but for $\lambda_{\text{sw,shift,2,a}} = 2$, others unity: The constantly larger amplitude for $i_{2,a}$ at each extremum results in higher conduction losses for this leg.

4.3.8. Minimization of Losses Appearing in DC-Link

It was shown in Section 3.1.3 that an appropriate switching activity can greatly reduce the rms-value of the DC-link capacitor current $i_{\text{dc,cap,rms}}$ and therefore also the anticipated losses in the DC-link capacitor bank. In order to consider such optimization goal for the model predictive controller, the DC-link capacitor current has to be included in the predictions and a respective cost function has to be constructed.

Nevertheless, the typical time characteristics of the drawn inverter current are to be analyzed in brevity first. Specifically and in contrast to Section 3.1.3, the current ripple related to the load and finite interleaving inductance is included in the following investigation.

Analysis of typical time characteristic of drawn inverter current
The drawn inverter current i_{d} can generally be calculated in the following manner:

$$i_{\text{d}}(t) = \sum_{l=\{1,2\}} \sum_{m\in\{\text{a,b,c}\}} s_{l,m}(t) \cdot i_{l,m}(t) \tag{4.34}$$

Note that $s_{l,m} \in \{0, 1\}$ differs from $u_{l,m} \in \{-1, +1\}$, but otherwise represents the switch positions of the inverter identically. In the definition above, $i_{\text{d}}(t)$ is based on the time-continuously changing currents and the switch positions. The switch positions belong to the control set of the FCS-MPC and are applied to the plant for the continuous time interval $[t_{\text{start}}, t_{\text{end}}[$ with $t_{\text{start}} = k$, $t_{\text{end}} = k + 1$, i.e. the are piece-wise constant. At $t = k$, a discontinuity appears for the switch positions and therefore also for i_{d}. This takes place for every controller time step where switching occurs. During the rest of the interval, i_{d} changes according to the evolution of the leg currents, which includes the current ripple from the machine as well as of the interleaving chokes. In other words, the switching activity modulates the continuous output currents, the product being i_{d}. An exemplary trajectory is given in Figure 4.29. Its key take-aways are:

1. Large positive or negative steps of i_{d} appear at every switching action.
2. In between the switching actions, i_{d} follows the evolution of the output currents. The significant impact comes from their evolution due to interleaved states, i.e. $s_{1,\text{ph}} \neq s_{2,\text{ph}}$. This is due to $M_{12} \ll M_{\text{sr}}$.
3. During interleaved states, the slope of i_{d} is always positive: If $s_{1,\text{ph}} = 1, s_{2,\text{ph}} = 0$ holds, $i_{1,\text{ph}}$ will increase and $i_{2,\text{ph}}$ will decrease. At the same time, $i_{1,\text{ph}}$ is part of i_{d}, whereas $i_{2,\text{ph}}$ is masked out (cp. Eq. (4.34)). Likewise, a positive slope of i_{d} occurs for $s_{1,\text{ph}} = 0, s_{2,\text{ph}} = 1$.
4. The slopes during interleaving states can differ. Depending on the specific switching state, $s_{1,\text{ph}} \neq s_{2,\text{ph}}$ can hold for only one or for several phases. The more phases are involved, the higher the slope of i_{d} is.

Since i_{d} can change strongly within a single controller time step and furthermore at the time instant of switching actions, it obviously is of interest to track both of these short-term evolutions.

Cost function for minimization of DC-link capacitor current
Keeping in mind the features of i_{d}, a cost term for minimizing the DC-link capacitor current can now be defined. Note that this cost term penalizes high values of $i_{\text{dc,cap,rms}}$, which represents the predicted rms-value of the capacitor current for the *whole* interval of the controller time step duration. This stands in contrast to the TDD minimization of the machine's stator current and electromagnetic torque, where the cost function merely involves the squared reference tracking error at specific time instants (coinciding with the future controller sampling time instants, cp. Section 4.1.5). Instead, the calculation of $i_{\text{dc,cap,rms}}$ involves a definite time integral over $i^2_{\text{dc,cap}}$, that can however be resolved with *quadratic* terms of the appropriate predictions as given in Eqn. (4.35).

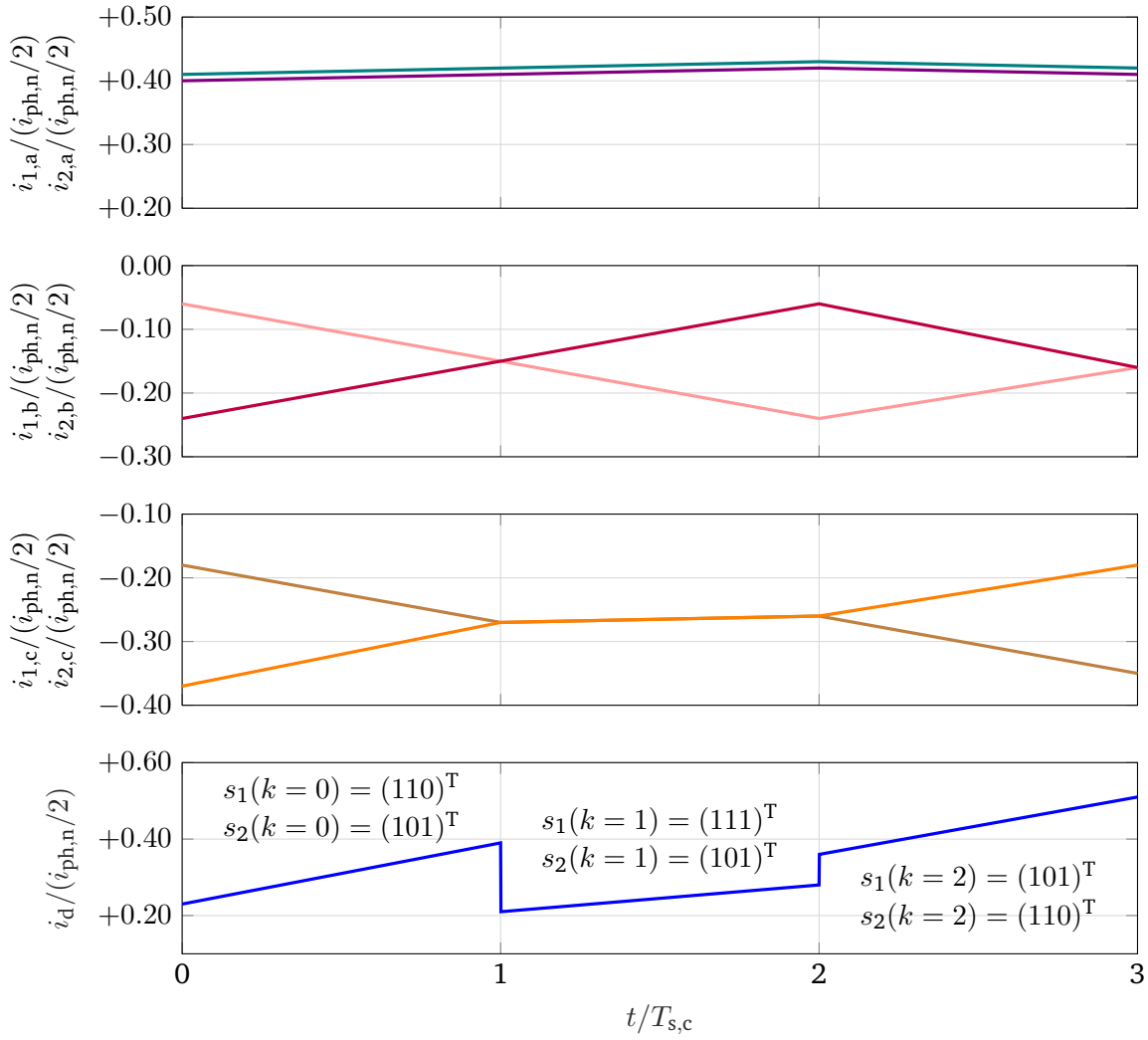


Figure 4.29.: Exemplary trajectory of drawn inverter current i_d.

$$
\begin{aligned}
J_{cap}(k) &= \lambda_{cap} \cdot i^2_{dc,cap,rms}(k) \\
i^2_{dc,cap,rms}(k) &= \frac{1}{T_{s,c}} \cdot \int_{k \cdot T_{s,c}}^{(k+1)\cdot T_{s,c}} \left(i_{dc,cap}(\tau)\right)^2 \mathrm{d}\tau = \frac{1}{T_{s,c}} \cdot \int_{k \cdot T_{s,c}}^{(k+1)\cdot T_{s,c}} \left(i_d(\tau) - i_{d,av}(\tau)\right)^2 \mathrm{d}\tau = \ldots \\
&\quad \left(i_d(k^+) - i_d(k^-)\right) \cdot \left(1/3 \cdot \left(i_d(k^+) - i_d(k^-)\right) + \left(i_d(k^-) - i_{d,av}(k)\right)\right) + \left(i_d(k^-) - i_{d,av}(k)\right)^2 \\
i_{dc,cap}(t) &= i_d(t) - i_{d,av}(t) \\
i_{d,av}(t) &\approx i_{d,av}(k) = \frac{1}{N_{av}} \cdot \left(\sum_{n=0}^{N_{av}-1} \left(i_d(k^+ - n) + i_d(k^- - n)\right)/2 \right) \\
i_d(k^+) &= \sum_{l=\{1,2\}} \sum_{m\in\{a,b,c\}} u_{l,m}(k) \cdot i_{l,m}(k+1) \\
i_d(k^-) &= \sum_{l=\{1,2\}} \sum_{m\in\{a,b,c\}} u_{l,m}(k) \cdot i_{l,m}(k)
\end{aligned}
\tag{4.35}
$$

The number of samples N_{av} for the moving average filter should be sufficiently large, e.g. chosen in a manner to cover a electrical evolution of the machine. In order to save computational resources, also other low-pass filter implementations are possible.

A justification for the relatively complex cost term of the DC-link current is provided in Figure 4.30. It includes three exemplary trajectories for the drawn inverter current i_{d} around its long-term (several $T_{\mathrm{s,c}}$) average $i_{\mathrm{d,av}}$. While all of the mentioned trajectories terminate at the same value for the end of the predicted time interval, it can easily be identified that the appearing magnitudes and rms-values of the respective DC-link capacitor current can strongly differ. Hence, a mere investigation or minimization of $i_{\mathrm{dc,cap}}$ at the discrete controller time steps does not (usually) coincide with the minimization of its rms-value. Conversely, in order to achieve a true minimization of the DC-link capacitor current, the overall trajectory within the predicted time interval should be considered, as it is performed in Eqn. (4.35).

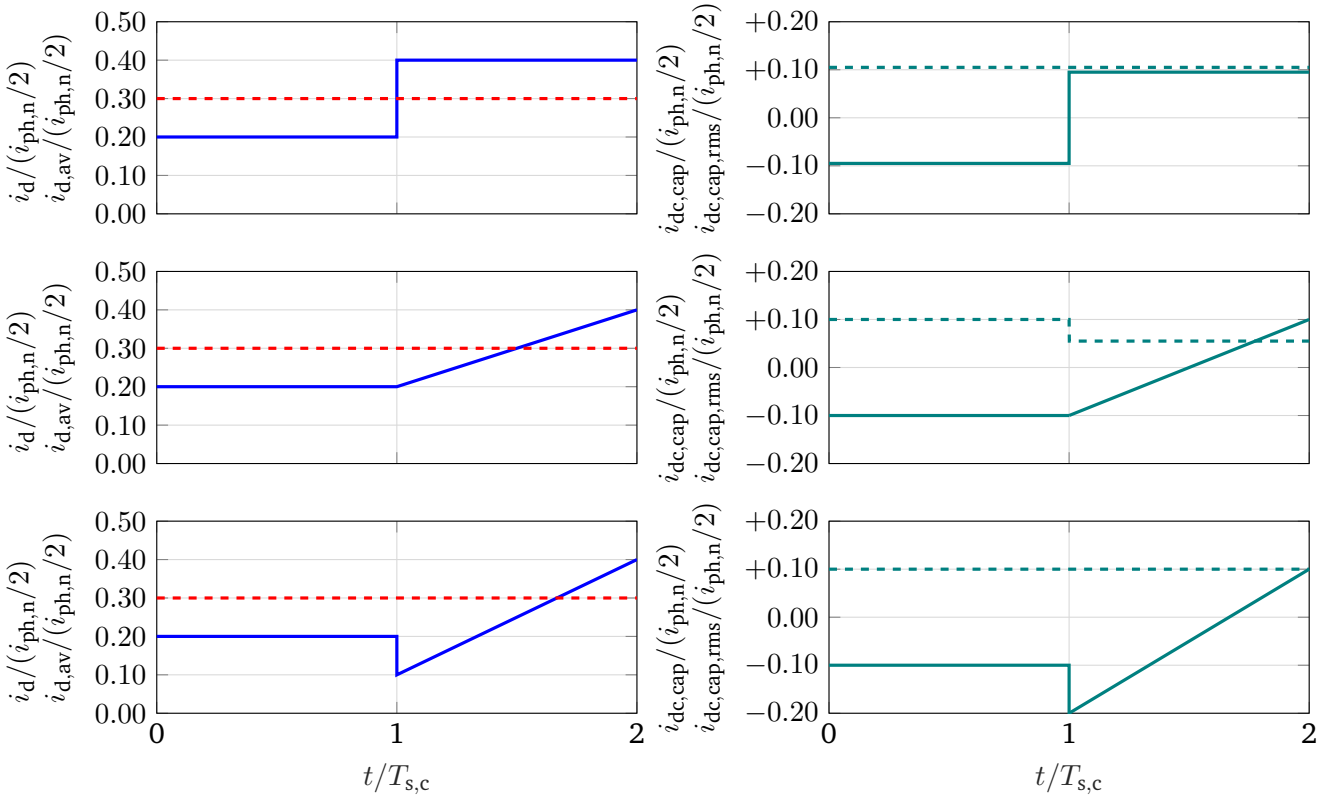


Figure 4.30.: Exemplary trajectories of drawn inverter currents i_{d} and the long-term average $i_{\mathrm{d,av}}$ (left), as well as the corresponding DC-link capacitor current and its average rms-value for the respective controller time step (right).

Performance analysis

As initial performance analysis, a sweep of λ_{cap} is performed for the rated operation point of the induction machine. The previously introduced cost terms $J_{\mathrm{magmode}}, J_{\mathrm{sw,ovv}}, J_{\mathrm{sw,dv/dt}}$ remain active, whereas the cost terms $J_{\mathrm{cm}}, J_{\mathrm{sw}}, J_{\mathrm{sw,loss}}$ are deactivated. The results are provided in Figure 4.31. As visualized in the figure, the DC-link capacitor current can strongly be reduced by increasing λ_{cap} accordingly. Interestingly, $i_{\mathrm{dc,cap,rms}}$ can be decreased by approximately 33 % ($i_{\mathrm{dc,cap,rms}}/i_{\mathrm{ph,rms}} = 0.25 \rightarrow 0.17$) before the TDDs of torque and current are subject to any significant worsening. It is advised to implement this corresponding λ_{cap}-tuning

for the rated machine operation (here: $\lambda_{\text{cap,opt}} = 4 \cdot 10^{-3}$), as it obviously implies a very beneficial operation mode for the overall drive system. Unfortunately, no algebraic tuning guideline can be provided for λ_{cap} in this thesis. Hence, the $\lambda_{\text{cap,opt}}$ has to be determined by simulation for any other operational points of the machine that come into question.

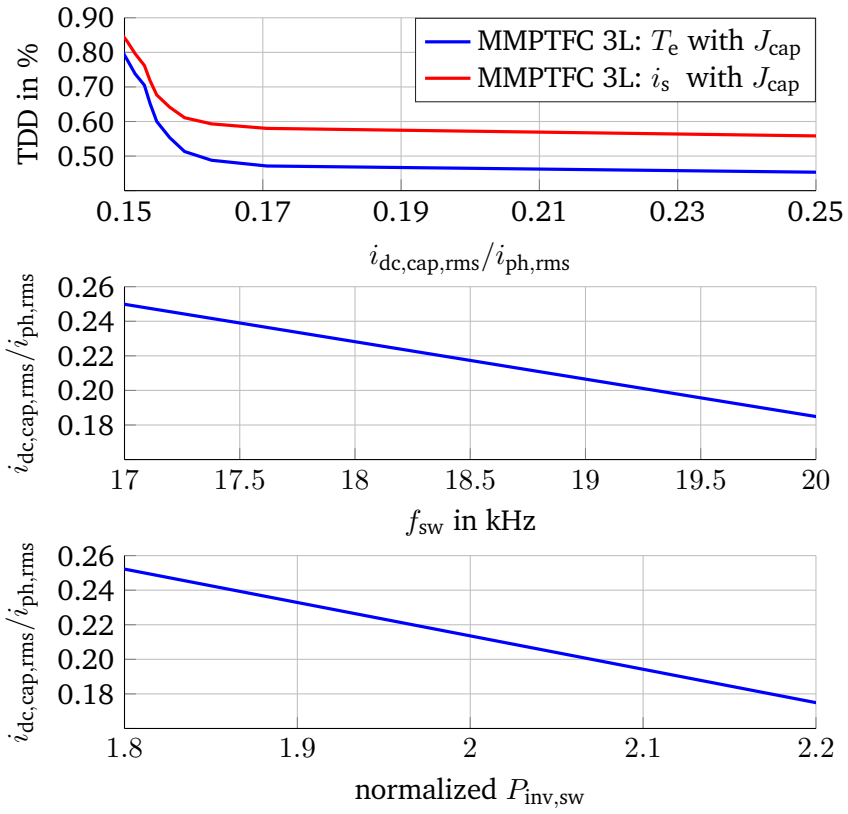


Figure 4.31.: Performance of torque and stator current TDD minimization vs. rms-value of capacitor current (top), rms-value of capacitor current vs. average switching frequency (middle) and rms-value of capacitor current vs. average switching losses (bottom) at rated machine operation.

A second insight provided by Figure 4.31 is that an activated cost term J_{cap} considerably increases the average switching frequency when achieving low values of $i_{\text{dc,cap,rms}}$ (cp. highest switching frequency in Figure 4.22). Similarly, but to an even stronger extent, the average inverter switching losses increase beyond the level that was reached with deactivated $J_{\text{sw,loss}}$ and J_{sw} (cp. highest losses in Figure 4.24), which corresponds to the inverter losses for minimal machine control TDD. Overall, this implies the necessity of a trade-off between anticipated inverter losses, losses in the DC-link and machine control TDD.

The trade-off between inverter losses[30], DC-link optimization and torque TDD is depicted as color plot in Figure 4.32. It is based on an exhaustive parameter sweep of λ_{cap} and $\lambda_{\text{sw,loss}}$. The figure also provides the performance for the sweep of $\lambda_{\text{sw,loss}}$ and $\lambda_{\text{cap}} = 0$, showing that although there is a strong negative correlation between inverter losses and minimization of $i_{\text{dc,cap,rms}}$, a true optimization of the DC-link requires the activated cost term J_{cap}. In other words, a high average switching frequency is a necessary but not sufficient condition for the DC-link optimization.

[30]The switching losses are normalized with respect to the average losses occurring for J_{sw} at an average switching frequency of $f_{\text{sw}} = 10\,\text{kHz}$ at rated machine operation.

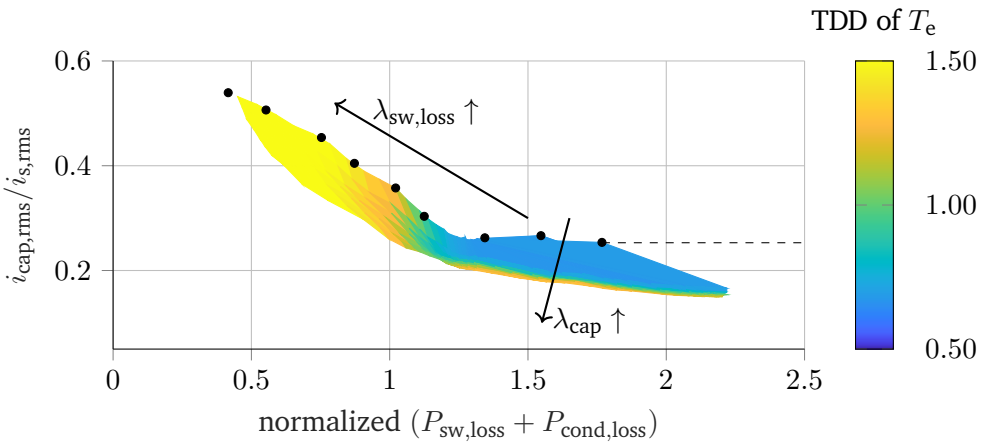


Figure 4.32.: Performance of torque TDD minimization vs. rms-value of capacitor current and average inverter losses for sweeping $\lambda_{sw,loss}$ and λ_{cap} (colored area) and for sweeping $\lambda_{sw,loss}$ with $\lambda_{cap} = 0$ (black markers) at rated machine operation.

Supplementary results in the style of Figure 4.32 are provided in Appendix C.6.

Lastly, the MPC's DC-link optimization potential over a larger operation region of the interleaved inverter[31] is depicted in Figure 4.33. The figure includes a comparison with the performance of a non-interleaved inverter and the achievable performance in case of a time-continuous PWM-based DC-link optimization that disregards any output current ripples (the origin of the two latter are described in more detail in Section 3.1.3). As it can be seen, the MPC's DC-link optimization strongly reduces the rms-value of the capacitor current when compared to the non-interleaved version, but mostly to a lower extent than the PWM-based optimization. There are three main reasons that come into question for its weaker performance:

1. While the FCS-MPC can only switch at the controller sampling intervals and therefore implements a rather coarse minimization, the PWM-based method provides the possibility to optimize switching activity within the quasi time-continuous domain. An improved, MPC-based solution is the principle of variable switching point model predictive control [78], which however requires a considerable increase in computational resources and therefore is not further discussed in this thesis.

2. The PWM-based method optimizes over a whole switching cycle, which allows every halfbridge to switch twice (e.g. off $\rightarrow$ on $\rightarrow$ off). In terms of a FCS-MPC, this obviously corresponds to a multi-step prediction, which is anticipated to be superior over a FCS-MPC with a prediction horizon of $N_p = 1$.

3. The provided results for the PWM-based method neglect any ripple linked to the load or the interleaving chokes. Hence, the shown performance is only an approximation of the true optimization capability. It is illustrated in [31] that the presence of a ripple often tends to worsen the minimization of the DC-link capacitor current.

While the first and second reason are directly linked to principle of (a one-step) FCS-MPC, the output current ripple mentioned in the third point is strongly related to the hardware design. Specifically, the magnitude of the ripple is predominantly dependent on the interleaving choke inductance M_{12}.

[31] The displayed operation region reflects the machine operation for no-load and nominal load conditions in motor and generator mode, as well as for machine speeds between stand-still and nominal speed for $V_{dc} = 800\,\mathrm{V}$.

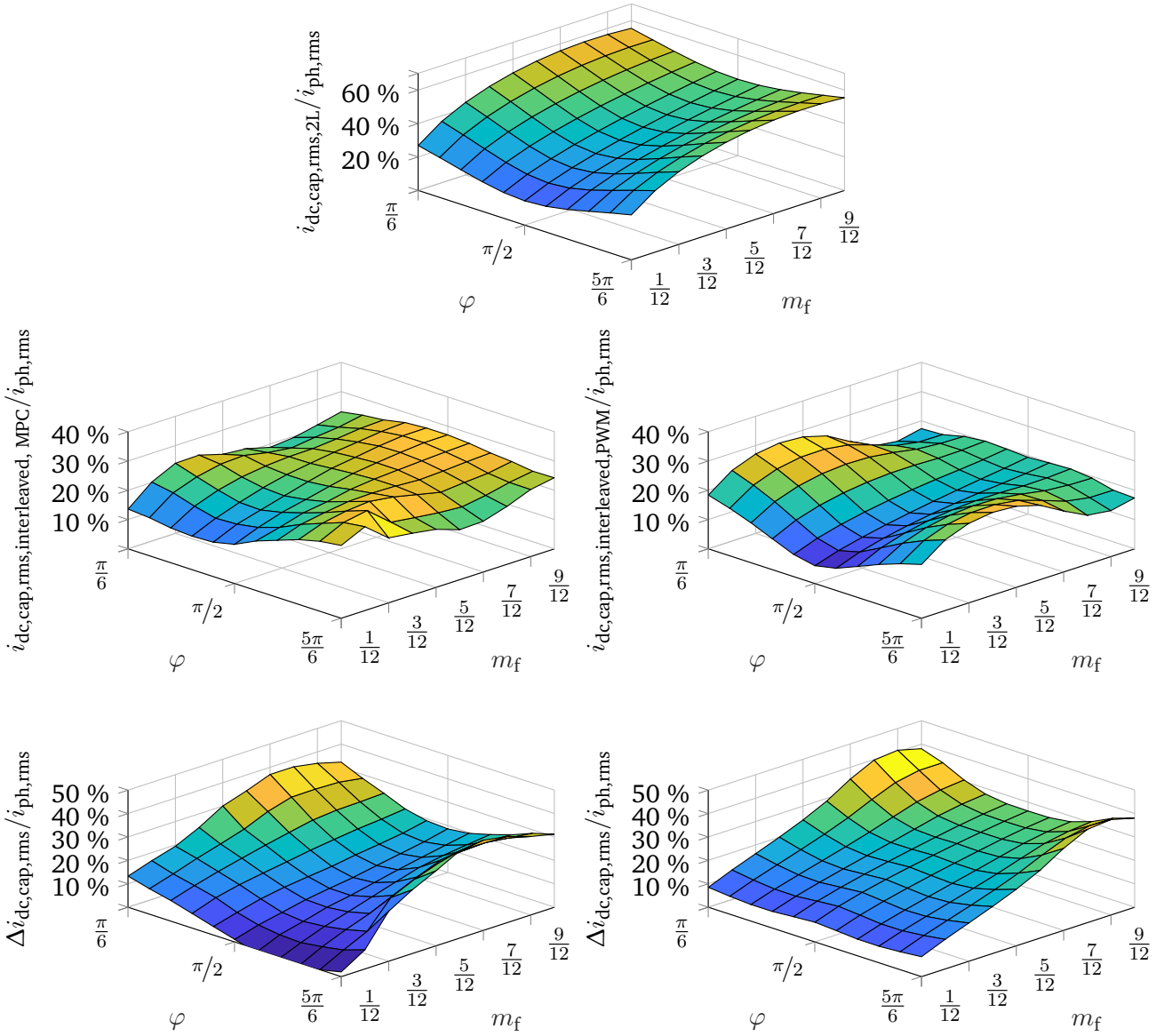


Figure 4.33.: DC-link capacitor current in dependency of the modulation factor m_{f} and phase angle φ (power factor $\rightarrow \cos(\varphi)$) for a two-level inverter (top) and interleaved inverter with optimized pulse pattern based on FCS-MPC (mid left) and based on time-continuous PWM (mid right). Absolute difference of DC-link capacitor current between two-level inverter and interleaved inverter with optimized pulse pattern based on FCS-MPC (bottom left) and based on time-continuous PWM (bottom right).

Impact of alternative values for interleaving choke inductance

As discussed, the inductance value of the interleaving chokes[32] strongly influences the output current ripple and hence also the ripple of the drawn inverter current i_{d}. The latter plays a crucial role for minimizing $i_{\mathrm{dc,cap,rms}}$. In Figure 4.34, a comparison of the time characteristics for i_{d} is shown for the nominal inductance value (M_{12}), as well as for a decreased ($0.5 \cdot M_{12}$) and a greatly increased value ($10 \cdot M_{12}$).

[32]This likewise applies for alternative DC-link voltages. For the sake of simplicity and due to the interchangeability with respect to the influence on the current ripple, V_{dc} remains to be viewed as constant.

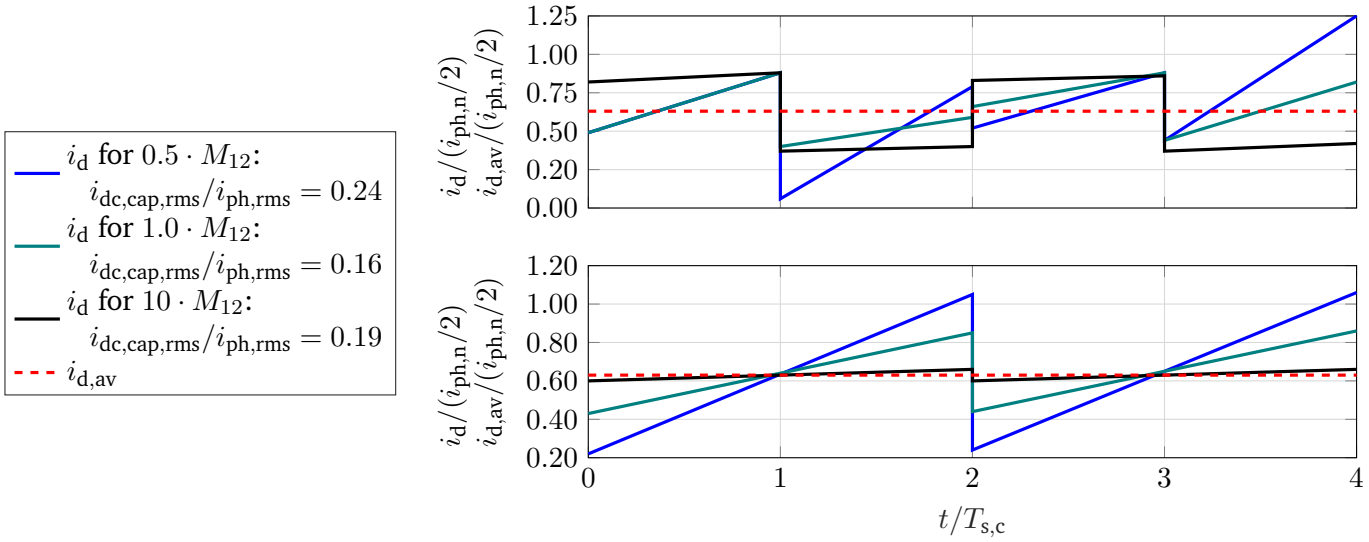


Figure 4.34.: Exemplary trajectories of drawn inverter current i_d and the long-term average $i_\mathrm{d,av}$ for various interleaving inductance values, displaying two different time frames (top vs. bottom) during rated machine operation. With respect to an entire electrical revolution, the inductance value $1.0 \cdot M_{12}$ minimizes $i_\mathrm{dc,cap,rms}$ best, as noted in the legend.

The trajectories reveal that within an electrical revolution of the machine, $i_\mathrm{dc,cap,rms}$ can sometimes be optimized better in case of a medium inductance value (upper displayed time frame) and conversely, sometimes better in case of a high inductance value (lower displayed time frame). The lower displayed time frame resembles a constellation of current loading and switch positions that leads to a drawn inverter current that matches its average almost perfectly. This situation is present often for high power factors and $m_\mathrm{f} \approx 0.5$. In this case, any stronger short-term changes of i_d lead to deviations to $i_\mathrm{d,av}$, deteriorating the performance. Hence, a large interleaving inductance is preferable. On the other hand, the upper displayed time frame illustrates a comparatively unfavorable current loading where large values of the interleaving choke inductance lead to a rectangular signal form of i_d. It includes rather large instantaneous values for $i_\mathrm{dc,cap} = i_\mathrm{d} - i_\mathrm{d,av}$. In this case, a sawtooth-like shape of i_d can significantly reduce the DC-link current. However, very high slopes of i_d, e.g. as for $0.5 \cdot M_{12}$, obliterate the advantage.

The occurrence and prevalence of the situations represented by the two time frames in Figure 4.34 depends on the operation point of the inverter. It is for this reason that the optimization potential for the DC-link varies strongly with the modulation and power factor (cp. Figure 4.33). Accordingly, a single optimal value for the interleaving inductance cannot be provided in a generalized manner. For example, in the case of low phase shifts (i.e. high power factors), lower inductance values may lead to a better performance than large inductance values, as shown in Figure 4.35. Simultaneously, the opposite is true for no-load operation, i.e. $\varphi \approx \pi/2$. Nevertheless, the overall simulation results in Figure 4.35 illustrate that the chosen value of $1.0 \cdot M_{12} \approx i_\mathrm{ph,n}/(2V_\mathrm{dc} \cdot T_\mathrm{s,c})$ within this thesis provides a fair performance in comparison to a much larger interleaving inductance, while it may entail less hardware costs.[33]

Lastly, Figure 4.34 also provides an insight with respect to a suitable saturation limit i_sat for the inter-

[33] See Section 6.3.2 for more details on the choice of the value for the interleaving inductance.

leaving chokes. While a large i_{sat} can effectively improve the performance for the trade-off between TDD vs. average switching frequency (less switching activity required for retaining the saturation limit), the benefit for the DC-link optimization is only little: As long as i_{sat} is large enough to enable a sawtooth-like shape that is of same amplitude as the rectangular shape established by very large interleaving inductances, the main minimization potential of $i_{\text{dc,cap,rms}}$ can be acquired.

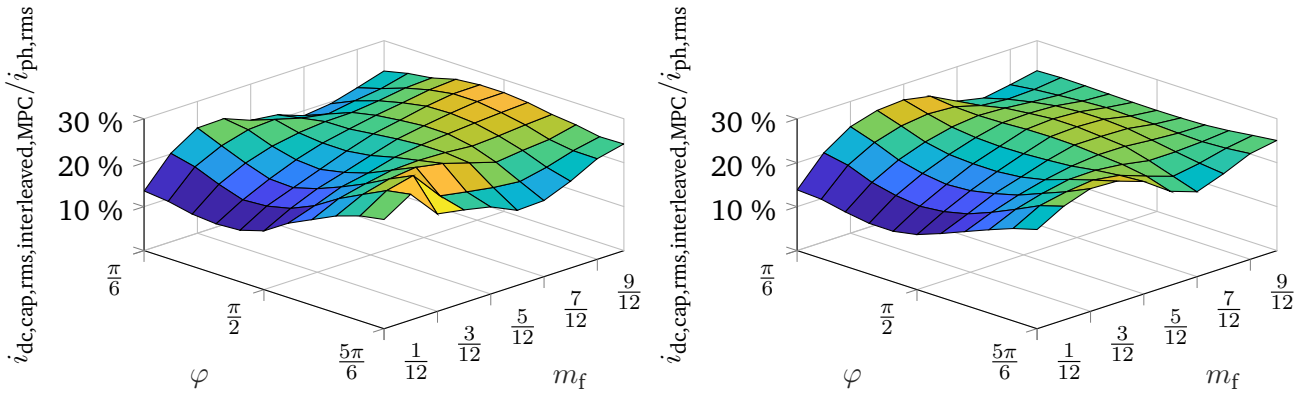


Figure 4.35.: DC-link capacitor current in dependency of the modulation factor m_{f} and phase angle φ (power factor $\rightarrow \cos(\varphi)$) for interleaved inverter with optimized pulse pattern based on FCS-MPC with $1.0 \cdot M_{12}$ (left) and $10 \cdot M_{12}$ (right).

Spectral analysis

Due to possible frequency dependencies of the equivalent series resistance in real capacitors, not only the overall reduction of $i_{\text{dc,cap}}$ is of interest, but also its spectrum. Likewise, this also applies due to the parasitic inductance of real capacitors. With respect to the latter, a spectrum of $i_{\text{dc,cap}}$ accumulated in the lower frequency regions is favorable. Together with sufficiently dimensioned values of the capacitance itself, it supports a steady DC-link voltage as inverter input.

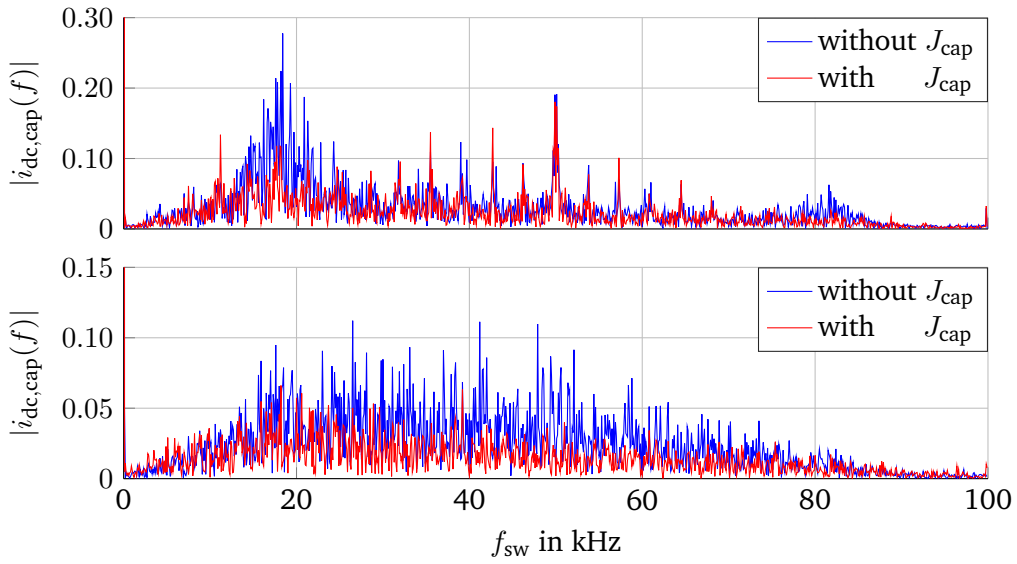


Figure 4.36.: Spectra of $i_{\text{dc,cap}}$ for an activated and deactivated J_{cap} at high (top) and low (bottom) penalization of switching activity and at nominal machine operation.

The simulation data provided in Figure 4.36 depict that the reduction of $i_{\text{dc,cap,rms}}$ appears fairly evenly distributed throughout the frequency domain as soon as J_{cap} is activated. Therefore, it can be anticipated that a reduction of the DC-link current's ripple via J_{cap} decreases the losses and DC-link voltage ripple with a proportionality of approximately $i^2_{\text{dc,cap,rms}}$ and $i_{\text{dc,cap,rms}}$, respectively. On the other hand, an increased penalization of switching activity via J_{sw} does shift the spectrum to lower frequencies, bringing upon the possibility of lowering the DC-link voltage ripple. However, eventually an investigation has to be made whether this frequency shift outweighs the overall reduction potential[34] of $i_{\text{dc,rms}}$ in terms of the DC-link voltages ripple, or vice versa.

4.3.9. Losses in Interleaving Chokes

In Section 3.1.2, the modeling of a real inductance is discussed in the context of interleaving chokes, including possibilities for implementing a respective loss model. For example, the rather generic approach via the Modified Steinmetz Equation (MSE) does provide the possibility to account for non-sinusoidal signals over one period of a completed hysteresis cycle [28] [79]. This is performed by determining an equivalent frequency of the respectively analyzed cycle:

$$f_{\text{hys,eq}} = \frac{2}{(\Delta B \pi)^2} \int_0^{T_{\text{hys}}} \left(\frac{\mathrm{d}B}{\mathrm{d}t} \right)^2 \mathrm{d}t \tag{4.36}$$

$$P_{\text{core}} = k \cdot (f_{\text{hys}} \,/\, \text{Hz}) \cdot (f_{\text{hys,eq}} \,/\, \text{Hz})^{a-1} \cdot \left({}^1\!/_2 \cdot \Delta B^b \right) \tag{4.37}$$

where $\Delta B = (B_{\text{max}} / \text{ T}) - (B_{\text{min}} / \text{ T})$
and k, a, b are the material specific values as for the regular Steinmetz Equation

Under negligence of the decaying properties for the magnetizing current $i_{1,\text{ph}} - i_{2,\text{ph}}$, the anticipated waveforms are either triangular or trapezoidal (cp. e.g. Figure 4.16). A corresponding evaluation of these waveforms with Eq. (4.36) leads to a correction factor of $f_{\text{hys,eq}} \approx 0.81 \cdot f_{\text{hys}}$. The factor ΔB is defined by the chosen magnetization mode and, under the above mentioned negligence of decaying properties, remains constant for any of the appearing hysteresis cycles.

Figure 4.37 provides the number of performed hysteresis cycles and covers the case of an activated and deactivated J_{cap}, as well as for a low and high penalization of switching activity. The given occurrences are based on on one phase and one electrical revolution of the machine. The data in the figure leads to the conclusion that performed hysteresis cycles of an arbitrary phase appear between approximately 50% to 90% over one electrical revolution and high frequencies generally are more common than low frequencies. Moreover, there is no strong correlation between the distribution of hysteresis cycles over their frequency and an explicitly activated or deactivated DC-link optimization. Nevertheless, the amount of performed hysteresis cycles tends to be larger in the case of a low penalization of switching activity.

4.3.10. Prolonged Prediction Horizons

It is a reasonable presumption that prolonged prediction horizons are generally beneficial for the performance of FCS-MPC implementations. For example, by evaluating switching actions and trajectories for several upcoming future time steps, the system's quantities that encounter time lags or that are of lower dynamics can be considered better when searching for optimality. Due to this reason, especially systems of higher

[34] requiring a low penalization of switching activity, cp. Figure 4.32.

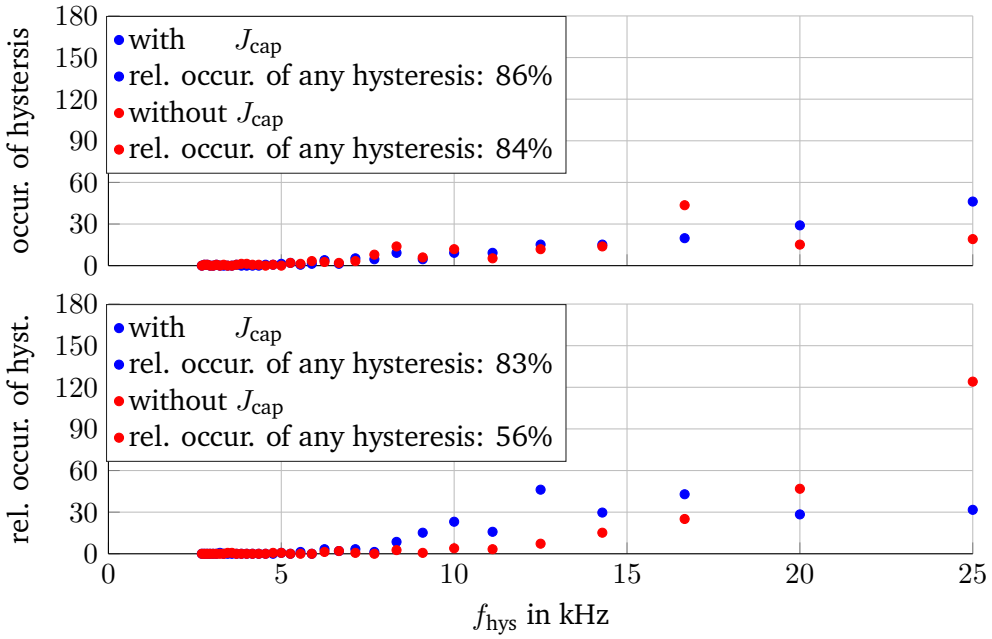


Figure 4.37.: Occurrences of hysteresis for an activated and deactivated J_{cap} at high (top) and low (bottom) penalization of switching activity and at nominal machine operation. Values are based on one phase and one electrical revolution.

order (e.g. inverter-fed induction machine with sine filter) are proven to profit from an increased number of prediction steps N_{p} in [55]. Nevertheless, also the control of directly fed induction machines can benefit from an increased N_{p}, albeit to a significantly lower extent. The performance boost can be linked to the generally less truncated evaluation of the switching sequences available for optimization.

In case of FCS-MPC implementations, an extended prediction horizon comes at the cost of exponentially increasing demand of computational resources. The reason for this is the expansion of the FCS to the set $\boldsymbol{\mathcal{U}}^{N_{\text{p}}}$, which represents all possible switching sequences (including the consideration of various permutations) for the respective amount of prediction steps. Implementational efforts can be made to decrease the overall size of the resulting FCS by curtailing it with specific rules, such as limiting the allowed voltage space vectors to a region in vicinity of the previously applied space vector. Nonetheless, this kind of particular measure generally comes along with the danger of losing the global optimum[35] [55], which eventually has the potential to even decrease the performance of the controller. Other options for limiting the growth of the FCS for increased prediction steps are branch-and-bound techniques [67], which however necessitate a sequentially structured FCS-MPC algorithm and bring upon the difficulty of a variable run time for the optimization.

In order to evaluate to which extent prolonged prediction horizons are beneficial with respect to the drive system investigated for this thesis, the performance of a two-step FCS-MPC implementation is to be compared with the results presented in the previous sections.

[35] In some cases, this kind of truncation is already made indirectly by other cost function terms, such as $J_{\text{dv,dt}}$ introduced in Section 4.3.4. If the curtailment comes from activation of such cost term, the according truncation obviously does not collide with finding the global optimum, since it comes from the specifically imposed operating conditions.

Performance analysis for two-step prediction
The performance analysis of the two-step prediction is based on the following three measures:

- DC-link optimization vs. machine control TDD
- Switching activity vs. machine control TDD
- Inverter switching losses vs. machine control TDD

These three characteristics are depicted in Figure 4.38, comparing the results with the previously introduced performance of the respective one-step implementations.

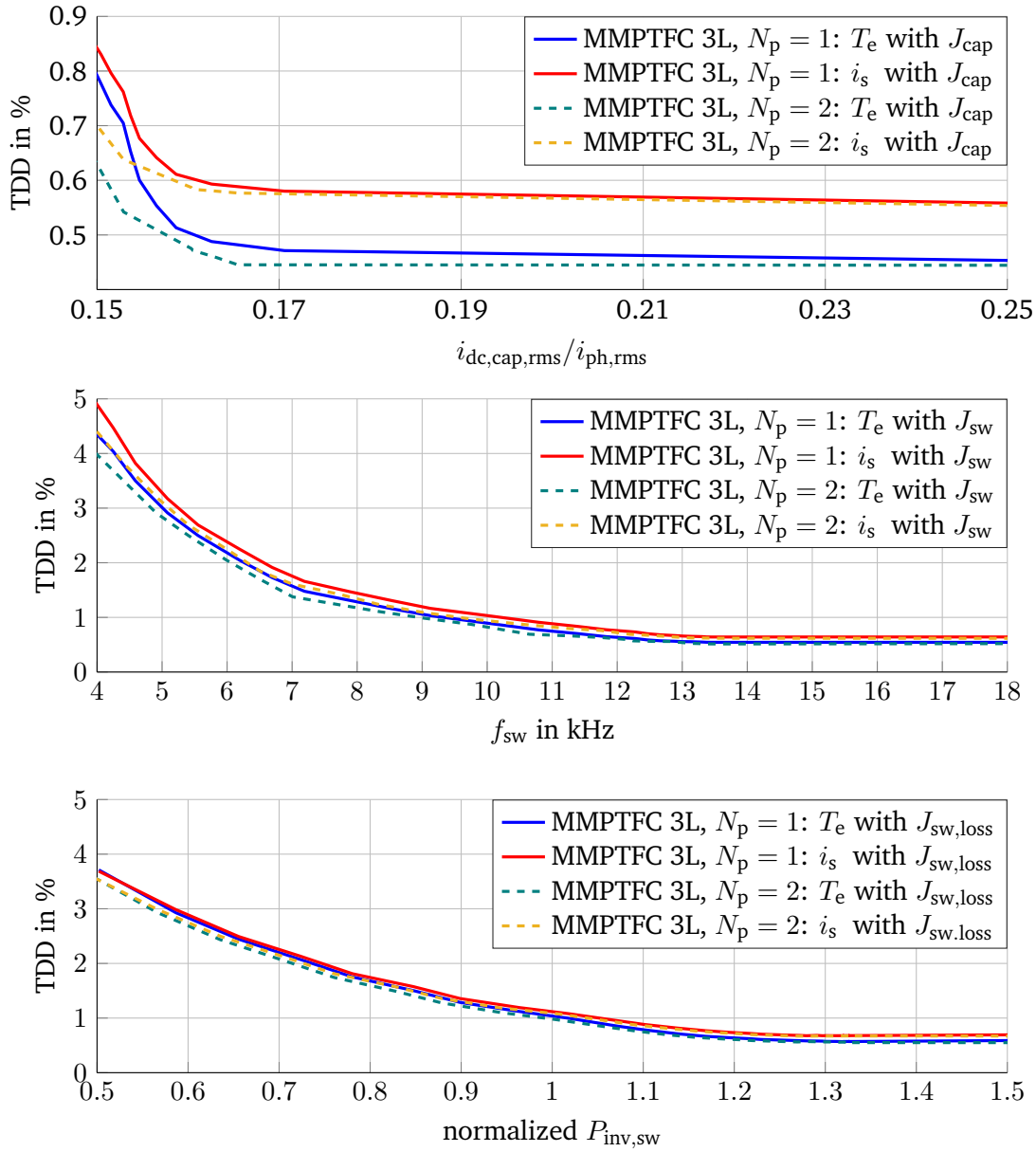


Figure 4.38.: Performance of torque and stator current TDD minimization vs. rms-value of capacitor current (top), rms-value of capacitor current vs. average switching frequency (middle) and rms-value of capacitor current vs. average switching losses (bottom) at rated machine operation.

Figure 4.38 reveals that a two-step prediction brings rather little improvement with respect to minimizing $i_{\mathrm{dc,cap,rms}}$. The Main difference is a slight shift of the transition point that implies a sudden and strong increase of machine TDD when lowering the DC-link current ripple. Similarly, only a very modest improvement can be achieved with respect to minimization of switching activity and switching losses. The improvements of TDD are predominantly concentrated in the band of low switching frequencies.

The performance benefit of prolonged prediction horizons usually is related to higher-order systems,[36] and strongest for a high relative increase of the prediction steps [55] [73], i.e. for example stronger for $N_{\mathrm{p}} = 1 \rightarrow N_{\mathrm{p}} = 2$ when compared to $N_{\mathrm{p}} = 2 \rightarrow N_{\mathrm{p}} = 3$. Although the interleaved motor drive system is of higher order than a regular two-level feeding (system matrix of rank 7 instead of rank 4, cp. Section 3.3), the insight given by Figure 4.38 hints that a one-step prediction is already sufficient to retrieve most of the interleaved inverters' optimization potential by means of FCS-MPC. A plausible explanation is the introduced cost term J_{magmode} of Section 4.3.2, which alleviates the control problem largely by already sustaining the desired choke magnetization.

4.3.11. Inverter Asymmetry and Parameter Mismatch

The performance analyses of the previous sections were based on symmetrical parameters of the parallelized inverters as well as identical parameters for the controller and the plant model. This however is a strong idealization, since manufacturing tolerances, variations of the ambient operating conditions or temperature changes due to internal power dissipation are disregarded. Therefore, a respective investigation of parameter mismatches and asymmetric parameter distributions is to be conducted.

Parameter mismatch
As discussed in Section 3.2.1, the induction machine's rotor resistance R_{r} is one of the rather critical parameters, since it is difficult to determine via measurements and is subject to comparably large temperature variations. For this reason, perturbations of R_{r} are representatively discussed for a present parameter mismatch. As an example, Figure 4.39 demonstrates the impact on torque control if the MPC and flux estimator either are based on the real rotor resistance, or on a value that is 1.5-fold higher than the real value[37].

The enlarged torque error in case of the parameter mismatch is clearly visible. It predominantly appears as a static offset, while the remaining performance of achievable TDD otherwise does not suffer. By comparing the rotor flux estimator's output with the actual plant output, it is evident that the parameter mismatch leads to a strong over-estimation of the rotor flux's magnitude, as well as to a phase error. This observation hints that the influence of the parameter mismatch mainly affects torque control due to estimation errors of the rotor flux. This presumption is supported by Figure 4.40, which gives the torque error due to a mismatched R_{r}, which however only is occurring for the prediction model, whereas the estimator's parameter $R_{\mathrm{r,est}}$ is kept identical to the plant.

The rather low sensitivity of the MPC towards the parameter mismatch is a positive feature, since it demonstrates the robustness of the controller and implies the possibility of implementing its predictions with static parameters, without having to anticipate any substantial performance losses (see also Chapter 5). On the other hand, the high sensitivity of the flux estimator can be encountered by improved and more robust estimators,

[36] Such as drive systems with implemented sine filters etc.
[37] This kind of mismatch can be interpreted as scenario in which the rotor resistance was determined by long term hardware measurements with an respectively heated up machine. If the MPC is configured with this value, it over-estimates the real rotor resistance during a cold start of the machine.

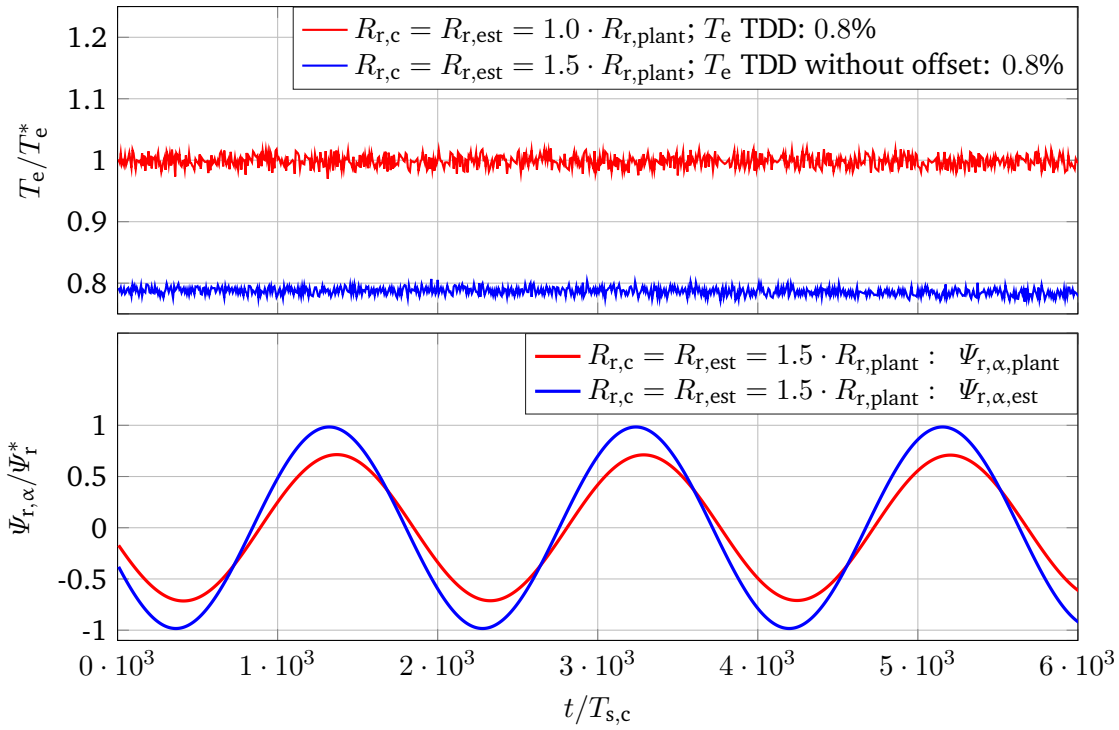


Figure 4.39.: Controlled machine torque with and without parameter mismatch (top) and estimated vs. real rotor flux in case of a present parameter mismatch (bottom) at rated machine operation.

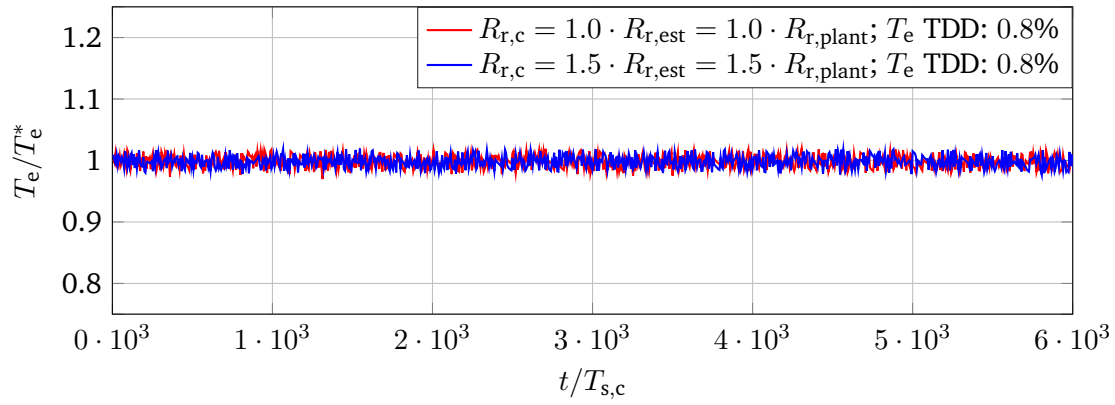


Figure 4.40.: Controlled machine torque with and without parameter mismatch at rated machine operation. The rotor flux estimator is omitted for the parameter mismatch.

such as a Kalman filter. The latter has already been combined successfully with FCS-MPC implementations for variable speed drives [80] and the investigated system of this thesis [81] [82].

Inverter asymmetry

With respect to unmatched, i.e. asymmetric parameters among the parallelized inverters, it is helpful to reconsider Eq. (3.23) and Eq. (3.24) introduced in Section 3.1.2, which however can be generalized to allow

individual parameters for each winding (cp. Appendix A for the derivation). These equations reveal that inverter asymmetries that can potentially deteriorate an equal current sharing[38] are the ohmic resistance and leakage inductance of the interleaving chokes' windings, R_{dc}, R_{ac} and L_{σ}. Conversely, the equivalent resistance for magnetization losses $R_{\mathrm{ac,m}}$ and the mutual inductance M_{12} are by definition matched parameters for each of the chokes.

$$\begin{aligned} I_{1,\mathrm{ph}}(s) =& \frac{V_{1,\mathrm{ph}}(s) - V_{2,\mathrm{ph}}(s)}{R_{1,\mathrm{dc}} + R_{2,\mathrm{dc}} + R_{1,\mathrm{ac}} + R_{2,\mathrm{ac}} + 4R_{\mathrm{ac,m}} + s\left(L_{1,\sigma} + L_{2,\sigma} + 4M_{12}\right)} + \ldots \\ & I_{\mathrm{ph}}(s) \cdot \frac{R_{2,\mathrm{dc}} + R_{2,\mathrm{ac}} + 2R_{\mathrm{ac,m}} + s\left(L_{2,\sigma} + 2M_{12}\right)}{R_{1,\mathrm{dc}} + R_{2,\mathrm{dc}} + R_{1,\mathrm{ac}} + R_{2,\mathrm{ac}} + 4R_{\mathrm{ac,m}} + s\left(L_{1,\sigma} + L_{2,\sigma} + 4M_{12}\right)} \end{aligned} \tag{4.38}$$

$$\begin{aligned} I_{2,\mathrm{ph}}(s) =& \frac{V_{2,\mathrm{ph}}(s) - V_{1,\mathrm{ph}}(s)}{R_{1,\mathrm{dc}} + R_{2,\mathrm{dc}} + R_{1,\mathrm{ac}} + R_{2,\mathrm{ac}} + 4R_{\mathrm{ac,m}} + s\left(L_{1,\sigma} + L_{2,\sigma} + 4M_{12}\right)} + \ldots \\ & I_{\mathrm{ph}}(s) \cdot \frac{R_{1,\mathrm{dc}} + R_{1,\mathrm{ac}} + 2R_{\mathrm{ac,m}} + s\left(L_{1,\sigma} + 2M_{12}\right)}{R_{1,\mathrm{dc}} + R_{2,\mathrm{dc}} + R_{1,\mathrm{ac}} + R_{2,\mathrm{ac}} + 4R_{\mathrm{ac,m}} + s\left(L_{1,\sigma} + L_{2,\sigma} + 4M_{12}\right)} \end{aligned} \tag{4.39}$$

In the case of higher frequencies, i.e. higher machine speeds, the current sharing is predominantly determined by the inductances. Since it can be assumed that the mutual inductance is considerably larger than the leakage values, any mismatch has only little impact. Nevertheless, in the case of lower frequencies, the ohmic parameters governs the current sharing: Because an equaling effect of $R_{\mathrm{ac,m}}$ can not be anticipated due to low magnetization losses at low frequencies, the asymmetry $R_{1,\mathrm{dc}} \neq R_{2,\mathrm{dc}}$ is expected to have a comparably strong impact. The simulation results[39] provided in Figure 4.41 support these presumptions.

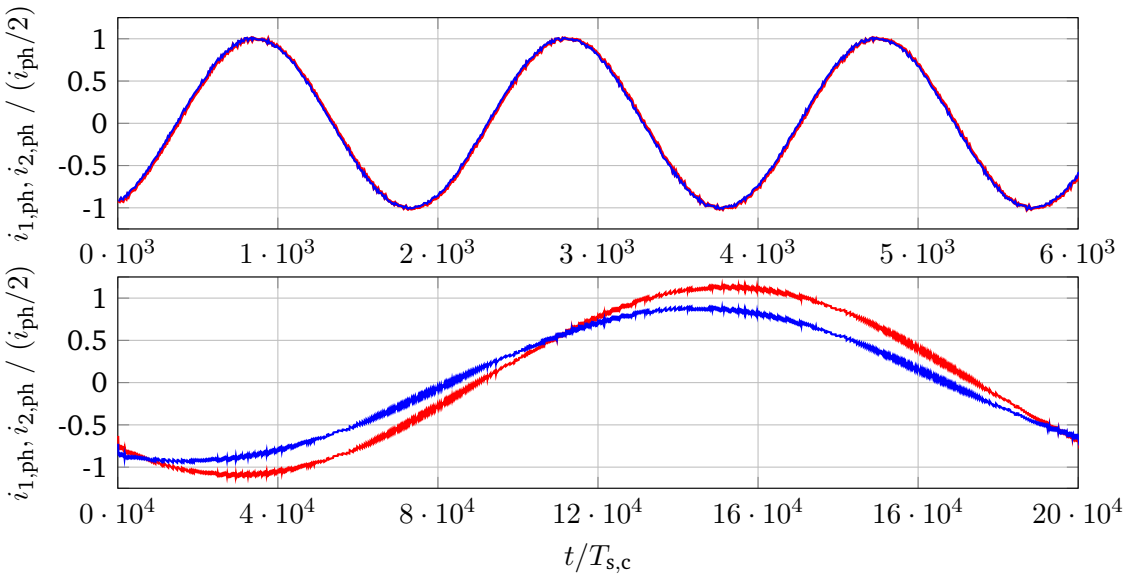


Figure 4.41.: Currents $i_{1,\mathrm{ph}}, i_{2,\mathrm{ph}}$ of an arbitrary phase for the inverter asymmetry $R_{1,\mathrm{dc}} = 1.5 \cdot R_{2,\mathrm{dc}}$ and $L_{1,\sigma} = 1.5 \cdot L_{2,\sigma}$ for high ($\omega_{\mathrm{r}} = \omega_{\mathrm{r,n}}$, top) and low machine speeds ($\omega_{\mathrm{r}} = 0.083 \cdot \omega_{\mathrm{r,n}}$, bottom) and otherwise rated machine operation.

[38] Under negligence of intentionally produced asymmetries via $V_{1,\mathrm{ph}}(s) - V_{2,\mathrm{ph}}(s) \neq 0$.

[39] Interleaving vectors are deactivated for the given simulations in order to provide a better visualization of the current sharing behavior.

Note that the FCS-MPC may be capable of balancing the currents by utilizing appropriate interleaving vectors, which can be promoted by an elevated $\lambda_{\mathrm{sat},2}$ in Eqn. (4.21). Nonetheless, the controller's granularity in the time domain allows only discrete steps for shifting the current loading between $i_{1,\mathrm{ph}}$ and $i_{2,\mathrm{ph}}$, which hinders a continuously balanced control of the current shares.

4.3.12. Impact of Discretization Method

As discussed in Section 4.1.3, the simulation results of the previous sections are all based on controller predictions discretized with the Euler exact method. This method prevents the occurrence of any discretization errors, but on the other hand can be problematic with respect to real-time controller implementations, if time-variant system matrices are present. This property indeed applies to the investigated system of this thesis, since the induction machine's speed can vary for different operating points.

It is to be evaluated whether the controller's performance with the Euler exact method can be approximately reached with the implementational less complex Euler forward method. In order to do so, the machine control TDD vs. average switching frequency is compared for both respective discretizations in Figure 4.42. In any case, the plant model is discretized with the Euler exact method, i.e. always delivers the true plant characteristics.

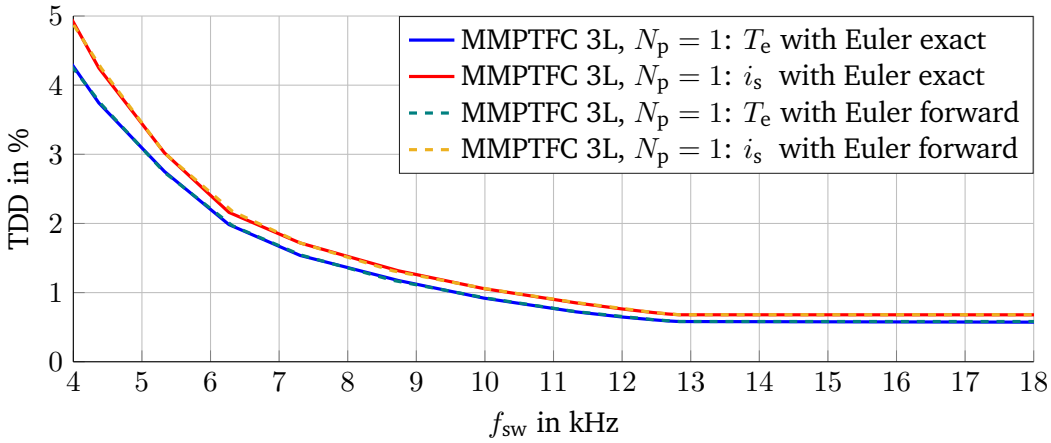


Figure 4.42.: Performance of torque and stator current TDD minimization of Euler exact and Euler forward discretization method for the MPC's predictions at rated machine operation.

Clearly, the Euler forward approximation does not impair the controller performance for the chosen sample time of $T_{\mathrm{s,c}} = 10\,\mu\mathrm{s}$ and the investigated, interleaved inverter drive system of this thesis. The property is supported by looking at the eigenvalues of the system matrix. The real parts of eigenvalues closest to 0 are in the range of -118 s^{-1} and -160 s^{-1}, depending on the rotor speed. Since the inverse of the respective eigenvalues corresponds with the time constants of the system, the smallest time constants are in the range of $8.5\,\mathrm{ms}$ and $6.3\,\mathrm{ms}$, i.e. of magnitudes larger than $T_{\mathrm{s,c}}$. This hints at both stability and small errors, particularly for a limited number of prediction steps, i.e. without any larger error propagation.

In case of the flux estimator (being based on the current model introduced in Section 3.2.1), a different situation occurs: Since the input of the estimator $\boldsymbol{i}_\mathrm{s}$ is not piece-wise constant and the estimator equations include internal feedbacks, significant accumulated errors can arise with the Euler forward method. They can eventually lead to offsets in torque control. Hence, it is advised to implement more sophisticated discretization methods for the estimator, e.g. Adams-Bashforth method [62].

4.3.13. Further Improvements for Investigated MPC Implementation

Next to the already proposed and implemented enhancements for the MPC, there are further possible improvements attainable. Therefore, and in conclusion to this chapter, further upgrades and alternatives are presented briefly in the following.

Consideration of dead-time and inverter non-linearities
In order to avoid unintentional short-cuicuits of the DC-link, a turn-on delaying dead-time is usually imposed on the switching signals (see also Section 3.1.1). This measure has the side effect that during the dead-time interval, the voltage output of the respective halfbridge is not directly controlled, but instead follows from the current's polarity. In case of a previously forward-conducting MOSFET that is to be turned off, the voltage output will transit to the opposite polarity. If however a backward-conducting MOSFET is to be turned off, the output voltage's polarity initially remains at the previous polarity until the dead-time interval has ended (cp. Figure 3.4). Hence, the output voltage and therefore also the MPC's predictions are distorted whenever the turn-off of a backward-conducting MOSFET is involved.

This described effect can be considered in order to attain more precise predictions. First, a detection for backward-conducting MOSFETs has to be implemented. This can be performed rather easily checking the polarity of the respective halfbrigde's output current $i_{1,\mathrm{ph}}$ and the current switching signal $s_{1,\mathrm{ph}}$. If their polarities are identical, the according MOSFET of the halfbridge is forward-conducting and no dead-time related distortions occur. If the polarities are opposed, the distortions can generally take effect. Any predictions that involve the switching of the backward-conducting MOSFET can now be adjusted by splitting up the prediction intervals in two parts, the first regarding the dead-time interval (previous voltage level applies) and the second one for the remaining controller time step (voltage level according to upcoming switch position).

Since the voltage transitions of the halfbridges are not necessarily appearing simultaneously but partially delayed, another aspect of the dead-time consideration is the possibility of allowing larger space vector steps with respect to the MPC's main prediction intervals. The dead-time interval can occur in between the main controller time step intervals, which may represent a low, short-term space vector step towards the previous and the future voltage space vector. Larger voltage steps at the machine terminal therefore may be split up into two smaller voltage steps. This may be beneficial for previously introduced control aims (cp. Section 4.3.4 and Section 4.3.6).

Similarly to the dead-time, non-linearities of the power switches can be considered, e.g. the actual time characteristics of the voltage transition, as well as the voltage drop over the semiconductors (both being dependent on the present transistor current and DC-link voltage). The benefits of such considerations can become particularly pronounced in the case of parameter estimation [41] or the implementation of accurate observers. With respect to the mere controller design, the distortions and therefore also the advantage of any compensation mechanisms are on the other hand anticipated to be rather small. This assumption can be justified by the insignificant deterioration of controller performance even for large parameter mismatches (cp. Section 4.3.11).

Increased MPC sampling frequency
As shown in the performance evaluation of various cost terms, the minimal machine TDD is reached at approximately $14\,\mathrm{kHz}$ in case of the interleaved inverter (cp. e.g. Figure 4.18). An elevated switching activity beyond this point does not occur, since switching actions are not penalized anymore and the resulting pulse pattern minimizes the activated cost terms in an optimal manner. Nevertheless, the machine TDD can in fact be minimized further if the time-granularity of the MPC is decreased, i.e. the controller's sampling interval

$T_{s,c} = 1/f_{s,c}$ is shortened. Due to the smaller predictions steps, the quantities can be controlled in a finer manner [55]. The benefit is usually pronounced strongest[40] if relations of $f_{c,s} \geq 10 f_{sw}$ can be maintained by implementing the measure. Likewise to the higher control quality, the maximum switching frequency of the MPC, i.e. the average switching frequency appearing for an deactivated penalization of switching actions, is anticipated to increase. An example is given in Figure 4.43, where the MPC's sampling time is reduced by a factor of 2.

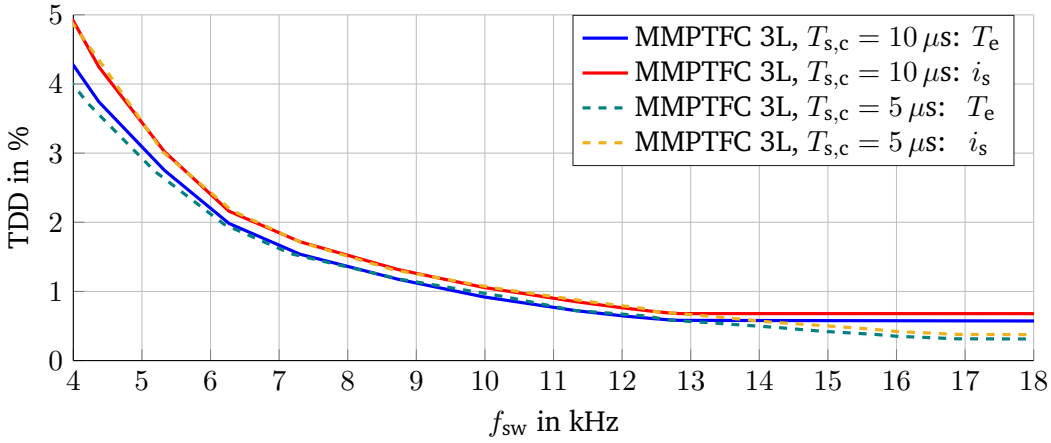


Figure 4.43.: Performance of torque and stator current TDD minimization for regular ($T_{s,c} = 10\,\mu s$) and faster sampling ($T_{s,c} = 5\,\mu s$) MPC at rated machine operation.

Note that an increased MPC sampling frequency also entails other adaptations to the controller implementation, e.g. the expansion of the finite state machine developed for maintaining the choke magnetization in Mode 1 (cp. Section 4.3.2).

Variable switching point MPC

The principle of variable switching point MPC extends the original optimization problem of the FCS-MPC (cp. e.g. Eq. (4.1)) by another optimization variable: Firstly, the switching point $t_{sw} \in \,]0, T_{s,c}]$ for the upcoming switching actions is optimized for each of the candidate switch positions of the FCS. This is performed by solving a continuous optimization problem. Secondly, the best switching state candidate is computed by comparing the cost function values obtained for the optimal switching times [78]. The resulting advantage of the variable switching point MPC is an elimination of the time granularity of the controller's output, promising additional improvements in control quality.

As discussed in Section 4.1.6, an efficient optimization for constrained, continuous variables (here: t_{sw}) requires a linear system description. If such a system is not provided, as it is for example the case when considering the DC-link current, according linearizations have to be performed, which may deteriorate the performance.

Fixed switching frequency MPC

A fixed switching frequency can be of great interest for grid applications, where limitations on specific harmonics are imposed by the respective standard or code, and hardware filters are a necessity. It can be implemented by truncating the set of switching states dynamically, e.g. to a set that imposes exactly one phase to switch for

[40] The exact relation depends on the concrete system. As depicted in Figure 4.43, the system of this thesis shows a distinct benefit of increased MPC sampling frequency if relations of $f_{c,s} > 7 f_{sw}$ are preserved by it.

each upcoming controller time step $T_{\mathrm{s,c}}$. Obviously, this principle can also be extended to whole switching sequences. This principle can be combined with the regular FCS-MPC or with a variable switching point MPC [83]. Nevertheless, it should be noted that the fixed switching frequency comes at the cost of inherently losing the property of omitting switching when it is not beneficial for overall TDD reduction. This property however is one of the fundamental advantages of the original FCS-MPC implementation presented in this thesis.

Consideration of voltage source topologies and DC-link equations
Throughout this thesis, the assumption is made that the inverter's DC-source provides the time-average of the drawn inverter current. This assumption is equivalent to presuming that all ac-components of i_{d} flowing through the DC-link capacitor. Furthermore, the voltage at the DC-link capacitors is assumed to be constant. Overall, this allows analyses independently of the feeding source for the inverter.

However, the properties described above can only be expected of rigid voltage DC-sources with negligible output impedance. If instead a battery with significant output resistance is used, voltage distortions at the DC-link capacitor will appear, and some ac-components of the drawn inverter current will also be supplied by the battery. Similarly, if simple three-phase diode rectifiers are used as DC-source, a $6 \cdot f_{\mathrm{grid}}$ voltage ripple with an amplitude dependent on the drawn load current and DC-link capacitor size has to be anticipated[41]. If measurements of the source current i_{source} (or the DC-link capacitor voltage $v_{\mathrm{dc,cap}}$) are available, the DC-link optimization can be adapted by determining the capacitor current via $i_{\mathrm{dc,cap}} = i_{\mathrm{d}} - i_{\mathrm{source}} = i_{\mathrm{d}} - C_{\mathrm{dc}} \cdot \mathrm{d}/\mathrm{d}t(v_{\mathrm{dc,cap}})$, i.e. by taking into account the ac-contribution of the source current towards i_{d}. If an appropriate model for the source is available, i_{source} can even be included in the MPC's predictions, allowing a precise evaluation and minimization of $i_{\mathrm{dc,cap,rms}}$.

Lastly, in the case of controlled rectifiers such as back-to-back converters, a combined MPC for both the rectifier and inverter can be developed. Again, this allows precise predictions, control and hence profound optimization potential for the DC-link capacitor current and voltage ripple [84]. Nonetheless, it has to be considered that the FCS obviously further increases in this case, e.g. to $\boldsymbol{\mathcal{U}}_{\mathrm{FCS}} = \{-1, 1\}^9$ or $64 \cdot 8 = 512$ possible switch positions in case of a one-step prediction with a two-level rectifier and the investigated interleaved inverter of this thesis.

[41] In this case, it is reasonable to commission hybrid DC-link banks as proposed in Section 3.1.3. The ripple related to the DC-link feeding can then be reduced by electrolytic capacitors with comparably large capacitance. At the same time, the ripple related to switching is mainly handled by foil or ceramic capacitors with low ESL.

5. Real-Time Implementation of Control Algorithm

With respect to the task of choosing a suitable computational unit for realizing any real-time capable control algorithm, two fundamental principles come into question, which are exemplarily discussed for the device types of microprocessors and FPGAs:

- Microprocessors: This family of computational units integrates arithmetic logical units (ALU) with registers (”fast” memory), control units for the native instruction sets, RAM (”slow” memory) and memory management, as well as possibly other peripherals such as bus connections or IO-interfaces.

  Since many basic instructions are usually split up into several clock cycles in order to shorten signal propagation time and enable high clocking frequencies[1], the principle of pipelining is usually applied here. This principle consists of continuously ”pushing” data and their instructions through the computation path for every clock cycle, as otherwise the discrete functional units are only utilized for a fraction during a performed instruction, and else remain idle. Sophisticated and greatly optimized enhancements such as super-scalar processors or even multi-core processors are widely available, which aim at increasing the data's and instruction's throughput rate by parallelizing the performed instructions [85]. However, a performance boost can only be expected if data dependencies can be ruled out, i.e. if an initialized parallelization does not depend on results that are not completely computed yet due to the pipeline's inherent latency. For this reason, microprocessors perform best for sequentially structured tasks.

  Program source code can be written in the native instruction set (assembly language), but usually is provided in generalized or higher-level languages. A compiler then optimizes the code and translates it into machine code, which can be executed on the processor unit.

- Field-programmable gate arrays (FPGAs): These kind of computational units contain an array of programmable or configurable logic blocks (CLBs), which may be subdivided into several slices. The CLBs often are implemented as lookup tables (LUTs), serving as function generators for logic operations, which are combined with storage elements (flip-flops, registers). The CLB slices can also contain further dedicated circuits that speed up synthesizable arithmetic operations, such as lookahead carry logic. Multiplexing is used to control a possible bypassing of the storage elements, which enables the user to individually design the propagation length of data paths. Secondly, dedicated multiply-accumulate units (MACCs) can be provided, which may be also organized in slices, then sometimes referred to as DSP-slices. Distributed (LUT-RAM) and block memory (Block-RAM) can be provided for data storage, e.g. for intermediate results. A clock management with high-speed buffers allows variable frequency synthesis and ensures low-skew and low-jitter clocking signals. An exemplary overview of components in a FPGA is given in [86] for the *7-Series* from the former hardware developer *Xilinx*.[2] More detailed explanations of the CLB's and MACC's / DSP-slice's structures are also available [87] [88].

[1] Consider a basic arithmetic operation $a + b$. In order to perform this task, the instruction 1) has to be loaded, 2) the variables a and b have to be read from registers or even slower-paced memory, 3) added in the ALU, and 4) the result has to be saved in registers.
[2] In 2022 completely acquired by the company *AMD*.

The advantage of utilizing FPGAs for specific computational tasks, e.g. the calculations necessary for a FCS-MPC, is the possibility to configure the hardware in an optimized manner. Separate modules, organized as so-called IP-cores, can be realized to fulfill specialized tasks with a configurable degree of parallelism, number of pipeline stages and clocking frequency.

Note that a wide variety of other computational units exist, which have to be interpreted as trade-offs and / or combinations and therefore can be categorized in between the above mentioned principles. Examples are digital signal processors (DSPs, specialized on performing matrix operations, filtering, FFTs etc. in real-time), microcontrollers (MCU, may include additional peripherals, such as ADCs, PWM-modules etc.), graphics processing units (GPU, similar to DSPs, but with a focus on the relative demand of graphics-related operations), complex programmable logic devices (CPLDs, with focus on LUTs) and application-specific integrated circuits (ASICs, arbitrary combinations, but not post-configurable) [85].

Since the approach via FPGAs provides full flexibility for an efficient implementation of the control algorithm, it is used for this thesis. Its configuration can be facilitated significantly by packages supplied by *MathWorks*' *HDL Coder toolbox* [89], which allows automated porting of *Simulink* designs towards supported evaluation boards. The evaluation board used for this thesis is the *ZedBoard* [90], which incorporates the SoC *Zynq-7020* [88] by *Xilinx*, as well as peripheral interfaces as UART, JTAG and Ethernet for configuration by and communication with the host computer. The SoC *Zynq-7020* (*7-Series*) includes a dual-core *ARM Cortex-A9 MPcore* (microprocessor) and a *Artix-7* (programmable logic / FPGA unit). While the former can be used for communication towards the host computer, e.g. for outputting measurements and controller data via FIFOs, the latter can be used to implement the actual control algorithm.

5.1. Considerations and Preparations for FPGA-based Implementation

The necessary online calculations[3] to perform the suggested control algorithm of Chapter 4 can be broken down to only a few basic arithmetic operations: Summations and subtractions, multiplications, absolute values and comparisons ($<, \leq, \geq, >$). Therefore, the FPGA's CLBs and MACCs already provide the required computational sub-units, and no complex operations, e.g. square roots or trigonometric operations, have to be synthesized.

This generally can be seen as an advantageous situation. However, it has to be considered that the CLBs and MACCs expect operands of a fixed-point datatype. For instance, the MACCs of *Xilinx*'s *7-Series* can compute operands with the word lengths of 25 bit and 18 bit. Therefore, the appropriate choice of data types is a crucial task, as multiplication of 25 bits with 19 bits would already require two MACCs units, which obviously is converse to resource-efficient design. For this reason, the FCS-MPC implementation of this thesis mainly uses these respective maximum word lengths for multiplications. Exceptions are made if these data types imply any crucial rounding errors (incl. their propagation of uncertainty), overflows or underflows, which can otherwise easily lead to deterioration of the controller performance or even instabilities. According checks can be performed via simulations, which compare the controller behavior for high precision data types with the limited ones. Extreme operation points such as overload conditions, varying V_{dc} etc. should be considered for these checks.

Note that alternatively also floating-point operations can be utilized, which however require the synthesis of one or several floating-point units (FPUs). Since these units demand a large amount of CLBs and MACCs and therefore become a very limited resource, this measure ultimately shifts the design principle

[3] See als Eqn. (4.21) as well as the cost terms of Section 4.3.3 to Section 4.3.8.

towards the one of microprocessors or DSPs. As this is not the chosen approach of this thesis, floating-point implementations are not further considered here.

In the context of multiplications on FPGAs, it stands to reason to make a distinction between the multiplication of two variables on the one hand or a variable and a constant on the other. While multiplying two variables indeed is best performed by employing MACCs, the multiplication of a variable with a constant can be interpreted as a gain operation. Gain operations can be implemented efficiently with shift and add operations, which provide the possibility of utilizing CLBs instead of the generally more scarce MACCs units. Luckily, many multiplications can be considered as gains in the FCS-MPC algorithm, e.g. the partial predictions $\boldsymbol{x}_{\text{partpred}}(k+1) = (\boldsymbol{A} \cdot T_\text{s} + \boldsymbol{I}) \cdot \boldsymbol{x}(k)$ for the evolution of the state variable according to Eq. (4.2). In this mentioned case, the system matrix is assumed to be constant. If however the system matrix is not constant, as it is the case for varying speeds of the induction machine, gains can still replace many multiplications by an appropriate split-up of the system matrix, as hinted at in Eq. (3.72).

5.2. Optimization of Hardware Resources for FPGA-based Implementation

The aim of the application-specific optimization of hardware resources is to implement the FCS-MPC with a low amount of necessary CLBs and MACCs without impairing the aspired sampling time of the controller at $T_{\text{s,c}} = 10\,\mu\text{s}$. The chosen measures are referred to as

1. Streaming: Sequential calculation of operations applied to vectors,

2. Resource Sharing: Reuse of arithmetic modules for different variables or vectors within the algorithm's signal path.

Before the implementation of these optimizations are explained in more detail, firstly the general trade-off with respect to pipelining FPGA designs is to be discussed shortly. Note that in all of the following paragraphs, the sampling instant k in the notation $x(k), u(k)$ etc. is based on the sampling period of the controller, i.e. on $T_{\text{s,c}}$, while delays of the registers at clock rate are display as fractions in this notation.

Pipelining
As mentioned in the introduction of Chapter 5, pipelining is used to decrease the propagation time of the data paths. The clock frequency can be chosen in a manner that the clock cycle T_{clk} matches the maximum propagation time of any data path. For this reason, an increasing number of pipeline stages (e.g. by splitting up the data path by means of buffers or registers) can allow higher clocking frequencies. Moreover, the buffering by additional pipeline stages provides the opportunity to increase the overall throughput rate for the respective computation module, since new data can be fed into the pipeline at an elevated frequency.

Consider the example illustrated in Figure 5.1. Given is a computation module that performs some arbitrary calculations on the variables $x(k), u(k)$ and outputs the final cost term $J(k)$. These calculations shall represent the prediction stage and cost function of a FCS-MPC. In the top part of Figure 5.1, only input buffers and a final output buffer are implemented, leading to a long signal path and propagation time. In the lower part however, the data path is split up into two pieces by buffering registers. The maximum propagation time is reduced, which enables higher clock frequencies. The overall delay of the two implementations in Figure 5.1 is determined by the respective product of T_{clk} and the overall count of registers in series. The throughput rate of the algorithms is the respective f_{clk}.

Note that the pipelining principle requires the buffering registers for all parallel signal paths, as otherwise the signals will not be properly time-aligned with respect to possible merges.

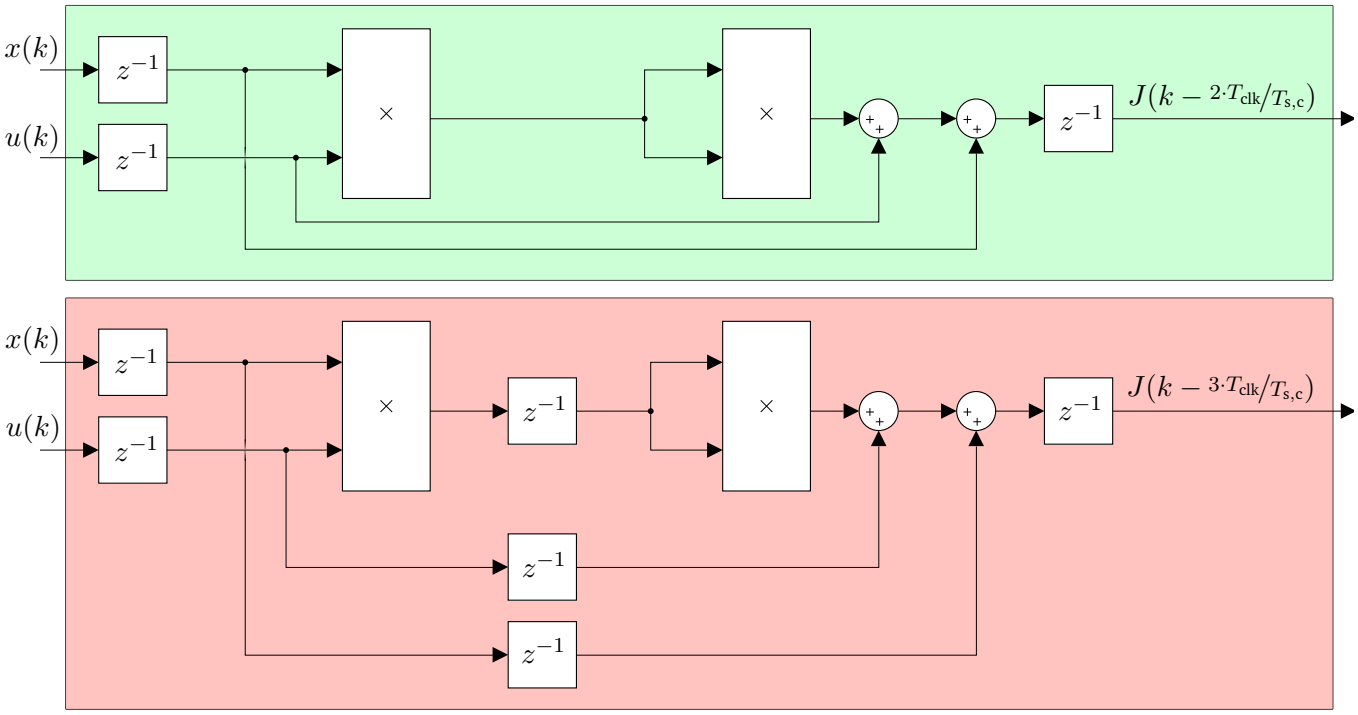


Figure 5.1.: Example for a computation module (top) with applied pipelining (bottom). The delays are implemented at clock frequency.

Streaming

The term streaming addresses the measure of serializing operations applied to a vector. In Figure 5.2 it is given exemplarily for the torque cost calculation $J_{\mathrm{T},2}(k) = \lambda_{\mathrm{T},2} \cdot \left(T_{\mathrm{e}}(k+1) - T_{\mathrm{e}}^{*}\right)^2$, which is part of the control optimization problem solved by the FCS-MPC (cp. Eqn. (4.21)). Note that the chosen approach for solving the optimization problem is total enumeration, as proposed in Section 4.1.6 for FCS-MPCs implementations with $N_{\mathrm{p}} = 1$.

As it can be seen, the original structure of the torque cost calculation (top part of Figure 5.2) already includes pipeline structures, but necessitates 64 subtractions and $2 \cdot 64$ multiplications. The streamed version of the calculation (bottom part of Figure 5.2) instead utilizes a serializer and a deserializer to stream the vector – in this case the predicted torque values for all elements of the FCS – through only one instance of subtraction and two multiplications. This implies it requires only $1/64$-th of the hardware resources,[4] but on the other hand also 64 additional clock cycles. The internal counter is needed at the deserializer for recomposing the vector with the correct order of serialized feeding. The trigger signal on the other hand is important for overall time-alignment of various signal paths. It can be interpreted as a global delay line that represents the latency of the signal paths at the investigated position of the algorithm. The trigger signal should also be used for synchronized data sampling at the initialization of every controller time step. This way it is ensured that none of the signals are changing during the streaming process.

[4] Neglecting the resources necessary for the serializing and deserialization, which indeed are comparably little.

The FPGA realization for the control algorithm of Section 4.3 utilizes streaming for all of the predictions and cost functions that are based on the FCS. This means that the serialization already takes place at the prediction stage of the FCS-MPC, and not as late as at the cost calculations. Since the individual cost terms can also be added and finally minimized in a serial manner[5], the deserialization in fact is not further needed.

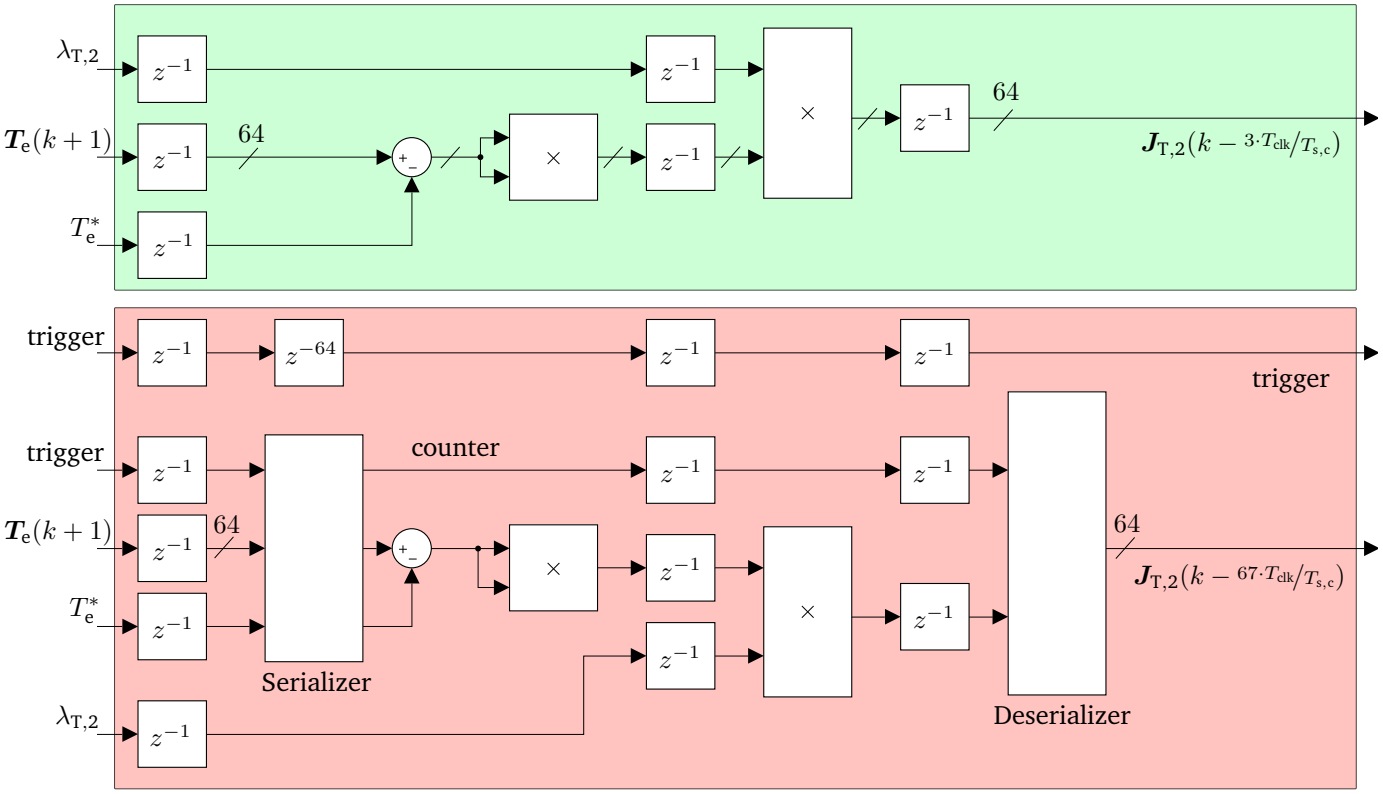


Figure 5.2.: Example for the torque error cost calculation (top) with applied streaming (bottom). The delays are implemented at clock frequency.

Resource sharing

Resource sharing is applied for reusing arithmetic modules for several variables or vectors within the signal path. A suitable part for this measure is the time compensation of the control algorithm. For the specific implementation of the FCS-MPC of this thesis and under consideration of the delays by the algorithm's computations and current measurement instrumentation (cp. Section 5.3 and Section 6.1), $(1+2/3)$-controller time steps with the respective inputs $\boldsymbol{u}(k)$ and $\boldsymbol{u}(k-1)$ should be compensated.

The resource sharing is implemented with a counter that is initialized by the global delay line or trigger signal, as indicated in Figure 5.3. Together with a multiplexing unit, it firstly routes $\boldsymbol{x}(k-3/5)$ and $\boldsymbol{u}(k-1)$ through the state-space equations of the time compensation. A second multiplexing unit at the output of the system equations takes into account possible correction factors due to fractional time steps. The partially time-compensated output $\boldsymbol{x}(k)$ is then fed back to the first multiplexing unit, that now feeds the state-space calculations with the inputs $\boldsymbol{x}(k)$ and $\boldsymbol{u}(k)$. Eventually, the fully time-compensated output $\boldsymbol{x}(k+1)$ is outputted.

[5]This is possible by simply comparing the serialized total costs with the most recently found minimum, and overwriting the latter whenever lower costs are registered.

Note that the state-space calculations include pipeline registers. Since the illustrated and implemented case in Figure 5.3 has two pipeline stages (which have to be run through twice due to the resource sharing), the trigger signal equivalently requires an additional delay of two clock cycles. Further, please note that $\boldsymbol{A}_\mathrm{c}, \boldsymbol{B}_\mathrm{c}$ are denoted as constant, but in fact may include variable or transient parameters, such as varying resistances due to temperature dependency, as well as varying ω_r and V_dc.

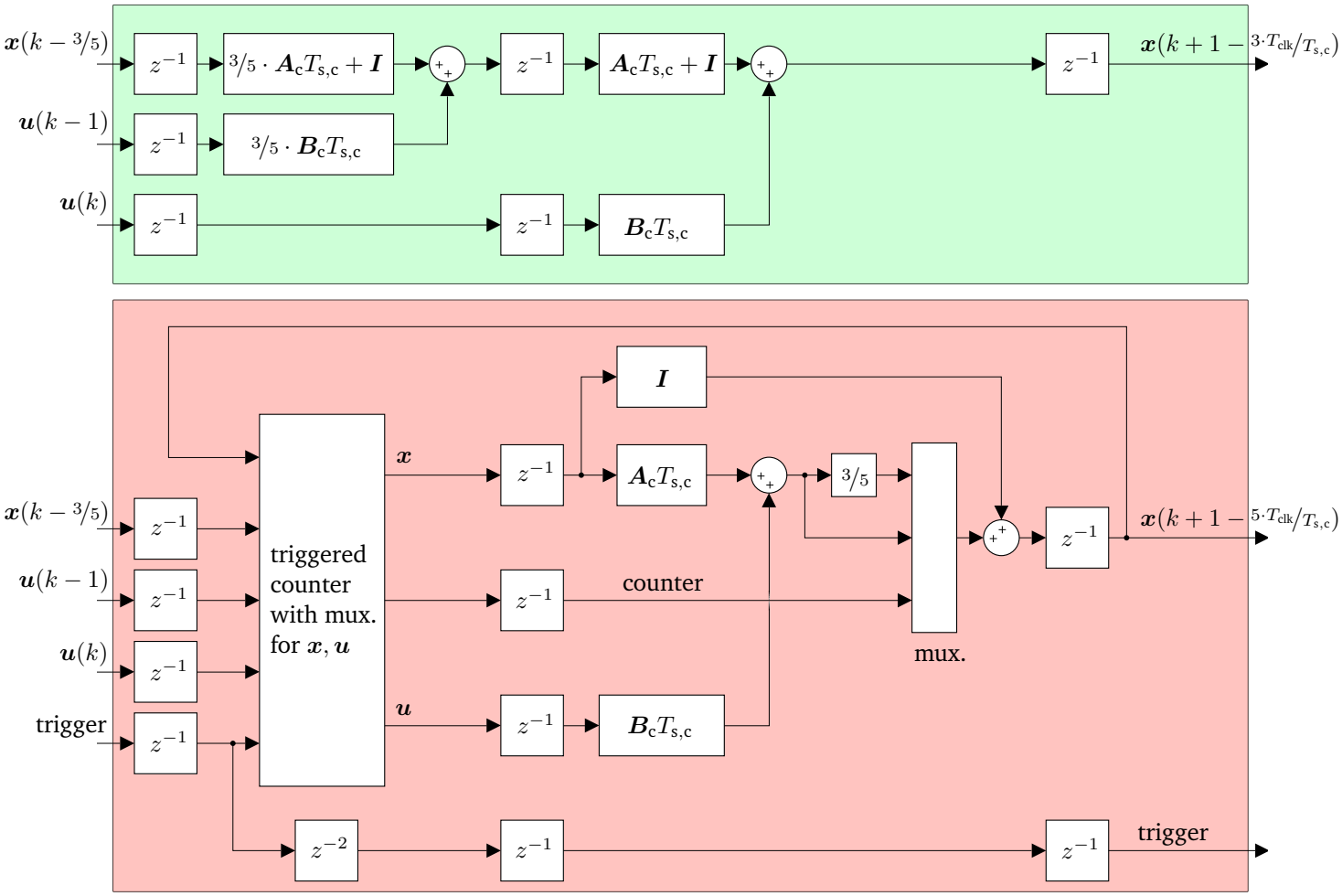


Figure 5.3.: Example for $(1 + 3/5)$-time compensation (top) with applied resource sharing (bottom). The delays are implemented at clock frequency.

Obviously, the resource sharing of the time compensation can also be expanded for the prediction stage, since it likewise requires the calculations of the state-space representation. However, due to reasons of redundancy, this possibility is not further elaborated in this thesis.

Reduced finite control set

Next to the explained opportunities of streaming and resource sharing, another supplementary method for saving computational resources is the attention towards reliably truncated finite control sets. Consider for example the case of a permanently activated cost term $J_{\mathrm{sw,dv/dt}}$, which prohibits larger voltage steps with respect to the phase-to-phase voltage at the machine terminals. This avoidance of large voltage steps can be translated to allowing only directly neighboring voltage space vectors for the respectively upcoming controller

time step (cp. Section 4.3.4, Figure A.1 and Table A.2). In the worst case, the current voltage space vector is the zero-voltage space vector $\boldsymbol{sv}_0$. Here, the possible direct neighbors (including the currently switched $\boldsymbol{sv}_0$, which implies a zero-voltage step) are six small space vectors. This adds up to $6 \cdot 6 + 1 \cdot 10 = 46$ candidate voltage space vectors for the next controller time step. A pre-filtering and sorting algorithm can be therefore be implemented to reduce the size of the FCS by a factor of $^{46}/_{64} \approx 0.72$.

Similarly, the saturation prevention and / or the implications of the cost term J_{magmode} can be utilized as a pre-filter to realize a dynamic restriction of the FCS. Nevertheless, it has to be noted that the pre-filtering itself as well as the necessary resources for an appropriate routing have to be traded off when considering such implementations.

Since the hardware implementation of this thesis is realized in the manner to maintain full flexibility, the measures for a reduced finite control set are not implemented for the specific algorithm realization ported on the commissioned computational platform.

5.3. Resulting Structure of FPGA-based Implementation

The possibilities for resource efficient design, as discussed in the previous section, are mostly implemented for the algorithm ported on the *Zedboard* (namely: pipelining, streaming and resource sharing). In order to evaluate the resulting overall delay of these strategies, a summarizing sketch of the structure is given in Figure 5.4. As it can be seen, the optimal control signals reach the output of the algorithm with a total delay 223 clock cycles. Since a delay of $120 \cdot T_{\text{clk}}$ is already introduced by the considered settling time of the filter for the current measurements,[6] the "true" delay due to the computations of the control algorithm is $90 \cdot T_{\text{clk}}$. This includes various pipeline stages within the resource-shared time compensation and streamed prediction.

A computational delay of $90 \cdot T_{\text{clk}}$ implies that the achievable controller frequency is $1/(90 \cdot T_{\text{clk}}) \approx 0.011 \cdot f_{\text{clk}}$. On the other hand, various conducted synthesis trials for the commissioned FPGA lead to the insight that a maximum frequency of $f_{\text{clk}} \approx 20\,\text{MHz}$ is realizable.[7] Hence, the acquirable controller sampling frequency is $f_{\text{s,c}} \approx 0.11 \cdot 20\,\text{MHz} = 220\,\text{kHz}$, correlating with $T_{\text{s,c}} \approx {}^{1}/_{220\,\text{kHz}} \approx 4.5\,\mu\text{s}$.

Since the control algorithm is designed for $T_{\text{s,c}} = 10\,\mu\text{s}$ and the current measurements have a -3 dB filter response of $131\,\text{kHz}$, the remaining pipelining "budget" of $(10\,\mu\text{s} \cdot 20\,\text{MHz} - 90) \cdot T_{\text{clk}} = 110 \cdot T_{\text{clk}}$ is merely filled up with a final delay at the output. Nevertheless, this remaining pipelining budged shows that even higher resource efficiency is generally possible.

The overall hardware utilization for the programmable logic of the commissioned *Zynq-7020*-device – including measurement filters, FIFOs for debugging and analysis, control parameter transmission etc. – is summarized for the FPGA implementation in Table 5.1. Although the chosen device is declared by *Xilinx* as cost-efficient portfolio option, the computational resources of the specific FPGA are not fully depleted. Moreover and as discussed in this and the previous section, further computational optimization is applicable, and the pipelining budget is by no means exhausted. Overall, this proves the proposed FCS-MPC implementation to be indeed a feasible option for cost-efficient and real-time capable hardware implementations.

[6] Anticipating a delay of $6\,\mu\text{s}$ (cp. Section 6.1) and $T_{\text{clk}} = {}^{1}/_{200} \cdot T_{\text{s,c}}$.

[7] This seemingly low value of f_{clk} is not necessarily related to sparsely implemented pipeline stages, but in fact is owing to a relatively high utilization of the FPGA, which can lead to congestion and routing issues.

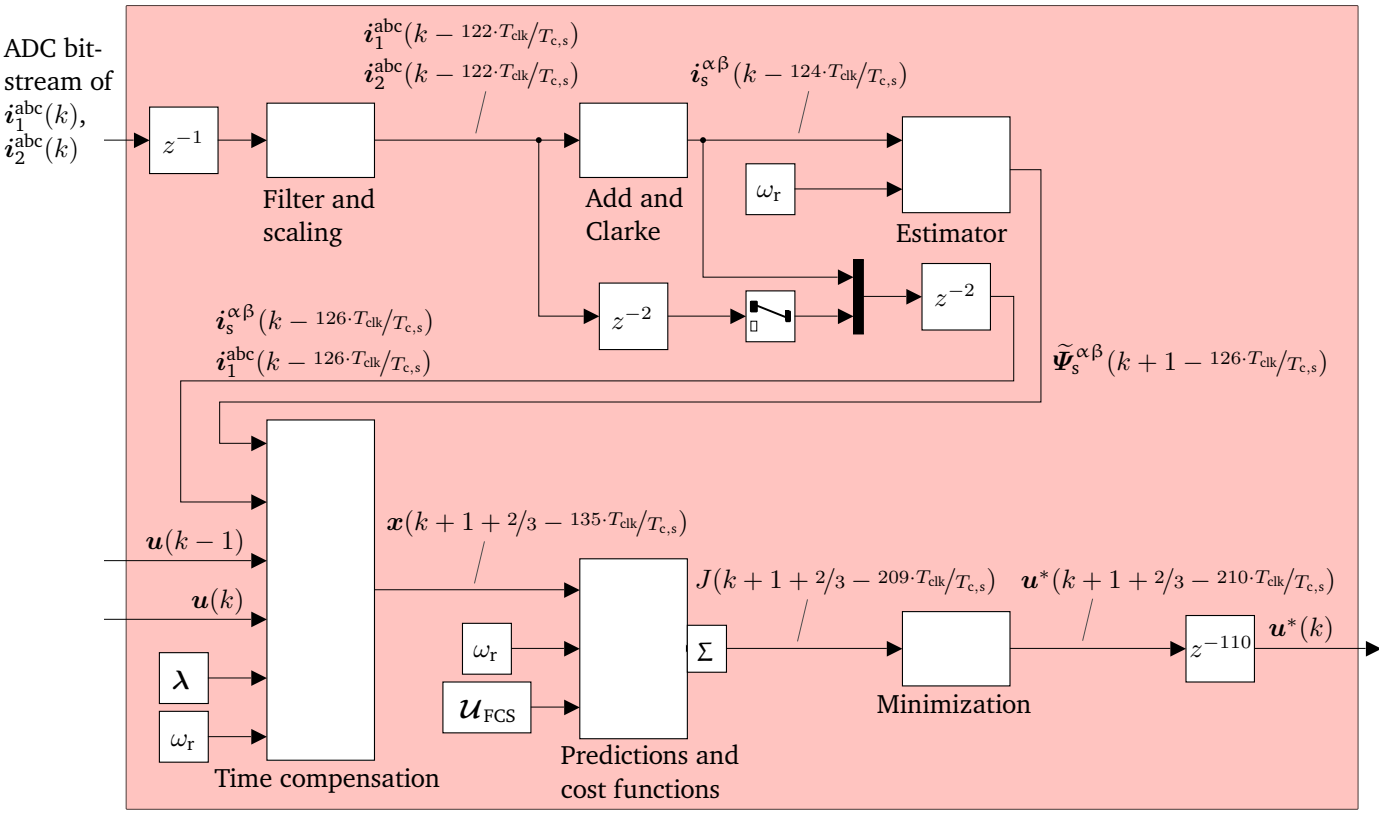


Figure 5.4.: Sketch of overall algorithm structure and resulting delay due to realized strategies for resource efficiency of the FPGA-design.

Table 5.1.: Utilized resources of the commissioned *Zynq-7020*-device for the proposed FPGA-implementation.

Resource type	Utilized percentage of available resource types
Lookup tables (LUTs)	42 %
Flip-Flops (FFs)	33 %
Block-RAM (BRAM)	72 %
Multiply-accumulate units (MACCs)	61 %

6. Experimental Setup and Evaluation

The appropriate system modeling, controller implementation and overall performance is to be validated not only in simulation, but also with respective hardware runs. For this reasons, an experimental setup was developed for this thesis. In this chapter, the explicit experimental setup is documented, and representative hardware measurements are provided. As it will be shown, the collected hardware results generally support the validity of the collected simulational data and the established presumptions of Chapter 4. Please consider that the hardware measurements are not conducted as detailed as the simulation results in Chapter 4 in order to remain in the scope of this thesis. Finally, this chapter contains a discussion on the collected insights, which are summarized and provided in form of guidelines for a possible future hardware optimization.

6.1. Description of Experimental Setup

This section briefly describes the main subsystems established to allow a fully functional experimental setup, including the machine test bench, inverter, DC-link and DC-source, interleaving chokes, measurement instrumentation, as well as the computational platform.

Machine test bench
The machine to be controlled is a standard IE1 $5.5\,\mathrm{kW}$, $400\,\mathrm{V}$ / $10.5\,\mathrm{A}$ (Y) squirrel-cage induction machine. Its parameters such as ohmic resistance, stray and mutual inductance are identified by the classic approach of no-load and stand-still measurements during grid-feeding [58], as conducted in [50]. The attained parameters are the ones given in Table B.1, which also are used for the simulations in Chapter 4.

The induction machine is coupled with an externally excited $15\,\mathrm{kW}$, $400\,\mathrm{V}$ DC-machine, which is implemented to be the load. The DC-machine can be speed-controlled with a *Lenze 4900* converter that is fed by the grid and provides bidirectionality. Its speed estimation is based on the machine's back-EMF. The estimation and hence also the controlled speed can contain offsets, which however can be adjusted by the speed measurement of the induction machine.

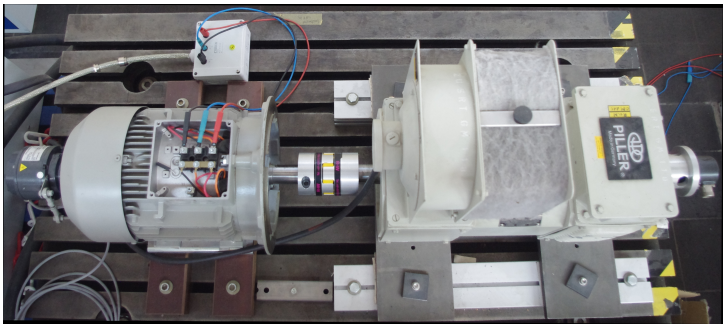


Figure 6.1.: Machine test bench with induction machine (left) and DC-machine (right).

Interleaved inverter
The overall inverter consists of two two-level three-phase inverters, the DC-link and the interleaving chokes. The hardware setup is shown in Figure 6.2. A more detailed description of the individual components is given in the following paragraphs.

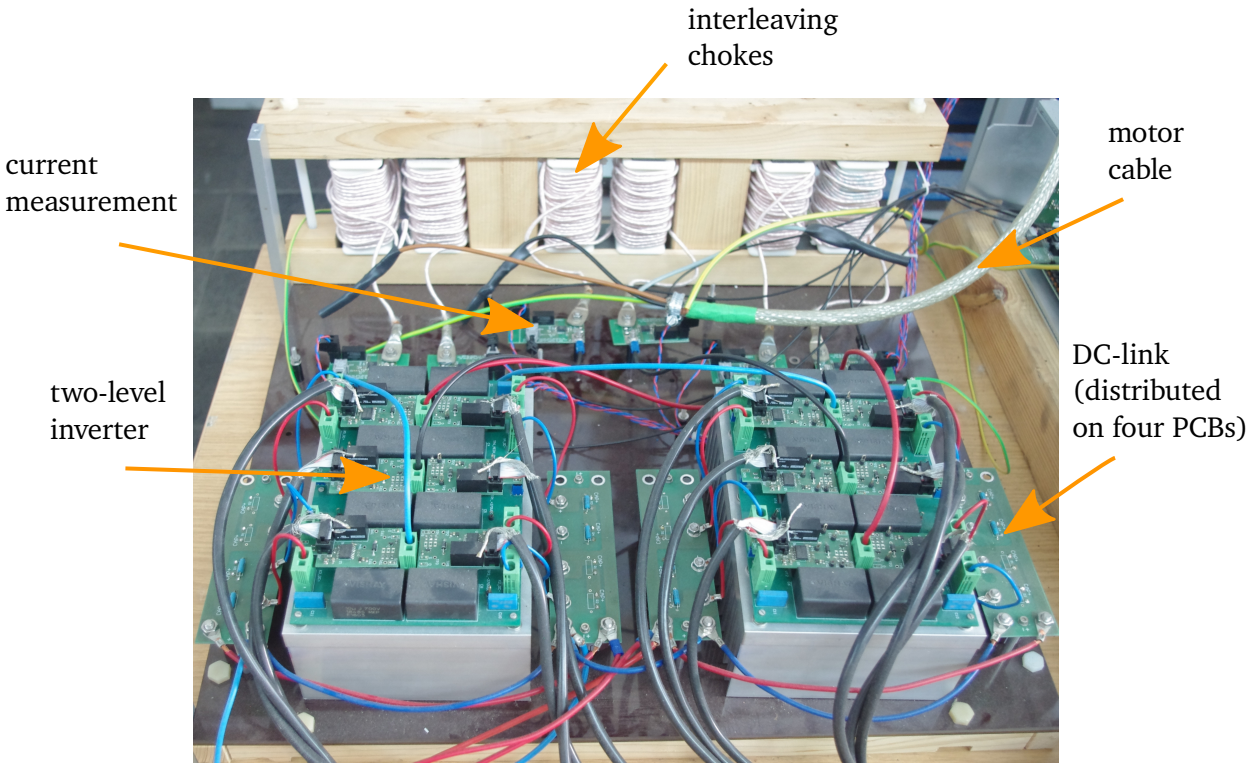


Figure 6.2.: Hardware setup of interleaved inverter.

Two-level inverter
The utilized two-level three-phase inverters are a self-designed iteration of a previous SiC-Inverter developed at the Institute for Power Electronics and Control of Drives at TU Darmstadt [91]. The implemented $1200\,\mathrm{V}$ N-channel SiC-MOSFETs are of the type *SCT2080KE* by *Rohm Semiconductor* (cp. Table B.2). These devices are discrete components in the TO-247 package. An additional anti-parallel diode is omitted, i.e. the internal body diode is used as freewheeling diode during the process of commutation.

An individual gate driver is commissioned and supplied galvanically isolated for every power switch. The specific driver IC is *1ED020I12-F2* by *Infineon*, which is placed on respective driver PCBs that are mounted directly above the according power switch. Together with the chosen voltage supply for the drivers, they supply gate-source voltages of $V_{\mathrm{ge}} \in \{-5\,\mathrm{V}, 20\,\mathrm{V}\}$ when switching related charging is complete. The maximum gate current is limited to $2.4\,\mathrm{A}$ and the external gate resistance is chosen to be $5\,\Omega$.

In order to prevent large over-voltages during transistor turn-off, foil capacitors of *Vishay Intertechnology*'s *MKP1848S* series are placed directly at each halfbridge. The foil capacitors are connected in a symmetrizing series-connection, leading to an overall buffer capacitance of approximately $5\,\mu\mathrm{F}$ per halfbridge.

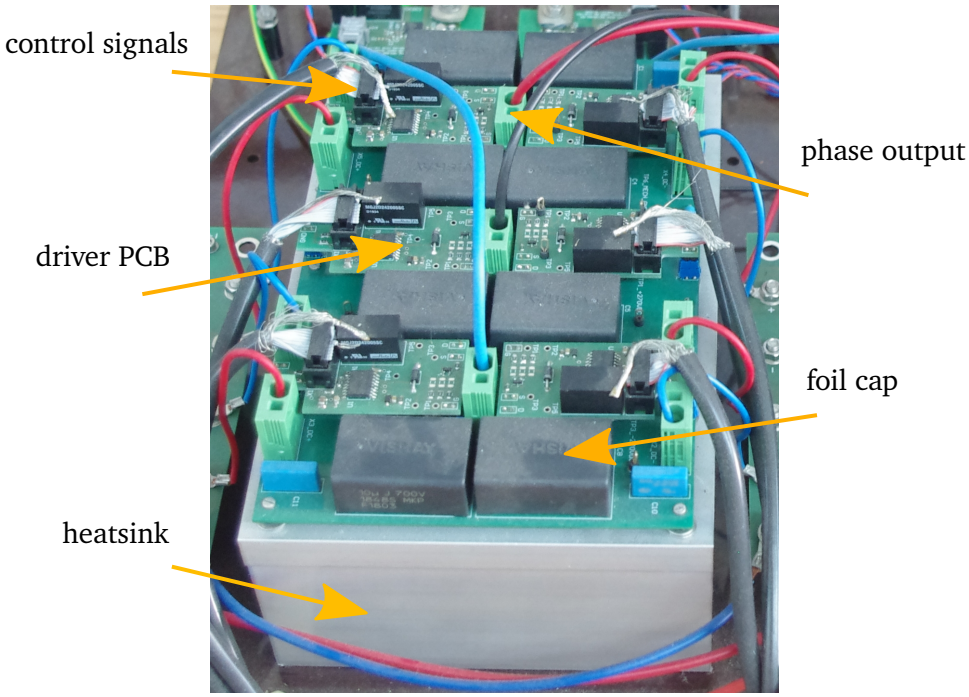


Figure 6.3.: Designed and commissioned two-level three-phase SiC inverter.

DC-link

In addition to the buffering foil capacitors, additional aluminum electrolytic capacitors of the *KMQ* series of *Nippon Chemi-Con* are providing a larger DC-link capacitor bank on separate PCBs. The overall capacitance supplied for one two-level inverter is $540\,\mu$F.

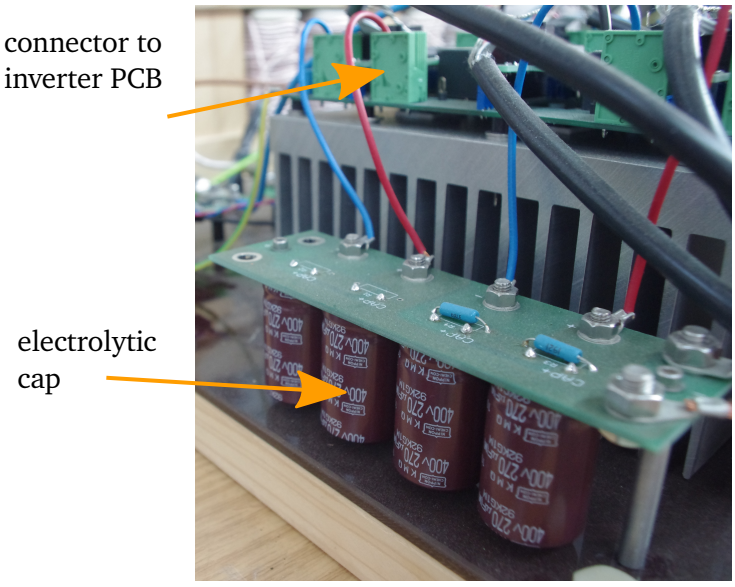


Figure 6.4.: DC-link capacitor banks based on aluminum electrolytic capacitors.

Due to the higher ESL, but also the extra leakage inductance formed by the wiring between the DC-link PCB

and inverter PCB, only the lower spectral components of the DC-link capacitor current will flow through the electrolytic capacitors. Altogether, the setup represents a hybrid DC-link implementation as mentioned in Section 3.1.3. In order to find optimality for this hardware setup, the precise knowledge of

- the DC-source's characteristics,
- demands for DC-link voltage ripple and losses, as well as the DC-link's parasitic ESL and ESR,
- acceptable over-voltage during transistor turn-off,
- and budget by means of cost and volume

has to be provided. With respect to this thesis, the hardware design was not optimized, but instead simply fulfills the prerequisite of stable inverter voltage supply as well as low over-voltages during machine demagnetization (electrolytic capacitor bank) and transistor turn-off (foil-caps).

DC-source
The utilized DC-source for providing the requested voltage to the DC-link is based on a device of *REGATRON*'s series *TopCon TC.GSS*. The power supply's topology provides up to $1500\,\mathrm{V}$ at $32\,\mathrm{kW}$, bidirectionality and can be configured remotely (e.g. controlled output voltage level and current limits, warning or error levels with automatic shut-off).

Interleaving chokes
The core of the interleaving chokes is based on two inversely stacked U-cores, each having an effective cross-section of $A_{\mathrm{eff}} = 840\,\mathrm{mm}^2$ and an effective length of $l_{\mathrm{eff}} = 354\,\mathrm{mm}$. The chosen core material is referred to as *Mf 102* by the manufacturer *TRIDELTA Weichferrite*, which is characterized as low-loss ferrite for use-cases with up to $500\,\mathrm{kHz}$, and it allows flux densities of up to $B_{\mathrm{sat}} = 320\,\mathrm{mT}$. The parameters of the Steinmetz Equation can be extracted from the datasheet by logarithmic transformation and curve fitting, and are determined to be $k = 0.0023, a = 1.34, b = 2.20$ for $25\,^{\circ}\mathrm{C}$ [92]. Together with the relative permeability of $\mu_{\mathrm{r}}' = 2000$, the parameters yield a magnetic resistance for the two stacked cores of $R_{\mathrm{m,core}} \approx 185\,\mathrm{kH}^{-1}$. In terms of number of turns N per winding, the resulting inductance is $M_{12} \approx 5400\,\mathrm{nH}/N^2$ and $i_{\mathrm{sat}} \approx 107\,\mathrm{A}/N$. Choosing $N = 31$ and adding an air gap that approximately increases the overall magnetic resistance fourfold, the inductance and saturation current attain values of $M_{12} \approx 1.2\,\mathrm{mH}$ and $i_{\mathrm{sat}} \approx 7\,\mathrm{A}$. In accordance with Eq. (4.23), the implemented controller saturation limit is $i_{\mathrm{sat,c}} \approx 1/2 \cdot i_{\mathrm{sat}}$, i.e. the regularly appearing flux density in the coil is also only $B = 1/2 \cdot B_{\mathrm{sat}} \approx 160\,\mathrm{mT}$. In other words, the full magnetization potential of the choke will not be used, which however is beneficial with respect to the appearing magnetization losses.

The stacked cores are held together by a wooden frame. The interleaving chokes' windings are placed on a 3d-printed winding body and are realized with high-frequency litz wire. The winding technique is implemented simply as sectional on each core leg, since leakage minimization as it could be acquired by bifilar windings is not strictly necessary for optimized performance (cp. Section 2.2).

Measurement instrumentation
The rotational speed of the machine is measured by an incremental encoder with 2000 cycles per revolution. Being passed through a galvanically isolating level shifter, the logic signals are read in by the computational platform. Since all of the hardware test runs are performed under quasi-stationary speed conditions, a second-order lowpass with a rather low time constant of $\tau_{\omega} = 2\,\mathrm{ms}$ is implemented as signal conditioning before passing over the value to the control algorithm.

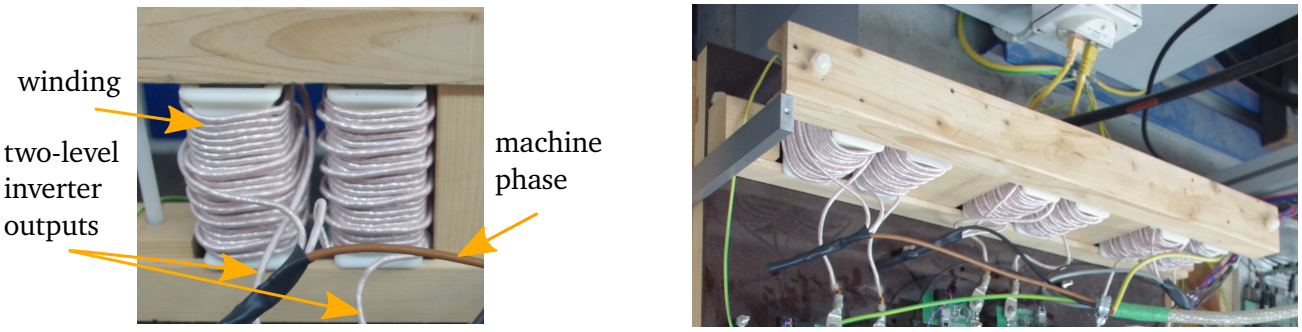


Figure 6.5.: Implemented interleaving chokes for one phase (left) and all phases (right).

The DC-link voltage V_{dc} is measured by breaking down the voltage at the electrolytic capacitor bank via a high-impedance voltage divider, which feeds an ADC that is implemented as a $20\,\mathrm{MHz}$, 16-bit second-order Delta-sigma modulator ($\Delta\Sigma$ modulator) of type *AD7403* by *Analog Devices*. One beneficial property of this $\Delta\Sigma$ modulator is that the digitilized data can be transferred as bitstream, generally allowing a 1-bit data path. Arriving at the actual control platform, the bitstream can then be conditioned according to a trade-off between bandwidth and accuracy. Specifically, the conditioning is performed via a Sinc3 lowpass filter with a decimation ratio of 512 and a -3 dB filter response of $10.2\,\mathrm{kHz}$, which provides sufficiently dynamic tracking of any source-related harmonics being superimposed on V_{dc}. The throughput rate of the filter is $39.1\,\mathrm{kHz}$. All of these values can be derived by basic formulas for the Sinc3 filter provided in [93].

The current sensors are implemented as $4\,\mathrm{m\Omega}$ shunts that are placed at each respective halfbridge output terminal. The voltage drop is sampled by the $20\,\mathrm{MHz}$ self-clocking, Manchester coded $\Delta\Sigma$ modulator *AMC1303E2520* by *Texas Instruments*. Due to the Manchester coding, this realization allows single-wire data with simultaneous clock transfer. This single-wire property also makes fiber optic transmissions feasible, which usually imply elevated spatial requirements and high component costs. Nevertheless, mismatches of the clocking between the computational platform and the $\Delta\Sigma$ modulator can appear. It therefore is necessary to implement an oversampling feature for reading in the Manchester coded bitstream data. This ensures the prevention of significant errors for the clock and data signal extraction (cp. Chapter 5). For this hardware setup, the Machester code is sampled with $160\,\mathrm{MHz}$. The data is then conditioned with a Sinc3 lowpass filter with a decimation ratio of 40, a -3 dB filter response of $131\,\mathrm{kHz}$ and a throughput rate of $500\,\mathrm{kHz}$. The settle time of the filter can be determined to $3/500\,\mathrm{kHz} = 6\,\mu\mathrm{s} = {}^{3}\!/_{5} \cdot T_{\mathrm{s,c}}$, which is being compensated by the control algorithm (cp. Section 5.2).

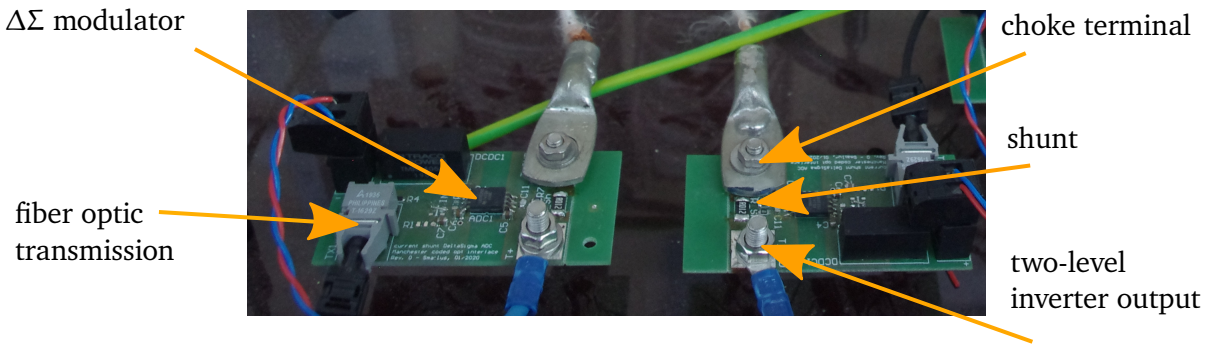


Figure 6.6.: Current measurement PCBs for one paralleled halfbridge (here: $i_{1,\mathrm{a}}$ and $i_{2,\mathrm{a}}$).

Control platform
The control platform is placed in an aluminum rack. A back plane realizes the physical connection of several measurement and adapter cards towards the actual computational platform (*Zedboard*), as hinted at in Figure 6.7.

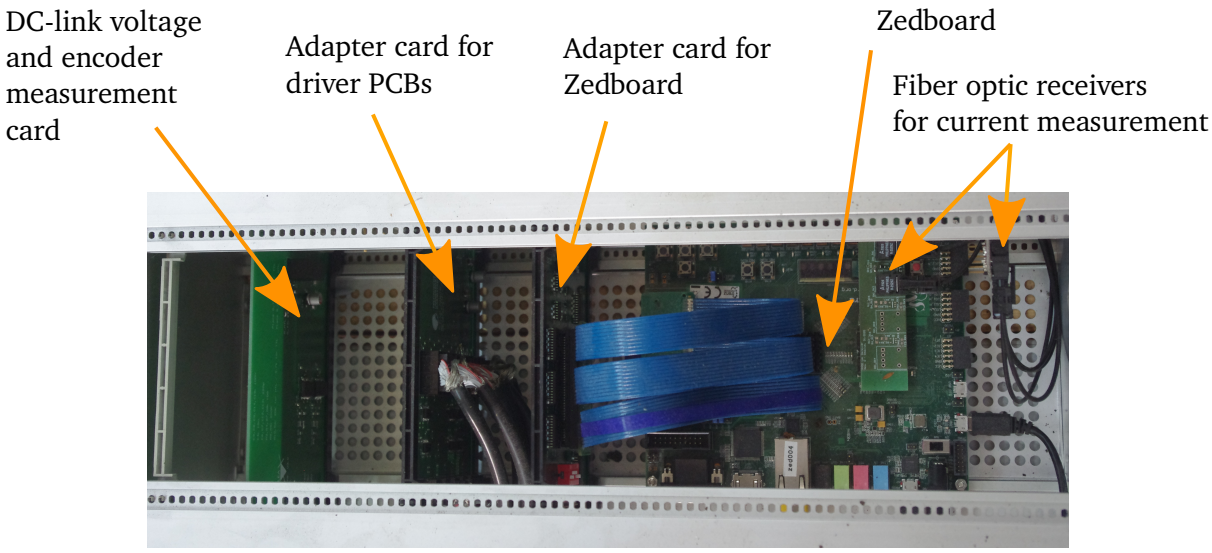


Figure 6.7.: Control rack containing measurement cards, adapter cards and the control platform *Zedboard*.

The configurable logic on the *Zedboard*'s SoC *Zynq Z-7020* (cp. Chapter 5) implements the real-time signal conditioning and the FCS-MPC control algorithm. The hard processor system of the *Zynq Z-7020*, which is *ARM Cortex-A9* based, runs a Linux operating systems and handles data transfer between the *Zedboard* and the host computer via Ethernet. By these measures, a *Simulink* interface model running on the host computer allows to transmit weighting factors, reference values etc. during inverter and machine operation. Likewise, captured measurement and controller data can be received and visualized on the host computer. The configuration of the Linux operating system as well as the general interface software architecture is provided by according support packages that are available for *MATLAB*.

6.2. Experimental Evaluation

The experimental evaluation in this section focuses on two specific operational points (OPs), namely no-load operation and nominal operating conditions of the induction machine. Due to the time consuming acquisition of experimental data, the supplementary OPs presented in Appendix C are mostly omitted in the experimental evaluation. The evaluated control objectives are the average switching frequency f_{sw}, the machine's TDDs for T_{e} and i_{s}, the DC-link capacitor current $i_{\mathrm{dc,cap,rms}}$, avoidance of large voltage steps at the machine terminals, and lastly also minimization of common-mode voltage. Unless noted otherwise, these quantities are captured by the measurement instrumentation of the control platform. For example, for this reason the TDD of the electromagnetic torque is based on the estimated torque instead of a mechanical sensor. Lastly, an experimental tracking of the inverter losses is not performed due to the lack of power meters with enough channels of sufficiently high bandwidth at the Institute for Power Electronics and Control of Drives.

With respect to the FCS-MPC realization, the aspired performance measures require the general implementation as well as tunability for the partial cost terms $J_{\mathrm{T},2}$, $J_{\Psi,2}$, J_{sw}. In case of interleaved operation, the cost terms J_{sat} and J_{magmode} are additionally activated. Moreover, the cost term $J_{\mathrm{sw,ovv1}}$ is always active for both, interleaved and regular (two-level) operation. Similarly as for Chapter 4, the composition of cost terms for the respective runs is summarized in Table B.5.

6.2.1. Basic Machine Control

Before the above mentioned performance measures are investigated in more detail, the basic functioning of the real-time implementation for the FCS-MPC is to be inspected first.

Stator currents and electromagnetic torque
For this purpose, the inverter currents $i_{1,\mathrm{ph}}, i_{2,\mathrm{ph}}$, the machine's phase currents $i_{\mathrm{s,ph}}$ and the (estimated) electromagnetic torque T_{e} are depicted in Figure 6.8. The machine is being operated under nominal conditions and with regular or interleaved inverter operation, respectively.

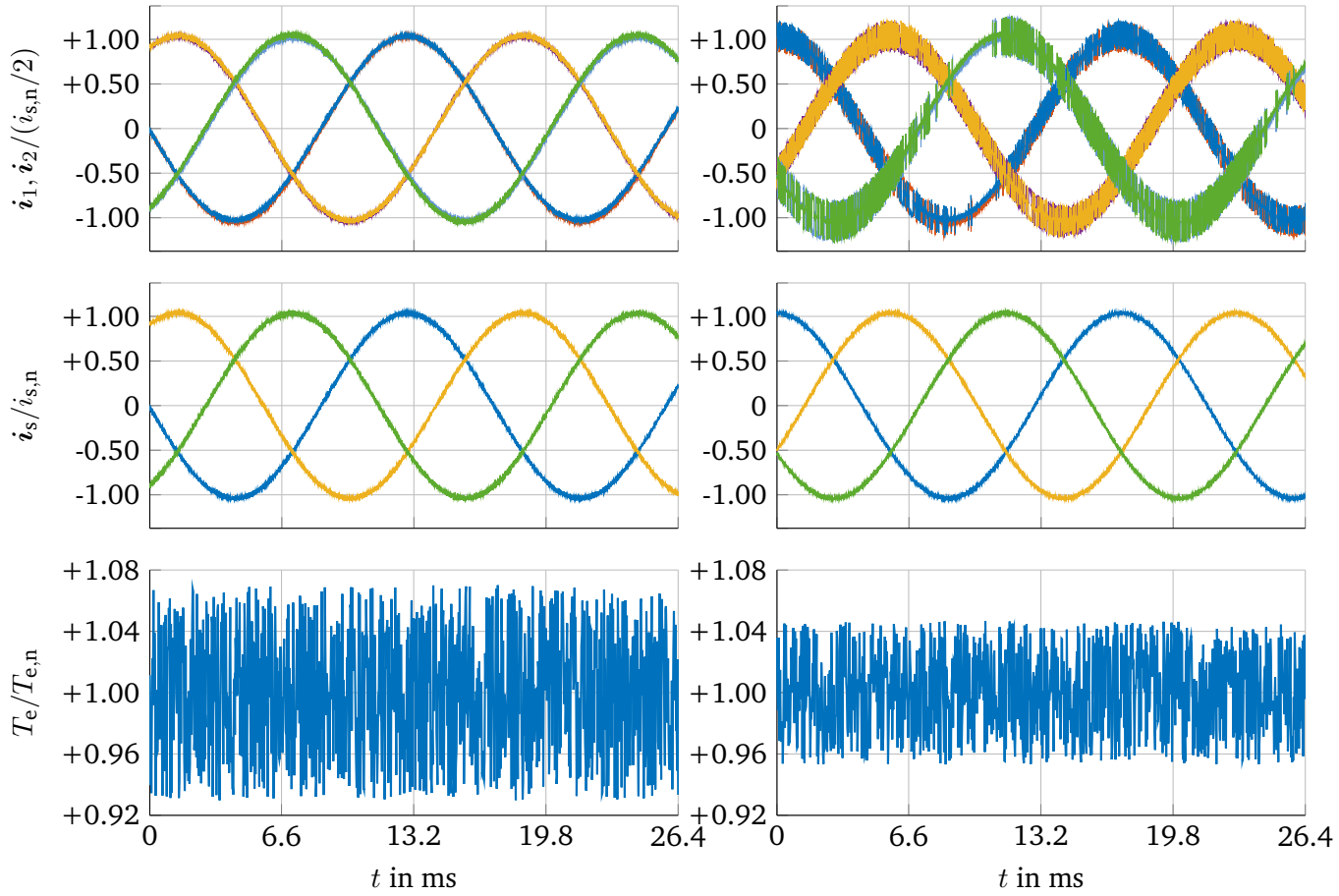


Figure 6.8.: Hardware evaluation of basic functioning for the regular two-level inverter operation (left) and for activated interleaving with choke magnetization in Mode 1 (right) at rated machine operation.

As it can be seen, the machine's stator currents mainly contain the fundamental frequency required for the torque and flux reference, albeit there obviously are distortions appearing as current ripple of high frequency.

Harmonics of lower order, which can potentially be induced by spatial harmonics within the machine[1], are being successfully compensated by the high dynamics of the FCS-MPC. Furthermore, during interleaved operation the inverter currents are kept in the pattern governed by J_{magmode} and the corresponding finite state machine.

Trade-off between torque and stator current TDD

Moreover, Figure 6.9 exemplarily displays the TDD of T_e and i_s at nominal machine operation and activated interleaving over the torque weighting $\lambda_{\text{T},2}$. The results support the validity of the proposed $\lambda_{\text{T},2}$-tuning for the implemented FCS-MPC style, namely MMPTFC (cp. Section 4.2.2).

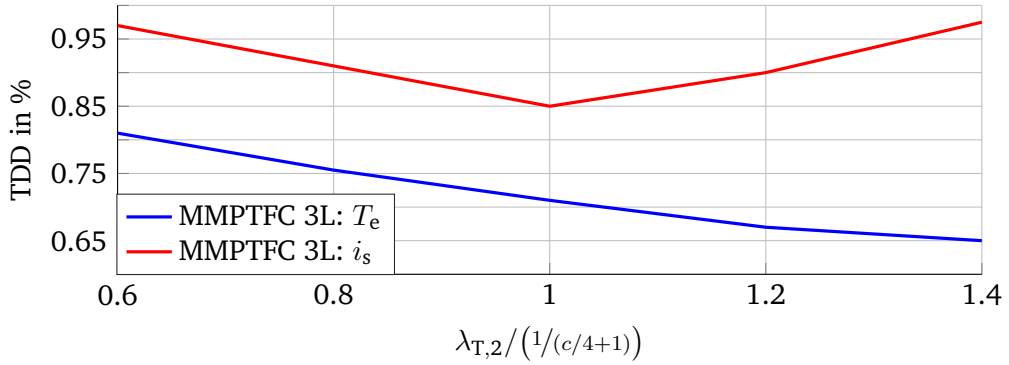


Figure 6.9.: Hardware evaluation of performance for torque and stator current TDD minimization for different $\lambda_{\text{T},2}$-tunings with activated interleaving and at nominal machine operation.

Trade-off between machine TDDs and average switching frequency

Lastly and in analogy to Figure 4.18, the hardware results of TDD minimization over the average switching frequency are depicted in Figure 6.10.

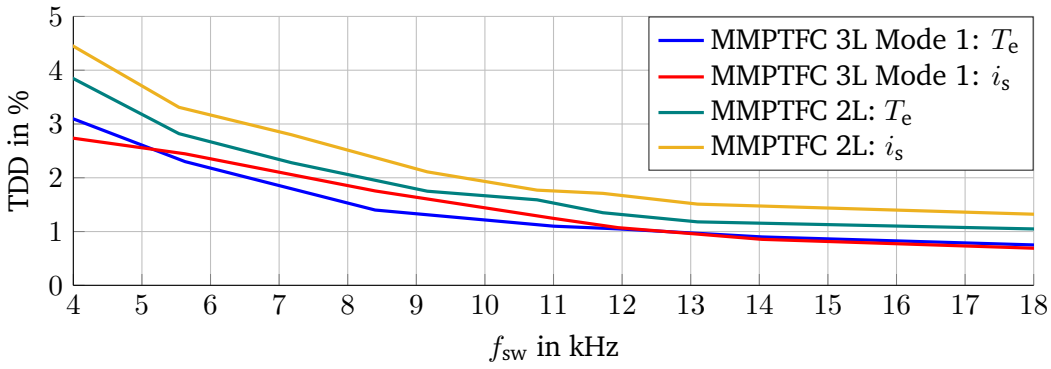


Figure 6.10.: Hardware evaluation of performance for torque and stator current TDD minimization vs. average switching frequency at nominal machine operation. Comparing the MMPTFC principle for the regular two-level inverter with the interleaved inverter system with choke magnetization in Mode 1.

The measurements are attained for a sweep with respect to the weighting factor λ_sw for regular and interleaved inverter operation. As for the most parts of Chapter 4, the torque tuning is set to optimal stator current TDD,

[1] Specifically: Harmonic stator currents induced by rotor field harmonics (cp. Section 3.2.2).

i.e. $\lambda_{\mathrm{T},2} = 1/(4c+1)$. Overall, the hardware results show consistency with the simulation results: When compared to regular inverter operation, the interleaving allows lowered TDD at identical average switching frequencies. The performance boost of activated interleaving is however slightly less than anticipated from the simulation results[2]. The machine TDDs fall monotonically for increasing f_{sw}, albeit with larger errors towards respective curve-fitted rational functions. Obviously, the latter can be explained with occurring parameter mismatches, as well as measurement noise and unmodeled non-linearities of the real plant, such as switching transients, on-state voltage drops at the inverter etc.

Supplementary hardware measurements are provided in Appendix D.1.

6.2.2. Advanced Control Aims

The advanced control aims investigated for the hardware setup are the optimization of the DC-link capacitor current, the inverter operation free of common-mode voltage and avoidance of large voltage steps at the machine terminals.

Minimization of losses appearing in the DC-link
The optimization potential of the DC-link capacitor current $i_{\mathrm{dc,cap,rms}}$ is evaluated via of sweep of λ_{cap} with deactivated penalization of switching activity. The hardware results are given in Figure 6.11 for rated machine operation. The anticipated, large reduction of $i_{\mathrm{dc,cap,rms}}$ without considerable impairment of machine TDD, as suggested by the simulation results, can be verified. Moreover, the transition point of sudden TDD increase for further DC-link optimization can be confirmed (cp. Figure 4.31). The hardware results also support the tendency of increasing average switching frequency for lowered DC-link capacitor currents. Lastly and in accordance to the insights of Section 6.2.1 and Figure 6.10, the acquired machine TDD of the hardware measurements is generally higher when compared to the simulation outputs.

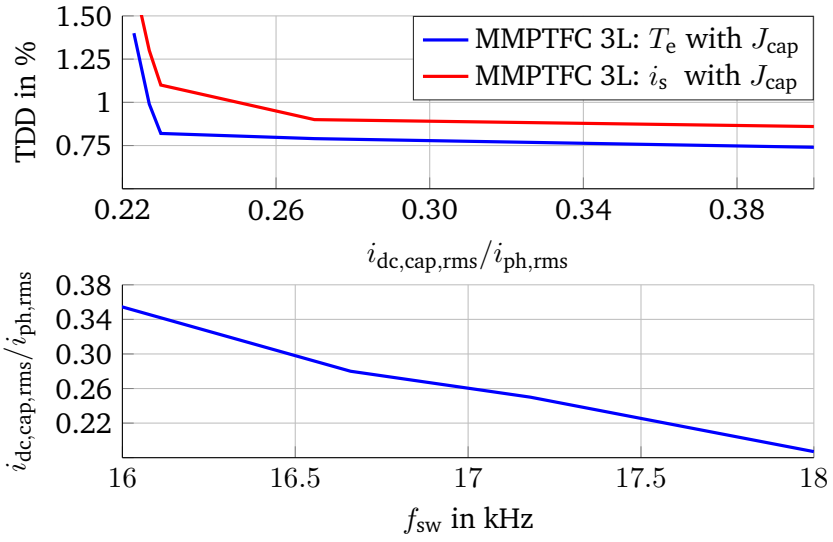


Figure 6.11.: Hardware evaluation of performance for torque and stator current TDD minimization vs. rms-value of capacitor current (top) and rms-value of capacitor current vs. average switching frequency (bottom) at rated machine operation.

[2]A possible reason for this is identified and discussed in Section 6.2.3.

Minimization of common-mode voltage

The minimization of common-mode voltage reaching the machine terminals is implemented as described in Section 4.3.5. The respective weighting factor is set to $\lambda_{\mathrm{cm}} = \lambda_{\mathrm{sat},1}/10$, which is designed for a complete avoidance of any space vectors that imply non-zero common-mode voltages for the machine's stator voltage $\boldsymbol{v}_{\mathrm{s}}$. The hardware measurements are presented in Figure 6.12. The hardware measurements generally support the simulation results for the common-mode free operation, i.e. higher average switching frequencies for activated λ_{cm}, albeit again with an overall poorer TDD performance.

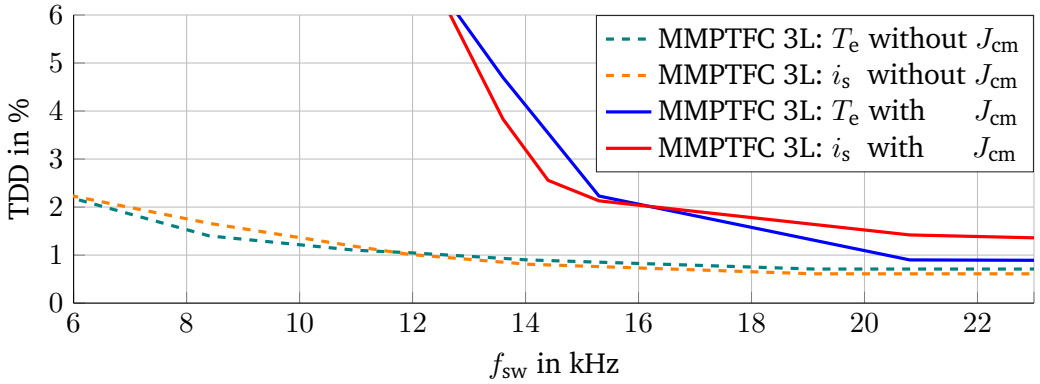


Figure 6.12.: Hardware evaluation of performance for respective torque and stator current TDD minimization vs. average switching frequency for zero-voltage common-mode space vectors at rated machine operation.

In order to verify that the applied voltage space vectors are indeed common-mode free with respect to $\boldsymbol{v}_{\mathrm{s}}$, differential probes are used to track the voltage output of each half bridge. The according scope data is provided in Figure 6.14. Note that the calculation of the overall common-mode voltage for the stator voltage $v_{\mathrm{s,cm}}$, which is given in Figure 6.13, is performed in analogy to Eq. (4.29). It neglects any effects at the interleaving chokes, cables etc. and therefore is only a rough estimate of the common-mode voltage reaching the machine terminals. Nevertheless, the proper functioning of the activated cost term J_{cm} can be validated.

Figure 6.13 further reveals that the resulting common-mode voltage includes short pulses that lead to deviations from $v_{\mathrm{s,cm}} = 0$. These pulses are related to the non-ideal switching behavior of the MOSFETs, explicitly varying fall / rise times and voltage overshoots, as well as the implemented dead-time.

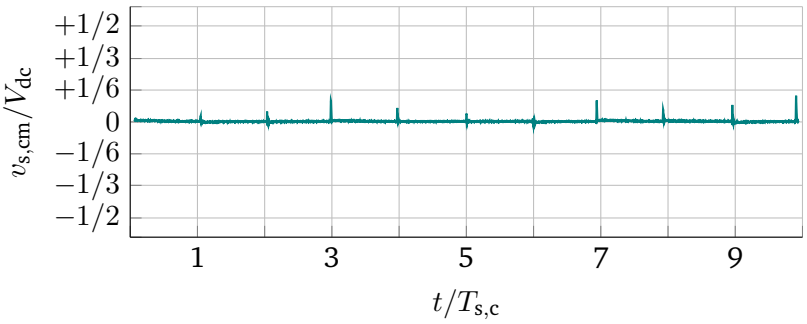


Figure 6.13.: Hardware evaluation of common-mode voltage time characteristics for activated J_{cm} at rated machine operation.

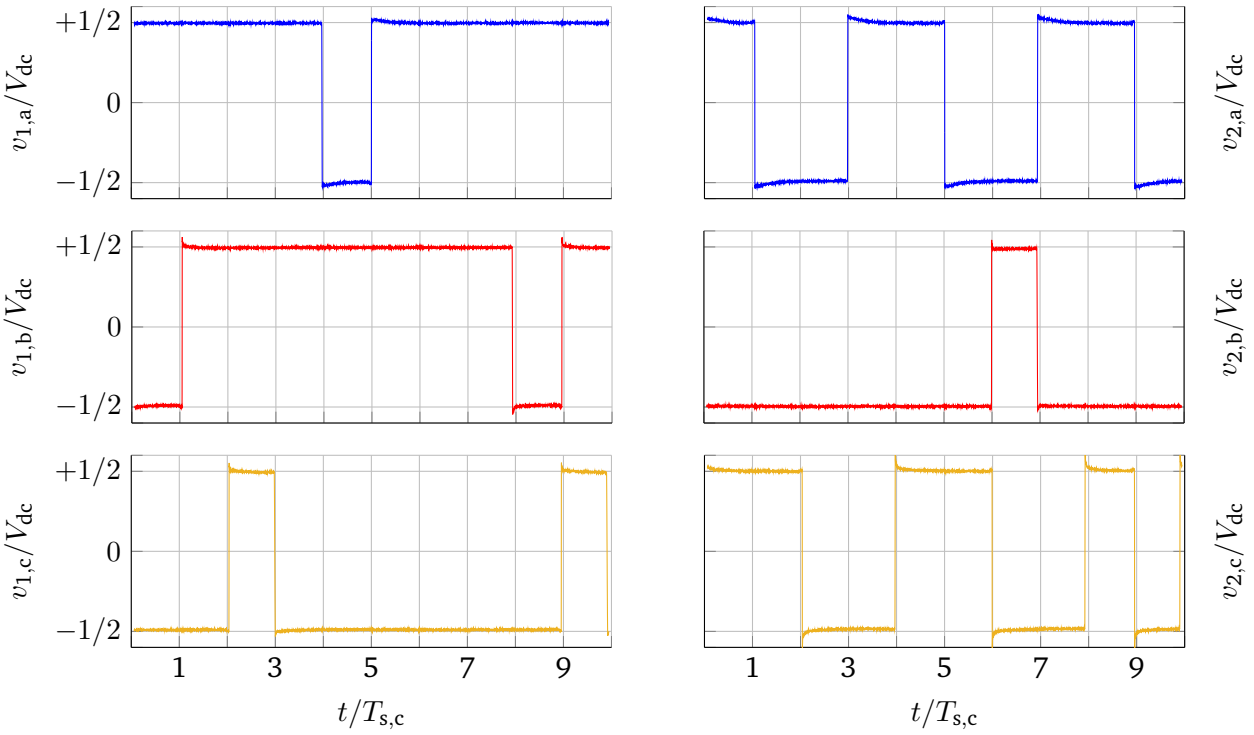


Figure 6.14.: Hardware evaluation of individual voltage time characteristics for activated J_{cm} at rated machine operation.

Supplementary hardware measurements are provided in Appendix D.2.

Avoidance of large voltage steps at the machine terminals

As proposed in Section 4.3.4, the cost term $J_{sw,dv/dt}$ can be activated to avoid large voltage steps at the machine terminals. The presumption of a low impact on the TDD minimization over average switching, as anticipated by simulation, can be confirmed by the hardware runs as given in Figure 6.15.

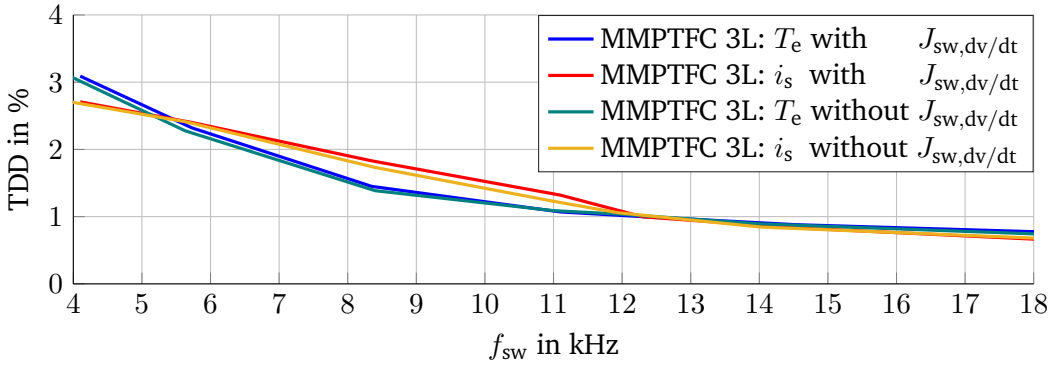


Figure 6.15.: Hardware evaluation of performance for respective torque and stator current TDD minimization vs. average switching frequency for restraining transient phase-to-phase $^{dv}/_{dt}$ at rated machine operation.

6.2.3. Discussion on Deviations between Hardware and Simulation Results

While the hardware measurements for the regular, i.e. two-level inverter operation are in very good accordance with the simulation results[3], the hardware evaluation shows noticeably larger machine TDDs for the interleaved operation than originally anticipated by simulation. The following list supplies possible reasons for the observed deviations and includes arguments for their plausibility, as well as feasible or realized countermeasures.

- Parameter mismatch: The mismatch of parameters between plant model and actual plant can be a significant source of deviations. Nonetheless, the hardware measurements generally imply a low mismatch / unmatched parameters for the interleaved inverter (cp. Figure 4.39 and Figure 6.8). With respect to the induction machine, most parameter mismatches rather entail an offset, i.e. DC-error of the controlled quantity (cp. e.g. Figure 4.39). However, the agreement between simulation and hardware results cannot be increased significantly if DC-offsets are excluded for the TDD evaluation.

  An exception of the above mentioned is the leakage inductance of the induction machine, which is the dominating parameter for limiting the TDDs related to switching frequency or high order harmonics (cp. Eq. (3.63)). However, if the deviations between hardware and simulation results relate to this issue, the corresponding errors should not be concentrated solely on the interleaved operation, which makes this reason less plausible.

- Unmodeled non-linearities of inverter, chokes and induction machine: Temperature dependencies can usually be interpreted as parameter mismatch due to comparably large time constants. Nevertheless, there also are other plant non-linearities which have to implemented as such, if a greater model accuracy is aspired. Concisely, non-linearities remaining unmodeled are found at the inverter (dead-time, switching transients), at the machine (spatial harmonics) and the chokes (wiring). Further, possible dependencies of frequency for the parameters, e.g. the Skin effect, is neglected. However, similarly as it is the case for parameter mismatches, the plausibility of these effects explaining the deviations solely for interleaved operation is reduced, as they should affect the regular operation to a similar extent, if the remaining operating conditions are conserved.

- Inaccurate compensation of time delays: The true time delay of measurement signals reaching the computational platform cannot be captured easily, and can therefore deviate from the simulated time delay as well as the deployed time compensation.

  In order to evaluate the possible impacts, the $\Delta\Sigma$ modulator ADCs including their respective filters can be modeled and included in the simulation [4]. However, there is no significant difference occurring in the simulation after alteration, making this possible error a less plausible explanation between the hardware and simulation results. Furthermore, an artificial increase or decrease of several µs does not crucially alter the simulation results, including the aspect of rapidly changing leg currents during interleaved operation.

- EMI-induced measurement noise: Although the ADCs' quantization noise is taken into account within the performed simulations by considering the respective ENOB, unmodeled measurement noise can yet exist due to parasitic coupling or electromagnetic interference (EMI). In order to avoid the strongest

[3] Cp. e.g. Figure 6.10 and Figure 4.18.

[4] The simulations in Chapter 4 are instead merely performed with a corresponding transfer function and decrease of accuracy by the corresponding effective number of bits (ENOB) produced by the respectively implemented filter.

interferences, it usually is advised to include a time offset between the measurement sampling time instant and the switching instant. This is linked to the strong $^{\mathrm{d}i}/_{\mathrm{d}t}$-effects during the commutation process. An appropriate delay indeed is implemented (and compensated) in the hardware implementation, but this however does not rule out the interferences completely. Particularly during interleaving, comparably high values of $|^{\mathrm{d}i}/_{\mathrm{d}t}|$ can occur, albeit substantially lower than those during commutation.

Nevertheless, noisy measurement signals can be a plausible reason for the attenuated performance boost during interleaving operation: The finer granularity of voltage space vectors for the interleaved, i.e. three-level operation (cp. e.g. Figure A.1) can only be utilized if the feedback's noise of the controller, particularly the measured currents, has a lower standard deviation than the difference that is implied by the variation of voltage space vectors for the upcoming controller time steps.

- Insufficient handling of common-mode rejection for current measurements: A plausible reason for the lowered TDD performance during interleaving operation are interferences with the current measurements due to common-mode voltages. As can be seen in Figure 6.6, which is provided below again for convenience, the measurement PCBs for a paralleled halfbridge are positioned in a mirrored manner. However, since the PCB design does not include any mirroring, the differential input of the respective ADCs are connected to the according halfbridges with alternating polarity, as shown in Figure 6.17.

  If $v_{1,\mathrm{ph}} = v_{2,\mathrm{ph}}$ holds, as it is the case for regular operation, the common-mode at the ADCs' inputs have opposite potential. Disturbances[5] cancel each other mostly out when calculating the phase current $i_{1,\mathrm{ph}} + i_{2,\mathrm{ph}} = i_{\mathrm{ph}}$. On the other hand, if $v_{1,\mathrm{ph}} \neq v_{2,\mathrm{ph}}$ holds, as it is the case for interleaved operation, the common-mode errors will sum up for i_{ph}. Measurement data supports this theory, as it shows higher current ripples than anticipated when interleaving vectors are applied.

  For this reason, it is strongly advised for future hardware setups to utilize current sensors without relevant sensitivity to common-mode voltage. Alternatively, the placement of current ADCs should be at the output terminals of the choke, i.e. at the terminals toward the machine. The latter will ensure that the disturbing common-mode voltages during interleaving are already rejected mostly by the mutual inductance of the choke.

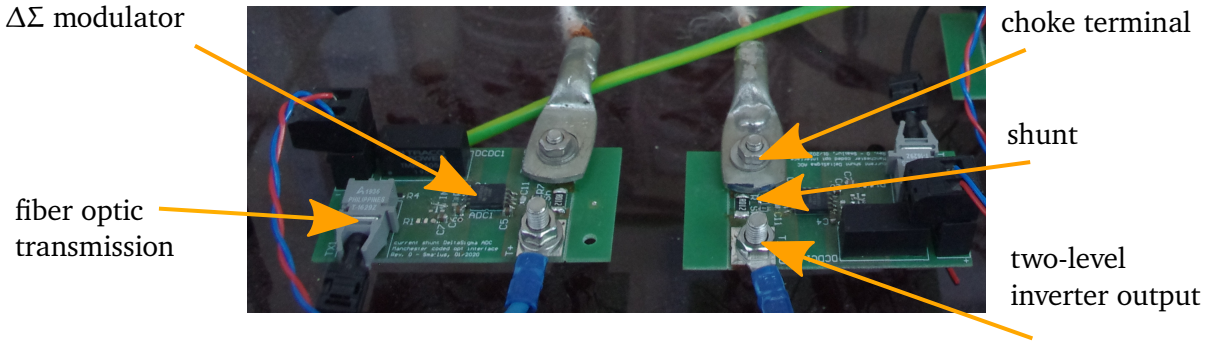


Figure 6.16.: Current measurement PCBs for one paralleled halfbridge.

[5]The disturbances also appear in the sampled signal due to a non-zero common-mode rejection ratio of the ADCs.

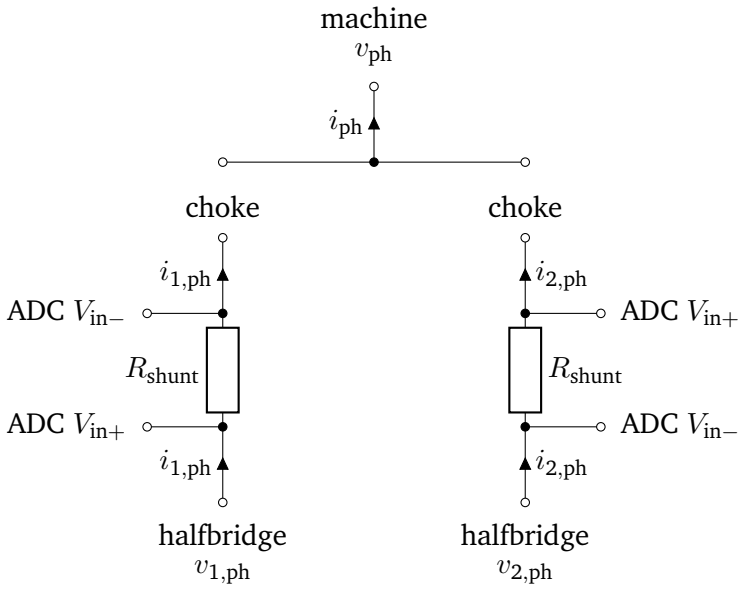


Figure 6.17.: Schematic of current measurement PCBs for one paralleled halfbridge.

6.3. Summarizing Discussion on Acquirable Optimization of Interleaved Topology

Since the actual physical values of the interleaved inverter and the induction machine are introduced in this chapter, it stands to reason to quantify the acquired optimized control in terms of actual loss reduction and improvement in overall system efficiency. Moreover and based on these insights, guidelines for future hardware optimization are discussed.

6.3.1. Quantification of Loss Minimization

For the purpose of quantifying the achieved loss minimization, the general trade-off of the investigated optimization goals is recapitulated in Figure 6.18. The respective vicinity of the nodes represents the degree of exclusion for acquiring the goals simultaneously.

The losses for various optimization tunings are summarized in Table 6.1. The given losses of the inverter are estimated by the proposed model of Section 4.3.6, while the inverter conduction losses are based on a R_{on} of the MOSFETs that is assumed to be constant (cp. Table B.2). The ohmic harmonic losses are determined by the corresponding TDD flowing through the estimated values of R_{s} and R_{r} in the induction machine.[6] The losses in the DC-link's capacitors is calculated by the respective $i_{\text{dc,cap,rms}}$ and the ESR of the electrolytic caps, assuming (arbitrarily) that the main current load appears at this capacitor type due to its much larger capacitance. Lastly, the magnetization losses appearing in the interleaving chokes are evaluated by the occurrences of

[6] In order to take account for the current displacement (or Skin effect) that follows from the high frequency harmonics, the stator and rotor resistance values are adjusted by the factors $\sqrt{f_{\text{sw}}/50\,\text{Hz}}$ and $\sqrt{f_{\text{sw}}/1.25\,\text{Hz}}$, respectively. This method therefore assumes that the acquisition of the resistance values was conducted at nominal machine operation and without any occurrence of harmonics (cp. Section 3.2.4).

hysteresis at respective frequencies (cp. Figure 4.37) and the correction factor following from the MSE, as discussed in Section 4.3.9. Further loss groups are not considered.

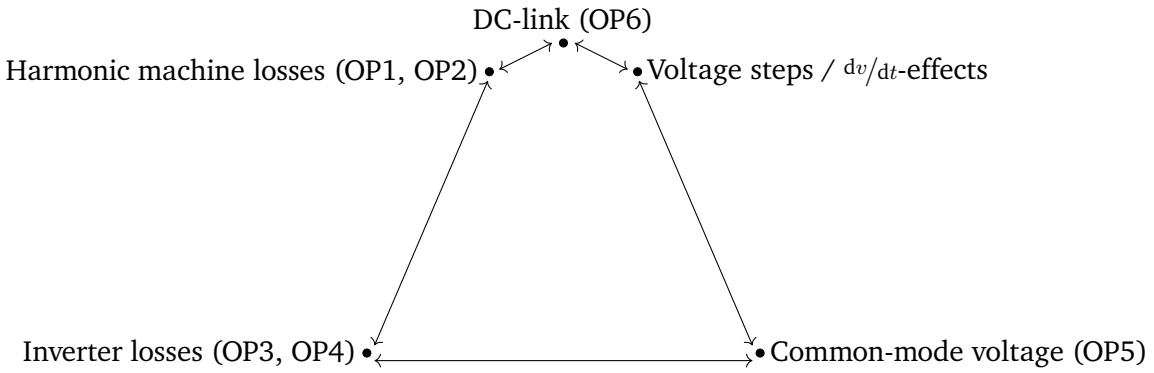


Figure 6.18.: Visualization of trade-off for investigated optimization goals.

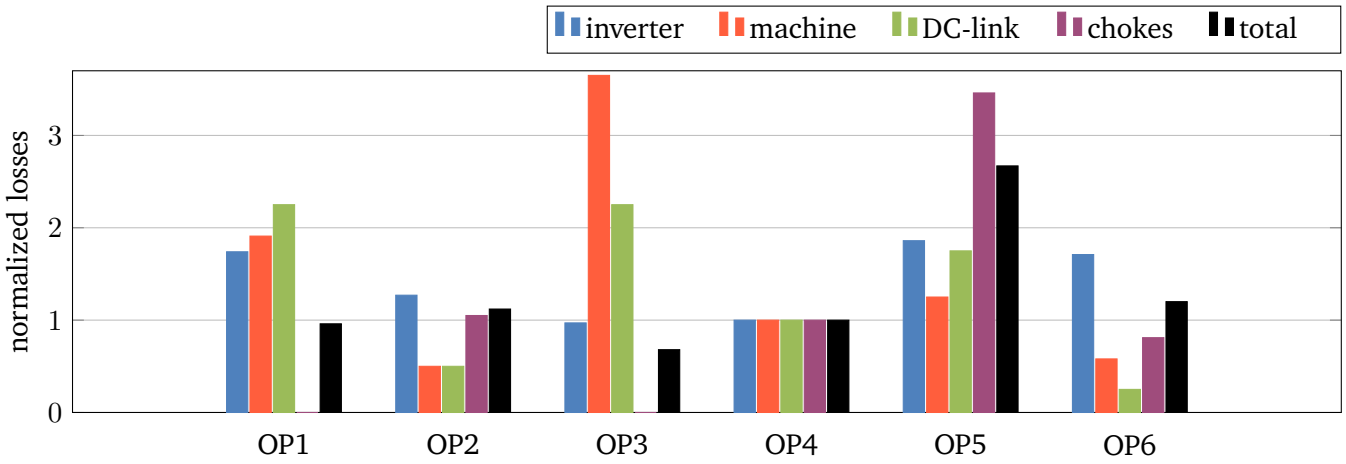


Figure 6.19.: Normalized values of adjustable losses of main components of drive inverter for various configurations / optimization goals. The reference for normalization is OP4.

Table 6.1.: Absolute values for operation points displayed in Figure 6.19.

OP	Optimization goal	tuning as in Figure.. (cp. Table B.3)	inverter $(P_{\mathrm{inv,sw}} + P_{\mathrm{inv,cond}})$	ind. machine (ohm. harmonic)	DC-link	chokes (hyst.)	total losses
1	2L, TDD	4.18, $f_{\mathrm{sw,max}}$	$27.2\,\mathrm{W} + 9.7\,\mathrm{W}$	$4.6\,\mathrm{W}$	$0.9\,\mathrm{W}$	$0.0\,\mathrm{W}$	$42.4\,\mathrm{W}$
2	3L, TDD	4.18, $f_{\mathrm{sw,max}}$	$16.3\,\mathrm{W} + 10.5\,\mathrm{W}$	$1.2\,\mathrm{W}$	$0.2\,\mathrm{W}$	$21.4\,\mathrm{W}$	$49.6\,\mathrm{W}$
3	2L, $P_{\mathrm{inv,sw}}$	4.24, $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$	$10.9\,\mathrm{W} + 9.6\,\mathrm{W}$	$8.7\,\mathrm{W}$	$0.9\,\mathrm{W}$	$0.0\,\mathrm{W}$	$30.1\,\mathrm{W}$
4	3L, $P_{\mathrm{inv,sw}}$	4.24, $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$	$10.5\,\mathrm{W} + 10.6\,\mathrm{W}$	$2.4\,\mathrm{W}$	$0.4\,\mathrm{W}$	$20.4\,\mathrm{W}$	$44.3\,\mathrm{W}$
5	3L, $v_{\mathrm{s,cm}}$	4.23, $\lambda_{\mathrm{cm,max}}$, $f_{\mathrm{sw,max}}$	$29.1\,\mathrm{W} + 10.2\,\mathrm{W}$	$3.4\,\mathrm{W}$	$0.7\,\mathrm{W}$	$74.8\,\mathrm{W}$	$118.2\,\mathrm{W}$
6	3L, $i_{\mathrm{dc,cap,rms}}$	4.31, $\lambda_{\mathrm{cap,opt}}$	$25.0\,\mathrm{W} + 10.1\,\mathrm{W}$	$1.4\,\mathrm{W}$	$0.1\,\mathrm{W}$	$16.5\,\mathrm{W}$	$53.1\,\mathrm{W}$

The main insights of Table 6.1 are summarized in the following:

- The interleaved inverter system can greatly reduce the losses of the inverter, the DC-link and the induction machine in a very balanced way when compared to the regular two-level inverter.
- The total adjustable losses are generally higher for the interleaved inverter than for the two-level inverter due to large magnetization losses in the interleaving chokes. Since the magnetization losses usually increase faster for higher field densities than for larger frequencies (MSE parameters: $a > b$, cp. Section 6.1), a migration from magnetization Mode 1 to Mode 2 alleviates this problem, albeit with the implication of lower TDD performance (cp. Figure 4.19). The relative contribution of the magnetization losses however tends to decrease for machines with higher power rating, i.e. an advantage with respect to the overall system losses is expected for bigger machines (cp. Section 6.3.2). Alternatively, adaptions of the choke design also give the prospect of improved efficiency.
- Although the relative loss reduction of machine harmonics and the DC-link is substantial, the absolute loss reduction is only minor. This is due to the generally rather high switching frequency und comparably low ESR of capacitors. Nevertheless, the TDD reduction should not only be considered as way for minimizing harmonic losses, but also as a gain with respect to control quality. Further, particularly the loss reduction in the DC-link brings upon another profound advantage, which is discussed in Section 6.3.2.
- The common-mode free control leads to very high switching and magnetization losses in the choke, which is owing to the permanent usage of interleaving vectors in all three phases.

6.3.2. Guidelines on Hardware Optimization

In this thesis, the hardware setup is designed for model verification and proof of concept for the developed control algorithm, as performed in Section 6.2.1 and Section 6.2.2. The hardware design itself is therefore by no means optimized. Nevertheless, the insights gained during this thesis allow the development of guidelines for the hardware design, which are shortly proposed in this section. Due to the challenging demand of necessary computational effort for prediction horizons of $N_\mathrm{p} > 1$, the guidelines are based on the assumption of a single-step predicting FCS-MPC.

Guidelines for interleaving choke
The choice of the mutual inductance of the interleaving choke M_{12} is based on several parameters. First it should be defined which average switching frequency $f_{\mathrm{sw,n}}$ is aspired. The necessary sampling frequency for the FCS-MPC can then by evaluated by the rule of thumb $f_{\mathrm{c,s}} = 10 f_{\mathrm{sw,n}}$. This ensures a good performance of the interleaved system for $f_{\mathrm{sw}} \in [1/2 \cdot f_{\mathrm{sw,n}}, 3/2 \cdot f_{\mathrm{sw,n}}]$ (cp. Figure 4.18 and Figure 4.43). Next, the maximum value for the DC-link voltage has to be defined at which the interleaving capability should still be acquirable. The product of the controller's programmed saturation limit $i_{\mathrm{sat,c}}$ and mutual inductance M_{12} can then be defined via $i_{\mathrm{sat,c}} \cdot M_{12} = k_{\mathrm{safety}} \cdot V_{\mathrm{dc}}/2 \cdot T_{\mathrm{s,c}}$, where k_{safety} is an arbitrary safety margin. This equality ensures that a magnetization pattern of Mode 1 is possible (cp. Figure 4.16).

In order to determine a design rule for M_{12}, a value for $i_{\mathrm{sat,c}}$ has to be found. In this thesis, the controller saturation limit was set to $i_{\mathrm{sat,c}} \approx 1/4 \cdot i_{\mathrm{ph,n}}$. Firstly, this particular limitation has the advantage that the conduction losses due to asymmetrical current loading during interleaving are hardly increased when compared to the symmetrical case, as shown in Figure 4.25 and supported by Table 6.1. Secondly, the combination

of $i_{\text{sat,c}} \approx 1/4 \cdot i_{\text{ph,n}}$ and $i_{\text{sat,c}} \cdot M_{12} = k_{\text{safety}} \cdot V_{\text{dc}}/2 \cdot T_{\text{s,c}}$ ensures sawtooth shapes of certain amplitudes for $i_{\text{dc,cap}}$ that are beneficial for the DC-link optimization (cp. Figure 4.34). Although larger values of M_{12} and accordingly lower values of $i_{\text{sat,c}}$ may be used to attain comparable performance (cp. Figure 4.35), a small interleaving inductance does indeed weaken the optimization potential of $i_{\text{dc,cap}}$ and therefore should be avoided. The anticipated magnetization losses of the chokes, as well as the implications on the necessary accuracy for current measurements should eventually be considered for the exact choice of $i_{\text{sat,c}}$, M_{12}.

It is noteworthy that the above described examples for $i_{\text{sat,c}}, M_{12}$ lead to the suggestion to design the choke according to $1/2 \cdot i_{\text{ph,n}} \cdot M_{12} \approx V_{\text{dc}} \cdot T_{\text{s,c}}$. Assuming that the power of an arbitrary load scales proportional to V_{dc} and $i_{\text{ph,n}}$, the proportionality $i_{\text{ph,n}}^2 \cdot M_{12} \sim i_{\text{ph,n}} \cdot V_{\text{dc}}$ can be derived. In other words, the nominal magnetic energy stored in the interleaving chokes should be scaled with the nominal power of the anticipated load. This is in fact a very beneficial situation for loads of higher power than the one investigated in this thesis, as the energy storage of chokes can usually be increased easily by modifying the magnetic resistance via an enlarged air gap. Consider the following two examples:

- Nominal power of load doubles due to higher phase currents: The saturation limit should also double according to $i_{\text{sat,c}} \approx 1/4 \cdot i_{\text{ph,n}}$, while M_{12} can be halved due to $i_{\text{ph,n}}^2 \cdot M_{12} \sim i_{\text{ph,n}} \cdot V_{\text{dc}}$. The chokes of this thesis could still be utilized, with the only difference of a larger air gap that doubles the magnetic resistance.

- Nominal power of load doubles due to higher stator voltage: While $i_{\text{sat,c}}$ remains unaltered, the choke inductance should be doubled according to $i_{\text{ph,n}}^2 \cdot M_{12} \sim i_{\text{ph,n}} \cdot V_{\text{dc}}$. In this case, the number of turns per winding could be doubled (initially quadrupling the inductance and halving $i_{\text{sat,c}}$) and the air gap then increased by the factor 2 (eventually doubling M_{12} and maintaining $i_{\text{sat,c}}$).

In both described cases for loads of higher power, the magnetization losses can be kept constant due to the possibility of maintaining both, the volume of active core material and the regularly appearing flux density within the chokes. Hence, the ratio of magnetization losses towards the overall adjustable losses (cp. Table 6.1) can be reduced substantially for bigger loads. However, since an increased number of turns per winding will also increase conduction losses, the benefit is much more profound for higher rated loads if the increase is based on larger currents. For this reason, the interleaved inverter is very well suitable for high-current or low-voltage machines that require an enhanced TDD characteristic.

Guidelines for DC-link capacitor bank

As it was shown in Section 4.3.8, the rms-value of the capacitor current can strongly be reduced when utilizing the interleaving capability of the inverter, and this reduction can even be enhanced considerably by implementing respective cost functions such as J_{cap}. This leads to a strong decrease of relative losses appearing in the DC-link capacitor bank, which however in absolute values has rather subtle impacts on the overall losses of the drive system (cp. Table 6.1). Nonetheless, losses in the DC-link can still be crucial to minimize, since capacitor current and loss ratings are generally rather low, and less power dissipation can significantly increase the expected lifetime of the devices. For this reason, it can be the case that the DC-link capacitor bank has to be enlarged not necessarily due to the demand of higher capacitance, but to meet the current rating or temperature constraints.

Firstly, in order to design the buffering capacitors at the halfbridges that aim at limiting voltage overshoots during transistor turn-off, the respective capacitors should be large enough to hold the DC-link voltage at a nearly constant level during the switching transients, which then ensures a feeding of the transients solely by these dedicated capacitors. The fall time t_{f} of the incorporated MOSFETs approximately shows a product

equality with the drain-source current i_{ds}, leading[7] to $C \cdot \Delta U \approx \int_0^{t_\text{f}} i_{\text{ds}} \text{d}t = 100\,\text{A ns} = 100\,\text{nF V}$ for a linearly falling current. Hence, regarding the setup of this thesis, a quasi-negligible voltage drop of $1\,\text{V}$ can already be reached with about $100\,\text{nF}$ per halfbridge.

The second crucial aspect for the DC-link design is the ripple related to the switching frequency, which is also the ripple that is strongly linked to $i_{\text{dc,cap,rms}}$. As an estimate, this ripple can be evaluated by $v_{\text{dc,ripple,rms}} = i_{\text{dc,cap,rms}}/(2\pi f_{\text{sw}} \cdot C_{\text{dc}})$, where f_{sw} is the average switching frequency for the respective load operation point and controller tuning. Allowing a voltage ripple of $v_{\text{dc,ripple,rms}} = 0.01 \cdot V_{\text{dc}} = 8\,\text{V}$ for the setup of this thesis,[8] the two-level operation of the inverter with minimizing TDD tuning requires a $4.7\,\mu\text{F}$ capacitor bank for nominal machine operation, while the interleaved operation with optimized $i_{\text{dc,cap,rms}}$ would meet the defined voltage ripple already at $1.4\,\mu\text{F}$, i.e. at less than a third of the capacitance to be installed. Moreover, the current rating of the utilized capacitors has to be checked, which may necessitate multiple capacitors installed in parallel to meet the ratings, particularly for the two-level inverter operation.

The third aspect of designing the DC-link is the occurrence of voltage ripples linked to the machine's fundamental frequency and – in case of a passive diode bridge rectifier as DC-source – also linked to the fundamental grid frequency. While this ripple requires rather large capacitances due to the comparably low frequencies such as $50\,\text{Hz}$, many other sources such as batteries in battery electric vehicles or rectifier solutions such as active-front-ends can be expected to be capable of stabilizing this ripple, which then may be neglected with respect to the drive inverter design. Close vicinity between these sources and the inverter is furthermore not strictly necessary, unless the parasitic inductance of the respective connection does not impair the transient performance of the load during reference steps etc.

Lastly, a fourth aspect for designing the DC-link relates to fault conditions. For example, if the machine is to be demagnetized fast and the connection towards the source is interrupted, it has to be ensured that the corresponding energy can be dissipated without leading to further damage to any of the system components. Several possibilities, such as dedicated devices or chopper circuits can be implemented as a remedy.

In summary, the DC-link optimization of the interleaved inverter decreases the demand of installed capacitance greatly and makes it feasible to utilize merely foil caps for transient over-voltage prevention *and* DC-link voltage stabilization, if certain conditions mentioned above are generally met.

Guidelines for two-level inverter

Generally speaking, the hardware design of a two-level inverter – or respectively of halfbridge modules or discrete switches – is dependent on the anticipated power of the load. The thermal capacitance of semiconductors or modules is rather small. Therefore, their overload capability by means of maximum power dissipation is usually defined in the range from $10\,\mu\text{s}$ up to ms, revealing an inverse relation between overload duration and respective power dissipation.[9] On the other hand, electrical machines can have overload capabilities of several seconds to minutes due to their comparably large thermal inertia. It is for this reason that if the

[7] @ Minimal gate resistance according to the datasheet and $V_{\text{gs}} = 18\,\text{V}$.

[8] It can be assumed that a voltage ripple of this magnitude does not impair the control quality. Nevertheless, due to the high dynamics of the FCS-MPC, which evaluates the predictions at every time step, it is anticipated that even larger voltage ripples can be compensated well as long the available voltage reserve for load control is not dramatically reduced. A necessary condition for this however is a sufficiently dynamic measurement of the DC-link voltage, which in this case should have the same bandwidth as the current measurements.

[9] These overload capabilities are usually valid for an initial case temperature of $T_{\text{c}} = 25\,^\circ\text{C}$ and require sufficient thermal conductance to limit the temperature rise of the semiconductor to tolerable levels, e.g. to a junction temperature of $T_{\text{j}} = 150\,^\circ\text{C}$.

overload capability of the machine is to be utilized, it is necessary[10] to design the inverter to withstand the respective power dissipation during machine overload in a static manner. In other words, the overload power of the machine (incl. its losses) has to correspond to the nominal power of the inverter.

The losses of MOSFETs normally show a quadratic relationship with the drain-source current with respect to the conduction losses, which is owing to their according on-resistance. On the other hand, the switching losses rise approximately linearly with the switching frequency and current, and often slightly more than linearly with the voltage to be switched.[11] This implies that there normally is a drain-source current where the overall losses are minimal for a specific nominal average switching frequency. It is a good practice to chose the power switches in a manner to match this point of minimal losses with the nominal power of the inverter. Since the interleaved inverter ensures an approximately equal sharing of the load current on the parallelized two-level inverters, the according drain-source current's can be halved when designing the two-level converters.[12]

If a reduced size of the DC-link capacitor bank is aspired, but larger DC-link voltage ripples can be tolerated during machine overload conditions, a reduced frequency operation can come into question during machine overload conditions. An example is the comparison between OP2 and OP4 in Table 6.1, where the dissipated energy is shifted between the inverter on the one hand and the machine and DC-link on the other. This measure implies that the rated inverter power does not entirely have to scale up with the machine overload capability, and may allow more economical designs. Nevertheless, It can come at the costs of higher necessary current ratings for the DC-link capacitors. If larger DC-link voltage ripples cannot be tolerated during overload however, either the DC-link or the rated power of the inverter has to be adjusted linearly with the overload capability of the machine.

In the facilitating case without utilized overload capability of the machine, the nominal power of the inverter can directly be optimized for the nominal power of the load, as well as the desired conditions with respect to the DC-link ripple and machine TDD.

[10] An exception are overload conditions that can *nearly* be met by the power switches. In this case, it stands to reason to artificially increase the thermal capacity of the modules, if possible.

[11] Estimating formulas for modulated sine wave outputs are provided in [33].

[12] As a rough estimate for the scenario at the proposed tuning of $i_{\mathrm{sat,c}} = {}^1\!/_4 \cdot i_{\mathrm{ph,n}}$, the rms-values of the currents for the two-level inverters can be scaled to $i^2_{1,\mathrm{ph,rms}} = i^2_{2,\mathrm{ph,rms}} = ({}^{i_{\mathrm{ph}}}\!/_2)^2 \cdot (1^2 + ({}^1\!/_4)^2) \approx 0.266 \cdot i^2_{\mathrm{ph,n}}$ instead of $i^2_{1,\mathrm{ph,rms}} = i^2_{2,\mathrm{ph,rms}} = ({}^{i_{\mathrm{ph}}}\!/_2)^2 = 0.25 \cdot i^2_{\mathrm{ph,n}}$, i.e. a 6% increase of conduction losses. Although this approach neglects further harmonics due to interleaving, it is a good approximation, as can be verified by Figure 4.25 and Table 6.1.

7. Conclusion and Outlook

The thesis at hand gave insights on the general capabilities of an interleaved inverter for a motor drive system. It was shown that the chosen approach of optimizing the overall system with a FCS-MPC controller type is a very effective way to handle various system constraints and control aims in a flexible manner. Specifically, issues such as the minimization of machine TDD, losses in the induction machine and the inverter, stress on the DC-link capacitor bank, and lastly remedies for undesirable $\mathrm{d}v/\mathrm{d}t$-effects and effects due to large common-mode voltage were provided and verified in simulation and hardware. The detailed analysis of superiority towards a regular two-level inverter, the feasability and also the necessary trade-offs between the respective optimization goals extend the existing literature on this topology substantially. Loads with a demand for low TDD and with a ratio of high current to voltage are identified to be most suitable for interleaving.

Even though the interleaved inverter's above mentioned capabilities were verified in simulation and hardware, the proof in the matter of overall loss minimization still has to be established. Therefore, it is advised to continue the research on optimized hardware setups that unfold the full capabilities of the interleaved topology when combined with sophisticated control algorithms. It stands to reason that this goal can be reached with the formulated guidelines for hardware design of this thesis. The given suggestions for necessary adaptions regarding higher powered loads – or alternatively an optimized choke design – as well as for different nominal average switching frequencies facilitates the upcoming research significantly.

Beyond these aspects, this thesis remains to be seen as a basis for future research. Firstly, an open topic that deserves further attention is the symmetrization of losses among the semiconductors. Although various techniques were presented in this thesis, a higher level controller based on thermal modeling yet has to be included and evaluated in the overall algorithm. Secondly, the opportunity of enhancing the TDD and DC-link optimization by considering variable switching point MPC implementations promises further optimization potential and should therefore be part of subsequent investigations. Since this kind of optimization approach requires a multitude of additional computational resources, it directly relates to the task of utilizing computationally more powerful platforms. Moreover, the creation of either even more advanced FPGA designs (e.g. with a respective optimization of resource sharing and pipelining) or alternatively algorithms such as branch-out-bound or sphere-decoding will likely be necessary.

Lastly, extensive comparisons of the capabilities and trade-offs for the interleaved inverter vs. common topologies such as NPC multi-level inverters yet have to be performed in the context of (FCS-)MPC. Likewise, deeper assessments of combined topologies (e.g. NPC + interleaved) for precisely formulated optimization goals are to be considered, as they indicate even more potential. These formulations and their according mathematical models should also reflect the explicit knowledge of the supplying topology for the DC-link (e.g. passive diode rectifiers, active-front-ends or batteries).

A. Derivations and Supplementary Modeling

A.1. Derivation of Complete Interleaving Choke Model

This derivation of the interleaving choke model maintains the complete dependency on any of the involved parameters. It for example allows the analysis for the case of unmatched windings, which can potentially occur due to tolerances in manufacturing, particular failure modes etc.

By applying elementary row operations to Eqn. (3.14) - (3.16), Eqn. (A.1) - (A.3) can be derived.

$$v_{\text{ph}} = \frac{1}{2}\Big(v_{1,\text{ph}} + v_{2,\text{ph}}\Big) - \frac{1}{2}\Big(\left(R_{1,\text{dc}} + R_{1,\text{ac,w}}\right)\cdot i_{1,\text{ph}} + \left(R_{2,\text{dc}} + R_{2,\text{ac,w}}\right)\cdot i_{2,\text{ph}}\Big) \ldots \\ - \frac{1}{2}\Big(L_{1,\sigma}\cdot\frac{\mathrm{d}}{\mathrm{d}t}i_{1,\text{ph}} + L_{2,\sigma}\cdot\frac{\mathrm{d}}{\mathrm{d}t}i_{2,\text{ph}}\Big) \tag{A.1}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}i_{1,\text{ph}} = \frac{v_{1,\text{ph}} - v_{2,\text{ph}} - i_{1,\text{ph}}\left(R_{1,\text{dc}} + R_{2,\text{dc}} + R_{1,\text{ac}} + R_{2,\text{ac}}\right) + \left(R_{2,\text{dc}} + R_{2,\text{ac}}\right)\cdot i_{\text{ph}}}{L_{1,\sigma} + L_{2,\sigma} + 4M_{12}} + \ldots \\ \frac{2R_{\text{ac,m}}\cdot\left(i_{\text{ph}} - 2i_{1,\text{ph}}\right)}{L_{1,\sigma} + L_{2,\sigma} + 4M_{12}} + \frac{L_{2,\sigma} + 2M}{L_{1,\sigma} + L_{2,\sigma} + 4M_{12}}\cdot\frac{\mathrm{d}}{\mathrm{d}t}i_{\text{ph}} \tag{A.2}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}i_{2,\text{ph}} = \frac{v_{2,\text{ph}} - v_{1,\text{ph}} - i_{2,\text{ph}}\left(R_{1,\text{dc}} + R_{2,\text{dc}} + R_{1,\text{ac}} + R_{2,\text{ac}}\right) + \left(R_{1,\text{dc}} + R_{1,\text{ac}}\right)\cdot i_{\text{ph}}}{L_{1,\sigma} + L_{2,\sigma} + 4M_{12}} + \ldots \\ \frac{2R_{\text{ac,m}}\cdot\left(i_{\text{ph}} - 2i_{2,\text{ph}}\right)}{L_{1,\sigma} + L_{2,\sigma} + 4M_{12}} + \frac{L_{1,\sigma} + 2M}{L_{1,\sigma} + L_{2,\sigma} + 4M_{12}}\cdot\frac{\mathrm{d}}{\mathrm{d}t}i_{\text{ph}} \tag{A.3}$$

As noted in chapter 3, the parameters M and $R_{1,\text{ac,w}}$, $R_{2,\text{ac,w}}$, $R_{\text{ac,m}}$ can show a high frequency dependency ($\underline{\mu}_{\text{r}}$, Skin effect, Proximity effect).

Interpretation of equations
Likewise as in Chapter 3, Equation (A.1) emphasizes the averaging effect of the interleaving choke with respect to the output voltage. The second and third term correspond to parasitic voltage drops at the ohmic resistance and leakage inductance of the windings etc.

Further implications of Eqn. (A.2) and (A.3) are best visible if transformed to the Laplace domain, as given in (A.4) and (A.5).

$$I_{1,\mathrm{ph}}(s) = \frac{V_{1,\mathrm{ph}}(s) - V_{2,\mathrm{ph}}(s)}{R_{1,\mathrm{dc}} + R_{2,\mathrm{dc}} + R_{1,\mathrm{ac}} + R_{2,\mathrm{ac}} + 4R_{\mathrm{ac,m}} + s\left(L_{1,\sigma} + L_{2,\sigma} + 4M_{12}\right)} + \ldots$$
$$I_{\mathrm{ph}}(s) \cdot \frac{R_{2,\mathrm{dc}} + R_{2,\mathrm{ac}} + 2R_{\mathrm{ac,m}} + s\left(L_{2,\sigma} + 2M_{12}\right)}{R_{1,\mathrm{dc}} + R_{2,\mathrm{dc}} + R_{1,\mathrm{ac}} + R_{2,\mathrm{ac}} + 4R_{\mathrm{ac,m}} + s\left(L_{1,\sigma} + L_{2,\sigma} + 4M_{12}\right)} \tag{A.4}$$

$$I_{2,\mathrm{ph}}(s) = \frac{V_{2,\mathrm{ph}}(s) - V_{1,\mathrm{ph}}(s)}{R_{1,\mathrm{dc}} + R_{2,\mathrm{dc}} + R_{1,\mathrm{ac}} + R_{2,\mathrm{ac}} + 4R_{\mathrm{ac,m}} + s\left(L_{1,\sigma} + L_{2,\sigma} + 4M_{12}\right)} + \ldots$$
$$I_{\mathrm{ph}}(s) \cdot \frac{R_{1,\mathrm{dc}} + R_{1,\mathrm{ac}} + 2R_{\mathrm{ac,m}} + s\left(L_{1,\sigma} + 2M_{12}\right)}{R_{1,\mathrm{dc}} + R_{2,\mathrm{dc}} + R_{1,\mathrm{ac}} + R_{2,\mathrm{ac}} + 4R_{\mathrm{ac,m}} + s\left(L_{1,\sigma} + L_{2,\sigma} + 4M_{12}\right)} \tag{A.5}$$

Again, the first term describes the strong impact of interleaving vectors on the cross-currents, i.e. switch positions where $v_{1,\mathrm{ph}} - v_{2,\mathrm{ph}} \neq 0$ holds. In this case, $i_{1,\mathrm{ph}}$ is strongly increasing and $i_{2,\mathrm{ph}}$ is strongly decreasing, or vice versa. Further, the influence of the interleaving vectors decays over time (first order lag element).

Moreover, the current sharing behavior reveals itself in the respective second term: In consideration of perfectly matched windings and abstinent interleaving vectors, the output current is shared equally. On the other hand, asymmetric parasitics of the windings lead to asymmetric current sharing. While the ohmic DC-parameters are dominant at very low frequencies, the leakage and ohmic AC-parameters govern the asymmetries at higher frequencies. The influence of unmatched AC-parameters is generally less, since the value of M_{12}, which by definition has identical values for both windings, is considerably larger than the leakage values. The same attributes hold for the core loss component modeled by $R_{\mathrm{ac,m}}$.

Expansion to three-phase system

Finally, Eqn. (A.1) - (A.3) are expanded to the three-phase system. The matrices $\boldsymbol{K}_1$,...,$\boldsymbol{K}_{10}$ are of diagonal shape and contain the according parameter compositions of these equations.

$$\boldsymbol{v}_{\mathrm{out}} = \boldsymbol{K}_1 \cdot \boldsymbol{i}_1 + \boldsymbol{K}_2 \cdot \boldsymbol{i}_2 + \boldsymbol{K}_3 \cdot \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_1 + \boldsymbol{K}_4 \cdot \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_2 + \boldsymbol{K}_5 \cdot \begin{pmatrix} \boldsymbol{v}_1 \\ \boldsymbol{v}_2 \end{pmatrix} \tag{A.6}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_1 = \boldsymbol{K}_6 \cdot \boldsymbol{i}_1 + \boldsymbol{K}_7 \cdot \boldsymbol{i}_{\mathrm{out}} + \boldsymbol{K}_8 \cdot \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_{\mathrm{out}} + \boldsymbol{K}_9 \cdot \begin{pmatrix} \boldsymbol{v}_1 \\ \boldsymbol{v}_2 \end{pmatrix} \tag{A.7}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_2 = \boldsymbol{K}_6 \cdot \boldsymbol{i}_2 + \boldsymbol{K}_{10} \cdot \boldsymbol{i}_{\mathrm{out}} + \boldsymbol{K}_8 \cdot \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_{\mathrm{out}} - \boldsymbol{K}_9 \cdot \begin{pmatrix} \boldsymbol{v}_1 \\ \boldsymbol{v}_2 \end{pmatrix} \tag{A.8}$$

$$\text{where } \boldsymbol{K}_1 = {}^{-1}\!/_{2} \cdot \begin{pmatrix} R_{1,\mathrm{dc,a}} + R_{1,\mathrm{ac,w,a}} & 0 & 0 \\ 0 & R_{1,\mathrm{dc,w,b}} + R_{1,\mathrm{ac,w,b}} & 0 \\ 0 & 0 & R_{1,\mathrm{dc,w,c}} + R_{1,\mathrm{ac,w,c}} \end{pmatrix}$$

$$\text{and } \boldsymbol{K}_9 = \begin{pmatrix} 1/(L_{1,\sigma,\mathrm{a}} + L_{2,\sigma,\mathrm{a}} + 4M_{12,\mathrm{a}}) & 0 & 0 & -1/(..) & 0 & 0 \\ 0 & 1/(..) & 0 & 0 & -1/(..) & 0 \\ 0 & 0 & 1/(..) & 0 & 0 & -1/(..) \end{pmatrix}$$

$$\text{and } \boldsymbol{v}_{\mathrm{out}} = (v_{\mathrm{a}}\ v_{\mathrm{b}}\ v_{\mathrm{c}})^{\mathrm{T}},\ \boldsymbol{i}_{\mathrm{out}} = (i_{\mathrm{a}}\ i_{\mathrm{b}}\ i_{\mathrm{c}})^{\mathrm{T}},\ \boldsymbol{i}_1 = \left(i_{1,\mathrm{a}}\ i_{1,\mathrm{b}}\ i_{1,\mathrm{c}}\right)^{\mathrm{T}} \text{ etc.}$$

Note that if the equation system of Eqn. (A.6) - (A.8) is transformed into the alpha-beta-gamma domain[1], the transformed matrices $\bar{\boldsymbol{K}}_1$,...,$\bar{\boldsymbol{K}}_{10}$ will lose their diagonal shape for the unmatched parameter case, while

[1]This can be performed via the substitution $\bar{\boldsymbol{K}} = T_{\mathrm{c},3} \cdot \boldsymbol{K} \cdot {T_{\mathrm{c},3}}^{-1}$, applied to $\boldsymbol{K}_1$,...,$\boldsymbol{K}_{10}$

$\boldsymbol{v}_{\text{out}}, \boldsymbol{i}_{\text{out}}$ are reduced to the 2-tuples $\boldsymbol{v}_{\text{out}}^{\alpha\beta}, \boldsymbol{i}_{\text{out}}^{\alpha\beta}$ (gamma-component vanishes, cp. Section 3.1.1).

Conversely, the matrices $\boldsymbol{K}_1, ..., \boldsymbol{K}_{10}$ can be reduced to scalar values $K_1, ..., K_{10}$, if matched parameters are assumed. These scalar values are further unaffected by to Clarke transformation.

A.2. Derivation of State-Space Representation of Overall Plant Model

In the following, exemplary steps for the derivation of the state-space representation of the overall plant model are given. In order to avoid any loss of generality, the derivation is given for the unmatched parameter case, i.e. uses the matrices $\boldsymbol{K}_1, ..., \boldsymbol{K}_{10}$ instead of scalar values.

Note that for any of the below mentioned substitutions, the order of the involved matrices has to be maintained, as matrix multiplications are non-commutative. Further, all of the below mentioned equations are assumed to be already transformed in the alpha-beta-gamma domain (usage of transformed matrices $\bar{\boldsymbol{K}}$).

1. Start with the differential equation for the phase currents of the second inverter, i.e. $\mathrm{d}/\mathrm{d}t\, \boldsymbol{i}_2$ of Eq. (A.8). Substitute $\boldsymbol{i}_2$ here via $\boldsymbol{i}_2 = \boldsymbol{i}_{\text{out}} - \boldsymbol{i}_1$ (three-phase and unmatched parameter version of Eq. (3.16)).
Result:

$$\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_2 = \bar{\boldsymbol{K}}_6 \cdot (\boldsymbol{i}_{\text{out}} - \boldsymbol{i}_1) + \bar{\boldsymbol{K}}_{10} \cdot \boldsymbol{i}_{\text{out}} + \bar{\boldsymbol{K}}_8 \cdot \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_{\text{out}} - \bar{\boldsymbol{K}}_9 \cdot \begin{pmatrix} \boldsymbol{v}_1 \\ \boldsymbol{v}_2 \end{pmatrix} \tag{A.9}$$

2. Substitute the derivatives of the inverter phase currents in the voltage output equation Eq. (A.6) via Eq. (A.7) and Eq. (A.9).

Result:

$$\begin{aligned}
\boldsymbol{v}_{\text{out}} =& \bar{\boldsymbol{K}}_1 \cdot \boldsymbol{i}_1 + \bar{\boldsymbol{K}}_2 \cdot (\boldsymbol{i}_{\text{out}} - \boldsymbol{i}_1) + ... \\
& \bar{\boldsymbol{K}}_3 \cdot \left(\bar{\boldsymbol{K}}_6 \cdot \boldsymbol{i}_1 + \bar{\boldsymbol{K}}_7 \cdot \boldsymbol{i}_{\text{out}} \; + \bar{\boldsymbol{K}}_8 \cdot \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_{\text{out}} + \bar{\boldsymbol{K}}_9 \cdot \begin{pmatrix} \boldsymbol{v}_1 \\ \boldsymbol{v}_2 \end{pmatrix} \right) + ... \\
& \bar{\boldsymbol{K}}_4 \cdot \left(\bar{\boldsymbol{K}}_6 \cdot (\boldsymbol{i}_{\text{out}} - \boldsymbol{i}_1) + \bar{\boldsymbol{K}}_{10} \cdot \boldsymbol{i}_{\text{out}} + \bar{\boldsymbol{K}}_8 \cdot \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_{\text{out}} - \bar{\boldsymbol{K}}_9 \cdot \begin{pmatrix} \boldsymbol{v}_1 \\ \boldsymbol{v}_2 \end{pmatrix} \right) + \bar{\boldsymbol{K}}_5 \cdot \begin{pmatrix} \boldsymbol{v}_1 \\ \boldsymbol{v}_2 \end{pmatrix}
\end{aligned}$$

$$\begin{aligned}
\rightarrow \boldsymbol{v}_{\text{out}} =& \left(\bar{\boldsymbol{K}}_1 - \bar{\boldsymbol{K}}_2 + \bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_6 - \bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_6\right) \cdot \boldsymbol{i}_1 + \left(\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_8 + \bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_8\right) \cdot \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_{\text{out}} + ... \\
& \left(\bar{\boldsymbol{K}}_2 + \bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_7 + \bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_6 + \bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_{10}\right) \cdot \boldsymbol{i}_{\text{out}} + \left(\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_9 - \bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_9 + \bar{\boldsymbol{K}}_5\right) \cdot \begin{pmatrix} \boldsymbol{v}_1 \\ \boldsymbol{v}_2 \end{pmatrix}
\end{aligned}$$

3. Expand the dynamic model of the induction machine in Eq. (3.42) with a gamma-component. This simply yields two additional rows with entries of 0. It is necessary for acquiring compatible matrix sizes for the following substitution.

4. Substitute v_{s} in the expanded version of Eq. (3.42) with the previously derived equation for v_{out} (step 2). Secondly, replace the inverter output current i_{out} with the stator input current i_{s}. A direct replacement is allowed, since these currents are identical.

Result:

$$\begin{aligned}\frac{\mathrm{d}}{\mathrm{d}t}\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\end{pmatrix} =& \boldsymbol{K}_{11}\cdot\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\end{pmatrix} + \omega_\mathrm{r}\cdot\boldsymbol{K}_{12}\cdot\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\end{pmatrix} + \dots\\ & K_{13}\cdot\begin{pmatrix}\left(\bar{\boldsymbol{K}}_1-\bar{\boldsymbol{K}}_2+\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_6-\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_6\right)\cdot\boldsymbol{i}_1+\left(\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_8+\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_8\right)\cdot\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_\mathrm{s}\\ \mathbf{0}\end{pmatrix}+\dots\\ & K_{13}\cdot\begin{pmatrix}\left(\bar{\boldsymbol{K}}_2+\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_7+\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_6+\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_{10}\right)\cdot\boldsymbol{i}_\mathrm{s}+\left(\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_9-\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_9+\bar{\boldsymbol{K}}_5\right)\cdot\begin{pmatrix}\boldsymbol{v}_1\\ \boldsymbol{v}_2\end{pmatrix}\\ \mathbf{0}\end{pmatrix}\end{aligned}$$

5. Rearrange the equation of step 4 to isolate the expression $\mathrm{d}/\mathrm{d}t\ \boldsymbol{i}_\mathrm{s}$.

Result:

$$\begin{aligned}&\frac{\mathrm{d}}{\mathrm{d}t}\begin{pmatrix}\left(\boldsymbol{I}_3-\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_8-\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_8\right)\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\end{pmatrix} = \dots\\ &\boldsymbol{K}_{11}\cdot\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\end{pmatrix} + \omega_\mathrm{r}\cdot\boldsymbol{K}_{12}\cdot\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\end{pmatrix} + K_{13}\cdot\begin{pmatrix}\left(\bar{\boldsymbol{K}}_1-\bar{\boldsymbol{K}}_2+\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_6-\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_6\right)\cdot\boldsymbol{i}_1\\ \mathbf{0}\end{pmatrix}+\dots\\ &K_{13}\cdot\begin{pmatrix}\left(\bar{\boldsymbol{K}}_2+\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_7+\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_6+\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_{10}\right)\cdot\boldsymbol{i}_\mathrm{s}+\left(\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_9-\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_9+\bar{\boldsymbol{K}}_5\right)\cdot\begin{pmatrix}\boldsymbol{v}_1\\ \boldsymbol{v}_2\end{pmatrix}\\ \mathbf{0}\end{pmatrix}\end{aligned}$$

$$\begin{aligned}\rightarrow\frac{\mathrm{d}}{\mathrm{d}t}\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\end{pmatrix} &= \bar{\boldsymbol{K}}_{14}\boldsymbol{K}_{11}\cdot\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\end{pmatrix} + \omega_\mathrm{r}\cdot\bar{\boldsymbol{K}}_{14}\boldsymbol{K}_{12}\cdot\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\end{pmatrix} + \dots\\ &\bar{\boldsymbol{K}}_{14}K_{13}\cdot\begin{pmatrix}\left(\bar{\boldsymbol{K}}_1-\bar{\boldsymbol{K}}_2+\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_6-\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_6\right)\cdot\boldsymbol{i}_1\\ \mathbf{0}\end{pmatrix}+\dots\\ &\bar{\boldsymbol{K}}_{14}K_{13}\cdot\begin{pmatrix}\left(\bar{\boldsymbol{K}}_2+\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_7+\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_6+\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_{10}\right)\cdot\boldsymbol{i}_\mathrm{s}+\left(\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_9-\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_9+\bar{\boldsymbol{K}}_5\right)\cdot\begin{pmatrix}\boldsymbol{v}_1\\ \boldsymbol{v}_2\end{pmatrix}\\ \mathbf{0}\end{pmatrix}\\ &\text{where } \bar{\boldsymbol{K}}_{14}=\begin{pmatrix}\boldsymbol{I}_3-\bar{\boldsymbol{K}}_3\bar{\boldsymbol{K}}_8-\bar{\boldsymbol{K}}_4\bar{\boldsymbol{K}}_8 & 0\\ 0 & \boldsymbol{I}_3\end{pmatrix}^{-1} \text{ and } \boldsymbol{I}_3=\begin{pmatrix}1&0&0\\0&1&0\\0&0&1\end{pmatrix}\end{aligned} \tag{A.10}$$

6. Expand Eq. (A.10) with the differential equation for $\mathrm{d}/\mathrm{d}t\ \boldsymbol{i}_1$ from Eq. (A.7) to acquire the full dynamic system description.

7. Summarize this system of equations to attain the compact (linear and time-variant) state-space representation form.

Result:

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\\ \boldsymbol{i}_1\end{pmatrix} = \left(\boldsymbol{A}_{\text{plant}'}+\omega_\mathrm{r}\cdot\boldsymbol{A}_{\text{plant}''}\right)\begin{pmatrix}\boldsymbol{i}_\mathrm{s}\\ \boldsymbol{\Psi}_\mathrm{r}\\ \boldsymbol{i}_1\end{pmatrix} + \boldsymbol{B}_\text{plant}\begin{pmatrix}\boldsymbol{v}_1\\ \boldsymbol{v}_2\end{pmatrix} \tag{A.11}$$

8. Cross out the rows corresponding to $\mathrm{d}/\mathrm{d}t\ i_{\mathrm{s},\gamma}$, $\mathrm{d}/\mathrm{d}t\ \Psi_{\mathrm{r},\gamma}$, as these components will remain 0 at any time. Note that while the gamma-component of $\boldsymbol{i}_\mathrm{s}$, $\boldsymbol{\Psi}_\mathrm{r}$ can be neglected, $i_{1,\gamma}$ can very well be non-zero and has to be considered (cp. Section 3.1.3).

The rank of the system matrix is 7.

A.3. Transformation of System Matrix for other State Vector Compositions

The system matrix for the MPTFC of Section 4.2.1 was neither explicitly derived in Chapter 3, nor its following chapters. However, a transformation for other state vectors can be acquired very easily. The conditions for this are

- that the overall system matrix is already set up, e.g. as derived in Appendix A.2 for the interleaved inverter system
- and that the relation of the respective quantities (being subject to the desired substitutions) is known.

In Chapter 3, the derived state-space matrices describe the system behavior (i.e. the behavior of an induction machine) for the state vector $\boldsymbol{x}_\text{given} = (\boldsymbol{i}_\mathrm{s}^{\alpha\beta}\ \boldsymbol{\Psi}_\mathrm{r}^{\alpha\beta})^\mathrm{T}$ in the following manner:

$$\begin{pmatrix} \boldsymbol{i}_\mathrm{s}^{\alpha\beta}\ (k+1) \\ \boldsymbol{\Psi}_\mathrm{r}^{\alpha\beta}(k+1) \end{pmatrix} = \boldsymbol{A}_\mathrm{c}(\omega_\mathrm{r}) \cdot \begin{pmatrix} \boldsymbol{i}_\mathrm{s}^{\alpha\beta}\ (k) \\ \widetilde{\boldsymbol{\Psi}}_\mathrm{r}^{\alpha\beta}(k) \end{pmatrix} + \boldsymbol{B}_\mathrm{c}\ \boldsymbol{T}_{\mathrm{c},2} \cdot (V_\mathrm{dc}/2) \cdot \boldsymbol{u}(k) \tag{A.12}$$

In case of the MPTFC and a two-level inverter, the desired space vector instead is $\boldsymbol{x}_\text{desired} = (\boldsymbol{i}_\mathrm{s}^{\alpha\beta}\ \boldsymbol{\Psi}_\mathrm{s}^{\alpha\beta})^\mathrm{T}$. With the help of Eqn. (3.39) - (3.40), an equation with $\boldsymbol{i}_\mathrm{s}, \boldsymbol{\Psi}_\mathrm{s}, \boldsymbol{\Psi}_\mathrm{r}$ can be found, eventually allowing to set up the relation between the given and desired space vector:

$$\begin{aligned} &\boldsymbol{\Psi}_\mathrm{s} = \sigma L_\mathrm{s} \cdot \boldsymbol{i}_\mathrm{s} + (M_\mathrm{sr}/L_\mathrm{r}) \cdot \boldsymbol{\Psi}_\mathrm{r} \\ &\boldsymbol{x}_\text{desired} = \begin{pmatrix} \boldsymbol{i}_\mathrm{s}^{\alpha\beta} \\ \boldsymbol{\Psi}_\mathrm{s}^{\alpha\beta} \end{pmatrix} = \begin{pmatrix} \boldsymbol{0}_\text{2x2} & \boldsymbol{0}_\text{2x2} \\ \sigma L_\mathrm{s} & M_\mathrm{sr}/L_\mathrm{r} \end{pmatrix} \cdot \begin{pmatrix} \boldsymbol{i}_\mathrm{s}^{\alpha\beta} \\ \boldsymbol{\Psi}_\mathrm{r}^{\alpha\beta} \end{pmatrix} = \boldsymbol{T}_\mathrm{sr} \cdot \begin{pmatrix} \boldsymbol{i}_\mathrm{s}^{\alpha\beta} \\ \boldsymbol{\Psi}_\mathrm{r}^{\alpha\beta} \end{pmatrix} \\ &\boldsymbol{x}_\text{desired} = \boldsymbol{T}_\mathrm{sr} \cdot \boldsymbol{x}_\text{given} \end{aligned} \tag{A.13}$$

Finally, Eq. (A.12) has to be multiplied to acquire the state-space representation for the desired state vector composition.

A.4. Relation of Switch Positions and Voltage Space Vectors / Cross-Current Evolution

The relation of switch positions and the resulting (approximate) evolution of cross-currents is given in Table A.1 for the interleaved inverter system. The letters indicate which phase has a positive or negative evolution with respect to $i_{1,\mathrm{ph}} - i_{2,\mathrm{ph}}$.

The relation of switch positions and the resulting output voltage space vectors is given in Table A.2 for the interleaved inverter system. The numbers in the table correspond to the enumerated space vectors depicted in Figure A.1 (identical to Figure 4.14).

Table A.1.: Relation of switch positions and the resulting (approximate) cross-current evolution.

	$\boldsymbol{s}_2^{\mathrm{abc}}$							
$\boldsymbol{s}_1^{\mathrm{abc}}$	000	100	110	010	011	001	101	111
000		-a	-a, -b	-b	-b, -c	-c	-a, -c	-a, -b, -c
100	a		-b	a, -b	a, -b, -c	a, -c	-c	-b, -c
110	a, b	b		a	a, -c	a, b, -c	b, -c	-c
010	b	-a, b	-a		-c	b, -c	-a, b, -c	-a, -c
011	b, c	-a, b, c	-a, c	c		b	-a, b	-a
001	c	-a, c	-a, -b, c	-b, c	-b		-a	-a, -b
101	a, c	c	-b, c	a, -b, c	a, -b	a		-b
111	a, b, c	b, c	c	a, c	a	a, b	b	

Table A.2.: Relation of switch positions and the resulting output voltage space vector [9]. Common-mode free vectors are marked in green.

.

	$\boldsymbol{s}_2^{\mathrm{abc}}$							
$\boldsymbol{s}_1^{\mathrm{abc}}$	000	100	110	010	011	001	101	111
000	0	13	14	15	16	17	18	0
100	13	1	7	14	0	18	12	13
110	14	7	2	8	15	0	13	14
010	15	14	8	3	9	16	0	15
011	16	0	15	9	4	10	17	16
001	17	18	0	16	10	5	11	17
101	18	12	13	0	17	11	6	18
111	0	13	14	15	16	17	18	0

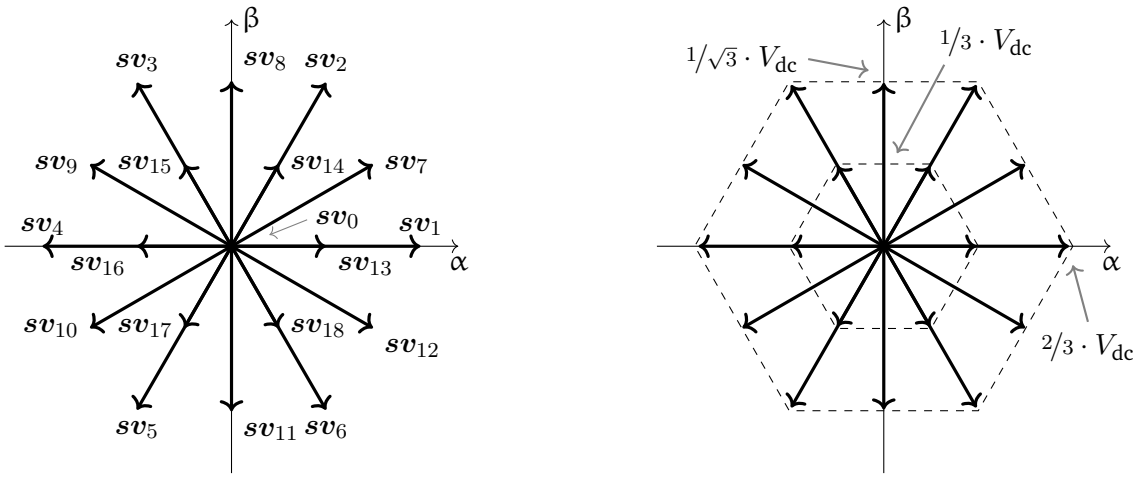
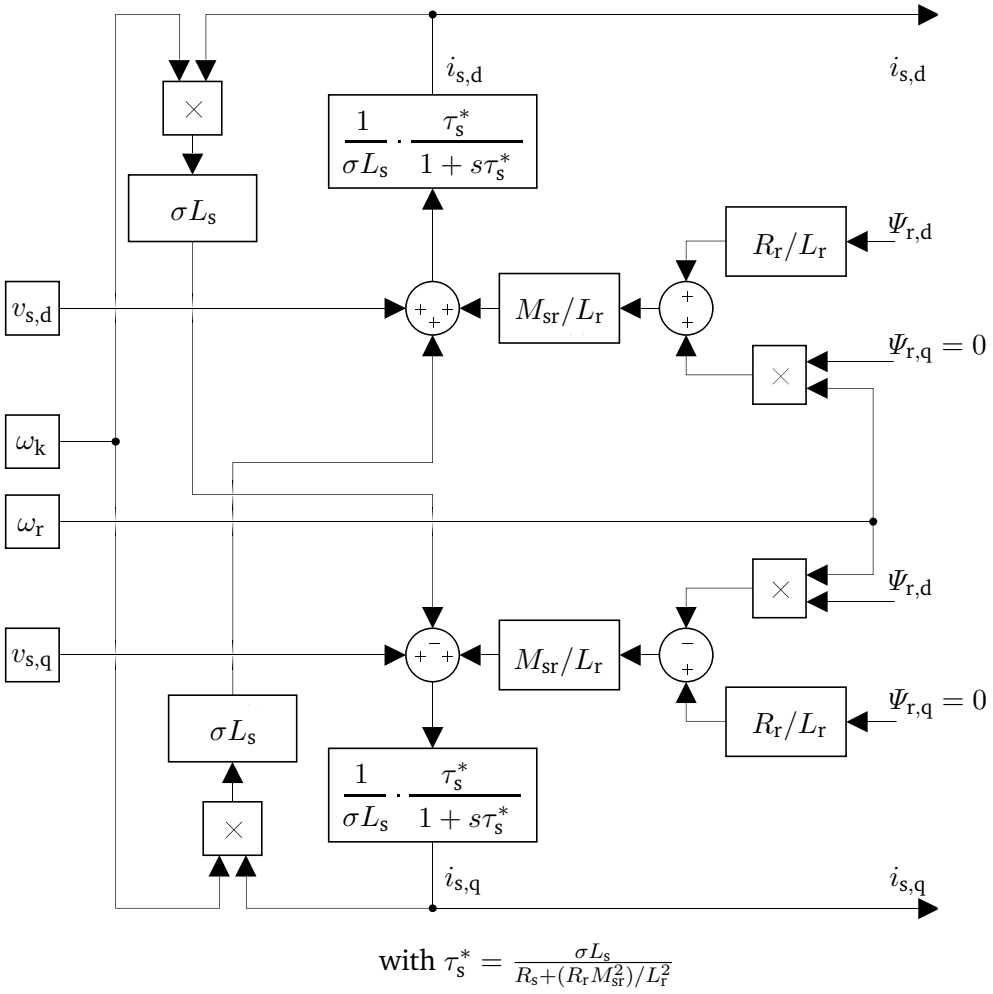


Figure A.1.: Enumerated unique space vectors of a three-level three-phase inverter in the alpha-beta plane (left) and the size of the spanning hexagons (right). This Figure is identical to Figure 4.14.

A.5. Block Diagrams for Induction Machine

The following block diagrams extend the illustrations and equations of Section 3.2.3 by describing the field-oriented stator and rotor dynamics of an induction machine.



with $\tau_s^* = \frac{\sigma L_s}{R_s + (R_r M_{sr}^2)/L_r^2}$

Figure A.2.: Block diagram of the field-oriented stator dynamics of an induction machine.

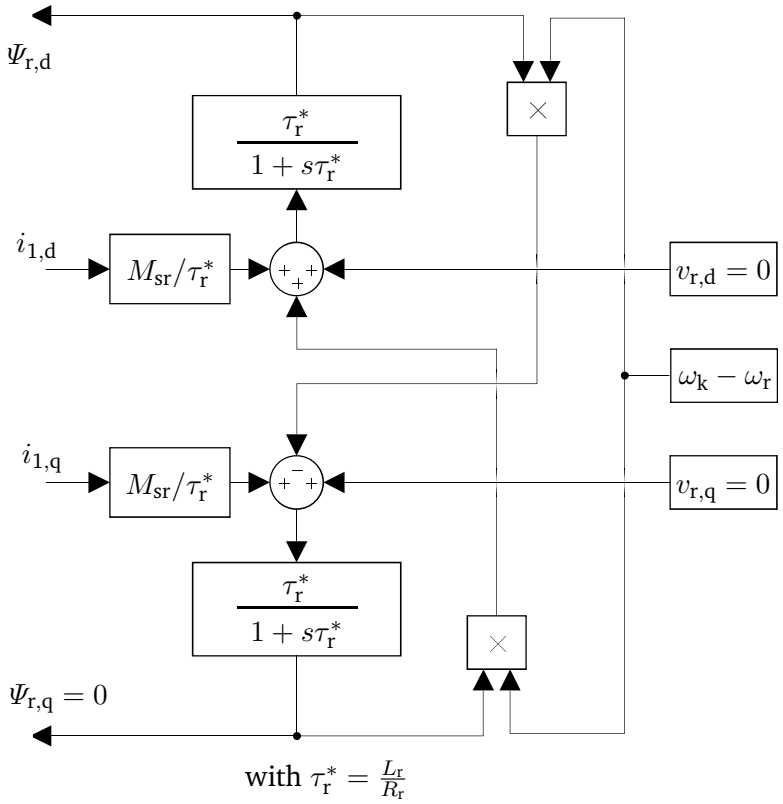


Figure A.3.: Block diagram of the field-oriented rotor dynamics of an induction machine.

B. Parameters

General Parameters

The parameters for the DC-link and induction machine are provided in Table B.1. Excerpts of the choke's and MOSFET's datasheets are given in Table B.2. The latter yield the basis for the respective loss calculations.

Table B.1.: Parameters for modeling of induction machine, interleaving choke and DC-link.

Name	**Nomen-clature**	**Value**
DC-link voltage	V_{dc}	$800\,\mathrm{V}$
IM rated rms line voltage	V_{n}	$400\,\mathrm{V}$
IM rated rms phase current	I_{n}	$10.5\,\mathrm{A}$
IM rated speed	ω_{n} / n_{n}	$306.3\,\mathrm{rad/s}$ / $2925\,\mathrm{min}^{-1}$
IM rated torque	$T_{\mathrm{e,n}}$	$17.96\,\mathrm{N\,m}$
IM rated stator flux	$\Psi_{\mathrm{s,n}}$	$1.06\,\mathrm{V\,s}$
IM pole pairs	z_{p}	1
IM power factor	$\cos(\varphi_{\mathrm{n}})$	0.89
IM inertia	J	$0.01\,\mathrm{kg\,m}^2$
IM stator resistance	R_{s}	$0.7\,\Omega$
IM rotor resistance	R_{r}	$0.6\,\Omega$
IM mut. inductance	M_{sr}	$0.20\,\mathrm{H}$
IM stator inductance	L_{s}	$0.21\,\mathrm{H}$
IM rotor inductance	L_{r}	$0.24\,\mathrm{H}$
IM leakage coefficient	σ	0.093
choke dc-resistance	$R_{1,\mathrm{dc}}$, $R_{2,\mathrm{dc}}$	$0.03\,\Omega$
choke ac-resistance	$R_{1,\mathrm{ac,w}}$, $R_{2,\mathrm{ac,w}}$	$0\,\Omega$
choke magnetizing resistance	$R_{\mathrm{ac,m}}$	$0.86\,\Omega$
choke mutual inductance	M_{12}	$1.2\,\mathrm{mH}$
choke stray inductance	$L_{1,\sigma}$, $L_{2,\sigma}$	$20\,\mu\mathrm{H}$
choke sat. current	i_{sat}	$7\,\mathrm{A}$
MPC sample time	$T_{\mathrm{s,c}}$	$10\,\mu\mathrm{s}$
MPC choke sat. current	$i_{\mathrm{sat,c}}$	$3.5\,\mathrm{A}$

Table B.2.: Parameters for loss estimation of interleaving choke, DC-link and MOSFETs.

Name	**Nomenclature**	**Value**
DC-link capacitors		
ESR of electrolytic caps	R_{ser}	$31\,\text{m}\Omega$
ESR of foil caps	R_{ser}	$11\,\text{m}\Omega$
interleaving chokes [92]		
core material		*Mf 102*
core sat. flux density	B_{sat}	$320\,\text{mT}$
core magnetic resistance	$R_{\text{m,core}}$	$185\,\text{kH}^{-1}$
eff. length of mag. path	l_{eff}	$354\,\text{mm}$
eff. cross-section	A_{eff}	$840\,\text{mm}^2$
air gap	δ	$1.5\,\text{mm}$
sat. current	i_{sat}	$7\,\text{A}$
MSE parameter for f	a	1.34
MSE parameter for B	b	2.20
MSE parameter for scaling	k	0.0023
MOSFETs [24]		
On-resistance	R_{on}	$80\,\text{m}\Omega$
Turn-on losses	E_{on}	$0.3\,\mu\text{J/AV}$ (assuming linear dependency on $V_{\text{dc}}, i_{\text{ds}}$) @ minimal gate resistance according to datasheet, $V_{\text{gs}} = 18\,\text{V}$
Turn-off losses	E_{off}	$0.1\,\mu\text{J/AV}$ (assuming linear dependency on $V_{\text{dc}}, i_{\text{ds}}$) @ minimal gate resistance according to datasheet, $V_{\text{gs}} = 18\,\text{V}$

Control Parameters for Interleaved System

The following tables give an overview on the configurations of respective simulations for the interleaved inverter system. Explicitly, Table B.3 provides the standard tuning for all of the derived cost function terms. On the other hand, Table B.4 summarizes which cost terms are in fact activated for the respective simulations. The entries have the following meanings:

- ”std.”: Indicates that the cost term is active and has standard tuning according to Table B.3.
- ”sweep”: Indicates that the cost terms tuning is swept.
- ”n/a”: Indicates that the cost term is inactive.
- ”dev.”: Indicates that the cost term is active, but the mode or tuning deviates from the standard tuning. The deviated tuning is provided in the respective figure’s legend and/or in its accompanying text.

Table B.3.: Standard tuning of cost terms for simulations of interleaved system.

$\lambda_{T,2}$	λ_{sw}	λ_{sat}	$\lambda_{magmode}$	$\lambda_{sw,ovv}$
$1/(c/4+1)$	e^{-2}	$\lambda_{sat,1} = 5 \cdot 10^4$	$\lambda_{sat}/10$	$\lambda_{sat,1}/10$
$\lambda_{sw,dv/dt}$	$\lambda_{sw,loss}$	$\lambda_{sw,shift}$	λ_{cm}	λ_{cap}
$\lambda_{sat,1}/10$	e^{-2}	1	$\lambda_{sat,1}/10$	$4 \cdot 10^{-3}$

Table B.4.: Activated cost terms for simulations of interleaved system.

Figure	$J_{T,2}$	J_{sw}	J_{sat}	$J_{magmode}$	$J_{sw,ovv}$
4.18	std.	sweep	std.	Mode 1, std.	n/a
4.19	std.	sweep	std.	dev.	n/a
4.20	std.	sweep	std.	Mode 1, std.	dev.
4.21	std.	sweep	std.	Mode 1, std.	dev.
4.22	std.	sweep	std.	Mode 1, std.	ovv3, std.
4.23	std.	sweep	std.	Mode 1, std.	ovv3, std.
4.24	std.	n/a	std.	Mode 1, std.	ovv3, std.
4.25	std.	n/a	std.	Mode 1, std.	ovv3, std.
4.27	std.	n/a	std.	Mode 1, std.	ovv3, std.
4.28	std.	n/a	std.	Mode 1, std.	ovv3, std.
4.31	std.	n/a	std.	Mode 1, std.	ovv3, std.
4.32	std.	n/a	std.	Mode 1, std.	ovv3, std.
4.33	std.	n/a	std.	Mode 1, std.	ovv3, std.
4.35	std.	n/a	std.	Mode 1, std.	ovv3, std.
4.36	std.	n/a	std.	Mode 1, std.	ovv3, std.
4.37	std.	n/a	std.	Mode 1, std.	ovv3, std.
4.38	std.	sweep	std.	Mode 1, std.	ovv3, std.
4.42	std.	sweep	std.	Mode 1, std.	ovv3, std.

Figure	$J_{sw,dv/dt}$	$J_{sw,loss}$	$J_{sw,shift}$	J_{cm}	J_{cap}
4.18	n/a	n/a	n/a	n/a	n/a
4.19	n/a	n/a	n/a	n/a	n/a
4.20	n/a	n/a	n/a	n/a	n/a
4.21	n/a	n/a	n/a	n/a	n/a
4.22	dev.	n/a	n/a	n/a	n/a
4.23	n/a	n/a	n/a	dev.	n/a
4.24	dev.	sweep	n/a	n/a	n/a
4.25	dev.	sweep	n/a	n/a	n/a
4.27	std.	std.	dev.	n/a	n/a
4.28	std.	std.	dev.	n/a	n/a
4.31	std.	n/a	n/a	n/a	sweep
4.32	std.	sweep	n/a	n/a	sweep
4.33	std.	n/a	n/a	n/a	std.
4.35	std.	n/a	n/a	n/a	std.

4.36	std.	n/a	n/a	n/a	dev.
4.37	std.	n/a	n/a	n/a	dev.
4.38	std.	sweep	n/a	n/a	sweep
4.42	std.	n/a	n/a	n/a	n/a

Table B.5.: Activated cost terms for hardware runs of interleaved system.

Figure	$J_{T,2}$	J_{sw}	J_{sat}	$J_{magmode}$	$J_{sw,ovv}$
6.9	sweep	std.	std.	Mode 1, std.	ovv1, std.
6.10	std.	sweep	std.	Mode 1, std.	ovv1, std.
6.11	std.	n/a	std.	Mode 1, std.	ovv1, std.
6.12	std.	sweep	std.	Mode 1, std.	ovv1, std.
6.15	std.	sweep	std.	Mode 1, std.	ovv1, std.

Figure	$J_{sw,dv/dt}$	$J_{sw,loss}$	$J_{sw,shift}$	J_{cm}	J_{cap}
6.9	n/a	n/a	n/a	n/a	n/a
6.10	n/a	n/a	n/a	n/a	n/a
6.11	n/a	n/a	n/a	n/a	sweep
6.12	n/a	n/a	n/a	std.	n/a
6.15	std.	n/a	n/a	n/a	n/a

C. Supplementary Simulation Results

C.1. Supplementary Simulation Results for Regular Two-Level Inverter

In this section, additional simulation results to Section 4.2.7 are provided. The simulation runs are extended with the following operation points:

- No-load operation (OP1) and generator mode (OP2): As representative modes for alternative power factors $\cos(\varphi)$. The parameter customization is $T_\mathrm{e}^* = 0$ and $T_\mathrm{e}^* = -T_\mathrm{e,n}$, respectively. Please consider that the TDD of the torque for no-load operation is based on the rated torque.
- Reduced flux at nominal speed (OP3): As representative operation point for lowered modulation factors and for pointing out the validity of the proposed tuning rule for $\lambda_{\mathrm{T,circ,2}}$. This mode is also suitable for machine loss optimization with respect to optimal reference magnetization (cp. Section 3.2.4).The parameter customization is $\Psi_\mathrm{s}^* = 1/2 \cdot \Psi_\mathrm{s,n}$ and $T_\mathrm{e}^* = 1/2 \cdot T_\mathrm{e,n}$. Please note that the average switching frequency is significantly lower and the TDD minimum is reach well below $f_\mathrm{sw} = 18\,\mathrm{kHz}$, since many consecutive zero-voltage vectors are required du to the lowered modulation factor.
- Field-weakening mode (OP4): As representative mode for higher speeds. The parameter customization is $\omega_\mathrm{r} = 3/2 \cdot \omega_\mathrm{r,n}$, $\Psi_\mathrm{s}^* = 2/3 \cdot \Psi_\mathrm{s,n}$ and $T_\mathrm{e}^* = 2/3 \cdot T_\mathrm{e,n}$.
- Reduced voltage mode (OP5): As representative mode for high modulation factors, i.e. very low voltage margins for the controller. The parameter customization is $V_\mathrm{dc} = 600\,\mathrm{V}$. The low voltage margin leads to less switching activity: The voltage space vector leading to the strongest rotational movement of $\boldsymbol{\Psi}_\mathrm{s}$ has to be held for several controller time steps in order to maintain the requested torque.

Other than the customizations mentioned above, the simulation parameters are kept at rated values as provided in Appendix B. Clearly, a proper functioning and the quasi-interchangeability[1] between the MPCC and MMPFTC is maintained throughout the various points of operation.

[1] With respect to current TDD minimization.

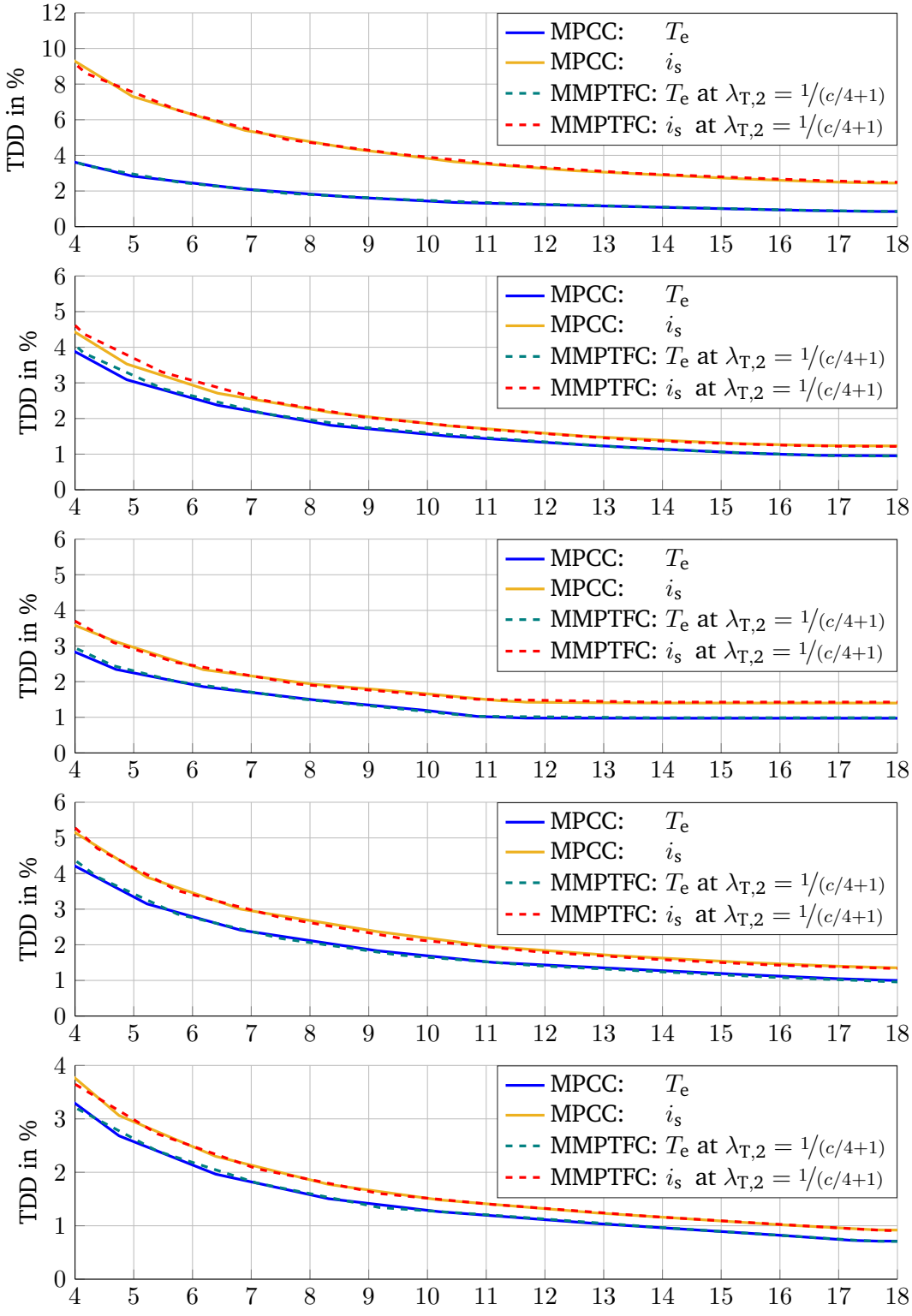


Figure C.1.: Performance of respective torque and stator current TDD minimization vs. average switching frequency at OP1 (top), OP2 (mid-top), OP3 (middle), OP4 (mid-bottom) and OP5 (bottom).

C.2. Supplementary Simulation Results for Interleaved Inverter with Different Choke Magnetization Modes

In this section, additional simulation results to Section 4.3.2 are provided. The simulation runs are extended with the following operation points:

- No-load operation (OP1): As representative modes for alternative power factors $\cos(\varphi)$. The parameter customization is $T_\mathrm{e}^* = 0$. Please consider that the TDD of the torque for no-load operation is based on the rated torque.
- Reduced speed (OP2): As representative operation point for lowered modulation factors. The parameter customization is $\omega_\mathrm{r} = {}^1\!/_4 \cdot \omega_\mathrm{r,n}$. Please note that the average switching frequency is significantly lower and the TDD minimum is reach well below $f_\mathrm{sw} = 18\,\mathrm{kHz}$, since many consecutive zero-voltage vectors are required du to the lowered modulation factor.

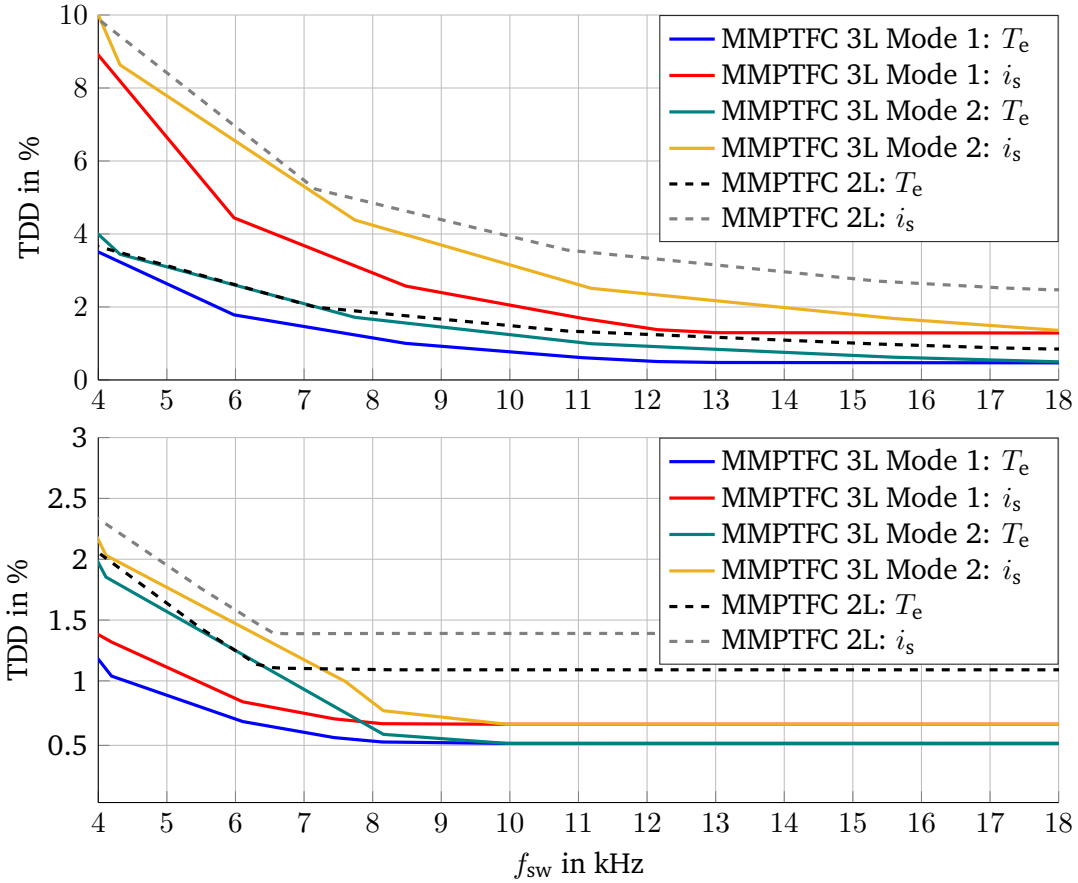


Figure C.2.: Performance of respective torque and stator current TDD minimization vs. average switching frequency. Comparing the MMPTFC principle for the regular two-level inverter with the interleaved inverter system with choke magnetizations Mode 1 and Mode 2 at OP1 (top) and OP2 (bottom).

Other than the customizations mentioned above, the simulation parameters are kept at rated values as provided in Appendix B. The results support the presumption that the choke magnetization Mode 1 is preferable over Mode 2.

C.3. Supplementary Simulation Results for Restraining of Over-Voltages during Transistor Turn-Off

In this section, additional simulation results to Section 4.3.3 are provided. Either the cost term $J_{\mathrm{sw,ovv3}}$ with $u_{\mathrm{ovv,off}} = 1.5$, or none of the introduced cost terms for restraining over-voltages is activated. The simulation runs are extended with the following operation points:

- No-load operation (OP1) and generator mode (OP2): As representative modes for alternative power factors $\cos(\varphi)$. The parameter customization is $T_{\mathrm{e}}^{*} = 0$ and $T_{\mathrm{e}}^{*} = -T_{\mathrm{e,n}}$, respectively. Please consider that the TDD of the torque for no-load operation is based on the rated torque.
- Reduced speed (OP3): As representative operation point for lowered modulation factors. The parameter customization is $\omega_{\mathrm{r}} = 1/4 \cdot \omega_{\mathrm{r,n}}$. Please note that the average switching frequency is significantly lower and the TDD minimum is reach well below $f_{\mathrm{sw}} = 18\,\mathrm{kHz}$, since many consecutive zero-voltage vectors are required du to the lowered modulation factor.

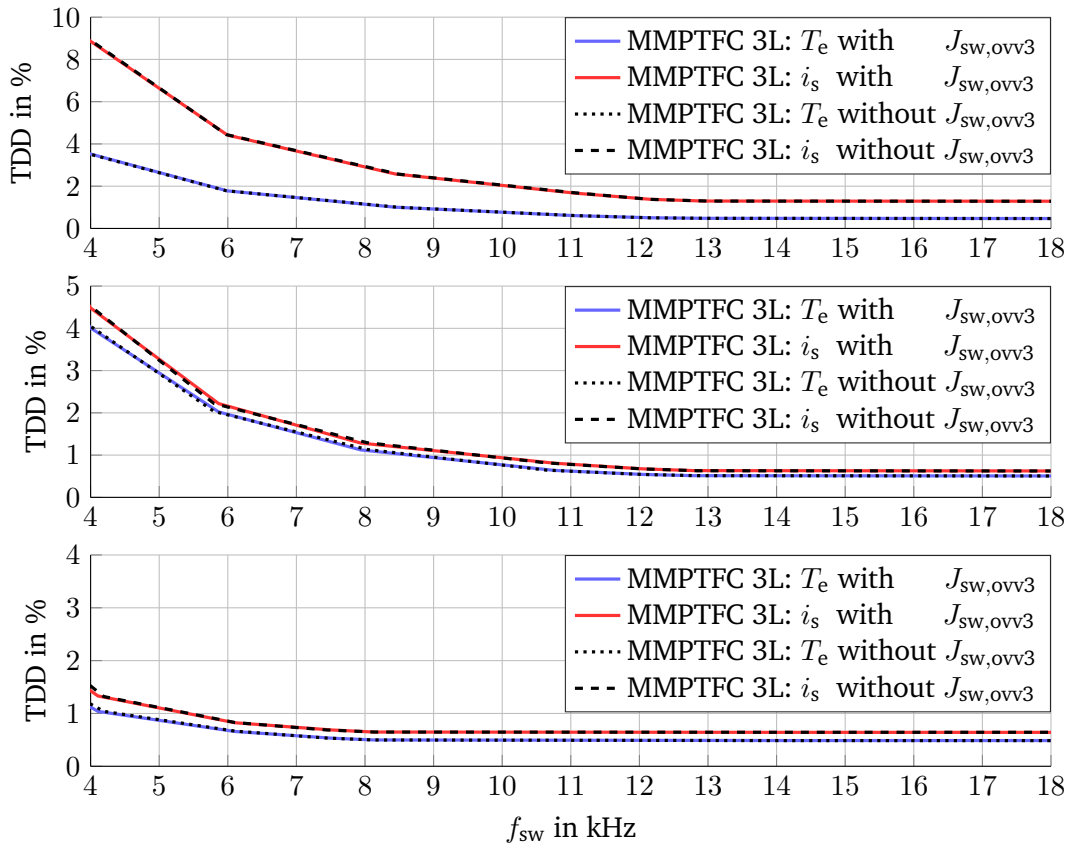


Figure C.3.: Performance of respective torque and stator current TDD minimization vs. average switching frequency for restraining transient over-voltages due to concurrent turn-off at OP1 (top), OP2 (middle) and OP3 (bottom).

Other than the customizations mentioned above, the simulation parameters are kept at rated values as provided in Appendix B. The results support the presumption that the cost term $J_{\mathrm{sw,ovv3}}$ does not impair machine control quality.

C.4. Supplementary Simulation Results for Reducing Large Voltage Steps at Machine Terminals

In this section, additional simulation results to Section 4.3.4 are provided. The simulation runs are extended with the following operation points:

- No-load operation (OP1) and generator mode (OP2): As representative modes for alternative power factors $\cos(\varphi)$. The parameter customization is $T_\mathrm{e}^* = 0$ and $T_\mathrm{e}^* = -T_\mathrm{e,n}$, respectively. Please consider that the TDD of the torque for no-load operation is based on the rated torque.

- Reduced speed (OP3): As representative operation point for lowered modulation factors. The parameter customization is $\omega_\mathrm{r} = {}^1\!/_4 \cdot \omega_\mathrm{r,n}$. Please note that the average switching frequency is significantly lower and the TDD minimum is reach well below $f_\mathrm{sw} = 18\,\mathrm{kHz}$, since many consecutive zero-voltage vectors are required du to the lowered modulation factor.

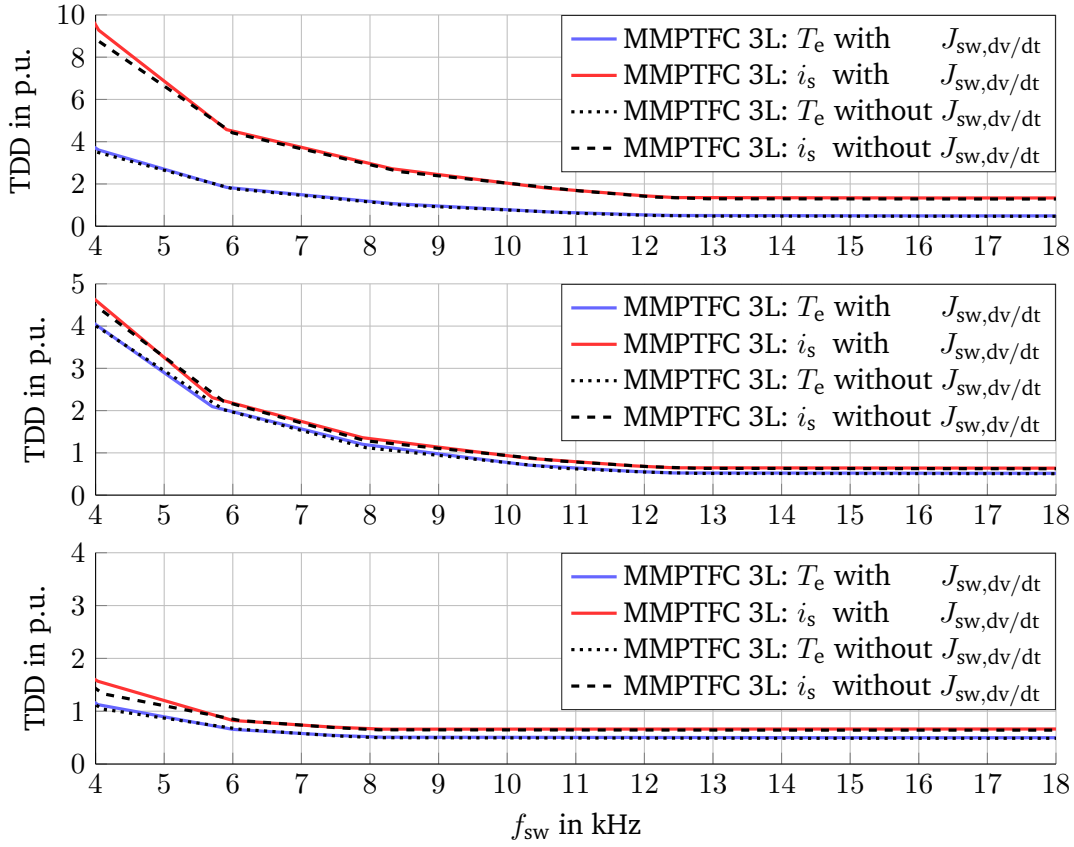


Figure C.4.: Performance of respective torque and stator current TDD minimization vs. average switching frequency for restraining transient phase-to-phase $\mathrm{d}v/\mathrm{d}t$ at OP1 (top), OP2 (middle) and OP3 (bottom).

Other than the customizations mentioned above, the simulation parameters are kept at rated values as provided in Appendix B. The results support the presumption that the cost term $J_\mathrm{sw,dv/dt}$ barley impacts the TDD minimization capability.

C.5. Supplementary Simulation Results for Minimization of Common-Mode Voltage

In this section, additional simulation results to Section 4.3.5 are provided. The simulation runs are extended with the following operation points:

- No-load operation (OP1) and generator mode (OP2): As representative modes for alternative power factors $\cos(\varphi)$. The parameter customization is $T_\mathrm{e}^* = 0$ and $T_\mathrm{e}^* = -T_\mathrm{e,n}$, respectively. Please consider that the TDD of the torque for no-load operation is based on the rated torque.

- Reduced speed (OP3): As representative operation point for lowered modulation factors. The parameter customization is $\omega_\mathrm{r} = {}^1\!/_4 \cdot \omega_\mathrm{r,n}$.

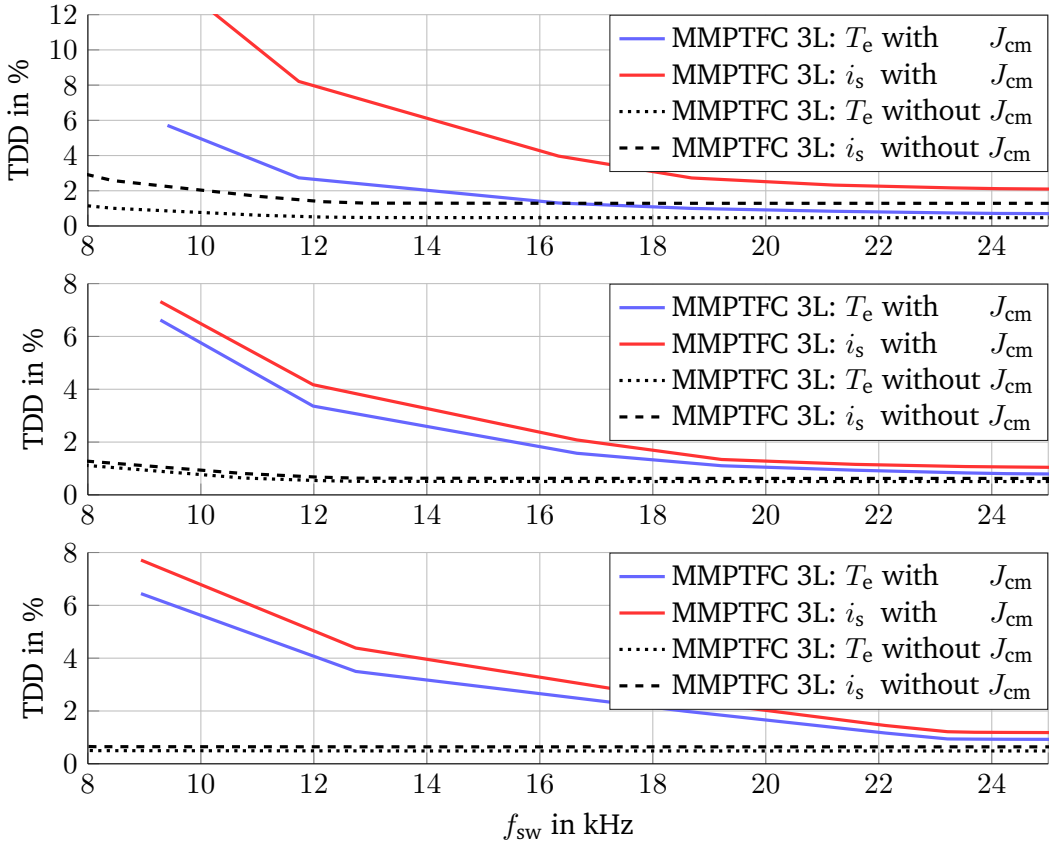


Figure C.5.: Performance of respective torque and stator current TDD minimization vs. average switching frequency for zero-voltage common-mode space vectors at OP1 (top), OP2 (middle) and OP3 (bottom).

Other than the customizations mentioned above, the simulation parameters are kept at rated values as provided in Appendix B. The results underpin the weaker performance of TDD minimization, as well as the necessity of high switching frequencies if J_cm is active. The zero common-mode voltage is however continuously maintained for every respective simulation.

C.6. Supplementary Simulation Results for Minimization of DC-link current

In this section, additional simulation results to Section 4.3.8 are provided. The simulation runs are extended with the following operation points:

- No-load operation (OP1) and generator mode (OP2): As representative modes for alternative power factors $\cos(\varphi)$. The parameter customization is $T_\mathrm{e}^* = 0$ and $T_\mathrm{e}^* = -T_\mathrm{e,n}$, respectively. Please consider that the TDD of the torque for no-load operation is based on the rated torque.
- Reduced speed (OP3): As representative operation point for lowered modulation factors. The parameter customization is $\omega_\mathrm{r} = 1/4 \cdot \omega_\mathrm{r,n}$.

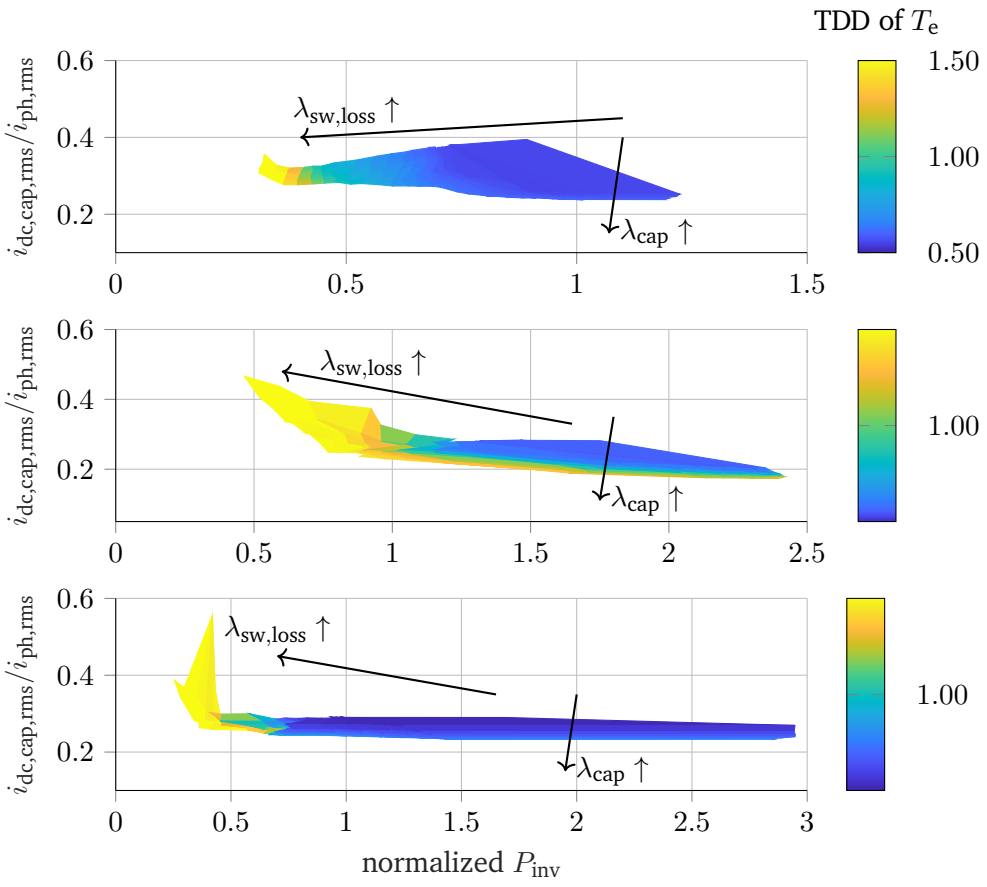


Figure C.6.: Performance of torque TDD minimization vs. rms-value of capacitor current and average inverter losses at OP1 (top), OP2 (middle) and OP3 (bottom).

Other than the customizations mentioned above, the simulation parameters are kept at rated values as provided in Appendix B. The switching losses are normalized with respect to the average losses occurring for J_sw at an average switching frequency of $f_\mathrm{sw} = 10\,\mathrm{kHz}$ at rated machine operation. The results accent the discussed trade-off in Section 4.3.8. However, the negative correlation between switching losses and DC-link optimization is distinctly less pronounced in the case of no-load operation, while the optimization potential of the DC-link via J_cap is significantly reduced for OP3.

D. Supplementary Hardware Measurements

D.1. Supplementary Hardware Measurements for Basic Machine Control

In this section, additional hardware measurements to Section 6.2.1 are provided. The hardware runs are extended with the following operation point:

- No-load operation (OP1): As representative mode for alternative power factors $\cos(\varphi)$. The parameter customization is $T_\mathrm{e}^* = 0$. Please consider that the TDD of the torque for no-load operation is based on the rated torque.

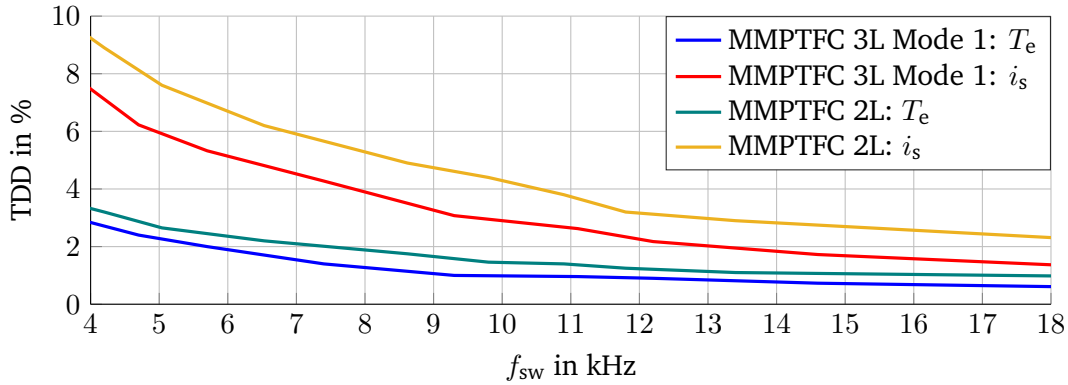


Figure D.1.: Hardware evaluation of performance for torque and stator current TDD minimization vs. average switching frequency at no-load machine operation. Comparing the MMPTFC principle for the regular two-level inverter with the interleaved inverter system with choke magnetization in Mode 1.

The results are generally in rather good accordance with the simulation results, albeit with the slightly deteriorated performance boost for the interleaved operation, which is also identified for the rated machine operation and discussed in Section 6.2.3.

D.2. Supplementary Hardware Measurements for Advanced Control Aiums

In this section, additional hardware measurements to the DC-link optimization of Section 6.2.2 are provided. The hardware runs are extended with the following operation point:

- No-load operation (OP1): As representative mode for alternative power factors $\cos(\varphi)$. The parameter customization is $T_\mathrm{e}^* = 0$. Please consider that the TDD of the torque for no-load operation is based on the rated torque.

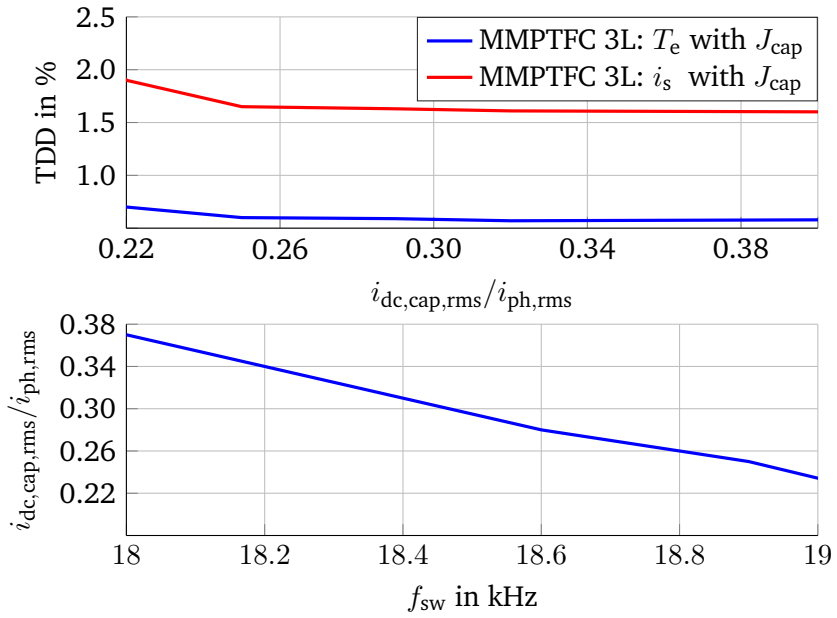


Figure D.2.: Hardware evaluation of performance for torque and stator current TDD minimization vs. rms-value of capacitor current (top) and rms-value of capacitor current vs. average switching frequency (bottom) at no-load operation.

The results are generally in rather good accordance with the simulation results, albeit with the slightly deteriorated performance boost for the interleaved operation, which is also identified for the rated machine operation and discussed in Section 6.2.3. Furthermore, the activation of J_cap does not imply a significant increase of f_sw as it is the case for rated machine operation.

List of Figures

List of Tables

Bibliography: Articles

[1] J. Sigg, M. Bruckmann, and P. Turkes, "The series connection of igbts investigated by experiments and simulation," in *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, IEEE, 1996, pp. 1760–1765, ISBN: 0-7803-3500-7. DOI: 10.1109/PESC.1996.548819.

[2] H. W. van der Broeck, H.-C. Skudelny, and G. V. Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Transactions on Industry Applications*, vol. 24, no. 1, pp. 142–150, 1988, ISSN: 00939994. DOI: 10.1109/28.87265.

[3] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "A high-performance generalized discontinuous pwm algorithm," *IEEE Transactions on Industry Applications*, vol. 34, no. 5, pp. 1059–1071, 1998, ISSN: 00939994. DOI: 10.1109/28.720446.

[6] Y. Beck, D. Medini, and S. Singer, "Magnetic topologies for distributed and interleaved switched converters," in *2008 IEEE 25th Convention of Electrical and Electronics Engineers in Israel*, IEEE, 12/3/2008 - 12/5/2008, pp. 338–342, ISBN: 978-1-4244-2481-8. DOI: 10.1109/EEEI.2008.4736717.

[7] A. K. Teeula and S. Kaboli, "A reliable and fast response buck converter based on interleaved converter," in *2019 27th Iranian Conference on Electrical Engineering (ICEE)*, IEEE, 4/30/2019 - 5/2/2019, pp. 804–807, ISBN: 978-1-7281-1508-5. DOI: 10.1109/IranianCEE.2019.8786512.

[8] T. Shimada, "Current sharing method using secondary voltage ripple for an interleaved llc resonant converter," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, IEEE, 9/3/2019 - 9/5/2019, P.1–P.7, ISBN: 978-9-0758-1531-3. DOI: 10.23919/EPE.2019.8915456.

[9] S. Ogasawara, J. Takagaki, H. Akagi, and A. Nabae, "A novel control scheme of a parallel current-controlled pwm inverter," *IEEE Transactions on Industry Applications*, vol. 28, no. 5, pp. 1023–1030, 1992, ISSN: 00939994. DOI: 10.1109/28.158825.

[10] A. Laka, J. A. Barrena, J. Chivite, and M. Rodriguez-Vidal, "Parallelization of two three-phase converters by using coupled inductors built on a single magnetic core," *Przeglad Elektrotechniczny*, vol. 89, pp. 194–198, 2013.

[11] G. in Park and S. I. Kim, "Modeling and analysis of multi-interphase transformers for connecting power converters in parallel," in *PESC97. Record 28th Annual IEEE Power Electronics Specialists Conference. Formerly Power Conditioning Specialists Conference 1970-71. Power Processing and Electronic Specialists Conference 1972*, 22-27 June 1997, pp. 1164–1170. DOI: 10.1109/PESC.1997.616895.

[12] A. M. Knight, J. Ewanchuk, and J. C. Salmon, "Coupled three-phase inductors for interleaved inverter switching," *IEEE Transactions on Magnetics*, vol. 44, no. 11, pp. 4119–4122, 2008, ISSN: 0018-9464. DOI: 10.1109/TMAG.2008.2004263.

[13] D. O. Boillat and J. W. Kolar, "Modeling and experimental analysis of a coupling inductor employed in a high performance ac power source," in *2012 International Conference on Renewable Energy Research and Applications (ICRERA)*, IEEE, 11/11/2012 - 11/14/2012, pp. 1–18, ISBN: 978-1-4673-2330-7. DOI: 10.1109/ICRERA.2012.6477401.

[14] C. Tan, D. Xiao, J. E. Fletcher, and M. F. Rahman, “Carrier-based pwm methods with common-mode voltage reduction for five-phase coupled inductor inverter,” *IEEE Transactions on Industrial Electronics*, vol. 63, no. 1, pp. 526–537, 2016, ISSN: 0278-0046. DOI: 10.1109/TIE.2015.2472815.

[17] G. Konstantinou, G. J. Capella, J. Pou, and S. Ceballos, “Single-carrier phase-disposition pwm techniques for multiple interleaved voltage-source converter legs,” *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4466–4474, 2018, ISSN: 0278-0046. DOI: 10.1109/TIE.2017.2767541.

[18] B. Vafakhah, J. Ewanchuk, and J. Salmon, “Multicarrier interleaved pwm strategies for a five-level npc inverter using a three-phase coupled inductor,” *IEEE Transactions on Industry Applications*, vol. 47, no. 6, pp. 2549–2558, 2011, ISSN: 00939994. DOI: 10.1109/TIA.2011.2168931.

[19] B. Hopfensperger, A. Daubner, F. Herrmann, and P. Mellor, “Investigation of shifted pwm methods for a dual three-phase system to reduce capacitor rms current,” in *PCIM Europe digital days July 2020*, Berlin: VDE VERLAG, pp. 124–131, ISBN: 978-3-8007-5245-4.

[20] H. Ye and A. Emadi, “An interleaving scheme to reduce dc-link current harmonics of dual traction inverters in hybrid electric vehicles,” in *APEC 2014*, New York: IEEE, 2014, pp. 3205–3211, ISBN: 978-1-4799-2325-0. DOI: 10.1109/APEC.2014.6803764.

[21] G.-J. Su and L. Tang, “A segmented traction drive system with a small dc bus capacitor,” in *IEEE Energy Conversion Congress and Exposition (ECCE), 2012*, Piscataway, NJ: IEEE, 9/15/2012 - 9/20/2012, pp. 2847–2853, ISBN: 978-1-4673-0803-8. DOI: 10.1109/ECCE.2012.6342375.

[22] Y. Huang, Y. Xu, W. Zhang, and J. Zou, “Pwm frequency noise cancellation in two-segment three-phase motor using parallel interleaved inverters,” *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2515–2525, 2019, ISSN: 0885-8993. DOI: 10.1109/TPEL.2018.2838764.

[23] N. Kesbia, J.-l. Schanen, L. Garbuio, and H. Alawieh, “An analytical model of the dc-link urrent ripple in multiphase pwm inverter,” in *PCIM Europe digital days July 2020*, Berlin: VDE VERLAG, pp. 711–715, ISBN: 978-3-8007-5245-4.

[25] A. Montazeri and G. Griepentrog, “New approach for optimizing inverter losses in finite control set model predictive control of induction machine, experimental evaluation,” in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, pp. 4001–4006. DOI: 10.1109/IECON.2019.8926637.

[29] S. Kim and D. P. Neikirk, “Compact equivalent circuit model for the skin effect,” in *1996 IEEE MTT-S International Microwave Symposium Digest*, IEEE, 17-21 June 1996, pp. 1815–1818, ISBN: 0-7803-3246-6. DOI: 10.1109/MWSYM.1996.512297.

[30] J. W. Kolar, “Analytical calculation of the rms current stress on the dc link capacitor of voltage dc link pwm converter systems,” in *9th International Conference on Electrical Machines and Drives*, IEE, 1-3 Sept. 1999, pp. 81–89, ISBN: 0 85296 720 9. DOI: 10.1049/cp:19990995.

[34] John Prymak, Peter Blais, William Buchanan, Edward Chen, and Boris Vildaver, “Capacitor eda models with compensations for frequency, temperature, and dc bias,” in *2010 Capacitor and Resistor Technology Symposium Proceedings*, Arlington, Va: Electronic Components Association, 2010.

[36] H. Wang, H. S.-H. Chung, and W. Liu, “Use of a series voltage compensator for reduction of the dc-link capacitance in a capacitor-supported system,” *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1163–1175, 2014, ISSN: 0885-8993. DOI: 10.1109/tpel.2013.2262057.

[38] H. Wang and F. Blaabjerg, “Reliability of capacitors for dc-link applications in power electronic converters—an overview,” *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3569–3578, 2014, ISSN: 1939-9367. DOI: 10.1109/TIA.2014.2308357.

[39] R. Wang, F. Wang, D. Boroyevich, and P. Ning, "A high power density single phase pwm rectifier with active ripple energy storage," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, IEEE, 2010. DOI: 10.1109/apec.2010.5433409.

[41] Z. Ye, T. Liu, M. Fuller, and G. Griepentrog, "Parameter identification of pmsm based on mras with considering nonlinearity of inverter," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, IEEE, 10/14/2019 - 10/17/2019, pp. 1255–1260, ISBN: 978-1-7281-4878-6. DOI: 10.1109/IECON.2019.8927595.

[44] V. Lesic, M. Vasak, G. Stojicic, N. Peric, G. Joksimovic, and T. M. Wolbank, "State and parameter estimation for field-oriented control of induction machine based on unscented kalman filter," in *2012 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM 2012)*, pp. 409–414. DOI: 10.1109/SPEEDAM.2012.6264421.

[46] M. Boesing, M. Niessen, T. Lange, and R. de Doncker, "Modeling spatial harmonics and switching frequencies in pm synchronous machines and their electromagnetic forces," in *2012 XXth International Conference on Electrical Machines*, IEEE, 2012. DOI: 10.1109/icelmach.2012.6350315.

[47] T. Lange, M. Boesing, and R. W. de Doncker, "Measurement-parameterized synchronous machine model with spatial-harmonics," in *2014 17th International Conference on Electrical Machines and Systems (ICEMS)*, IEEE, 10/22/2014 - 10/25/2014, pp. 3289–3295, ISBN: 978-1-4799-5162-8. DOI: 10.1109/ICEMS.2014.7014060.

[48] W. Bischof, B. Chatterjee, M. Boesing, M. Hennen, and R. Kennel, "Modeling inverter-fed three-phase squirrel-cage induction machines including spatial and temporal harmonics," in *2017 IEEE International Electric Machines and Drives Conference (IEMDC)*, IEEE, 5/21/2017 - 5/24/2017, pp. 1–8, ISBN: 978-1-5090-4281-4. DOI: 10.1109/IEMDC.2017.8002150.

[52] A. Binder, "Measures to cope with ac motor insulation stress due to igbt-inverter supply," in *6th International Conference on Power Electronics and Variable Speed Drives*, IEE, 23-25 Sept. 1996, pp. 569–574, ISBN: 0 85296 665 2. DOI: 10.1049/cp:19960976.

[54] R. M. Tallam, D. Leggate, D. W. Kirschnik, and R. A. Lukaszewski, "Reducing common-mode current: A modified space vector pulsewidth modulation scheme," *IEEE Industry Applications Magazine*, vol. 20, no. 6, pp. 24–32, 2014, ISSN: 1077-2618. DOI: 10.1109/MIAS.2013.2288376.

[55] P. Karamanakos and T. Geyer, "Guidelines for the design of finite control set model predictive controllers," *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 7434–7450, 2020, ISSN: 0885-8993. DOI: 10.1109/TPEL.2019.2954357.

[57] S. Kouro, P. Cortes, R. Vargas, U. Ammann, and J. Rodriguez, "Model predictive control—a simple and powerful method to control power converters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 1826–1838, 2009, ISSN: 0278-0046. DOI: 10.1109/TIE.2008.2008349.

[63] P. Karamanakos, T. Geyer, and R. Kennel, "On the choice of norm in finite control set model predictive control," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 7105–7117, 2018, ISSN: 0885-8993. DOI: 10.1109/TPEL.2017.2756092.

[65] A. Bemporad, M. Morari, V. Dua, and E. N. Pistikopoulos, "The explicit solution of model predictive control via multiparametric quadratic programming," in *Proceedings of the 2000 American Control Conference. ACC (IEEE Cat. No.00CH36334)*, IEEE, 2000, 872–876 vol.2, ISBN: 0-7803-5519-9. DOI: 10.1109/ACC.2000.876624.

[66] A. Bemporad, F. Borrelli, and M. Morari, "Model predictive control based on linear programming - the explicit solution," *IEEE Transactions on Automatic Control*, vol. 47, no. 12, pp. 1974–1985, 2002, ISSN: 0018-9286. DOI: 10.1109/TAC.2002.805688.

[67] T. Geyer, "Computationally efficient model predictive direct torque control," *IEEE Transactions on Power Electronics*, vol. 26, no. 10, pp. 2804–2816, 2011, ISSN: 1941-0107. DOI: 10.1109/TPEL.2011.2121921.

[68] S. A. B. Khalid, E. Liegmann, P. Karamanakos, and R. Kennel, "High-level synthesis of a long horizon model predictive control algorithm for an fpga," in *PCIM Europe digital days July 2020*, Berlin: VDE VERLAG, pp. 1544–1551, ISBN: 978-3-8007-5245-4.

[70] P. Karamanakos and T. Geyer, "Model predictive torque and flux control minimizing current distortions," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2007–2012, 2019, ISSN: 0885-8993. DOI: 10.1109/TPEL.2018.2862253.

[71] T. Geyer, "Algebraic tuning guidelines for model predictive torque and flux control," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 4464–4475, 2018, ISSN: 00939994. DOI: 10.1109/TIA.2018.2835375.

[72] V. Pratt, "Direct least-squares fitting of algebraic surfaces," *ACM SIGGRAPH Computer Graphics*, vol. 21, no. 4, pp. 145–152, 1987, ISSN: 0097-8930. DOI: 10.1145/37402.37420.

[74] A. Montazeri and G. Griepentrog, "Explicit consideration of inverter losses in the cost function for finite control set model predictive control of induction machine, experimental results," in *2019 IEEE 28th International Symposium on Industrial Electronics (ISIE)*, pp. 521–526. DOI: 10.1109/ISIE.2019.8781320.

[76] D. Jiang, Z. Shen, and F. Wang, "Common-mode voltage reduction for paralleled inverters," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3961–3974, 2018, ISSN: 1941-0107. DOI: 10.1109/TPEL.2017.2712369.

[78] F. Grimm and M. Baghdadi, "Variable switching point model predictive control for dc-link capacitance minimization of back-to-back converters," in *2020 27th International Workshop on Electric Drives: MPEI Department of Electric Drives 90th Anniversary (IWED)*, 2020, pp. 1–6. DOI: 10.1109/IWED48848.2020.9069557.

[79] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *2002 IEEE Workshop on Computers in Power Electronics, 2002. Proceedings*, IEEE / Institute of Electrical and Electronics Engineers Incorporated, 2002, pp. 36–41, ISBN: 0-7803-7554-8. DOI: 10.1109/CIPE.2002.1196712.

[80] N. Stati, M. Abdelrahem, M. H. Mobarak, and R. Kennel, "Finite control set-model predictive control with on-line parameter estimation for variable-speed wind energy conversion systems," in *2016 International Symposium on Industrial Electronics (INDEL)*, pp. 1–6. DOI: 10.1109/INDEL.2016.7797775.

[83] P. Karamanakos, M. Nahalparvari, and T. Geyer, "Fixed switching frequency direct model predictive control with continuous and discontinuous modulation for grid-tied converters with lcl filters," *IEEE Transactions on Control Systems Technology*, pp. 1–16, 2020, ISSN: 1063-6536. DOI: 10.1109/TCST.2020.3008030.

[84] F. Grimm, Y. Li, X. Liu, and Z. Zhang, "Predictive control of back-to-back converters with dc-link capacitance minimization," in *2019 IEEE International Symposium on Predictive Control of Electrical Drives and Power Electronics (PRECEDE)*, 2019, pp. 1–6. DOI: 10.1109/PRECEDE.2019.8753202.

Bibliography: Books

[4] F. L. Luo and H. Ye, *Power electronics: Advanced conversion technologies*. Boca Raton, Fla.: CRC Press, 2010, ISBN: 9781420094299.

[5] M. H. Rashid, *Power electronics handbook: Devices, circuits, and applications handbook*, 3rd ed. Burlington, MA: Elsevier, 2010, ISBN: 9780123820365. [Online]. Available: http%3A//www.worldcat.org/oclc/704241788.

[26] T. Brander, A. Gerfer, B. Rall, and H. Zenkner, Eds., *Trilogie der induktiven Bauelemente: Applikationshandbuch für EMV-Filter, getaktete Stromversorgungen & HF-Schaltungen*, 5. überarbeitete und erweiterte Auflage. Künzelsau: Swiridoff Verlag, November 2019, ISBN: 9783899291513.

[32] W. Mathis and A. Reibiger, *Küpfmüller Theoretische Elektrotechnik: Elektromagnetische Felder, Schaltungen und elektronische Bauelemente*, 20., aktualisierte Auflage 2017. Berlin, Heidelberg: Springer Berlin Heidelberg, 2017, ISBN: 9783662548370. [Online]. Available: http://nbn-resolving.org/urn:nbn:de:bsz:31-epflicht-1506212.

[33] Semikron, *Application manual power semiconductors*. Ilmenau: ISLE-Verl., 2015, ISBN: 978-3-938843-83-3. DOI: Arendt.

[37] *Increasing the life of electrolytic capacitor banks using integrated high performance film capacitors*. 2013. [Online]. Available: https://ppmpower.co.uk/wp-content/uploads/increasing-life-electrolytic-capacitor-banks-integrated-high-performance-film-cap.pdf.

[40] Rik De Doncker, Duco W. J. Pulle, and André Veltman, *Advanced electrical drives: Analysis, modeling, control* (Power Systems), 1st ed. Berlin et al.: Springer-Verlag, 2011, ISBN: 978-94-007-0179-3.

[42] D. Simon, *Optimal state estimation: Kalman, H [infinity], and nonlinear approaches*. Hoboken, NJ: Wiley-Interscience, 2006, ISBN: 0471708585. DOI: 10.1002/0470045345. [Online]. Available: http://site.ebrary.com/lib/alltitles/docDetail.action?docID=10308111.

[43] R. Marchthaler and S. Dingler, *Kalman-Filter: Einführung in die Zustandsschätzung und ihre Anwendung für eingebettete Systeme* (Lehrbuch). Wiesbaden: Springer Vieweg, 2017, ISBN: 978-3-658-16728-8. [Online]. Available: http://www.springer.com/.

[45] A. Binder, *Elektrische Maschinen und Antriebe: Grundlagen, Betriebsverhalten*, 2. Aufl. 2017. Berlin, Heidelberg: Springer Berlin Heidelberg, 2018, ISBN: 9783662532416. [Online]. Available: http://nbn-resolving.org/urn:nbn:de:bsz:31-epflicht-1506482.

[49] A. M. Trzynadlowski, *Control of induction motors* (Academic Press series in engineering). San Diego: Academic Press, 2001, ISBN: 9780080503080. [Online]. Available: https://search.ebscohost.com/login.aspx?direct=true&scope=site&db=nlebk&db=nlabk&AN=230864.

[51] N. Ida, *Engineering electromagnetics*, Fourth edition. Cham: Springer, 2021, ISBN: 9783030155575. [Online]. Available: https://ebookcentral.proquest.com/lib/kxp/detail.action?docID=6455926.

[56] J. Rodríguez Pérez and P. C. Estay, *Predictive control of power converters and electrical drives*. Chichester, West Sussex and s.l.: IEEE, 2012, ISBN: 9781119963981. [Online]. Available: http://ieeexplore.ieee.org/servlet/opac?bknumber=6198919.

[58] D. Schröder and J. Böcker, Eds., *Elektrische Antriebe – Regelung von Antriebssystemen*, 5. Aufl. 2021, neu bearb. Berlin, Heidelberg: Springer Berlin Heidelberg, 2021, ISBN: 9783662627006. [Online]. Available: http://nbn-resolving.org/urn:nbn:de:bsz:31-epflicht-1866218.

[59] J. Adamy, *Systemdynamik und Regelungstechnik* (Berichte aus der Steuerungs- und Regelungstechnik). Aachen: Shaker Verlag, (2007), ISBN: 978-3-8322-6002-6.

[60] E. D. Sontag, *Mathematical control theory: Deterministic finite dimensional systems* (Texts in applied mathematics), 2nd ed. Berlin: Springer, 2006, vol. 6, ISBN: 9780387984896.

[61] *Numerical methods for ordinary differential equations*. Chichester: Wiley, 2005, ISBN: 0470868279. DOI: 10.1002/0470868279. [Online]. Available: http://onlinelibrary.wiley.com/book/10.1002/0470868279.

[64] G. Sierksma and Y. Zwols, *Linear and integer optimization: Theory and practice* (Advances in applied mathematics), Third edition. Boca Raton, FL: Chapman and Hall/CRC, an imprint of Taylor and Francis, 2015, ISBN: 9781498743129. [Online]. Available: https://ebookcentral.proquest.com/lib/kxp/detail.action?docID=5148571.

[69] *Model Predictive Control of High Power Convertersand Industrial Drives*. John Wiley & Sons, Ltd, 2016.

[75] *Elementary Functions: Algorithms and Implementation* (SpringerLink Bücher), Second Edition. Boston, MA: Birkhäuser Boston, 2006, ISBN: 9780817644086. DOI: 10.1007/b137928.

[85] K. Wüst, *Mikroprozessortechnik: Grundlagen, Architekturen, Schaltungstechnik und Betrieb von Mikroprozessoren und Mikrocontrollern* (SpringerLink Bücher), 4., aktualisierte und erweiterte Auflage. Wiesbaden: Vieweg+Teubner, 2011, ISBN: 9783834898814. DOI: 10.1007/978-3-8348-9881-4.

Bibliography: PhD Theses

[28] E. S. Smailus, "Konzepte zur verbesserung des teillastwirkungsgrades von dab-wandlern," Ph.D. dissertation, TU Darmstadt, Darmstadt, 2021. DOI: 10.26083/TUPRINTS-00019648.

[53] M. Weicker, "Gleichtakteffekte bei umrichtergespeisten elektromotoren," Ph.D. dissertation, TU Darmstadt, Darmstadt, 2021. DOI: 10.26083/TUPRINTS-00019145.

[73] A. Montazeri Najafabadi, "Efficiency optimization of induction machine drives with model predictive control," Ph.D. dissertation, TU Darmstadt, Darmstadt, 2021. DOI: 10.26083/tuprints-00017562.

[91] D. Drozhzhin, "Consideration of electromagnetic noise during design of inverter for transportation applications," Ph.D. dissertation, TU Darmstadt, Darmstadt, 2020. DOI: 10.25534/TUPRINTS-00012789.

Bibliography: Datasheets and Company Websites

[24] Rohm Semiconductor, *Datasheet sct2080ke*. [Online]. Available: https://fscdn.rohm.com/en/products/databook/datasheet/discrete/sic/mosfet/sct2080ke-e.pdf.

[27] TDK, *Ferrites and accessories: Siferrit material n87*. [Online]. Available: https://www.tdk-electronics.tdk.com/download/528882/71e02c7b9384de1331b3f625ce4b2123/pdf-n87.pdf.

[86] Xilinx, *Zynq-7000 soc overview*. [Online]. Available: https://docs.xilinx.com/v/u/en-US/ds190-Zynq-7000-Overview.

[87] Xilinx, *7 series fpgas configurable logic block user guide*. [Online]. Available: https://docs.xilinx.com/v/u/en-US/ug474_7Series_CLB.

[88] Xilinx, *7 series dsp48r1 slice user guide*. [Online]. Available: https://docs.xilinx.com/v/u/en-US/ug479_7Series_DSP48E1.

[89] MathWorks, *Hdl coder*. [Online]. Available: https://mathworks.com/products/hdl-coder.html.

[90] Avnet, *Zedboard - complete development kit for designers*. [Online]. Available: https://www.avnet.com/wps/portal/us/products/avnet-boards/avnet-board-families/zedboard.

[92] Tridelta Weichferrite, *Datasheet manifer 102*. [Online]. Available: https://www.tridelta-weichferrite.de/fileadmin/user_upload/manifer_102.pdf.

[93] Analog Devices, *Datasheet ad7403*. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/AD7403.pdf.

Bibliography: Own Publications and Supervised Student Theses

[15] M. Fuller, G. Griepentrog, and H. Wang, "Economical implementation of model predictive control for minimization of current and torque distortions in induction machines," in *PCIM Europe*, Berlin: VDE VERLAG, 2022, pp. 1374–1383, ISBN: 978-3-8007-5822-7. DOI: 10.30420/565822191.

[16] M. Fuller, G. Griepentrog, O. Koenig, and B. Pariti, "Design and evaluation of finite control set model predictive control of interleaved inverter topology with induction machine," in *PCIM Europe digital days July 2020*, Berlin: VDE VERLAG, pp. 124–131, ISBN: 978-3-8007-5245-4.

[31] M. Fuller, G. Griepentrog, and O. Koenig, "Linear and nonlinear programming approach for dc-link current optimization applied to interleaved inverters," in *Electromechanical Drive Systems 2021; ETG Symposium*, 2021, pp. 1–7.

[50] N. Niemuth, "Wirkungsgradoptimierung bei umrichtergespeisten asynchronmaschinen mit vorgeschalteten interleaving drosseln mittels modellprädiktiver regelung," Masterarbeit, TU Darmstadt, Darmstadt, 19.10.2020.

[62] H. Wang, "Design of a model predictive control for induction machines with soft transition between low-torque and low-current-thd," Masterarbeit, TU Darmstadt, Darmstadt, 14.09.2021.

[81] Johann Mesin, "Realisierung und evaluierung eines kalman-filters zur regelung einer asynchronmaschine mittels wechselrichtern mit interleaving-zuständen," Masterarbeit, TU Darmstadt, Darmstadt, 10.04.2019.

[82] D. Pavlovic, "Realisierung und evaluierung eines nichtlinearen beobachters zur erhöhung der regelgüte bei asynchronmaschinen mit vorgeschalteten interleaving-drosseln," Masterarbeit, Darmstadt, TU Darmstadt, 2.07.2020.

[94] Martin Flath, "Strategien zur ripple-reduzierung im zwischenkreis von parallelgeschalteten wechselrichtern mittels modellprädiktiver regelung," Masterarbeit, TU Darmstadt, Darmstadt, 19.05.2021.

[95] Dennis Freischlader, "Analyse und implementierung von regelungsverfahren für asynchronmaschinen mit über interleaving-drosseln parallel geschalteten wechselrichtern," Masterarbeit, TU Darmstadt, Darmstadt, 21.04.2020.

[96] M. Fuller, "Model predictive control eines 2 x dreiphasigen wechselrichters mit zwischengeschalteten interleaving-drosseln," Masterarbeit, TU Darmstadt, Darmstadt, 22.12.2017.

[97] Y. Hao, "Predictive frequency spectrum shaping for torque controlled induction machines," Masterarbeit, TU Darmstadt, Darmstadt, 18.08.2020.

[98] Ehsan Sharifian, "Field-oriented motion control of pwm-assisted synchronous reluctance motors for low-voltage electric vehicles," Masterarbeit, TU Darmstadt, Darmstadt, 23.02.2021.

[99] Z. Ye, "Parameter identification of pmsm based on mrac with considering nonlinearity of the drive system," Masterarbeit, TU Darmstadt, Darmstadt, 20.06.2019.