Chapter 5

Analysis of large-scale production of CNTFETs and applications for future industrial use

In 2008, the time at which this dissertation is written, numerous papers are available on CNTFETs with sophisticated features, like several gates, high-κ dielectric or advanced electrode materials. However, nearly all papers only report on individual single devices, i.e. prototypes with probably very long fabrication time. Perhaps they cannot be fabricated twice. Except for [106], no publications are available on the large scale fabrication of CNTFETs, even with simple back gated devices. Hardly any data is available on yield, reproducibility or reliability.

In basic research on nanoelectronic devices for future generations of integrated circuits, two important aspects must be studied. First, new concepts must be developed. Their feasibility must be demonstrated, their theoretical and experimental limits investigated. In the research on nanotube electronics, it has been shown that s-SWNTs can act as the channel in field-effect transistors. In contrast to graphene FETs, devices with high on/off ratio have been demonstrated using carbon nanotubes. The second aspect in nanoelectronic research as in engineering science generally is the demonstration of fabrication feasibility, i.e., the investigation of the possibility of transferring to large scale fabrication and integration of the devices. The reproducibility and the reliability must also be investigated, as well as the degradation of the electrical characteristics within a period of time. To evaluate the possibility of integrating new devices in industrial processes, a statistical evaluation of relevant parameters must be performed.

The self-aligned fabrication process for Pd contacted and PMMA-passivated CNTFETs reported in the previous chapter enables the production of almost one thousand devices on a single wafer in only a few days, using standard CMOS equipment. To perform an evaluation with statistical relevance of the CNTFETs, more than 20 wafers have been produced. The results of these experiments and measurements are reported in this chapter (see also list of publications and conference contributions, 3).

5.1 Statistical evaluation of CNTFET fabrication process.

5.1.1 Definitions and framework of statistical evaluation.

To perform the statistical evaluation of the process for PMMA passivated CNTFETs reported in the previous chapter, eight wafers out of more than 20 wafers were selected. The eight wafers belong to two different batches: lot TT, produced in August 2007 and lot FRA, produced in January 2008.

- **On six wafers:** one complete chip (102 devices) of the regular chips (see Fig. 4.1a top right corner and b) is measured. The chip is always chosen at the same location near the center of the wafer. Approximately 8% of the devices are found to be defective due to process failure, inducing e.g. dielectric breakdown under one contact, absence of contact or presence of particles between the layers.
- **On two wafers:** only two thirds of the devices of the regular chip situated near the center of the wafer could be measured due to adhesion problems of the Pd contacts. The problems probably resulted from some resist residuals after development.

The statistics presented below are only based on CNTFETs without process failure because the goal is to evaluate the yield of *in situ* growth process and not the quality of standard processing techniques like optical lithography which are well-known and would quickly be improved with more advanced equipment in industry.

The total number of CNTFET devices which are taken for statistical evaluation is 647. The 647 CNTFETs have a nominal channel width (S/D width) ranging from 5 to 50 μm and a nominal channel length (S/D spacing) between 1.6 and 6 μm. The evaluation of each transistor is based on the transfer characteristics measured at V_{ds} = -400 mV and a gate voltage ranging from -3 and 3 V. According to their current in the on-state (at negative gate voltages) and off-state (at positive gate voltages), the devices are classified into four groups: "high on/off ratio", "small on/off ratio", "metallic" and "no link". Table 5.1 gives the definition of these groups. The

on-current	on/off ratio	device type
< 1 nA	~ 1	no link
≥ 1 nA	$\geq 10^3$	high on/off ratio
≥ 1 nA	$\in [2; 10^3[$	small on/off ratio
≥ 1 nA	< 2	metallic

Table 5.1: Classification of CNTFETs according to their transfer characteristics.

group "no link" corresponds to the devices with on-currents well below 1 nA, typically below 10 pA. These devices are basically defective because no SWNT links source and drain: source and drain are open. The devices are labeled in this work as "non-working devices". The three other groups have been already described in the previous chapter (see subsection 4.3.3). The groups with high and small on/off ratios correspond both to devices which have clearly different current levels at positive and negative voltages. In high on/off ratio devices, the link between source and drain is composed exclusively of s-SWNTs, probably a single s-SWNT (see the end of subsection 4.3.3). In small on/off ratio devices, either the link between S/D is formed by a single larger diameter SWNT inducing a smaller band gap or, most likely, the S/D link is a mixture of one metallic and one semiconducting SWNTs. The fourth class of devices, called "metallic", includes devices for which the gate voltage has no or very little influence on the current, i.e., their current on/off ratio is below 2. However, **only devices with high on/off ratio are good quality devices** and suitable for applications in CMOS technology (as a replacement for MOSFET for example).

To evaluate our *in situ* fabrication process, three different "indicators" are calculated and compared:

- the percentage of functional devices (with any sort of SWNT(s) link between S/D) within all measured devices, it is called here "process yield". It gives an indication on the accuracy of the SWNT growth, especially on the SWNT density.

- the part of good quality devices (with high on/off ratio) within all measured devices, which is essential to evaluate the suitability of the process.

- the distribution of device types (metallic, high or small on/off ratio) within the functional devices which gives an indication on the selectivity (semiconducting over metallic) of the *in situ* growth of SWNTs.

5.1.2 Process yield, good quality devices percentage and device type distribution.

In the 647 measured devices, only 188 do not show any current between source and drain leading to a process yield of 71% (see Fig. 5.1). The individual process yield for each of the eight wafers is given in Table 5.2. The yield is found to fluctuate between 61 and 81% depending on the wafer. A small fluctuation in the thickness of the catalyst could explain these changes because catalyst thickness strongly influences SWNT density, and thus the probability of S/D link.

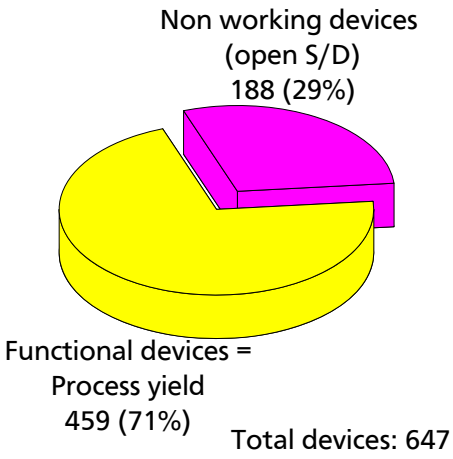


Figure 5.1: Process yield, all wafers together.

wafer name	functional devices %	devices with open S/D %
TT30	75	25
TT32	71	29
TT33	68	32
FRA2	62	38
FRA3	69	31
FRA4	80	20
FRA5	61	39
FRA9	81	19

Table 5.2: Process yield for each of the eight wafers.

Accordingly, 459 devices are found to have some kind of functionality, i.e., one or several SWNTs connecting source and drain. The distribution of the device type within these 459 devices is given in Fig. 5.2. As a result, 58% of the functional devices show high on/off ratio.

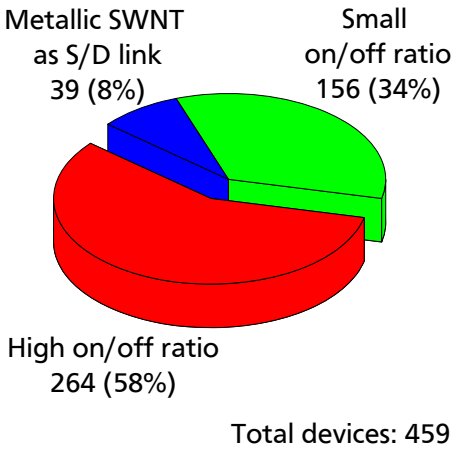


Figure 5.2: Distribution of device type within functional devices.

wafer name	high on/off ratio %	small on/off ratio %	m-SWNT as S/D link %
TT30	78	22	0
TT32	70	21	7
TT33	60	26	14
FRA2	51	39	10
FRA3	64	36	0
FRA4	36	46	18
FRA5	73	20	7
FRA9	43	48	9

Table 5.3: Distributions of device type, for each of the eight wafers.

However, the distribution is fluctuating from one wafer to the other. The same explanation as

for fluctuations in the number of devices with at least one SWNT link is assumed: The aluminum and nickel thicknesses probably fluctuate causing deviation in the SWNT density.

Lastly, the quantity of good quality devices (fully functional high on/off ratio devices) within all measurable CNTFETs (i.e., without damaging due to the process) is a very important indicator. Based on the measurement of the 647 devices mentioned previously, 41% of the devices exhibit high on/off ratios (see Fig. 5.3). Looking at the percentage for each of the eight wafers separately (Table 5.4), the part of high on/off ratio devices can reach almost 60%. This is a very satisfactory result for a first approach and considering university laboratory equipment. Numerous improvements, such as an even more precise control of the catalyst thickness or a better optimization of the gas mixture/growth time, could increase the percentage of high on/off ratio CNTFETs.

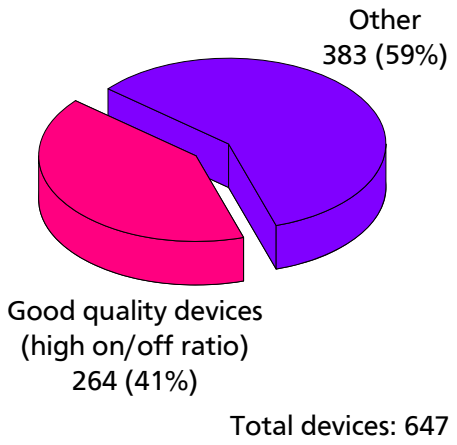


Figure 5.3: Distributions of good quality devices within all devices.

wafer	high on/off ratio %	other %
TT30	59	41
TT32	50	50
TT33	41	59
FRA2	32	68
FRA3	44	56
FRA4	29	71
FRA5	45	55
FRA9	35	65

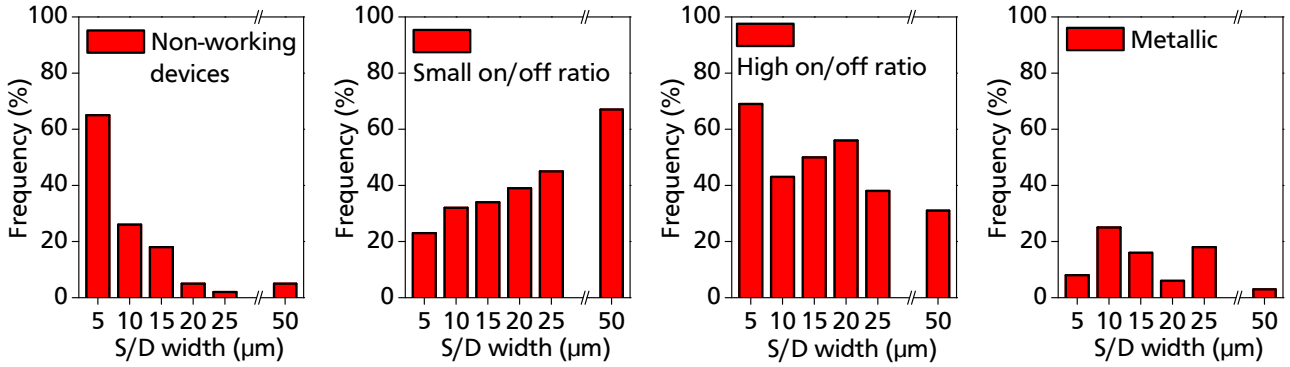
Table 5.4: Distributions of good quality devices within all devices, for each of the eight wafers.

The yield of the novel fabrication process reported in this work should be compared to similar assignments. Unfortunately, comparable statistics made by other research groups could not be found in literature. Tseng and co-workers who also report on a large scale fabrication of CNTFETs, do not mention any percentage of working devices [106]. Apparently, their process leads to the fabrication of devices in which it is very probable that several SWNTs link source and drain, reducing probably the yield of good quality (high on/off ratio) transistors.

5.1.3 Influence of device geometry on process yield and device type distribution.

In the last subsection, the calculations of process yield, part of good quality devices and distribution of device type were performed on devices including all different nominal channel lengths and widths. This gives a first impression on the quality of the process reported here. However, it sounds logical that the yield of the process fluctuates according to the parameters of the designed device geometries and this also needs to be investigated.

First, Fig. 5.4a shows the influence of the nominal channel width on the percentage of non-working devices. As expected, the part of devices without any SWNT as channel reduces drastically with increasing S/D width. This is easily explainable: The wider the electrodes, the higher



(a) Non-working devices within all devices.

(b) Devices with small on/off ratio **within working devices**.

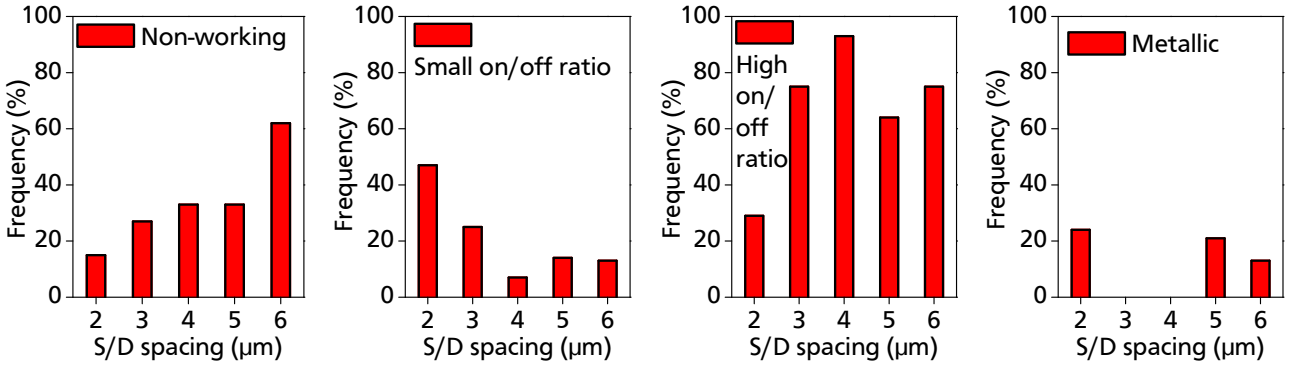
(c) Devices with high on/off ratio **within working devices**.

(d) Devices with m-SWNT as S/D link **within working devices**.

Figure 5.4: Dependency of non-working device percentage with nominal device channel width (Fig. 5.4a). Dependency of device type distribution with nominal device channel width (Fig. 5.4b, Fig. 5.4c and Fig. 5.4d). S/D spacing: 2 to 3 μm, considered here as equivalent. Total devices: 231, working devices: 185.

the probability that at least one SWNT forms a link. Furthermore, Fig. 5.4b to c shows the distribution of devices within the working ones. The part of small on/off ratio devices also increases with increased S/D width for the same reason. Indeed, it is more probable that several SWNTs are contacted when the S/D electrodes are wider. However, the percentage of devices with high on/off ratio remains constantly high and the percentage of devices with metallic behavior remains constantly low, again confirming the robustness of the *in situ* process.

A summary of the influence of the nominal channel length (S/D spacing) on device functionality is given in Fig. 5.5. Similarly to the S/D width influence, the S/D spacing affects the



(a) Non-working devices within all devices.

(b) Devices with small on/off ratio **within working devices**.

(c) Devices with high on/off ratio **within working devices**.

(d) Devices with m-SWNT as S/D link **within working devices**.

Figure 5.5: Evolution of the process yield (Fig. 5.5a) and the devices distribution (Fig. 5.5b, Fig. 5.5c and Fig. 5.5d) with increasing S/D spacing (nominal channel length). S/D width: 10,15 and 20 μm, considered here as equivalent. Total devices: 105, working devices: 69.

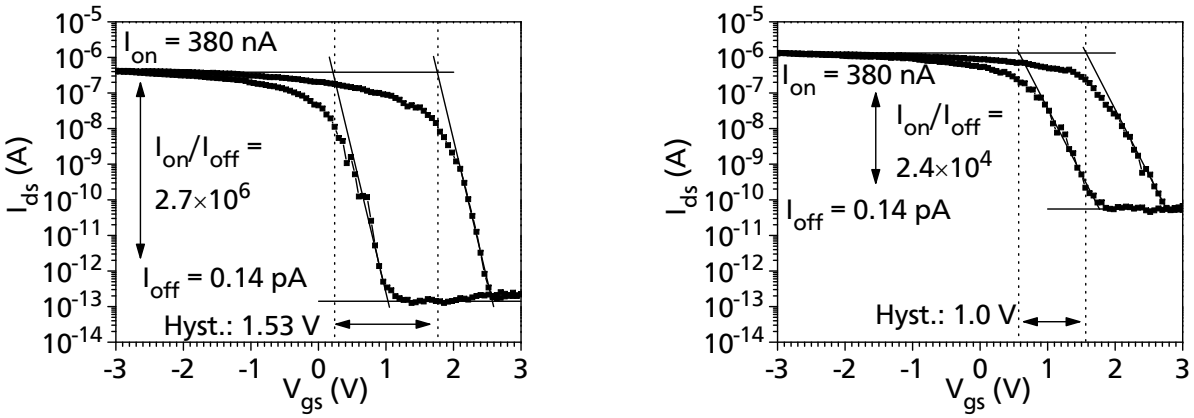
probability that one or several SWNTs link the adjacent electrodes. The closer the S/D spacing, the more likely that even short SWNTs can form the channel. This explains why the part of non-working devices is found to increase with increased space between the electrodes (see Fig. 5.5a). In the same way, the contribution of small on/off ratio devices decreases with in-

creased S/D spacing, although this tendency is not as clear as for increased S/D width (see Fig. 5.5b). Again, devices with metallic behavior are very rare and high on/off ratio devices form the majority, whatever the geometry. Again, this is a very satisfactory result in view of the suitability of the developed fabrication process.

5.1.4 Attempts to improve yield by piranha cleaning

There are several possibilities to explain the observation that devices are not working (i.e., without S/D link). Either the density of the tubes is too low and not well adapted to S/D geometry or too many SNWTs are defective. Defects could e.g. originate from contaminations during the fabrication process [107]. Shimauchi et al. [99] cleaned the CNTs after growth using piranha cleaning. This solution is composed of four parts of H_2SO_4 and one part of H_2O_2 and is supposed to remove any organic substances by oxidation. Shimauchi et al. demonstrate that this cleaning reduces the hysteresis and reinforces the effectiveness of the PMMA passivation [99].

To try to improve the yield of the fabrication process and/or to reduce the hysteresis, four wafers were immersed in a piranha solution after CVD (i.e., before lithography) but in all other aspects processed in the same way as reported in subsection 4.4.2. However, no differences in the transfer characteristics of the high on/off ratio CNTFETs could be observed. The hysteresis remains fluctuating between 0.9 and 1.8 V, based on the evaluation of 16 devices using the transfer characteristics. There is no significant change with respect to the hysteresis in the CNTFETs without piranha cleaning in which the hysteresis fluctuates between 0.8 and 2.2 V. Fig. 5.6 shows two examples of sweeps which are as satisfactory as the ones in Fig. 4.27 except that the on-current is slightly reduced (380 nA instead of ∼1 μA). Fig. 5.6a shows a device with high on/off ratio and high hysteresis, whereas the device in Fig. 5.6a shows on the contrary reduced hysteresis together with reduced on/off ratio. This tendency is also observed on the devices which are not cleaned with the piranha cleaning (see later subsection 5.3.2).

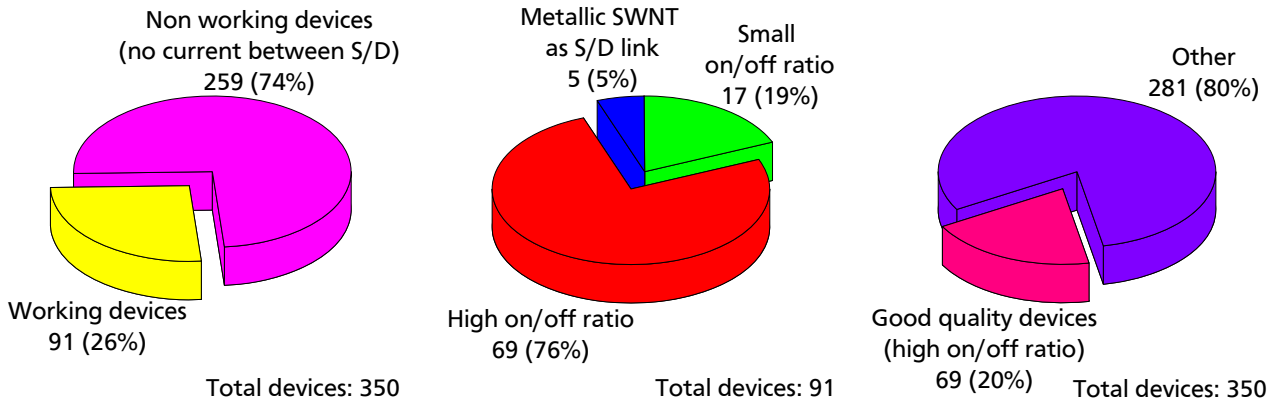


(a) Device with high on/off ratio and large hysteresis.

(b) Device with smaller on/off ratio and reduced hysteresis.

Figure 5.6: Two examples of transfer characteristics measured on devices with semiconducting SWNT as channel. The SWNTs have been cleaned in a piranha solution after growth.

Additionally to the fact that the cleaning does not improve the characteristics of the transistors, it also decreases the process yield drastically, as shown in Fig. 5.7a. Only a few percent of the whole transistors have a SWNT connection between source and drain. The devices distribution within the working ones (see Fig. 5.7b) shows some improvements compared to the distribution of the working devices fabricated without having cleaned the SWNTs in a piranha solution (see Fig. 5.2). The percentage of the devices with high on/off ratio is increased, which is an advantage for the process. However, the absolute number is reduced (see Fig. 5.7c and Fig. 5.3). It must be concluded that the piranha cleaning neither improves the yield of the process nor reduces the hysteresis width. These results are not in accordance with the ones of Shimauchi et al. [99]. Probably we have a cleaner process than Shimauchi et al., this is why the supplementary cleaning is not necessary and does not improve the yield. Since the piranha cleaning does not show any advantages in the present work, it will not be used in future investigations.



(a) Yield of the CNTFETs fabrication process with piranha cleaning.

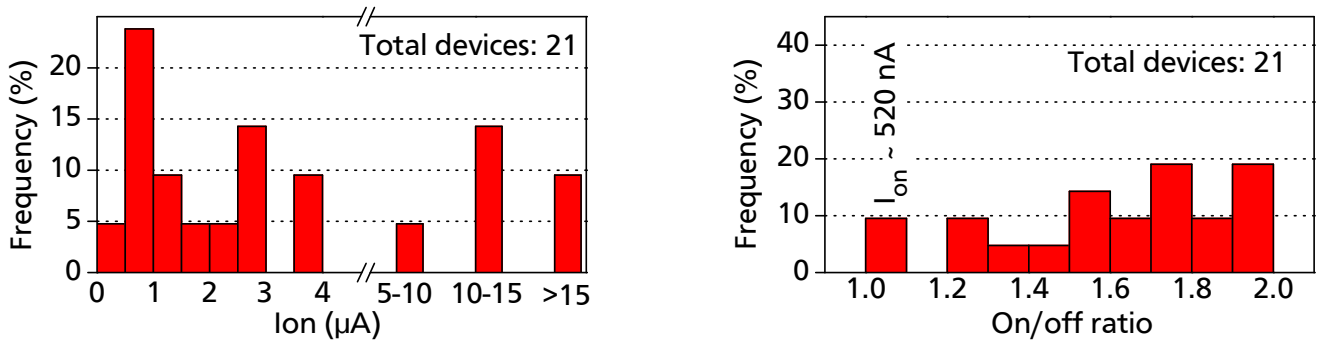
(b) Devices distribution within the working devices.

(c) Part of good quality (i.e., high on/off ratio) devices within all measured devices.

Figure 5.7: Statistics on CNTFETs fabrication process with piranha cleaning. All S/D spacings and widths together.

5.2 Discussion on devices with small on/off ratios or metallic SWNT S/D links

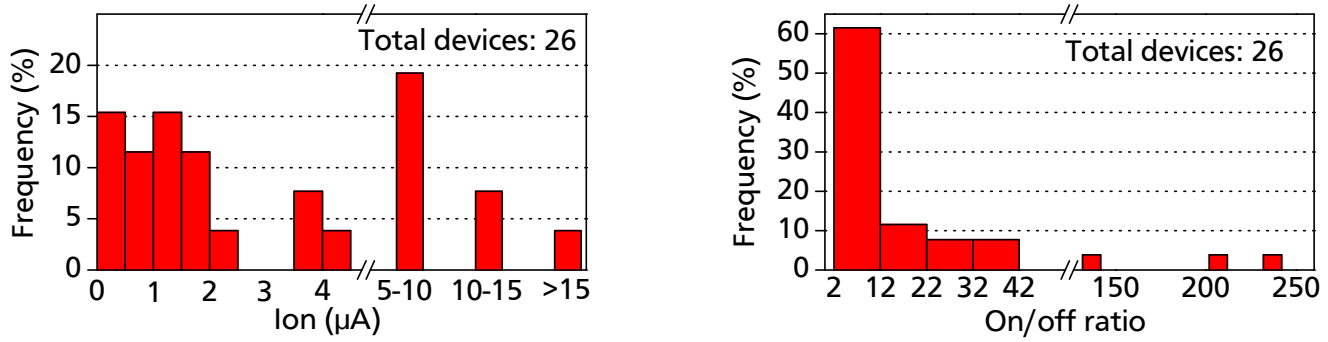
As already explained, the devices which have an on/off ratio between 1 (i.e., continuous current independent of gate voltage) and 2 (i.e., the current for positive gate voltages is the half of the current for negative voltages) are considered as devices which have a metallic SWNT as electrical link between source and drain electrodes. 21 of such devices have been analyzed in detail. The results are given in Fig. 5.8. The majority of the devices have a fairly high current between 500 nA and 4 μA, as shown in Fig. 5.8a. Devices with "perfect" metallic behavior, i.e., in which the current is perfectly constant, are found to be very rare. Most devices have an on/off ratio between 1.5 and 2. This corresponds to the fact that only armchair SWNTs are real metals, zigzag and chiral nanotubes for which n-m is a multiple of three are only quasi metallic because they have a narrow band gap induced by their curvature. The curvature of armchair nanotubes does not have any influence on their band gap due to their symmetry but these nanotubes by which n=m are statistically less frequent than the ones with n-m = 3 k. The rareness of real metallic SWNTs has also been reported by other researchers [108, 109, 110].



(a) on-current (b) on/off ratio

Figure 5.8: Statistics on devices with metallic SWNT as source/drain link.

As already mentioned, the group of devices called small on/off ratio devices exhibit an intermediate on/off ratio between 2 and 10^3. 26 sweeps of such devices have been evaluated. The distribution for the on-current, given in Fig. 5.9a is found to be similar to the one of the "metallic" group. Most devices have an on-current below 3 μA. Interestingly, a large majority of the devices exhibit an on/off ratio below 12 (see Fig. 5.9b), whereas less than 30% of the devices have a ratio between 12 and 42 and only a few devices between 100 and 300. The first category corresponds most likely to devices with a mixture of a thin s-SWNT and a m-SWNT as channel. For higher ratios devices, the assumption that a single thicker s-SWNT serves as S/D link is more probable.



(a) on-current (b) on/off ratio

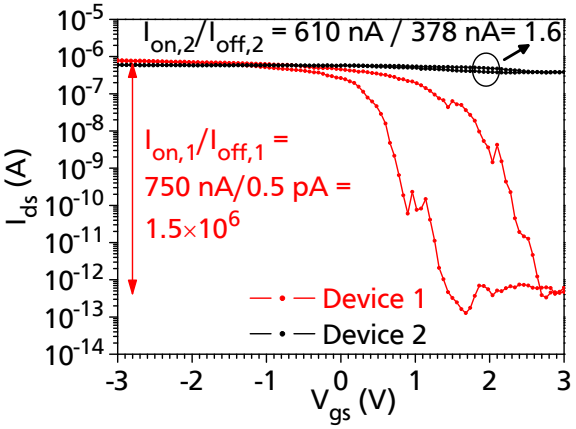
Figure 5.9: Statistics on devices with small on/off ratio.

To prove that m-SWNTs and s-SWNTs in parallel possibly form the channel of devices with reduced on/off ratios, three devices, called device 1 to device 3, have been selected from the measured CNTFET database. Due to the large number of evaluated transfer characteristics, it is possible to select appropriate devices:

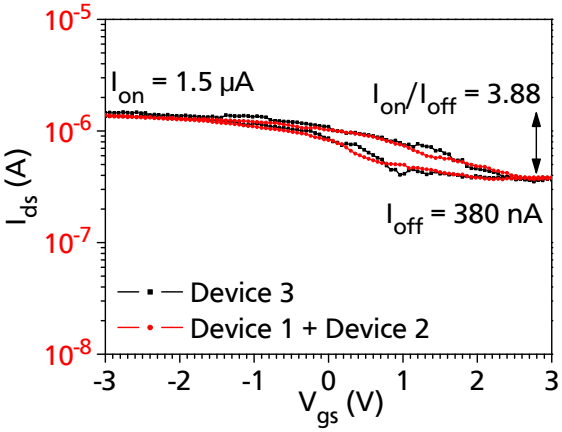
- device #1 with a high on/off ratio (see Fig. 5.10a)
- device #2 with a gate independent current (metallic, see Fig. 5.10a)
- device #3 with a small on/off ratio but same I_{on} as device #1 and same I_{off} as device #2 (i.e., $I_{on,device\#1} = I_{on,device\#3}$ and $I_{off,device2} = I_{off,device3}$, see Fig. 5.10b)

The result, presented in Fig. 5.10, is very convincing because adding the sweeps of device #1 and #2 point by point exactly resembles the sweep of device #3 (see Fig. 5.10b). This supports

our assumption that devices with reduced on/off ratios (below 12) are most likely formed by multiple SWNTs in parallel. A better control of the density of *in situ* grown nanotubes should lead to the reduction or even elimination of such devices and increase the percentage of high quality CNTFETs. Also, the use of a short burn impulse of current to eliminate metallic SWNTs, as mentioned in section 4.2, could be used to turn devices with small on/off ratios into devices with high (or at least higher) on/off ratios.



(a) Transfer characteristics of device 1 (high on/off ratio) and device 2 (metallic behavior). Both devices have the same I_{on}.



(b) Transfer characteristics of device 3 (small on/off ratio, same I_{off} as device 2) compared to the addition of the currents of the devices 1 and 2. The characteristics are almost identical.

Figure 5.10: Experiment to demonstrate the possibility that devices with small on/off ratio have two parallel SWNTs as channel: one metallic and one semiconducting.

5.3 Analysis of CNTFET electrical parameters based on a large number of devices.

In this section, 90 transfer characteristics have been chosen randomly within all high on/off ratio CNTFETs which have been completely evaluated, i.e., the following quantities have been determined from I-V sweeps: the current in the on-state (I_{on}, at negative V_{gs}), the current in the off-state (I_{off}, at positive V_{gs}), the threshold voltages of forward and backward sweeps ($V_{th,f}$ and $V_{th,b}$) and the subthreshold slopes. Moreover, the ratio of both currents (I_{on}/I_{off}) and the hysteresis (i.e., difference of both threshold voltages = $V_{th,b}$-$V_{th,f}$) have been calculated from the measured elements. Mean values and distributions are also computed and plotted for each quantity. From these electrical parameters, one can judge the quality of the devices. At the end of the section, the results are compared to the requirements given by the International Technology Roadmap for Semiconductors (ITRS) of 2007 (the newest ITRS at the time of writing of this PhD) as well as to published data of comparable devices from well recognized groups working on CNTFETs.

5.3.1 Preliminary remarks on nominal/effective channel lengths and widths

In view of conventional MOSFETs, effective channel widths and lengths are very important parameters since they are used e.g. to compute device normalized currents. For MOSFETs,

the effective channel length is the distance between the S/D junctions, i.e., between the doped regions within the silicon substrate. The effective channel length can be computed from the gate length (geometrical data known from the lithography step) since the doping process is self adjusted: the gate serves as implantation mask. The MOSFET effective channel width is equal to the lateral dimension of the gate electrode (in polysilicon or metal) structured on top of the oxide. For the CNTFETs fabricated in this work, effective channel lengths and widths are not related to the geometrical data determined by the lithography step. Fig. 5.11 right illustrates the four different quantities. Nominal channel length and width are the geometrical dimensions of the palladium source and drain electrodes whereas the effective channel length and width are determined by the SWNT which links S/D.

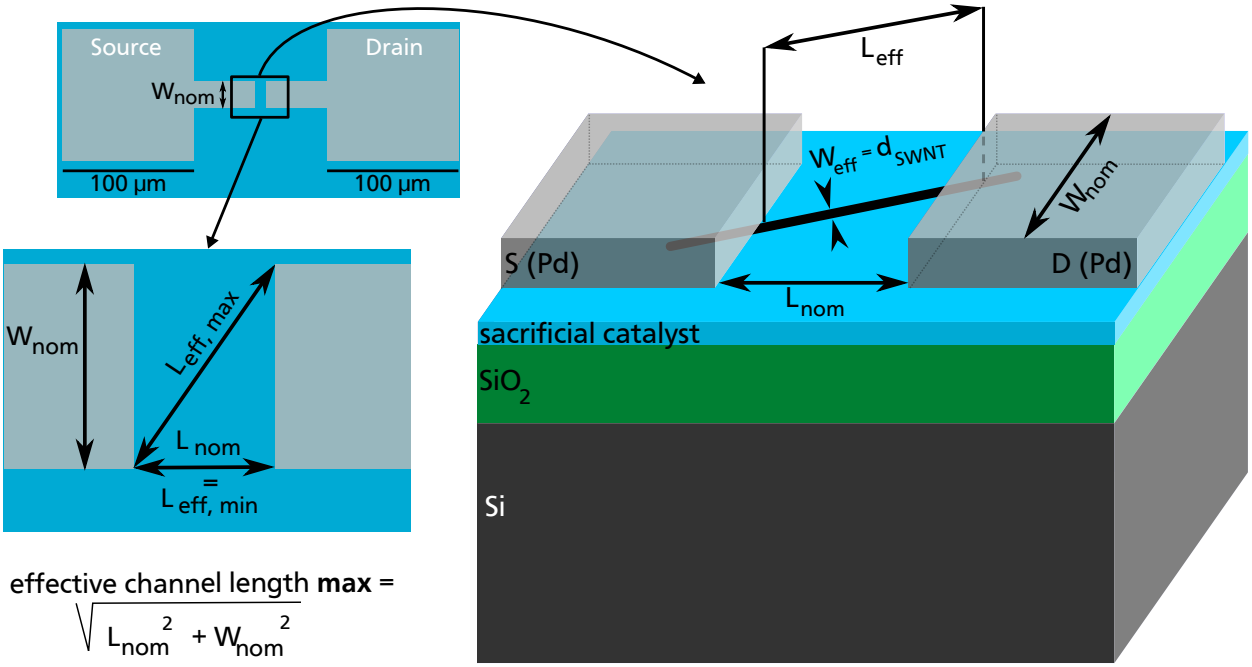


Figure 5.11: Schematic of CNTFET indicating nominal channel length and width, as well as effective channel width and shorter and longer possible effective channel lengths.

CNTFET effective channel width

The electrically relevant channel width is the diameter of the SWNT or in the case of multiple SWNTs in parallel the sum of the individual diameters. The 90 devices which have been selected to perform a statistical evaluation of the CNTFET electrical parameters exhibit high on/off ratios combined with farily steep subthreshold slopes. Hence, we assume that the channel is most likely formed by a single s-SWNT, leading to a channel width around 1 nm, the average diameter of the SWNTs grown in these experiments.

CNTFET effective channel length

The question of the effective channel length is more difficult to answer. It is determined by the orientation of the SWNT. If the SWNT has grown perpendicularly to the electrodes, the channel length is minimal and equal to the nominal channel length (S/D spacing). However, because of

their random orientation during growth, the SWNTs can also have grown in a slanting direction not perpendicular to the S/D electrodes (i.e., non-directed growth). This situation is illustrated in Fig. 5.11 right. For given nominal channel length and width, a maximal effective channel length can be computed (see Fig. 5.11 bottom left). Table 5.5 shows examples of minimal and maximal effective channel lengths for different given geometrical S/D dimensions. The values

W_{nom} (μm)	L_{nom} (μm)	$L_{eff,\ min}$ (μm)	$L_{eff,\ max}$ (μm)
5	2 / 3 / 4 / 5 / 6	2 / 3 / 4 / 5 / 6	5.4 / 5.8 / 6.4 / 7.1 / 7.8
10	2 / 3 / 4 / 5 / 6	2 / 3 / 4 / 5 / 6	10.2 / 10.4 / 10.8 / 11.2 / 11.7
15	2 / 3 / 4 / 5 / 6	2 / 3 / 4 / 5 / 6	15.1 / 15.3 / 15.5 / 15.8 / 16.2

Table 5.5: Effective channel lengths according to nominal device length and width.

are distributed over a wide range and partly overlap: when comparing two devices, a smaller nominal channel length does not imply a smaller effective channel length and vice versa.

Accordingly, the effective channel length of the devices is unknown. However, only this effective channel length is electrically relevant and can be used to judge on device performance, e.g. to verify if, similarly to MOSFET, I_{on} is inversely proportional to the channel length. Statistics on the influence of the channel length on electrical parameters using the nominal channel length would be irrelevant and were not performed in this work.

Clearly, aligned *in situ* growth of SWNTs would be a major advantage. Some published results of other groups indicate that aligned growth seems possible when using sapphire substrates instead of SiO_2 substrates [111, 112]. During this PhD, some preliminary experiments on sapphire substrates were performed, using directly the parameters optimized for SWNT growth on SiO_2. The results are not yet satisfactory, further investigations are required.

5.3.2 Statistics and discussion on electrical parameters

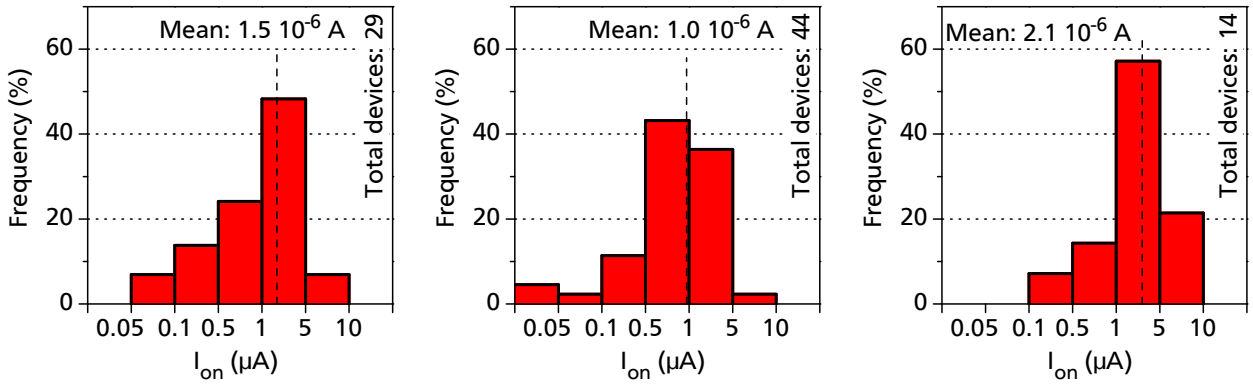
In this subsection, the statistical evaluation of the electrical parameters of the selected 90 devices fabricated with our novel CNTFET fabrication process is given to test process suitability and reproducibility. All nominal channel lengths and widths, i.e., S/D electrodes dimensions, are evaluated together for two reasons: firstly, most devices show very similar transfer characteristics for any S/D width or spacing. The on- and off-currents, the slope and hysteresis are not completely random. Secondly, the effective channel width is situated around 1 nm for all devices, since it is assumed that a single SWNT with a diameter around 1 nm links S/D. Only a variation in effective channel length, which has been previously analyzed (see subsection 5.3.1), is implied by the variations in S/D dimensions. The following discussion on electrical parameters will take this variation into account.

Within the 90 devices selected for statistical evaluation, 29 devices have been fabricated with an oxide thickness of ∼30 nm, 44 devices with ∼40 nm, 14 devices with ∼90 nm and three devices with a ∼250 nm thick SiO_2 layer. The SiO_2 thicknesses have been verified by ellipsometer measurements. According to their oxide thickness, the devices show quite different transfer characteristics. Accordingly, three different statistical evaluations are performed for each evaluated electrical parameter, one for 30 nm, one for 40 nm and one for 90 nm SiO_2 thickness. The three devices with a 250 nm thick SiO_2 layer are statistically rather insignificant and thus

only used for hysteresis evaluation (see Fig. 5.21). Note that the thickness of the metal catalyst layer lying on the SiO_2 layer, which has been used to catalyze SWNT growth, is identical for all samples (0.9 nm of Ni on 5 nm of Al). The resulting sacrificial catalyst layer (Al_xO_y, Ni clusters) is thus presumed to have the same thickness for all devices.

On-current

Fig. 5.12 shows the three distributions of the on-current for devices with 30, 40 and 90 nm thick SiO_2. The distributions look similar. The mean values are found to vary between 1 and



(a) SiO_2 thickness: 30 nm. (b) SiO_2 thickness: 40 nm. (c) SiO_2 thickness: 90 nm.

Figure 5.12: Distribution and average value of the on-current at V_{ds} = -400 mV for different silicon dioxide thicknesses. The x axis has a logarithmic scale.

2 μA, depending on SiO_2 thickness. However, no clear relationship between oxide thickness and on-current can be observed, the variations in the mean on-current are attributed to statistical fluctuations. From the on-current, the corresponding on-resistance can be calculated. As a result, the s-SWNT on-resistance is found to be much higher than the theoretical value. 2 μA at -400 mV for one SWNT leads to 200 kΩ whereas the theoretical limit for SWNTs is 6.5 kΩ. This high value is most likely due to an imperfect contact between SWNT and palladium, as already mentioned.

The variations of the on-current for devices with same oxide thickness may be caused by fluctuations in the effective channel length, since it is known from the conventional MOSFET that the on-current depends on the channel length. Since the electrically relevant channel length and width have been shown to fluctuate even for devices with the same nominal geometry, it should be determined whether the fluctuations of the on-current can be entirely attributed to different channel dimensions or if other facts may also influence the on-current. For this investigation, 37 devices are selected with the same oxide thickness (approx. 40 nm) and nearly the same nominal channel length (2 to 4 μm). The dispersion of the on-current is represented in Fig. 5.13, according to the nominal channel width. Each dot represents a device. For each different nominal S/D width, the corresponding effective channel length range can be calculated (see Table 5.5). The ranges are indicated in Fig. 5.13. If an analogy with MOSFET is done, the on-current should be inversely proportional to the channel length for a given channel width (here assumed to be equal to 1 nm). In Fig. 5.13, the red bars represent the I_{on} ranges which correspond to the effective channel length ranges when assuming that for each nominal S/D width, the device with the highest I_{on} has the shortest possible effective channel length. As

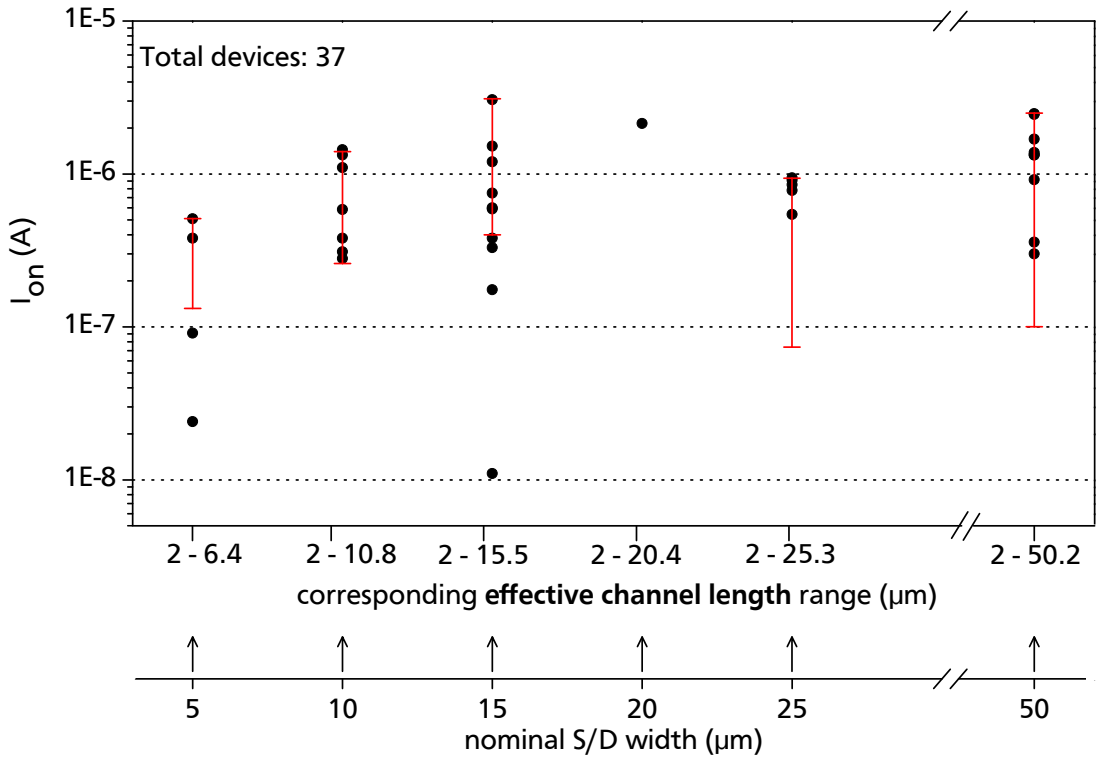
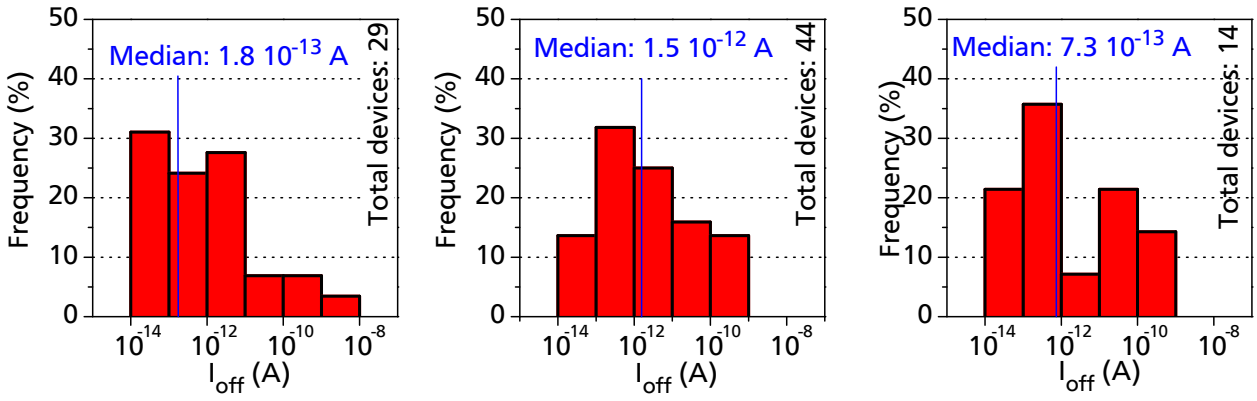


Figure 5.13: Influence of S/D electrodes width on on-current. Total devices: 37. SiO_2 thickness: 37-40 nm. S/D spacing: 2 to 4 μm, considered here as equivalent.

a result, the variation of the on-current for devices with an S/D width of 10 μm corresponds approximately to the possible variation of their channel length: the on-current which ranges from 0.2 to 2 μA corresponds to a channel length of 2 to 20 μm, almost the maximum channel length possible (15.5 μm). For devices with S/D widths of 25 or 50 μm, the variation of I_{on} is much smaller than expected for the effective channel length variation. In contrast, for devices with S/D widths of 5 and 15 μm, the dispersion of the on-current is much wider and cannot be explained only by a difference in the channel length. A locally degraded quality of the SWNT/Pd contacts, due to process variations or external contamination, may explain a drastic reduction in the on-current in some devices.

Off-current

The magnitude of the off-state leakage current is an important feature in view of power consumption in an integrated circuit. Fig. 5.14 shows the distributions for the off-current of the fabricated CNTFETs. The median value (i.e., center of the distribution in the sense that half the devices have a smaller off-current) is indicated on the off-current distributions, instead of the mean value, because the small number of devices with high off-currents would have a misleadingly major contribution in the simple arithmetic mean value. I_{off} is found to be distributed between 51 fA (smallest value, see Fig. 4.27d) and 100 pA for more than 85% of the devices. The few devices with increased off-currents may contain a larger SWNT as the channel (diameter> 1.5 nm). More than half of the devices have an off-current below 1 pA with a good portion even below 100 fA. Such remarkably reduced off-currents make the devices compatible with ultra low power applications.

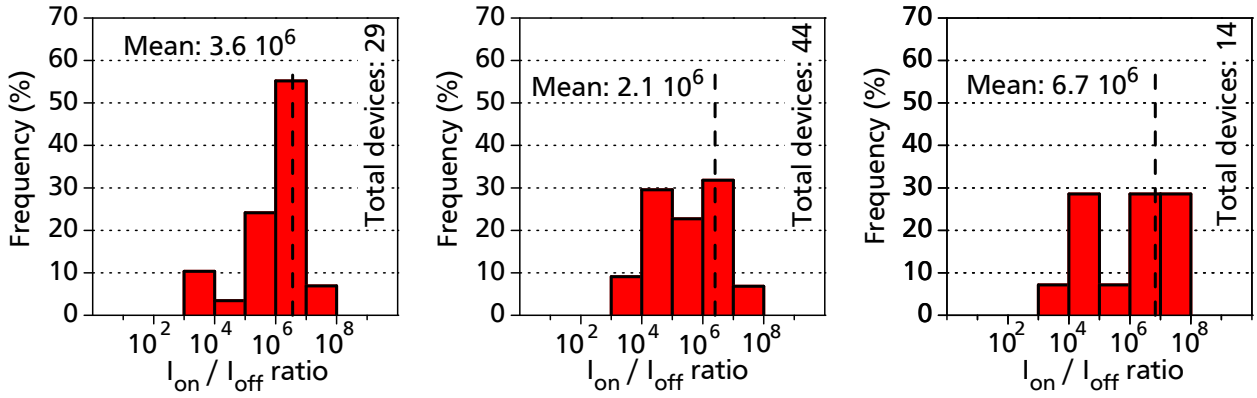


(a) SiO_2 thickness: 30 nm. (b) SiO_2 thickness: 40 nm. (c) SiO_2 thickness: 90 nm.

Figure 5.14: Distribution and average value of off-current for different silicon dioxide thicknesses. The x axis has a logarithmic scale.

On/off ratio

Fig. 5.15 shows the distribution of the on/off ratio for devices with different oxide thicknesses. Low off-currents combined with high on-currents leads to excellent on/off ratios: A large majority of the devices have an on/off ratio in the 10^6 range. This proves that the *in situ* CVD method



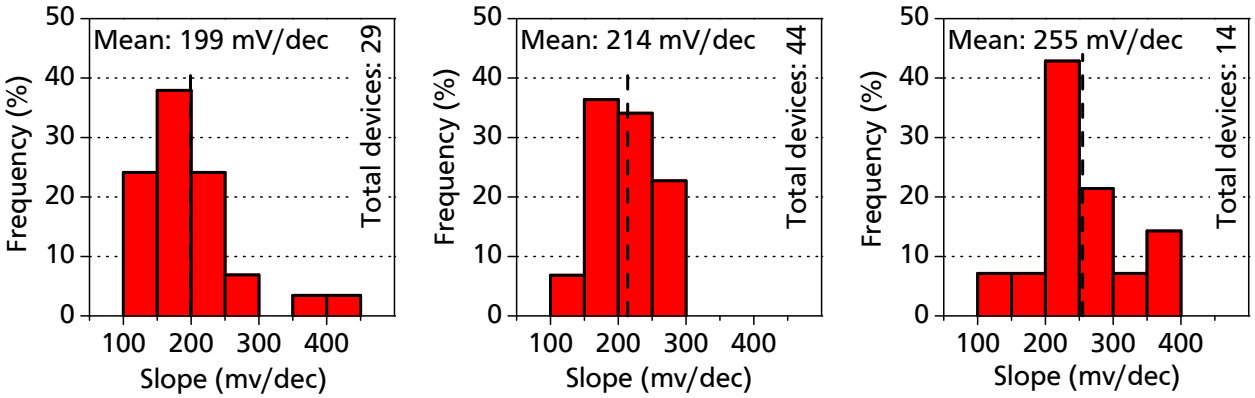
(a) SiO_2 thickness: 30 nm. (b) SiO_2 thickness: 40 nm. (c) SiO_2 thickness: 90 nm.

Figure 5.15: Distribution and average value of the on/off ratio for different SiO_2 thicknesses. The x axis has a logarithmic scale.

for SWNT growth is suitable for the fabrication of high on/off ratio devices. High on/off ratios are obtained only when the band gap of the SWNTs is sufficiently high, i.e., when their diameter is small enough. This disproves the argument that "CVD leads to large CNT diameter and thus small on/off ratio devices". This argument is often written in publications promoting other growth methods, as in [100]. Furthermore, in [100], the method of the direct assembly of *ex situ* grown SWNTs on predefined areas on the wafer leads to devices with a much lower on/off ratio than thosefor each evaluated electrical parameter grown within this PhD, i.e., only $\sim 5.10^5$.

Subthreshold slopes

Fig. 5.16 shows the distributions and mean values of the subthreshold slope in devices with 30, 40 and 90 nm SiO_2. As already mentioned, both forward and backward subthreshold slopes are identical for most devices. In the few cases in which the sweeps are slightly different, a mean value of both slopes is used for statistical evaluation. Contrary to the on- and off-currents, a clear



(a) SiO_2 thickness: 30 nm. (b) SiO_2 thickness: 40 nm. (c) SiO_2 thickness: 90 nm.

Figure 5.16: Distribution and average value of the slope for different SiO_2 thicknesses.

relationship between slope and SiO_2 thickness can be observed. The slope is situated between 122 mV/dec (steepest slope of all devices, see Fig. 4.27b) and 300 mV/dec for the majority of devices with 30 or 40 nm SiO_2 whereas the slope shows values degraded to 400 mV/dec for devices with a 90 nm thick SiO_2. The influence of the oxide thickness on the slope is also known from the MOSFET technology: the thinner the oxide, the better the switching properties of the device. In Fig. 5.17, the mean slope is plotted versus the SiO_2 thickness. When fitting the curve

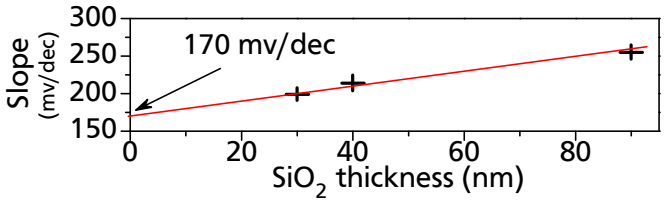


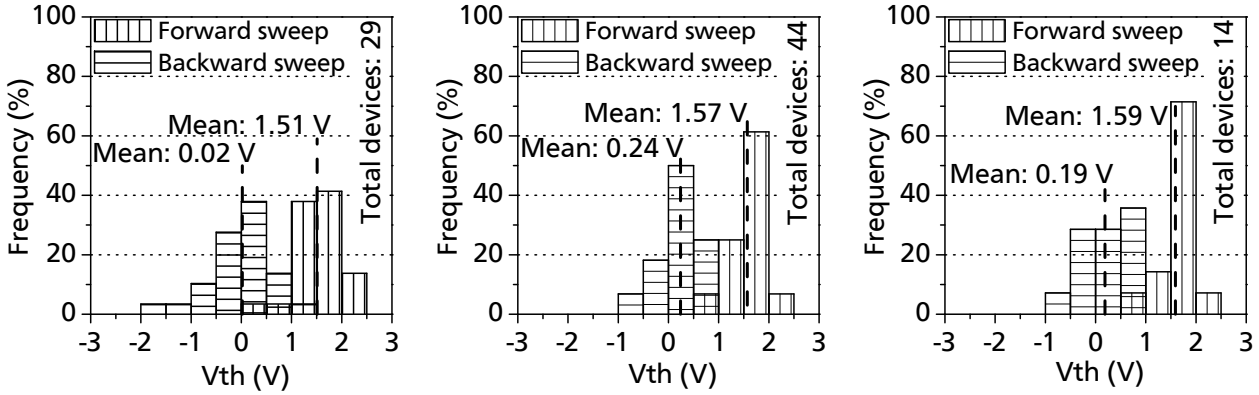
Figure 5.17: Mean slope versus SiO_2 thickness, from Fig. 5.16.

linearly, a possible value for ultra down-scaled devices is obtained. As a result, the minimum slope which could be obtained is approximately 170 mV/dec, which is a fairly disappointing result since the theoretical limit of MOSFETs at 300 K is 60 mV/dec. The results concerning the slope are insufficient to prove that CNTFETs are a possible replacement for conventional MOSFETs. Further investigations should be performed to understand the origin of the degraded slope and to optimize it.

Threshold voltages and hysteresis

In this work, the threshold voltage has been defined by geometrical extrapolation, directly from the transfer characteristics (see subsection 4.3.3). Typically, the threshold voltage of CNTFETs in literature is found to be sometimes negative, sometimes positive, depending on the gate

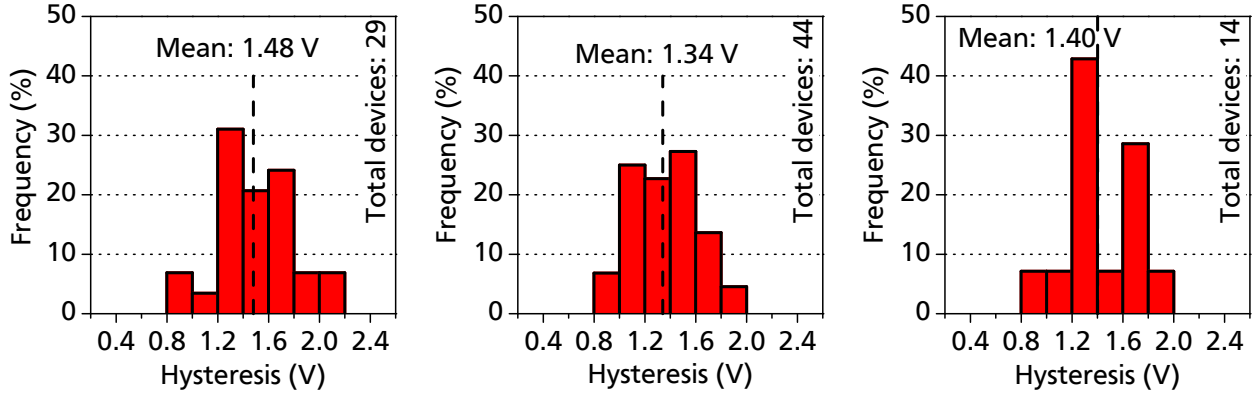
voltage cycling range or on the measurement direction (increasing or decreasing gate voltage). The achievement of a stable and reproducible threshold voltage is definitely a challenge for CNTFET researchers intending to prove that CNTFETs can replace MOSFETs in the future. Fig. 5.18



(a) SiO_2 thickness: 30 nm. (b) SiO_2 thickness: 40 nm. (c) SiO_2 thickness: 90 nm.

Figure 5.18: Distribution and mean value of threshold voltages for different SiO_2 thicknesses.

shows the distribution of the threshold voltages of both forward and backward sweeps. The mean value of the forward sweep threshold voltage is 2, 240 and 190 mV for devices with 30, 40 and 90 nm SiO_2 thickness respectively and for a cycling range of -3 to 3 V. For the backward sweep, the values are 1.51, 1.57 and 1.59 V. The threshold voltages seem to be independent of the SiO_2 thickness. However, the distributions are quite wide. From the difference between



(a) SiO_2 thickness: 30 nm. (b) SiO_2 thickness: 40 nm. (c) SiO_2 thickness: 90 nm.

Figure 5.19: Distribution and average value of the hysteresis for different SiO_2 thicknesses.

forward and backward threshold voltages, the hysteresis is obtained. The hysteresis is found to be around 1.4 V for all SiO_2 thicknesses, with Gaussian distributions around the mean values, as seen in Fig. 5.19. By measuring hundreds of devices, one important feature could be recorded: devices with fairly reduced on/off ratios combined with high on-currents (above 500 nA) often exhibit reduced hysteresis. This correlation is obvious when plotting hysteresis versus on/off ratio for the 66 devices with I_{on} greater than 500 nA (device SiO_2 thickness: 30, 40 or 90 nm). The very interesting result of this study is given in Fig. 5.20: there is effectively an apparent relation between on/off ratio of high on-current devices and the magnitude of hysteresis. 83% of the devices are found to be between two lines (log(on/off ratio) = 5.7 hysteresis - 0.7 and log(on/off ratio) = 5.7 hysteresis - 3.7). Since a reduced on/off ratio for devices with similar

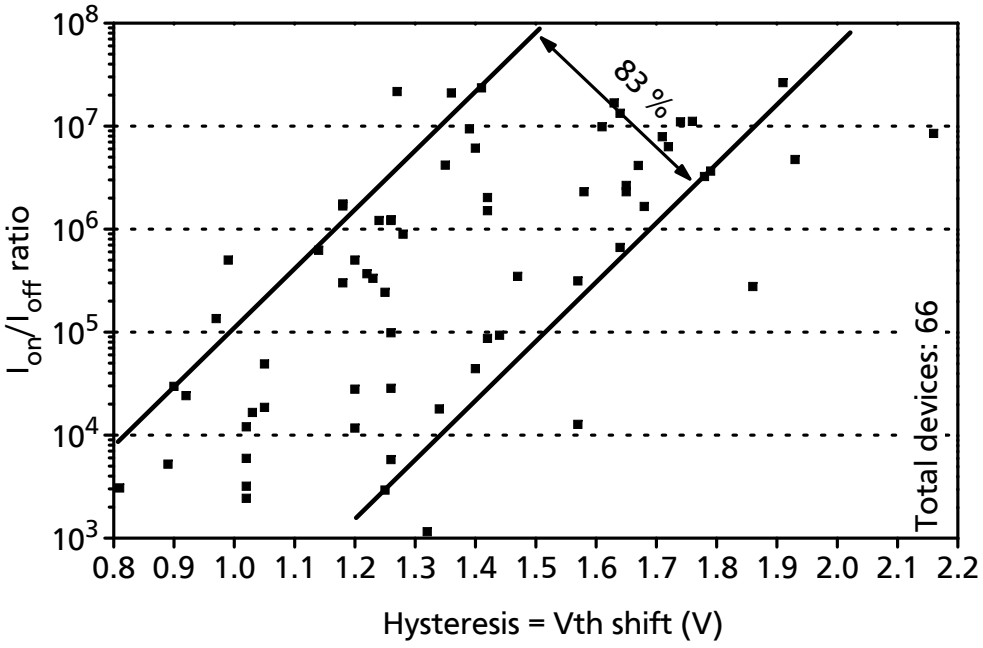


Figure 5.20: On/off ratio versus hysteresis for devices with I_{on} >5 10^7.

high on-current is most likely due to a decreased band-gap (increased SWNT diameter), it can be concluded that the hysteresis is dependent of the SWNT band-gap, i.e., of the diameter of the tube. This means that for CNTFET applications taking advantage of hysteresis effects (see section 5.4), very thin SWNTs should be preferred. On the contrary, when the hysteresis is undesirable, e.g. in logic circuits, the diameter of SWNTs need to be increased, but at the cost of the on/off ratio. The SWNT diameter/hysteresis width dependency can be explained by the fact that for a given V_g, smaller diameter SWNTs lie under a higher electric field than thicker SWNTs, since the electric field at the interface oxide/SWNT is inversely proportional to the diameter of the tube (for small diameters) [104]. The higher electric field in smaller diameter SWNTs increases the number of electron trapping/detrapping into the gate oxide (see subsection 4.3.4), and thus the hysteresis effect.

A final question should be answered concerning hysteresis. It should be clarified, whether the magnitude of the hysteresis is influenced by the SiO_2 thickness in CNTFETs or not. According to Fig. 5.19, no clear dependency can be observed and the mean hysteresis is around 1.4 V. A further analysis is performed by plotting the average hysteresis of seven groups of devices versus their SiO_2 thickness. The oxide thicknesses 30 and 32 nm are separated into two groups (for all other parameters, they were considered as equivalent). The same is done with the thicknesses 37, 38 and 40 nm. The 14 devices with a thickness around 90 nm form another group. Lastly, three devices with a very thick SiO_2 layer (250 nm) are also taken into account as the seventh group. The result is given in Fig. 5.21. Except for 250 nm, each main hysteresis is calculated as an average value of around 15 devices. The bars represent the corresponding standard deviation. Both main hysteresis and standard deviation are found to be independent of the oxide thickness. They are all almost equal to the mean value for all devices together, i.e., 1.39 V. However, hysteresis has been shown to be caused by charge trapping/detrapping from the gate oxide (see subsection 4.3.4). If the traps are located into the SiO_2 layer, the hysteresis will increase with increasing SiO_2 thickness. Since this is not the case, we believe that

the principal source of electron traps causing the hysteresis is not the SiO_2 but the sacrificial catalyst, i.e., the aluminum oxide. Indeed, it has been demonstrated that ultra thin layers of Al_2O_3 (8 nm) contain electron traps [113]. The catalyst used for all tests is composed of 0.9 nm Ni on 5 nm Al before SWNT growth. This most likely results to a constant Al_xO_y layer thickness, which in turn is assumed to deliver a constant amount of electron traps. Accordingly, scaling down the SiO_2 layer to a few nm, but keeping the catalyst constant, would not affect the hysteresis magnitude. This is clearly a disadvantage if CNTFETs are supposed to replace MOSFETs in logic circuits, as the hysteresis is in this case a parasitic phenomenon. However, for applications in which the hysteresis is desirable, it becomes a great advantage. This is the case when CNTFETs are used e.g. as memory cells (see section 5.4).

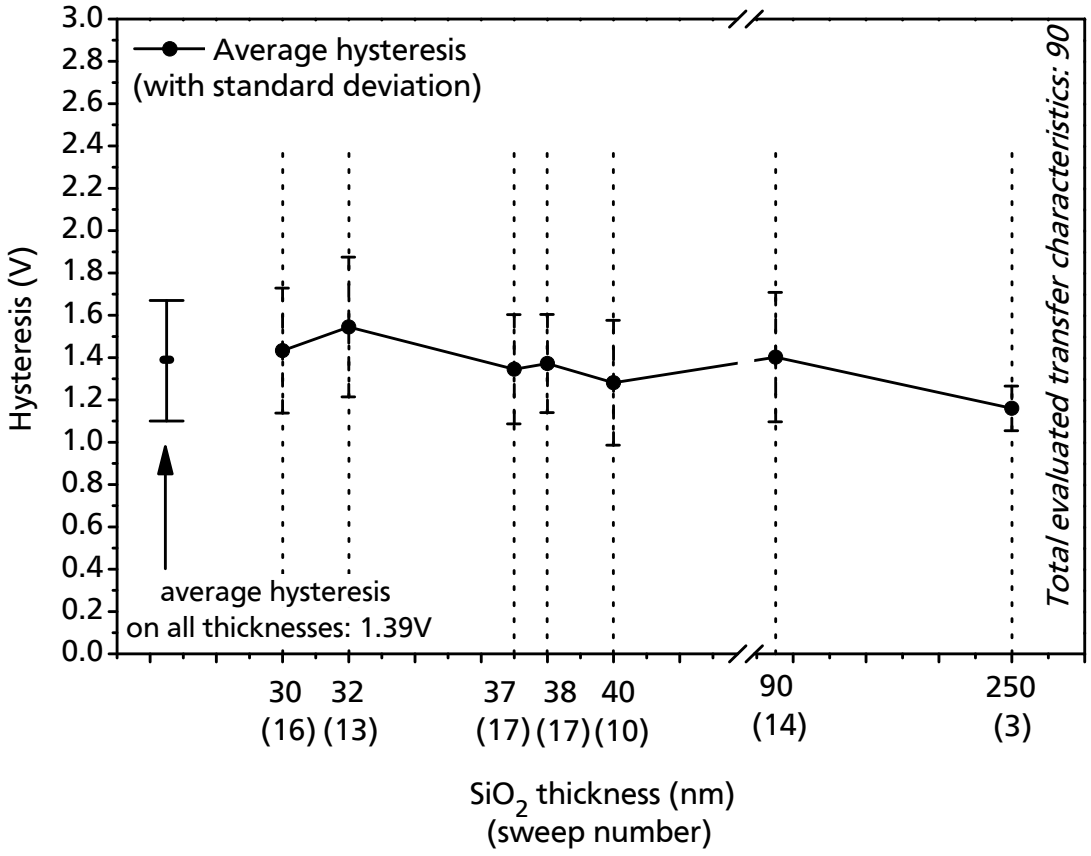


Figure 5.21: Hysteresis versus SiO_2 thickness for devices with on/off ratio > 10^3. All S/D dimensions together. Total devices: 90.

5.3.3 Performance evaluation - ITRS benchmark

To evaluate the suitability of the CNT devices fabricated within this PhD, the average electrical parameters reported in the previous subsection are compared to the parameters given by the International Technology Roadmap for Semiconductors (ITRS). The ITRS is the reference in semiconductor technology. Semiconductor industries around the world have agreed jointly on the future requirements of devices and circuits for the next 15 years. An extract of the ITRS 2007 is reproduced in Table 5.6. The indicated geometrical and electrical requirements are the

Year of Production		2016	2017	2018	2019	2020	2021	2022
Physical Gate Length	(nm)	9	8	7	6.3	5.6	5	4.5
EOT	($\AA$)	5.5	5.5	5.5	5	5	5	5
V_{dd}	(V)	0.8	0.7	0.7	0.7	0.65	0.65	0.65
$V_{t,sat}$	(mV)	110	109	114	119	123	115	118
$I_{d,sat}$	(μA/μm)	2627	2533	2804	2768	2677	2799	2786
$I_{sd,leak}$	(μA/μm)	0.44	0.48	0.45	0.47	0.43	0.62	0.6
on/off ratio	$x10^3$	6.0	5.3	6.2	5.9	6.2	4.5	4.6

Table 5.6: Extract of Table PIDS2b: "High-performance Logic Technology Requirements – Long-term Years", in "Process Integration, Devices, and Structures", ITRS 2007 [114].

ones for MOSFETs in Microprocessor Units (MPU) and Application-Specific Integrated Circuits (ASIC) in the next 8 to 15 years.

Physical gate length

For the CNTFETs in this work, the physical gate length corresponds to the effective channel length. The devices produced in this PhD work have been realized with conventional optical lithography, and their gate lengths above 2 μm are of course not comparable with the requirements of the ITRS (i.e., below 10 nm). The reduction of the oxide thickness should be the subject of future works.

Equivalent oxide thickness

The *Equivalent Oxide Thickness* (EOT) is a parameter which is used when the gate dielectric of the device is not SiO_2 but a material with another dielectric constant (κ). It is calculated as the equivalent SiO_2 thickness which is needed to obtain the same gate capacitance as the one obtained with the other dielectric. The materials implied in the ITRS table are high-κ dielectrics, so that the required EOT of 0.5 nm turns into a higher physical thickness for these dielectrics, e.g. 1.15 nm for Al_2O_3. In this work, the dielectric is a dual layer composed of a layer of SiO_2 covered by a layer of sacrificial catalyst. Currently, the catalyst layer is investigated by reference-free total reflection X-ray fluorescence analysis with synchrotron radiation in cooperation with the "Physikalisch-Technische Bundesanstalt" in Berlin [115], to determine the exact composition of the Al/Ni based insulator, and thus its dielectric constant κ_{cat}. When assuming that the Al layer converts entirely into Al_2O_3 whereas the Ni layer turns into a discontinuous layer of Ni clusters, the gate oxide after growth is composed of a double layer of Al_2O_3 on SiO_2. According to [116], the Al_2O_3 thickness resulting from the oxidation of Al can be assumed to be approximately 1.4 times the original thickness of the Al layer. For a 5 nm thick Al layer, the resulting Al_2O_3 is thus 7 nm thick. In equation (5.2), the required SiO_2 underlayer thickness

following the ITRS requirement (i.e., EOT = 0.5 nm) is calculated, based on the calculation of the equivalent capacitances in equation (5.1).

$$\frac{1}{C_{equ}} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{Al_2O_3}} \quad \Leftrightarrow \quad \frac{EOT}{\epsilon_0\ \kappa_{SiO_2}} = \frac{T_{SiO_2}}{\epsilon_0\ \kappa_{SiO_2}} + \frac{T_{Al_2O_3}}{\epsilon_0\ \kappa_{Al_2O_3}} \tag{5.1}$$

$$\Rightarrow \quad T_{SiO_2} = EOT - \kappa_{SiO_2}\ \frac{T_{Al_2O_3}}{\kappa_{Al_2O_3}} = 5 - 3.9\ \frac{7}{9} < \ 0 \text{ nm !!!} \tag{5.2}$$

Accordingly, the combination of 0.9 nm Ni on 5 nm Al as catalyst before growth cannot be used to obtain an EOT of 0.5 nm, as required by the ITRS. With the same calculations, it can be found that a minimum EOT of 4 nm can be reached with this catalyst combination when using a SiO_2 underlayer of 1 nm. In the same way, the EOT of the devices fabricated within this PhD can be obtained: underlayers of 30/40/90 nm SiO_2 correspond to EOT of 33/43/93 nm.

Power supply voltage

V_{dd} is the power supply voltage, which corresponds to V_{ds} for our CNTFETs. The ITRS requirements are between 650 and 800 mV, which is entirely compatible with the devices reported here since the CNTFETs are already fully functional at a drain voltage of only 400 mV.

Saturation threshold voltage

$V_{t,sat}$ is the saturation threshold voltage, corresponding to $V_{th,f}$ and $V_{th,b}$. The threshold voltage which defines the beginning of the conductive state of the device, should be around 115 mV in the next 8 to 15 years according to the ITRS. The mean values of the forward threshold voltage for devices with 30, 40 and 90 nm SiO_2 are 20, 240 and 190 mV which corresponds approximately to the ITRS requirements. However, the ITRS gives requirements for n-MOSFETs, and implies that forward and backward threshold voltages are similar, i.e., that no hysteresis effect occurs. As shown in chapter 4, the hysteresis effect cannot be avoided in our CNTFETs, which is a major counter-argument for a direct use of CNTFETs as MOSFET replacement in logic circuits.

Drive current

$I_{d,sat}$ is the drive current (given here for a n-type MOSFET). It corresponds to I_{on}. In order to compare CNTFETs with MOSFETs, an on-current in μA/μm needs to be used, i.e., normalized to channel width. As already mentioned, the CNTFETs fabricated in this work have a channel width of around 1 nm (a single SWNT), i.e, the current should be multiplied by 1000 to obtain the current normalized to channel width. Moreover, looking at the CNTFET output characteristics (see Fig. 4.17 for an example), the drain-source current is not found to saturate and is linear to 1 V. This means that the on-currents measured at -400 mV should be doubled for comparison with the ITRS requirements, as the power supply, V_{dd}, is around 0.8 V. According to Fig. 5.12, $I_{on,mean}$ is situated around 1 to 2 μm, leading to a majority of devices with 2000 to 4000 μA/μm @ -800 mV. Since the ITRS mentions currents around 2600 μA/μm for the next 8

to 15 years, the big majority of the CNTFETs show sufficiently high or even higher on-currents than required.

Off-state leakage current

$I_{sd,leak}$ is the off-state leakage current corresponding to I_{off}, which is found to be smaller than 1 pA for approximately half of the devices (see Fig. 5.14). The off-current should be normalized. 1 pA for a 1 nm thick SWNT converts to 10^{-3} μA/μm, which is a good result, in accordance with the ITRS ($\sim$ 5 10^{-2} μA/μm). However, the CNTFETs are measured at a drain-source voltage of only 400 mV. It should be investigated in a future work, whether the off-current increases with increasing V_{ds} to 800 mV. Moreover, $I_{sd,leak}$ is indicated for an EOT of approximately 0.5 nm, while the CNTFETs of this work have EOT between 33 and 93 nm. From the MOSFET technology, the leakage currents in the off-state are known to increase drastically when decreasing SiO_2 thickness, this is one of the reasons for the use of high-κ dielectrics. However, comparing the distributions for the three different oxide thicknesses in Fig. 5.14, no real difference can be seen. I_{off} is not found to be increased for decreased SiO_2 thickness. This should be further investigated for ultra down scaled SiO_2 layer. A reduction of the off-currents when replacing MOSFET with CNTFETs would be very promising.

On/off ratio

The on/off ratio is not indicated in the original table of the ITRS. It has been appended into Table 5.6 as the result of $I_{d,sat}/I_{sd,leak}$. The requirements of the ITRS are situated around 5.10^3, whereas more than half of the CNTFETs show an on/off ratio above 10^6, clearly exceeding the requirements of the ITRS.

5.3.4 Performance evaluation - Comparison with other CNTFETs

The second performance evaluation for our novel CNTFET fabrication process is a comparison between the transfer characteristics measured on our devices and the sweeps obtained by other groups fabricating CNTFETs. Within the numerous published papers on CNTFET fabrication and evaluation, four papers have been selected for comparison based on the following criteria: only CNTFETs with a single gate have been chosen. CNTFETs with complicated layer arrangement like double gate or floating gate are not comparable. Also, only Pd contacted CNTFETs have been chosen. There is no report on a more suitable metal than Pd for contacting p-type CNTFETs. Lastly, only papers which are well-recognized by the scientific community and which are often cited have been taken into account. The first selected paper, published by Javey et al. from Stanford University in Nature in 2003, is the first report on Pd contacted CNTFETs [30]. Furthermore, two papers, one from Infineon and one from IBM, have been selected, which report on CNTFETs with back gate structure and Pd electrodes [117, 118]. Lastly, the paper of Tseng et al. from the University of California at Berkeley has been selected because this is one of the very rare groups which also reports on the evaluation of several hundreds of CNTFETs [106]. When CNTFETs with different geometries are mentioned and measured in these four papers, only the CNTFET with back gate electrode and Pd contacts is taken into account. The electrical properties of these four devices are summarized in Table 5.7. These values have been

extracted from transfer characteristics published in the papers and need to be considered for this reason as approximate values. To simplify comparison, the mean values of our CNTFETs are also indicated in Table 5.7.

EOT (nm)	L (μm)	V_{gs} range	I_{on}	I_{off}	On/off ratio	Slope (mV/dec)	$V_{th,f}$ (V)
[30] — Nature, 2003							
67	3	-8 to 2 V	3 μA @ 100 mV	$\sim$ pA	10^6	150	0
[117] — Nano Letters, 2005							
12	0.36	-2 to 2 V	3 μA @ -100 mV	0.4 pA	7.5 10^6	80	0.1
[118] — IEEE Electron Device Letter, 2005							
10	0.6	-2 to 2 V	9 μA @ -500 mV	100 pA	10^5	200	0.2
[106] — Nano Letters, 2006							
160	2	-15 to 15 V	7 μA @ not indicated	4 pA	10^6	1250	-10
Mean values from this work (median for I_{off})							
33	2-50.4	-3 to 3 V	1.5 μA @ -400 mV	0.18 pA	4 10^6	199	0.0
43	2-50.4	-3 to 3 V	1.0 μA @ -400 mV	1.5 pA	2 10^6	214	0.2
93	2-50.4	-3 to 3 V	2.1 μA @ -400 mV	0.73 pA	7 10^6	255	0.2

Table 5.7: Four important examples of Pd contacted and back gated devices found in literature compared to the devices fabricated within this work (SiO_2 underlayer: 30 nm).

Concerning the on-current, Javey et al. obtain in [30] a better result than the average currents of the devices fabricated in this work, i.e., 3 μA @ 100 mV for long channel devices (3 μm) instead of 1 to 2 μA @ -400 mV. As their devices are supposed to have only a single tube as S/D link, this turns to an on-resistance of $\sim$ 33 kΩ. They also fabricate devices with shorter channel (300 nm) and obtained an ultra low on-resistance of 10 kΩ (@ 1 mV), i.e., almost the theoretical limit of 6.5 kΩ. The diameter of their SWNTs, i.e., 3.5 nm, is bigger than those in this work, which leads to the normalized current of 860 μA/μm @ 100 mV. However, no indication about the number of fabricated devices with comparable properties is given. The results refer to a single transfer characteristic for each different device geometry. The on-currents in [117] and [118] are logically much higher due to reduced channel lengths (360 and 600 nm only). The on-current of [106] is also higher, but the drain voltage is unfortunately not indicated so that no comparisons are possible.

Concerning the off-currents, our devices show improved performances compared to the other groups. This proves again the suitability of the devices reported in this work for low power low voltage applications. Due to excellent on- and off-current properties, our devices show very competitive on/off ratio, i.e., an **average** value above 10^6.

Concerning the subthreshold slope, the results of [30] are comparable to our results (i.e., 200-250 mV/dec for EOT of 33-93 nm) since the subthreshold slope is found to be around 150 mV/dec for an EOT of 67 nm. On the contrary, the slope of [106] is found to be much worse (1250 mV/dec) which could be explained by the very large gate voltage cycling range. Indeed, we also noticed that the slope increases slightly with increased gate voltage cycling range (see Fig. 4.22). In [117], Seidel et al. obtain an excellent result, i.e., a very steep slope of 80 mV/dec for a device with 360 nm as channel length, which can be explained by the ultra

thin EOT they used (i.e., 12 nm). However, they also show that the lateral down-scaling of the transistors degrades substantially the subthreshold slope, in a similar way as in short channel MOSFETs. Their 18 nm channel device, which is the CNTFET with the shortest channel length ever published, shows indeed a degraded slope of 200mV/dec. Note that there is again in the paper neither an indication of large-scale fabrication, nor of the reproducibility of the results.

Lastly, the results obtained for the forward threshold voltages are comparable to ours. For reduced gate voltage cycling ranges (-2 to 2 V), $V_{th,f}$ is close to 0 V. In [106], the high value of $V_{th,f}$ (i.e., -10 V) is easily explainable through the very large V_g cycling range (i.e., -15 to 15 V). Such a V_g cycling width / $V_{th,f}$ magnitude dependency was also observed during this work (see Fig. 4.22). However, none of the four papers give any indication of backward threshold voltages, since they only plot the forward sweep of the transfer characteristics. The hysteresis effect is neither commented on nor mentioned so that no comparison with our results are possible.

5.4 Application of CNTFETs as memory cells

When looking at the previous results, the hysteresis of the CNTFETs fabricated in this work is found to be a very reproducible effect and could be an advantage for memory technologies, i.e., CNTFETs could be used as memory cells which store an information in the form of a bit (“0” or “1”) and retain it for a sufficiently long time.

Fig. 5.22 shows the evolution of the hysteresis in the transfer characteristics of a s-SWNT CNTFET for different gate voltage cycling ranges. When the gate voltage cycling range is enlarged,

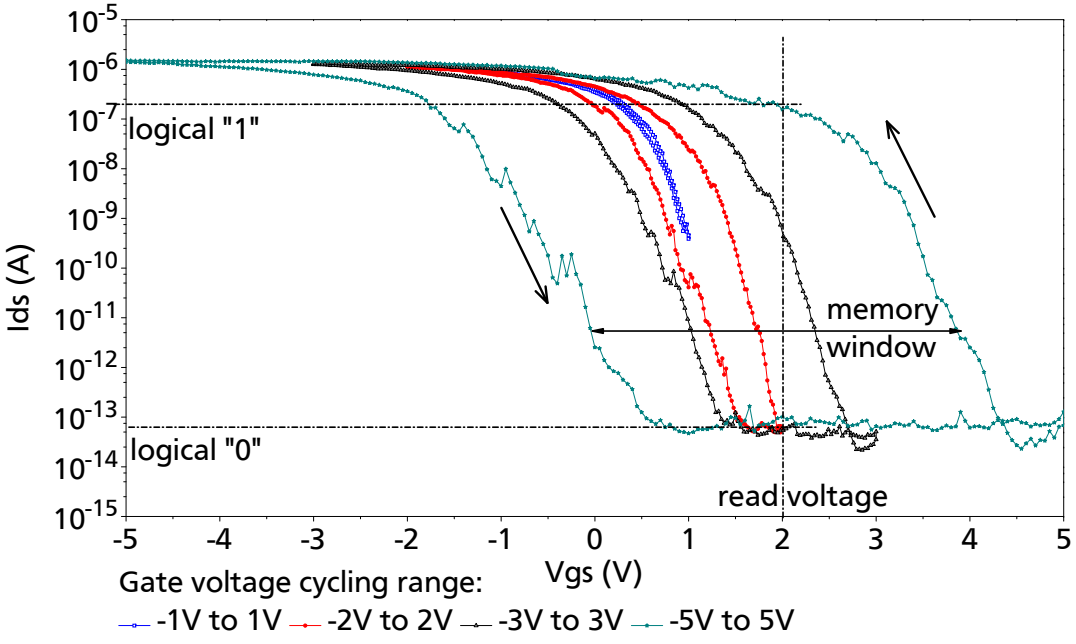


Figure 5.22: Transfer characteristics of CNFTET: development of hysteresis width (i.e., memory window) with increasing gate voltage cycling range, basics of memory operation. Oxide thickness: 40 nm.

the shift in the threshold voltage of the forward and backward sweeps becomes wider (see also subsection 4.3.4). This voltage-programmable shift may also be called *memory window*, which forms the basis for CNTFETs working as memory devices. The operation is explained as fol-

lows: when the gate voltage cycling starts with 5 V, the current measured at a fixed reading voltage of V_{gs} = 2 V is equal to the off-current (∼ 60 fA). In contrast, when the gate voltage ramp starts with -5 V, the current measured at Vgs = 2 V corresponds almost to the full on-current (∼ 200 nA). The gate voltage Vgs = 2 V is called *read voltage* whereas the gate voltages Vgs = 5 V and Vgs = -5 V are the *write voltages* for a logical "1" and "0" respectively.

The voltage-programming also occur when, instead of a continuous voltage ramp, a discrete gate voltage pulse is applied. As shown in Fig. 5.23, applying a gate voltage pulse of -5 V is sufficient to obtain nearly the on-current value of 10^{-7} A at a reading voltage of 2 V. Accordingly, when applying a programming gate voltage pulse of 5 V and subsequently reading at 2 V, the measured current is equal to the off-current of 10^{-13} A. The "0" and "1" current levels are seen to be temporally stable and stay within the same decade when measuring them 120 times successively, which corresponds to four and two minutes, respectively. The current ratio at the reading voltage between the logical "1" level (on-current) and the logical "0" (off-current) is called in this work the *1/0 ratio*. To insure sufficient signal-to-noise properties this ratio should be as high as possible. The device in Fig. 5.23 exhibits a 1/0 ratio of 10^6. Comparing with some other groups who published on CNTFET memory cells, such a high 1/0 ratio cannot be found. Radosavljevic et al. published on non volatile memory based on ambipolar transistors [102]. However, the measurement of I_{ds} versus time and V_{gs} is not shown so that no comparison of on/off ratio can be done. In [119], the ratio of the logical levels is only about 10^2. Fuhrer et al. published on high mobility CNTFET memory cells [61]. However, the I_{ds} versus time and V_{gs} measurement is plotted without using the logarithmic scale so that a comparison is not possible. To the best of our knowledge, the CNT memory devices processed in this work possess the highest "1/0" ratio ever published of about 10^6 already at ultra low drain bias of Vds = -400 mV.

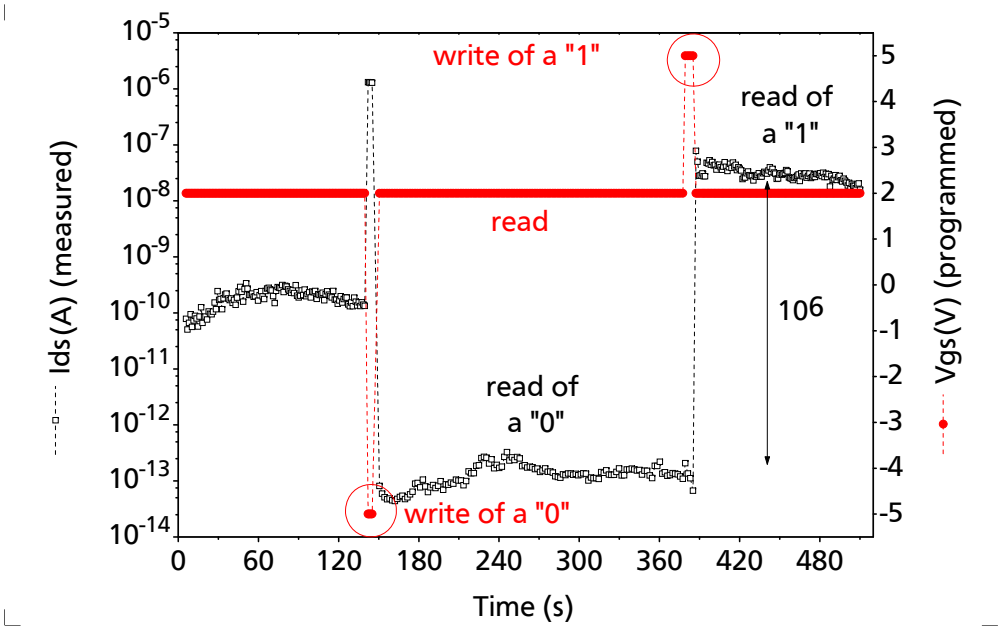


Figure 5.23: Cycling of CNTFET memory cell. Applied gate voltage and measured drain-source current plotted versus time.

Fig. 5.24 illustrates the endurance, i.e., the reproducibility of the "0" and "1" current levels after performing several write operations. The current obtained by reading remains at the same

level and depends only on the programming gate voltage applied before (i.e., -5 or 5 V). Also, the current levels do not depend on the previous history of read/write cycles.

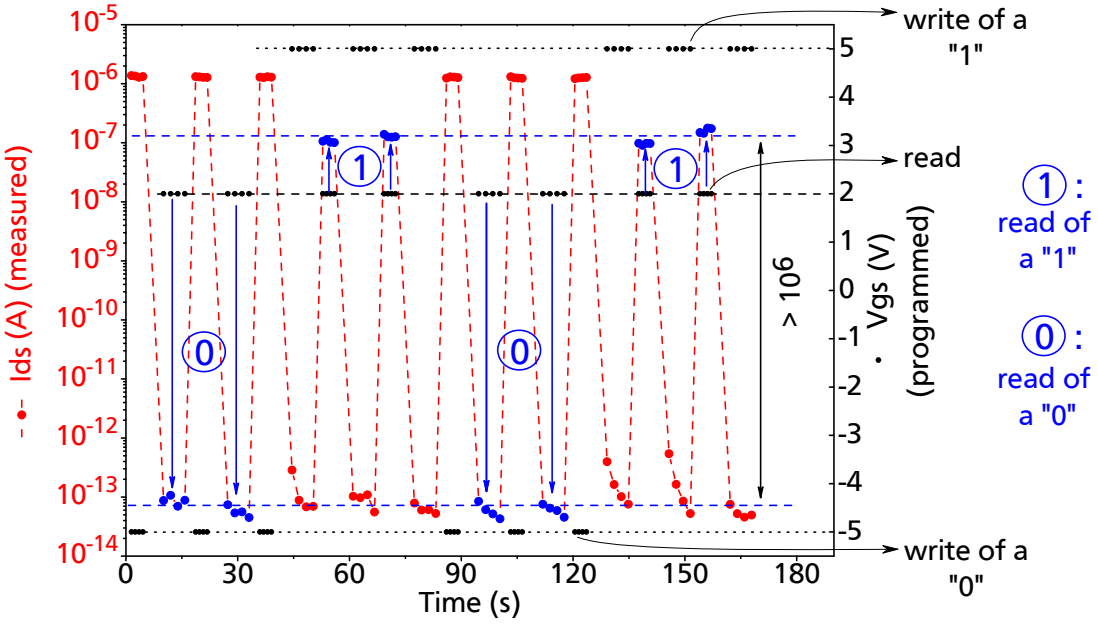


Figure 5.24: Reproducibility of drain voltage levels for different applied gate voltage cycles. By applying V_{gs} = -5 V (5 V), a logical "0" ("1") is written. By applying V_{gs} = 2 V (read voltage), the I_{ds} are measured, which gives the information if a logical "0" or a "1" has been stored.

As shown in the previous sections, all fabricated devices which contain a single s-SWNT as channel (58% of the working devices, i.e., devices with at least one SWNT as S/D link) work in a similar way. Accordingly, they can all be used as memory cells. To confirm this, many devices have been measured as memory cells in the same way as presented in Fig. 5.23. All measurements give the same satisfying result. Consequently, the yield of high quality memory cells within all functional devices is 58%. By adjusting the SWNT density (through the catalyst thickness) and/or the geometry of devices (S/D width/spacing), the percentage of small on/off ratio (i.e., 34% of all functional devices) can be reduced or eliminated. In the same way, the portion of non-working cells (devices without SWNT) can be eliminated. The only problem is the remaining few percent of devices with exclusively metallic tubes. They cannot be used as memory cells because their current does not (or not sufficiently) depend on the gate voltage. However, in memory application, the so-called *redundancy* technology is well-known and extensively used. It means that more cells are fabricated than those normally addressable. The additional cells are used if necessary to replace defective cells within the normally addressable cells, which are detected during the test phase [120]. For this reason, the selective growth of s-SWNTs over m-SWNTs is not crucial in memory technology. Important is that the process is optimized for the growth of a single SWNT per cell (i.e., a single SWNT links source and drain electrodes).

As a conclusion of this section, the novel process reported in this PhD work is suitable for large-scale fabrication of CNT memory cells (see list of publications and conference contributions, 1). Since the hysteresis measured at a gate voltage cycling range of 3 V is found to be independent of the SiO_2 thickness (see subsection 5.3.2, especially Fig. 5.21), the charges participating in the memory effect originate most likely from the sacrificial catalyst (i.e., the aluminum oxide) rather than from the SiO_2. Accordingly, this process is applicable for devices with downscaled

EOT. Moreover, the nanometer scaled size of the SWNTs opens the possibility of a high density integration of the memory cells: Bit density in the range of the terabit per square centimeter are theoretically expected for carbon nanotube based memories when an appropriate lithography method is used [121, 122].

5.5 Conclusion

In this chapter, an evaluation of the yield and capability of the novel self-aligned fabrication process for Pd contacted and PMMA passivated CNTFETs reported in chapter 4 has been performed on a large scale, i.e., based on the measurement of almost 700 devices. Statistics on electrical parameters based on the complete evaluation of transfer characteristics are performed on 90 devices with different oxide thicknesses.

The results are encouraging. The percentage of functional devices (with any kind of SWNT connection) is above 70%. Within this 70%, almost 60% of the transistors are high on/off ratio devices. The other devices exhibit either a metallic SWNT as S/D link (8%) or a reduced on/off ratio (34%) due to a mixture of s- and m-SWNTs which serve as channel. Both non-working and small on/off ratio devices should be eliminated by further optimization of the catalyst and the device geometry, leading to exactly one SWNT per device. The electrical parameters are found to be fairly competitive when compared to other leading groups working on CNTFETs or to the ITRS requirements for the next 8 to 15 years. The on-current of present CNTFETs should be increased by improving the contact between Pd and SWNTs, e.g. by annealing the devices after fabrication. The hysteresis is found to be a stable phenomenon, both in the time and by comparing all devices with each other.

Lastly, the utilization of CNTFETs as non volatile memory cells is found to be very promising, probably more than as replacement for the MOSFETs in logic circuits. The CNTFET fabrication process reported in this work is suitable for the production of memory cells firstly because, a 100% yield is not necessery in memory manufacturing due to the use of redundance technology, which solves the problem of the remaining devices with metallic SWNTs. Furthermore, the devices produced in this work can be down scaled since the hysteresis is not found to depend on the SiO_2 thickness. We believe that the hysteresis is caused by the charges located in the sacrificial catalyst or at the interface SiO_2/catalyst. The catalyst thickness being only a few nanometers (EOT$\sim$3 nm), reducing the SiO_2 underlayer to 1 nm would correspond to a reduced EOT of 4 nm.

Chapter 6

Conclusions and future prospects

6.1 Conclusions

Carbon nanotubes field-effect transistors are recognized as a major topic in nanoelectronics because they could replace traditional MOSFETs in future generations of integrated circuits. The active part of CNTFETs, i.e., the channel, is formed by a semiconducting single-walled carbon nanotube, the growth of which represents one of the great challenges of CNT technology. Most publications on this topic report on a separate growth of nanotubes, which often requires complicated manipulation and assembly after growth. However, this is not practical for fabrication of integrated circuits with millions of transistors.

One major goal of this PhD thesis deals with the investigation of the large scale integration of CNTFETs. The work reports on the development of a novel fabrication process for CNTFETs, which is self-aligned and based on *in situ* growth of carbon nanotubes, i.e., the growth directly in their final place on the wafer. With this process, feasibility of mass fabrication of CNTFETs could be demonstrated for the first time. The major novelty of the process consists in the introduction of a "sacrificial catalyst". The sacrificial catalyst is composed of a bilayer of aluminum and nickel of precisely optimized thickness, which transforms itself into an insulator (aluminum oxide covered with nickel nanoclusters) during the high temperature growth process. When comparing to the often practiced external production of SWNTs with subsequent coating or placement, the *in situ* growth method is more reliable, time-saving and reduces the risk of contamination of SWNTs. Furthermore, we used a complete *in situ* approach, i.e., not only the growth of the nanotubes, but also the formation of the catalytic particles occurs *in situ*. Although *in situ* CNT growth can also occur from particles which are externally fabricated and subsequently randomly disperse on the substrate, this approach often exhibits large distribution in cluster diameter and thus variations in CNT diameter and electrical characteristics. In contrast, the process presented in this work requires only standard electron-beam evaporation of common metals (Al/Ni). The simple optimization of the metal thicknesses (down to 0.9 nm) allows the precise control of the size and the density of the catalytic nickel nano-particles and thereby the control of the diameter and the density of the SWNTs. The *in situ* grown SWNTs have a diameter of approximately 1 nm and a narrow diameter distribution. With this simple and time saving novel fabrication process, more than 15,000 CNTFETs have been fabricated, using only standard CMOS equipment.

An extended electrical characterization of the devices has been performed. First, the hysteresis in the transfer characteristics of CNTFETs has been studied in detail. It has been demonstrated that the most probable cause of hysteresis is related to trapping and detrapping of electrons: electrons of the SWNTs are injected into aluminum oxide traps at high positive gate voltages and are detrapped at high negative gate voltages. The electron charge which is trapped in the aluminum oxide adds to the gate potential "seen" by the SWNTs, which causes the hysteresis. Since the Al/Ni sacrificial catalyst used for all tests has a constant thickness, the resulting aluminum oxide after processing has also a constant thickness and thus, a constant amount of traps. This explains why the hysteresis of the device transfer characteristics has been found to be constant, i.e., independent of the thickness of the SiO_2 underlayer. This indicates that the fabrication process proposed in this thesis has a potential for further down scaling.

Based on the comprehensive study which has been performed, the hysteresis is found to be a very stable and reproducible effect. Accordingly, CNTFETs are very suitable candidates to be used in memory applications. Details on the operation of s-SWNT memory cells have been presented in chapter 5. The current ratio at the reading voltage between the logical "1" level

(on-current) and the logical "0" (off-current) is up to 10^6, which is, to the best of our knowledge, the highest current ratio of logical levels ever published for CNT memory cells. The "0" and "1" current levels are temporally stable indicating the possibility for non-volatile memory usage.

The suitability for mass fabrication of this process has been verified on more than 15,000 devices. Extended yield statistics on 700 devices have been performed, leading to the result of 41% of fully functional high on/off ratio devices (better than 10^3) within all fabricated devices, i.e., devices with source/drain spacing ranging from 1.6 to 6 μm and width from 5 to 50 μm. Optimization of the device geometry should further improve the yield drastically. Almost one hundred of the devices have been completely evaluated, i.e., on- and off-currents, threshold voltages and subthreshold slopes have been recorded and analysed to perform statistics on device performance and reliability. The devices exhibit very good performances, at a very low drain source biais of -400 mV. Table 6.1 summurized the parameters of devices with a SiO_2 thickness of 30 nm. Such a low-voltage low-power technology is compatible with mobile applications. Moreover, all parameters show a quite narrow distribution of their values around the mean value (see chapter 5, subsection 5.3.2).

	I_{on}	on/off ratio	slope
best value	5.8 μA	2.3×10^7	122 mV/dec
mean value	1.5 μA	3.6×10^6	199 mV/dec

Table 6.1: Performances of CNTFETs fabricated within this PhD, with an SiO_2 thickness of approximately 30 nm.

On the one hand, this well-grounded study clearly attests to the potential for large scale manufacturing of CNTFETs for future industrial applications. On the other hand, the process is also a remarkable technolgy platform for research on CNT electronics because a large number of devices can be realized easily and in a short time, which opens the possibility to investigate the influence of numerous fabrication parameters or environmental impacts on CNTFET electrical characteristics and reliability.

6.2 Future prospects

The scalability of CNTFETs, which is a major requirement for replacing MOSFETs in logic applications or for being used in memory technology, needs to be investigated more in detail. For example, CNTFETs with sub-100 nm channel length could be fabricated by means of electron beam lithography. Special alignment marks are already available in the mask for optical lithography which has been designed during this PhD. The marks allow the alignment of two patterning steps on each other, i.e., the electron beam lithography (patterning of the narrow channel region) on the optical lithography (patterning of the source and drain electrodes).

As an additional perspective, the process developed in this thesis opens the possibility to fabricate circuits, either by structuring a top gate on the *in situ*-grown SWNTs or by using isolated buried bottom-gates on silicon-on-insulator wafers. Theoretical studies on circuit and device design in the on-going collaboration with the Nanoelectronics Lab of IMS (Laboratory of Integration From Materials to System) in Bordeaux, France, could further complement this investigation.

In this context, further structural characterization and correlation with electrical results appear also to be of interest. For this, the PMMA layer needs to be etched off on wafers which have already been measured extensively with the semiconductor parameter analyzer. Subsequently, AFM and C-AFM measurements on unprotected SWNTs and structures need to be performed to enable precise measurements of effective channel length (i.e., length of the SWNT). From the comparison with the macroscopic measurements, e.g. transfer characteristics, a better understanding of the CNT devices should result, which would allow further optimization of CNTFETs fabrication.

The influence of alternative S/D electrode materials could also be investigated, to confirm the theoretical expectation outlined in chapter 2. For example, it could be verified if the fabrication of unipolar n-type CNTFETs is possible when using a metal with the appropriate work function (e.g. Al). The realization of stable n-type CNTFETs, which do not convert into p-type in various ambient environments, is a major requirement to make the devices suitable for industrial production.

The final perspective discussed is related to the investigation of CNTFETs as sensors. The observed hysteresis in CNTFET transfer characteristics is a first evidence that the devices are very sensitive to their environment, which means that they have a potential as sensors in numerous applications, like in biology or chemistry. Intensive research activities in carbon nanotube based sensors have been reported over the past years, since carbon nanotubes may have the potential of revolutionizing the sensor industry [123]. The CNT technology developed in this thesis is an ideal basis for sensor research (when using the fabrication process for unpassivated CNTFETs) and may be used in a future work as a technology platform to test different applications, also in collaboration with other research groups, working in biology or chemistry. For example, the

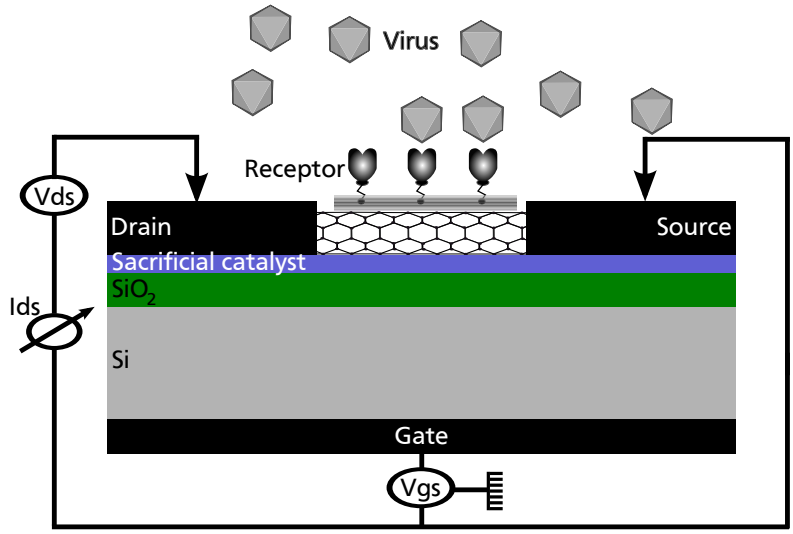
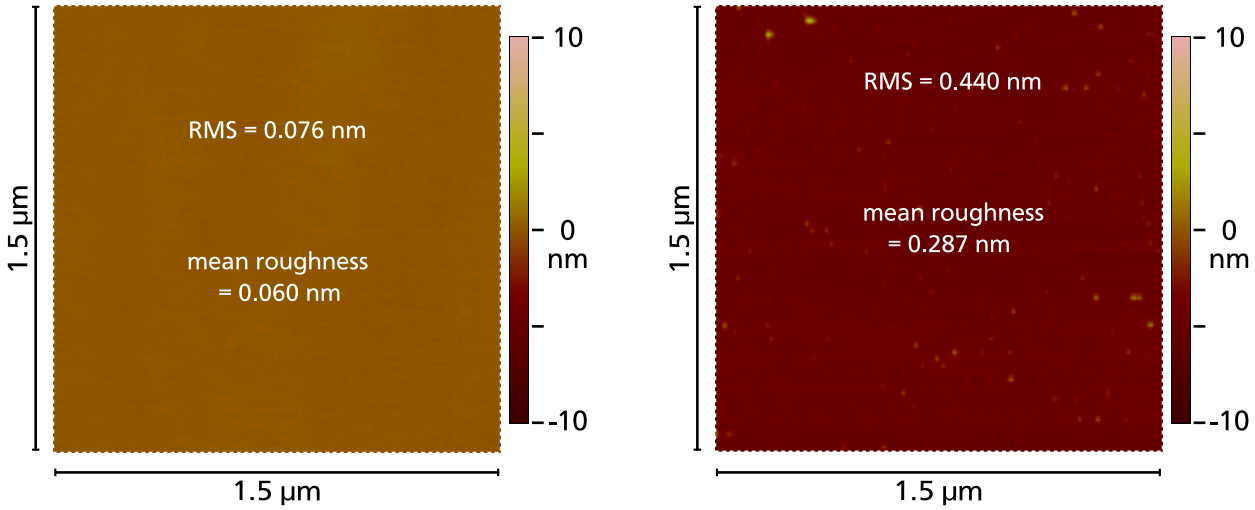


Figure 6.1: Illustration of proposed CNTFET-sensor for virus detection. The semiconducting SWNT is functionalized with a suitable receptor to allow selective bonding of virus.

detection and identification of single viral particles is possible using functionalized CNTFETs acting as sensors as illustrated in Fig. 6.1. The binding of a virus to a suitably functionalized semiconducting SWNT may measurably affect the characteristics of the SWNT due to a charge transfer with the virus. The virus detection is thus performed electronically via the CNTFET which alters its transfer characteristics in presence of a virus (see also list of publications and conference contributions, 4).

Appendix: Investigation of SiO_2 roughness

To investigate SiO_2 roughness, comparisons of the roughness of different materials has been carried out. Fig. 0.2 shows the AFM measurements of silicon and SiO_2 roughnesses. The rough-



(a) silicon

(b) SiO_2 after catalyst patterning

Figure 0.2: Comparison of surface roughness measured by AFM.

nesses are evaluated with two indicators: mean and RMS roughnesses. The program calculates the roughness either for the whole scan ("image statistics") or for a defined region ("box statistics"). The reference plane for roughness calculations is called mean plane and is calculated as average of all height values (Z) of the whole scan or of the selected box, as expressed in equation (6.2) where N is the number of points of the whole scan or of the selected box. It can be negative because the Z values are measured relative to the height value when the microscope is engaged, considered as zero. [124]

$$MP = \frac{1}{N}\sum_{i=0}^{N} Z_i$$

The mean roughness is then the arithmetic average of the surface height deviations (absolute values) measured from the mean plane, as expressed in equation (6.2).

$$mean\ roughness = \frac{1}{N}\sum_{i=0}^{N} |Z_i - MP|$$

The RMS roughness is the root mean square average of height deviations taken from the mean plane, as expressed in equation (6.2).

$$RMS\ roughness = \sqrt{\frac{1}{N}\sum_{i=0}^{N}(Z_i - MP)^2}$$

As a result, the roughness of a silicon wafer after chemical cleaning is found to be under 0.1 nm whereas the roughness of SiO_2 after catalyst patterning is about 0.3-0.4 nm (see 0.2). This is sufficient to detect 1 nm diameter SWNTs lying on the surface but a small incertitude about the measurement of their diameter can appear. According to the scan line chosen to do the cross section, the diameter of the measured SWNTs can be smaller or larger, due somewhat to AFM tolerance (in the sub-nm range) and mostly to residual SiO_2 surface roughness. For this work, it has been decided to always take as a result the cross section along the line giving the biggest SWNT diameter.

List of publications and conference contributions

Publications

1 L. Rispal, U. Schwalke, "Large-Scale In Situ Fabrication of Voltage-Programmable Dual-Layer High-κ Dielectric Carbon Nanotube Memory Devices With High On/Off Ratio,", IEEE Electron Device Lett., vol. 29, pp. 1349-1352, 2008.

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3 L. Rispal, T. Tschischke, H. Yang, and U. Schwalke, "Mass-Production of Passivated CNTFETs: Statistics and Gate-Field Dependence of Hysteresis Effect," ECS Trans., vol. 13, p. 65, 2008.

4 U. Schwalke and L. Rispal, "Fabrication of Ultra-Sensitive Carbon Nanotube Field-Effect Sensors (CNTFES) for Biomedical Applications," ECS Trans., vol. 13, p. 39, 2008.

5 L. Rispal, R. Heller, G. Hess, G. Tzschöckel, and U. Schwalke, "Self-aligned Fabrication Process Based on Sacrificial Catalyst for Pd-Contacted Carbon Nanotube Field-Effect Transistors," ECS Trans., vol. 11, pp. 53-61, 2007.

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Conference contributions

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12 L. Rispal, H. Yang, R. Heller, G. Hess, G. Tzschöckel, and U. Schwalke, "Self-aligned Fabrication Process for Pd-Contacted and PMMA-Passivated Carbon Nanotube Field-Effect Transistors," in Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba (Japan), 2007.

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22 F. Wessely, L. Rispal, and U. Schwalke, “Mix-and-match Lithography Based Ultrathin-body SOI Nanowires and Schottky-S/D-FETs,” in 10th Annual Workshop on Semiconductor Advances for Future Electronics and Sensors (SAFE), Veldhoven (The Netherlands), 2007.

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- **S 251** W. Kutschenko: Herstellung und Auswertung von in-situ-kontaktierten Kohlenstoff-Nanoröhrchen. 2005
- **S 255** P. Hofmeyer: Zusammenfassung des aktuellen Standes der Forschung zu Kohlenstoffnanoröhrchen-Transistoren. 2006
- **S 258** H. Yang: Passivierung von Kohlenstoff-Nanoröhrchen Feld-Effekt-Transistoren mittels PMMA zur Verbesserung der elektrischen Eigenschaften. 2007
- **S 259** T. Tschischke: Optimierung des selbst justierten Herstellungsprozesses von PMMA-passivierten Kohlenstoff-Nanoröhrchen Feld-Effekt-Transistoren. 2007

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2000-2002	Ecole Supérieure d'Electricité (Supélec), Gif-sur-Yvette, Frankreich Electrical Engineering, Information Technology and Computer Sciences Certification: Diplôme d'ingénieur de l'Ecole Supérieure d'Electricité Supélec (short for "Ecole Supérieur d'Electricité") is one of France's prestigious Grandes Ecoles, one of the top in its field of electrical and computer engineering.
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1991-1998	High Schools, Brétigny sur Orge/Arpajon, Frankreich Certification: Baccalauréat (very good)

Darmstadt, den 19. August 2009