## Schottky Diode Based Envelope Detectors in Planar Topology for UWB and W-Band

Vom Fachbereich Elektrotechnik und Informationstechnik der Technischen Universität Darmstadt zur Erlangung des akademischen Grades eines Doktor-Ingenieurs (Dr.-Ing.) genehmigte

#### Dissertation

von

M.Sc.

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## **Preface**

This thesis presents my research results obtained as a Ph.D. candidate in the Institute for Microwave Engineering and Photonics (IMP) at the Technische Universität Darmstadt and at the Technische Hochschule Mittelhessen. At this point, I would like to express my most sincere gratitude to all the people who have supported me on the long road to my doctorate, whether they were directly involved as supervisors, colleagues or coworkers, or were part of my life outside the PhD, both friends and family.

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During my PhD, I have stayed in a total of four universities: THM and TU Darmstadt in Germany, DTU and TU/e in Denmark and the Netherlands. Indeed, I feel really thankful to all of the people with whom I have worked and from whom I have learnt so much. Most of them have become friends as well. I would like to start thanking Idelfonso, for all his trust during these years and for all his guidance and kind recommendations; Tom, for always challenging me to learn more; Jesper, for placing me on the road to be an RF engineer. I shall not forget my other colleagues. Bruno, who has always been there, both in technical and personal areas; Alvaro, Dimitris, Yunfeng, Simon, Javi, Andrés, Sebastian: with you I have learnt so many things, spent so much time in the lab and enjoyed many great moments.

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## Abstract

The massive growth in the demand of wireless communication data rates and services require new technologies to grant broader bandwidths to end users. This work is encompassed in the European project CELTA (Convergence of Electronics and Photonics Technologies for Enabling Terahertz Applications) within the beamformer demonstrator, which aims to develop a transmitter and a receiver capable of providing high bitrate wireless indoor communications operating at W-band (75 GHz to 110 GHz).

This dissertation presents the design of five Schottky diode based balanced Envelope Detectors (ED). The first two detectors, UWB1 and UWB2, operate in the Ultra-WideBand (UWB) frequency range from 3.1 GHz to 10.6 GHz and are used to compare different architectures at low complexity and cost. The other three, ED1, ED2 and ED3, work in the W-band for the final goal of the beamformer demonstrator.

UWB1 is composed of a balun that splits the input signal into two 180° out of phase signals and a single balanced detector circuit. It demodulates in real time and error free up to  $4\,\mathrm{Gbit/s}$  Amplitude Shift Keying (ASK) signals with carrier frequencies between  $4\,\mathrm{GHz}$  and  $8\,\mathrm{GHz}$ . It reaches a World record in the State of The Art in terms of bitrate to carrier frequency ratio,  $\Delta b$ , of  $100\,\%$  for the  $4\,\mathrm{GHz}$  carrier frequency.

UWB2 introduces a novel architecture, combining the functionality of a balun and, at the same time rectification of the input signal, providing a more compact configuration and featuring a higher sensitivity than UWB1. As a consequence of its lower phase balance bandwidth, it demodulates in real time and error free up to  $2.5\,\mathrm{Gbit/s}$  ASK signals modulated onto a  $8\,\mathrm{GHz}$  carrier, providing a  $\Delta\mathrm{b}$  of  $31.25\,\%$ .

In the three W-band EDs, UWB2's architecture is chosen, prioritising sensitivity, size, weight, complexity and cost over demodulated bitrate and phase balance bandwidth. The W-band EDs are built in microstrip line technology, and provide a WR-10 waveguide interface through a microstrip line to WR-10 waveguide transition.

ED1's prototype features an input RF bandwidth of 20 GHz within the W-band, 6 GHz of videobandwidth and demodulates in real time and error free up to 12 Gbit/s ASK signals.

When tested in a wireless system it demodulates up to 7 Gbit/s ASK signals with a 82 GHz carrier transmitted through 1 m. These results not only fulfil the goals set for this dissertation and the CELTA's beamformer requirements, but in addition, it improves the state of the art, since the prior envelope detector using the same diodes and substrate demodulated 3 Gbit/s through 0.5 m.

Moreover, two additional W-band EDs designs are presented. According to simulation

results, both detectors widen the input bandwidth, ED2 up to 35 GHz, i.e. the full W-band, and ED3 up to 29 GHz. Although both envelope detectors have been manufactured, their experimental characterization remains as future work, since due to time constraints it could not be performed.

# Kurzfassung

Die immer wachsende Zunahme der Nachfrage nach Datenraten und Diensten für die drahtlose Kommunikation erfordert neue Technologien, um Endbenutzern breitere Bandbreiten zu gewähren. Diese Arbeit ist ein Teil vom das europäische Projekt CELTA (Convergence of Electronics and Photonics Technologies for Enabling Terahertz Applications) im Rahmen des Beamformer-Demonstrators, mit dem ein Sender und ein Empfänger entwickelt werden sollen, die eine drahtlose Innenkommunikation mit hoher Bitrate im W-Band (75 GHz bis 110 GHz) ermöglichen.

In dieser Arbeit werden fünf Schottky Dioden als Envelopendetektoren (ED) vorgestellt. Die ersten Detektoren, UWB1 und UWB2, arbeiten im Ultra-WideBand Frequenz- bereich (UWB), d.h.von 3.1 GHz bis 10.6 GHz und werden verwendet, um verschiedene Architekturen bei geringer Komplexität und geringen Kosten zu vergleichen. Die anderen drei, ED1, ED2 und ED3, arbeiten im W-Band und sollen für das Endziel des Beamformer-Demonstrators eingesetzt werden.

UWB1 besteht aus einem Balun, der das Eingangssignal in zwei phasenverschobene  $180^{\rm o}$  Signale und eine einzige symmetrische Detektorschaltung aufteilt. Er demoduliert in Echtzeit und fehlerfrei bis zu 4 Gbit/s Amplitude Shift Keying (ASK) Signale mit Trägerfrequenzen zwischen 4 GHz und 8 GHz. Es erreicht eine Weltbestmarke im Stand der Technik in Bezug auf das Verhältnis von Bitrate zu Trägerfrequenz  $\Delta$ b von 100% für die Trägerfrequenz 4 GHz.

UWB2 stellt eine neuartige Architektur dar, die die Funktionalität eines Baluns besitzt und gleichzeitig das Eingangssignal gleichrichtet, eine kompaktere Konfiguration bietet und eine höhere Empfindlichkeit als UWB1 aufweist. Infolge seiner geringeren Phasenausgleichsbandbreite demoduliert es in Echtzeit und fehlerfrei ASK-Signale mit bis zu  $2.5\,\mathrm{Gbit/s}$ , die auf einen  $8\,\mathrm{GHz}$  Träger moduliert sind. Dies entspricht einem  $\Delta b$  von  $31.25\,\%$  entspricht.

In den drei W-Band-EDs wird die Architektur von UWB2 ausgewählt, wobei Empfindlichkeit, Größe, Gewicht, Komplexität und Kosten Vorrang vor demodulierter Bitrate und Phasenausgleichsbandbreite haben. Die W-Band-EDs sind in Mikrostreifenleitungstechnologie aufgebaut und bieten eine WR-10 Hohlleiter über eine Mikrostreifenleitung zum WR-10 Hohlleiterrübergang.

Der Prototyp von ED1 verfügt über eine HF-Eingangsbandbreite von 20 GHz im W-Band, eine Videobandbreite von 6 GHz und demoduliert in Echtzeit und fehlerfrei bis zu 12 Gbit/s ASK-Signalen.

Die Überprüfung in einem drahtlosen System zeigte, dass es demoduliert es ASK-Signale mit bis zu 7 Gbit/s mit einem 82 GHz Träger, der über 1 m übertragen wird. Diese Ergebnisse erfüllen nicht nur die für diese Dissertation festgelegten Ziele und die Anforderungen des CELTA Strahlformers, sondern sie verbessern auch den

Stand der Technik, da der bisherige Hüllkurvendetektor mit denselben Dioden und Substrat  $3\,\mathrm{Gbit/s}$  über  $0.5\,\mathrm{m}$  demoduliert.

Darüber hinaus werden zwei zusätzliche Designs von W-Band-EDs vorgestellt. Gemäß den Simulations- ergebnissen erweitern beide Detektoren die Eingangsbandbreite, ED2 auf 35 GHz, d. h. auf das gesamte W-Band, und ED3 29 GHz. Obwohl beide Hüllkurvendetektoren hergestellt wurden, stellt ihre experimentelle Charakterisierung eine wichtige Aufgabe für zukünftige Vorhaben dar, da sie aus zeitlichen Gründen nicht durchgeführt werden konnte.

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## Acronyms

ADS Advance Design System's

**ASK** Amplitude Modulated Signals

**BER** Bit Error Ratio

**BERT** Bit Error Rate Tester

**BW** Bandwidth

**BWO** Backward Wave Oscillator

 $C_g$  Capacitance Related with the Schottky diode Pads

 $C_j$  Schottky diode Junction Capacitance

**CL** Conversion Loss

 $C_p$  Schottky diode Parallel Capacitance

**CT** Co-Propagating Tone

**CW** Continuous Wave's

**DD** Data Detection

**DRW** Dielectric Rod Waveguide

**DTU** Technical University Of Denmark

ECL External Cavity Laser

**ED** Envelope Detector

**EDFA** Erbium Doped Fibre Amplifier

**EM** Electromagnetic

 $f_c$  Carrier Frequency

**FR** Frequency Response

**HW** Hollow Waveguide

ITN International Training Network

L1 Level Of "1" Bits

LC Liquid Crystal

**LNA** Low Noise Amplifier

LO Local Oscillator

**LPF** Low Pass Filter's

**LPF** Low-Pass Filter

 $L_s$  Schottky diode Series Inductance

MPA Medium Power Amplifier

MSL Microstrip Line

**MZM** Mach-Zehnder Modulator

OS Optical Signal

PC Polarisation Controller

PCB Printed Circuit Board

**PD** Photodiode

**PPG** Pulse Pattern Generator

PRBS Pseudo-Random Bit Sequence

PVNA Photonic Vector Network Analyser

 $R_j$  Schottky diode Junction Resistance

 $R_s$  Schottky diode Series Resistance

**SMD** Surface Mounting Device

**SoTA** State Of The Art

SSB Single Sideband Demodulation

TU/E University Of Technology

TUDa Technical University Of Darmstadt

**UWB** Ultra-Wideband

VOA Variable Attenuator

 $\mathbf{VSG}$  Vector Signal Generator

**WSS** Wavelength Selective Switch

## 1 Introduction

This doctoral (PhD) dissertation stems from the author's work over the last four years, where he was involved within an European project named CELTA [CEL] and completed secondments in the Eindhoven University of Technology (TU/e), the Technical University of Denmark (DTU) and in Bifrost Communications [Com].

This first chapter starts describing CELTA, follows listing the goals which have been pursued during the PhD and ends explaining this dissertation's structure.

CELTA is the acronym for Convergence of Electronics and Photonics Technologies for Enabling Terahertz Applications. It is an European International Training Network (ITN) project, led by the Eindhoven University of Technology (TU/e) and concentrates the work of 15 PhD students from 12 partners located in 9 different countries [CEL]. CELTA's spirit is to introduce the strategy of converged electronics and photonics co-design and establish a common engineering language in its training programme across the electronics, photonics and applications disciplines. In CELTA the research is structured in three subprojects, named demonstrators, in which PhDs collaborate and join efforts to develop a solution to a challenge or an application.

The first demonstrator is a free space photonic vector network analyser (PVNA) based on homodyne photomixing. Its frequency is ultra-wide tunable and can be used in mmW characterization, spectroscopy and material characterization.

The second demonstrator is an imager based on a GaN plasmonic FET camera, used in non destructive material testing, biomedical diagnoses and safety inspection.

The third demonstrator, named the beamformer demonstrator, aims to develop a transmitter and a receiver capable of providing high bitrate wireless indoor communications using high directive antennas and beamforming to align the beam from the transmitter antenna with the receiver. The author's work contributes exclusively to the beamformer demonstrator.

#### 1.1 Beamformer demonstrator

In the last years there has been a steady increment in the demand of wireless communication bandwidth which will rise even faster in the future [Cis20]. This growth in the demand motivates the research of new spectrum allocations in the THz range, in order to provide broad bandwidth for signal transmission [NDR16]. Migrating to higher frequencies implies increasing the attenuation due to higher free space losses [Rap+13].

The beamformer demonstrator operates at W-band (75 GHz to 110 GHz) and is designed for high speed short range wireless communication. It takes advantage

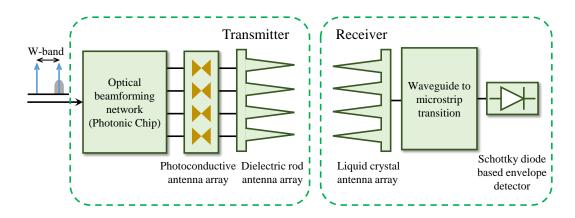


Figure 1.1: Beamforming demonstrator schematic.

of high directive antennas that counteract attenuation and low achievable power levels at THz frequencies [UK16; Rap+13]. By applying beamsteering, the usage of future portable devices with high data rate becomes possible. Figure 1.1 shows the beamformer demonstrator's schematic, which is divided into a transmitter and a receiver.

The beamformer transmitter is composed by a 1x4 optical true time delay beamforming network integrated into a Si<sub>3</sub>N<sub>4</sub> photonic chip [MM18] and a dielectric rod waveguide antenna array which uses photoconductive antennas as antenna elements [Mor+19].

The beamforming network is fed with an optical signal containing two optical carriers, which are separated by the frequency of the desired output electrical signal, which in this project is within the W-band (75 GHz to 110 GHz). One carrier is modulated with the desired data signal. The delay of the four branches can be tuned by using thermo-optic modulators at the desired wavelength, which leads to the change in the beam direction [MM18]. For each branch, the optical beam, composed of the two optical signals is focused onto a semiconductor region with a photomixer on each one, where the electrical current is generated.

The photomixer substrate is glued on a high-resistivity silicon rod antenna (DRW) as shown in figure 1.2. The transmitter antenna array is composed by four elements, spaced by  $\lambda/4$ . The simulated radiation pattern at 85 GHz when the phase difference ( $\Delta\Phi$ ) between the adjacent antenna elements is shifted is depicted in figure 1.3 . The maximum spatial beam steering is 25°, obtained with a  $\Delta\Phi=90$ °.

Alvaro Morales Vicente from the Eindhoven University of Technology (TU/e) [Teca] and Serguei Smirnov from KTH Royal Institute of Technology [Tecb] are in charge of the design of the photonic chip and the DRW antenna respectively. At the time when the dissertation was finished, the transmitter antenna was still under fabrication, therefore, it is not possible to show experimental results. A more detailed discussion about both elements can be found in [Mor+19],[MM18] and in their PhD dissertations.

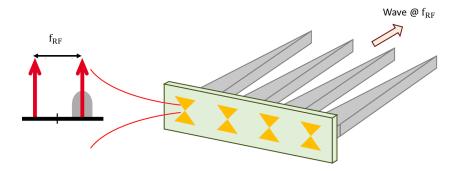


Figure 1.2: Schematic of a dielectric rod waveguide (DRW) antenna array integrated with four photomixers for sub-THz beam steering [Mor+19].

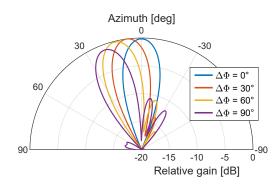


Figure 1.3: Simulated radiation pattern in the horizontal plane at 85 GHz of the DRW antenna array [Mor+19].

Two different receiver architectures are designed within the CELTA's beamformer demonstrator: one by the Warsaw University of Technology, presented in [NY19] and another one by the TU Darmstadt (TUDa), which is the one discussed in this dissertation. The receiver designed at TUDa consists of two blocks: A liquid crystal (LC) antenna array and a Schottky diode based envelope detector (ED) built in planar technology. The interface connection between both blocks is realized as a WR-10 waveguide to microstrip line transition.

#### Liquid crystal antenna array

The beamforming receiver antenna consists of a 1 x 4 rod antenna array and a liquid crystal (LC) based phase shifter. The LC mixture GT7-29001 provided by Merck KGaA is specifically synthesised for microwave applications [Ree+19].

The phase shifter design was first presented in [Jos+16], and its fabrication process is described in detail in [Ree+19]. The phase shifter is made of a cross-linked plastic Revolite with  $\epsilon_r$ =2.53 and  $\tan \delta = 0.0006$  at 100GHz, filled with the GT7-29001 LC

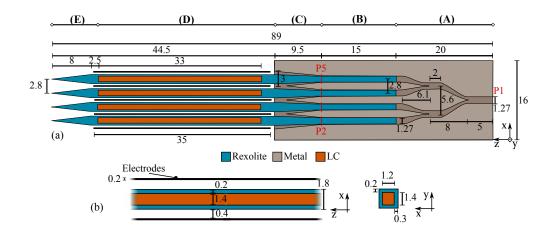


Figure 1.4: Cross section of the proposed rod antenna array. a) (A) Cascaded E-plane power divider. (B) Dielectric taper. (C) Horn-like transition from metallic waveguide to dielectric waveguide. (D) Phase shifter section. (E) Rod antennas. b) Detailed view of the phase shifter section including the electrodes. All dimensions are given in mm. [Ree+19].

[FB97; Ree+19].

The phased array antenna follows the schematic from figure 1.4. It is composed of a cascaded E-plane power divider (A), a dielectric taper (B) inserted into the waveguide, horn-like transitions from waveguide to dielectric waveguides (DW) (C), the phase shifter section (D) and the rod antenna elements (E). Figure 1.5 shows the manufactured LC antenna. More details about the design and fabrication can be found in [Ree+17; Ree+19].

The phased array was manufactured and evaluated at TU Darmstadt facilities obtaining 11.5 dBi of antenna gain at 85 GHz for the non-steered radiation towards 0°and 9.1 dBi when steering towards -25°[Ree+19]. The radiation patterns for each

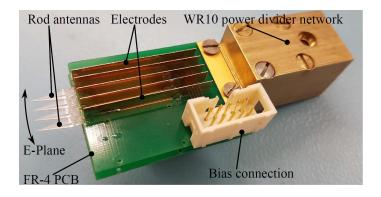
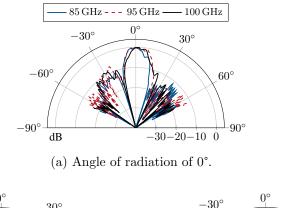


Figure 1.5: Manufactured LC antenna [Ree+19].



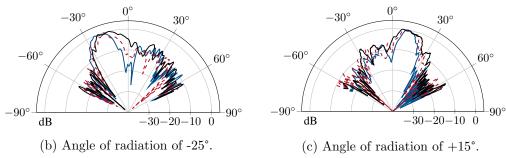


Figure 1.6: Measured E-plane antenna pattern at three frequencies for three different angle of radiations [Ree+19]

steering angle are displayed in figure 1.6.

The LC phased array antenna was designed and measured by Roland Reese, PhD at the Institute for Microwave Engineering and Photonics at TU Darmstadt. Similarly, as with the transmitter, a more thorough description and discussion about the LC phase shifters and the antenna can be found in [Ree+17; Ree+19] and in Roland Reese's PhD dissertation [Ree20].

#### Schottky diode based envelope detector

The receiver circuit used in the CELTA beamformer demonstrator includes a zero bias Schottky diode based envelope detector.

Envelope Detectors (ED) are able to rectify an input signal obtaining its baseband harmonic, which can be used to demodulate high data rate Amplitude Shift Keying (ASK) modulated signals. At high frequencies ( $f > 100\,\mathrm{GHz}$ ), they provide a less complex and cost effective solution to build receivers in comparison with heterodyne architectures, which need of a LO [Stö+16; Rom+16a] that has to be fed and cooled down [Hoe+13]. Moreover, the receiver's weight, volume and power consumption are reduced when using envelope detectors, which can be an interesting feature [Coj+19] depending on the application, e.g. space systems [Hoe+15]. On the other hand, heterodyne architectures feature a higher sensitivity and are able to demodulate

phase modulated signals [Rom+16b; Stö+16; Bla+19].

New telecommunication technologies, such as 5G, reduce the cell size, which is cheaper and more power efficient than macrocells [And+14]. In this scenario, sensitivity is no longer such a big limitation as with macrocells, and envelope detectors can play a key role, providing high data rate receivers at lower cost and complexity.

The original objective agreed in the CELTA project proposal was to build a Schottky detector with 20 GHz videobandwidth, using a target frequency of 240 GHz.

The requirements of this dissertation, reduced from the original objective in CELTA due to practical project goals, aimed with this envelope detector were:

- The wireless transmitted ASK signal is modulated using a 90 GHz 95 GHz carrier frequency.
- The envelope detector should be built in planar technology, using Schottky diodes provided by ACST GmbH [ACS].
- The ED's input interface is a WR-10 waveguide, because the LC beamforming antenna and the W-band equipment available at our partners facilities is WR-10 rectangular waveguide based. A waveguide to microstrip transition is needed to provide this interface.

The last goal was the experimental validation of the beamformer receiver by joining this work to the LC antenna designed by Roland Reese [Ree+19].

During the mid term review which took place in December 2017 at TU/e in Eindhoven, the beamformer demonstrator requirements were specified in more detail, being the following:

- The wireless transmitted ASK signal is modulated using a carrier frequency in the range of 80 GHz 85 GHz.
- The envelope detector should provide 5 GHz to 10 GHz input bandwidth, being able to demodulate up to 5 Gbit/s ASK signals.

These specifications are relaxed from the initial envelope detector requirements, to meet the updated features from the beamformer transmitter. They were agreed after the design phase of the first W-band ED, ED1, which was optimised for a target frequency of 92.5 GHz, and operates in the full W-band, therefore the project requirements were met. A summary of all these requirements is summarised in the state of the art in figure 1.7.

This dissertation presents the design of five envelope detectors used to demodulate high data rate ASK signals. The first two work in the Ultra-WideBand (UWB) frequency range (3.1 GHz to 10.6 GHz), are used as an initial approach to envelope detector design, allowing to test different configurations and architecture designs, handling a lower complexity and without having some manufacturing constraints and costs for higher frequency prototypes. They were designed during the internship

at Bifrost Communications and presented within the author's master thesis. The three other envelope detectors operate in the W-band (75 GHz to 110 GHz) and are the final goal of this dissertation.

During the PhD the author accomplished two secondments or external stays, one at the Technical University of Denmark (DTU) for two months in the beginning of 2018 and one at Eindhoven University of Technology (TU/e) for three months between October 2018 and January 2019. The purpose of these secondments was to test the manufactured envelope detector prototypes, learn from the expertise of each team's knowledge and attending to technical specialised courses, such as JePPIX [JeP].

#### 1.2 State of the art envelope detectors

Table 1.1 and figure 1.7 summarise the state of the art of envelope detectors when demodulating ASK signals. They compare the signal's bitrate in [Gbit/s], which equals the video or baseband bandwidth in [GHz] for ASK modulated signals and carrier frequency,  $f_c$ . In addition, table 1.1 presents the figure of merit  $\Delta$ b, introduced in [TMA15; Cim+16; Bla+17], which depicts the demodulated ASK signal's bitrate normalised to its carrier frequency ( $f_c$ ), also addressed fractional bandwidth [Sac12; Poz12]. The state of the art is divided into two groups: those envelope detectors with a carrier frequency comprised in the ultrawideband (UWB) (3.1 GHz - 10.6 GHz); and those working at W-band (75 GHz - 110 GHz). The envelope detectors are sorted according to their architecture, which can be single ended or balance and the connection used when they were tested. More W-band detectors were studied during this dissertation, e.g. [Yao+15; Hoe+14; ZYW15; Hro+13; Xie+10; Tsa+10; Moy+08; Ali+18], but are not added in table 1.1 since they were not used in a communication system.

Single ended architectures have a theoretical  $\Delta b$  limit of 50 % due to the presence of an output spurious at the fundamental harmonic frequency [Poz12]. The mathematical calculation of the demodulated ASK signal can be found within this dissertation in section 2.3. The best experimental  $\Delta b$  value in this architecture family is 41.7% [Cim+18].

It will be mathematically justified in sections 2.3 that introducing a balanced architecture presents the advantage of cancelling the fundamental harmonic at the envelope detector's output [Poz12; Bla+17]; hence relaxing the output low pass filter's (LPF) requirements, which only needs to reject the second harmonic spurious.  $\Delta b$  can be therefore boosted to 100%, as shown in [Bla+17]. Moreover, the use of a balanced architecture reduces the common mode noise at the ED's output [Poz12]. As drawback, balanced envelope detectors present higher conversion loss and lower sensitivity than single ended ones. Additionally, if a behaviour mismatch between the two diodes exists, designing the ED's matching network becomes more complex.

This dissertation's goal is to design a W-band envelope detector with the requirements listed in the previous section. Its connections, in contrast with the other

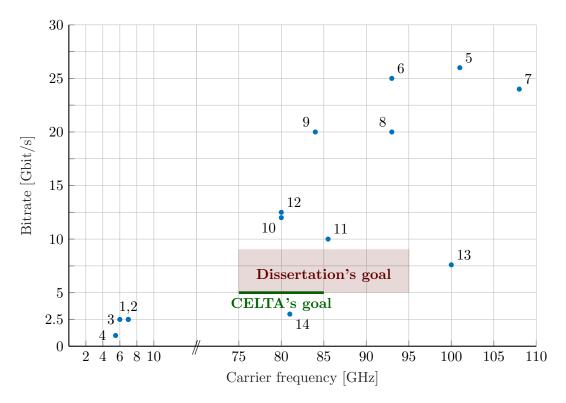


Figure 1.7: UWB and W-band envelope detectors state of the art. References in table 1.1

W-band envelope detectors of the state of the art, should be a WR-10 waveguide at its input, to be able to connect it to the beamformer receiver antenna, and a coaxial at its output. These interfaces allow to use the envelope detector in several systems, just plugging it to the antenna's waveguide, without the need of using expensive probe tips or adapter. In addition, when used in a wireless system, the transmission distance should be of at least 1 m, instead of just a few centimetres.

Ultrawideband (UWB) wireless communication is a technology that allows the transmission high data rates in the unlicensed spectrum from 3.1 GHz to 10.6 GHz [PH03]. The transmitted signal occupies 20 % or more of the relative bandwidth from the central frequency [ECC04] in Europe, or an absolute bandwidth of 500 MHz or more in the USA [FC02].

The advantage of using this frequency range is that UWB communication can operate together with existing wireless systems without assigning new spectrum [Sac12; Rom+17]. Due to the low power spectral density from UWB communication, the other wireless applications will see their interference with UWB signals to behave as noise [OHI04; TE05; Int04]. Since it employs low power emission, it is only suitable for short range radio transmissions [SM04].

The low manufacturing costs convert UWB communication to an attractive technology to be implemented in several applications related to short range wireless

#	Ref	$f_c$ [GHz]	Bitrate [Gbit/s]	$\Delta \mathbf{b}$ [%]	Connection	Architecture
1	[Cim+16]	7	2.5	35.7	Coaxial	Single Ended
2	[Sil+17]	7	2.5	35.7	Coaxial	Single Ended
3	[Cim+18]	6	2.5	41.7	Coaxial	Single Ended
4	[SO07]	5.5	1	18.2	Probe tip on chip	Single Ended
5	[TMA15]	101	26	25.7	Probe tip on chip	Balanced
6	[Kuo+12]	93	25	26.9	Wireless $(0.3 \mathrm{m})$	n/a
7	[Tho+14]	108	24	22.2	Probe tip on chip	n/a
8	[Pan+11]	93	20	21.5	Wireless $(20  \text{cm})$	n/a
9	[Lee+16]	84	20	23.8	Probe tip on chip	Single Ended
10	[Lee+15]	80	12	15	Wireless $(1.2  \text{cm})$	Single Ended
11	[Nak+09]	85.5	10	11.7	Probe tip on chip	Single Ended
12	[Nak+14]	80	12.5	15.6	Wireless $(2  \text{cm})$	Balanced
13	[Nak+14]	100	7.6	7.6	Wireless $(2  \text{cm})$	Balanced
14	[Guz+19; Ali+18]	81	3	3.7	Wireless $(0.5 \mathrm{m})$	Single Ended

Table 1.1: UWB and W-band envelope detectors state of the art.

transmission [PH03], e.g. in-home data networks [Cab+09]; short distance data buses in relation to the "Internet of things" [Ham+13; Rom+15a]; medical, or automotive applications [ECC04; OHI04].

Future wireless communication networks require a large bandwidth increment related with several intensive services and applications, such as mobile communication, 8k video streaming, cloud computing, e-health, holographic conferences, smart devices connection, 5G applications, or point to point data transmission [Wel09; Koe+13; Rom+15b; And+14]. Consequently, new spectrum assignments in the W-band (75 GHz - 110 GHz) are currently being considered to achieve peak user data rates in the Gbit/s range [Stö+16; Xia+17; Dah+14], for this reason, the CELTA beamformer demonstrator's working frequency was chosen in this range.

#### 1.3 Content of the dissertation

The remainder of this dissertation is organised in 4 chapters as follows:

- Chapter 2 presents an overview of the Schottky diodes detection theory.
- Chapter 3 describes the design process and simulation results of the five envelope detectors, dividing them into UWB and W-band envelope detectors.
- Chapter 4 shows and analyses the experimental results of all detectors, and the integration of the W-band envelope detectors into the CELTA demonstrator.
- Chapter 5 summarises the dissertation, shows its conclusions and suggests the outlook of this project.

# 2 Fundamentals of Schottky Diode Detection

In 1923 Walter Schottky proposed the first model for the junction layer in metal semiconductors, experimentally confirmed in 1929. In his honour, Schottky diode is used to name those diodes which are composed by a junction between a metal and a p- or n- type semiconductor.

By placing the metal and n-type semiconductor together some of the free electrons move to the metal. As a result, the area of the semiconductor near the metal becomes positively charged due to a lack of electrons, giving it the name of depletion region. An electric field is then set between the metal and the semiconductor that opposes to the migration of electrons to the metal. The junction state of equilibrium provides a potential difference, called diffusion potential or built-in voltage [SMS95]. If the semiconductor is p- type, the analysis is similar: the holes from the semiconductor attract electrons from the metal, and the depletion region is negative charged.

Forward biasing the diode narrows the depletion region and decreases the charge, reducing the junction's electric field and the barrier seen by the electron. Hence the diffusion potential becomes weaker and the energy required for an electron to move to the metal decreases, allowing the electrons to cross the barrier resulting into a current between the terminals of the diode.

When reverse biased, the Schottky diode's depletion region wideness until a certain voltage, called breakdown voltage, where the equilibrium is no longer possible, allowing that the current goes through the diode. Shockley's equation (equation (2.1)) models the diode only in the forward bias region.

Schottky diodes, both p- or n- doped, are considered majority carrier devices because the conduction occurs mostly from the emission of majority carriers over a barrier as opposite to junction diodes whose properties are determined by minority carriers, therefore suffering from carrier storage effects [Maa03; VPR05]. Moreover, when removing the forward voltage from a Schottky diode the current stops almost instantly, allowing Schottky diodes to provide a much higher switching speed in comparison with junction diodes [Inc].

The current travelling through an ideal Schottky diode is expressed with the exponential function from equation (2.1), known as Shockley's equation [SB10],

$$I = I_S \cdot \left(e^{\alpha \cdot V_d} - 1\right) = I_S \cdot \left(e^{\frac{q}{nKT} \cdot V_d} - 1\right) \tag{2.1}$$

where q is the electron charge, k is Boltzmann's constant, T is temperature, n is the diode ideality factor, ranging from 1 to 2, and  $I_s$  is the saturation current [Poz12].

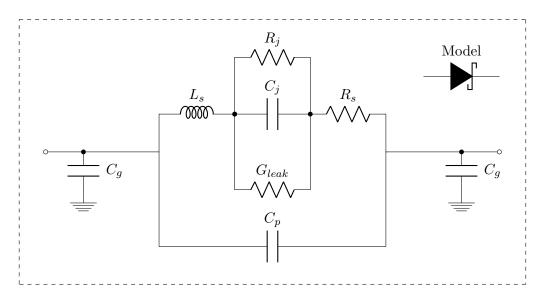


Figure 2.1: Equivalent AC circuit of a Schottky diode.

Equation (2.1) describes the Schottky diode's I-V characteristic and is proportional to the number of electrons having energy greater than the barrier's [SMS95; Maa03].

The threshold voltage or "knee", which is the voltage at which the conduction of current forward current begins is lower for Schottky diodes than for p-n diodes [VPR05]. Furthermore, the reverse leakage current is higher for a Schottky diode than those of p-n ones which are manufactured using the same semiconductor material [BP03], while the reverse breakdown voltage of a p-n diode is larger [Inc].

A thorough discussion about the physics of the different types of diodes, and specially Schottky diodes can be found in [SMS95; Maa03; VPR05; Rho82; Inc] and will not be discussed further in this dissertation.

### 2.1 Schottky diode model

Simulation software needs of an accurate estimation of how the Schottky diodes used in this project perform. The Schottky diode model used in this dissertation was presented in [Hoe+11], where the diodes provided by ACST GmbH were characterised. Figure 2.1 depicts the equivalent AC circuit model of these Schottky diodes [Hoe+11], that will be used in the frame of ADS simulations in chapter 3, and can be discomposed into:

- $C_g$ : The pad capacitance is caused when connecting the diode's pads with the substrate where it is mounted.
- $C_p$ : The parallel capacitance arises from the couplings beside the anode.

- $C_j$ : the junction capacitance is due to the charge accumulated in the depletion region.
- $L_s$ : The series inductance is related to the anode finger.
- $R_j$ : The junction or differential resistance  $(R_{diff})$ , is the inverse of the Schottky diode's I-V curve's first derivative defined in equation (2.3).
- $R_s$ : The series resistance accounts for ohmic losses in the contacts and substrate. n-type semiconductors provide a lower  $R_s$  than p-type semiconductors [Coj07; Höf14].
- $C_d$ : The diffusion capacitance is caused by minority carriers diffusion, and is present in p-n diodes, where it is placed in parallel with  $R_{diff}$ . Since Schottky diodes are majority carrier devices, this capacitance is negligible, and therefore is not plotted in figure 2.1. The lack of  $C_d$  is the reason why Schottky diodes switching speed is much higher than p-n junction diodes [BP03; RCN13].

#### 2.2 Small signal analysis

In the envelope detectors designed in this project, Schottky diodes rectify the RF signal which carries information or data using Amplitude Shift Keying (ASK) as modulation format. Figure 2.2 graphically illustrates the rectification of a sinusoidal signal using a Schottky diode. The variation of voltage at the diode's input leads to a current going through it, the Schottky diode will conduct current when the voltage is greater than the threshold voltage while the reverse current is negligible in comparison during the negative cycles.

The process described in figure 2.2 can be mathematically explained starting from equation (2.1) to show the diode's output current under the assumption that it operates in the square-law region, presenting a quadratic response.

As shown in figure 2.3, a Schottky diode can operate in two regions attending to its input power: square-law and saturation. The square-law behaviour can be obtained only over a limited range of input power. Once this limit is exceeded, the output signal will be saturated and the relation between input power and output voltage will approach a linear, and then a constant, characteristic [Poz12].

We will consider an input voltage  $V_{in} = V_{bias} + v_{in}$  (t), where  $V_{bias}$  is the DC voltage applied to the diode, and  $v_{in}(t)$  is the small signal input.

Assuming that the amplitude oscillation from  $v_{in}(t)$  is small compared with  $V_{bias}$ , we can approximate equation (2.1) through a Taylor expansion with a three term approximation [Poz12; Spi], obtaining that:

$$I(V) = I_{bias} + v_{in}(t) \left. \frac{dI(V)}{dV} \right|_{V_{bias}} + \frac{1}{2} v_{in}^{2}(t) \left. \frac{d^{2}I(V)}{dV^{2}} \right|_{V_{bias}} + \varepsilon$$
 (2.2)

where  $\varepsilon$  are the higher order terms used in the mathematical definition of the Taylor expansion. Furthermore, by expanding the current's first derivative, we obtain

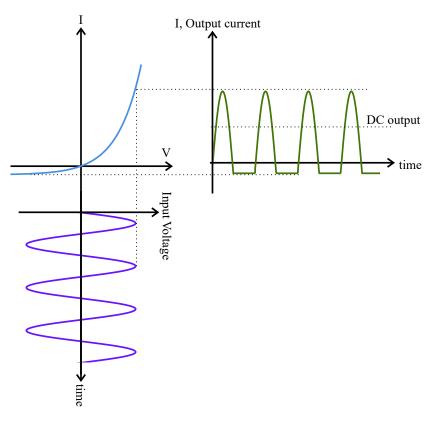


Figure 2.2: Rectifying process using a Schottky diode.

 $G_d$ , the dynamic conductance of the diode, which equals to  $\frac{1}{R_{\text{diff}}}$ , where  $R_{\text{diff}}$  is the diode's differential resistance.  $G_d$  can then be described by:

$$\frac{dI(V)}{dV} = I_s \cdot \alpha \cdot e^{\alpha V_{bias}} = I_s \cdot \alpha \cdot \left(\frac{I}{I_s} + 1\right) = \alpha (I + I_s) = G_d = \frac{1}{R_{\text{diff}}}$$
(2.3)

Similarly, the second current derivative can be evaluated as:

$$\left. \frac{d^2 I\left(V\right)}{dV^2} \right|_{V_{bias}} = \frac{d \left(I_s \cdot \alpha \cdot e^{\alpha V_{bias}}\right)}{dV} = I_s \cdot \alpha^2 \cdot e^{\alpha V_{bias}} = \alpha^2 \cdot \left(IV_{bias} + I_s\right) = \alpha \cdot G_d = G_d' \quad (2.4)$$

Combining the results from equations (2.2), (2.3) and (2.4), we obtain the second order Taylor's approximation from the diode's output current:

$$I(V) = I_{bias} + v_{in}(t)G_d + \frac{1}{2}v_{in}^2(t)G_d' + \varepsilon$$
(2.5)

### 2.3 Single-ended and balanced Schottky diode detection

If we assume that the signal fed into the Schottky diode is a sinusoidal, described as:

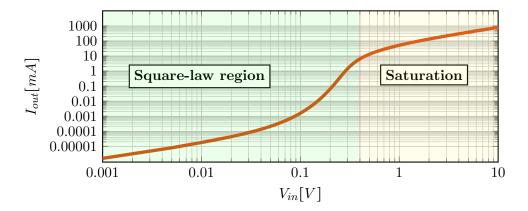


Figure 2.3: Skyworks SMS7621 I-V curve in double logarithmic scale.

$$v_{in}(t) = V_{bias} + V_{RF} \cdot \cos(2\pi \cdot f_c \cdot t) \tag{2.6}$$

and insert equation (2.6) into equation (2.5), we obtain equation (2.7), which depicts the diode's output current with three frequency components: one at DC or downconverted signal; one at a frequency  $f_c$ , called first or fundamental harmonic, and one with a frequency  $2 \cdot f_c$ , which is the second harmonic.

$$I(V) = I_{bias} + V_{RF}(t) G_d \cos(2\pi \cdot f_c \cdot t) + \frac{1}{2} (V_{RF})^2 G'_d (\cos 2\pi \cdot f_c \cdot t)^2 + \varepsilon = I_{bias} + V_{RF}(t) G_d \cos(2\pi \cdot f_c \cdot t) + \frac{V_{RF}^2}{4} G'_d + \frac{V_{RF}^2}{4} G'_d \cos(2 \cdot 2\pi \cdot f_c \cdot t) + \varepsilon$$
(2.7)

#### Single-ended detection

The final goal of every envelope detector designed in this project is to rectify or demodulate an RF signal which carries information or data using amplitude shift keying (ASK) as modulation format, not just a single tone as the one shown in equation (2.6).

ASK signals' baseband bandwidth equals the non return to zero (NRZ) data pattern bitrate. In order to simplify the mathematical calculations, we can approximate the ED's input signal with a sinusoidal with frequency  $f_{sb}$ , which modulates the carrier at  $f_c$  instead of using data pattern with a baseband bandwidth from 0 to  $f_{sb}$ , where  $f_{sb}$  represents the bitrate of the data signal [Raz].

The ASK signal fed to the diode can then be mathematically expressed by equation (2.8) [Poz12], which has a spectrum shown in figure 2.4.

$$V_{in}(t) = V_{RF} \cdot (1 + m \cdot \cos(2\pi \cdot f_{sb} \cdot t)) \cos(2\pi \cdot f_c \cdot t)$$
(2.8)

where  $f_{sb}$  is the modulating tone frequency,  $f_c$  is the carrier frequency and m is the modulation index [OWH96; Poz12].

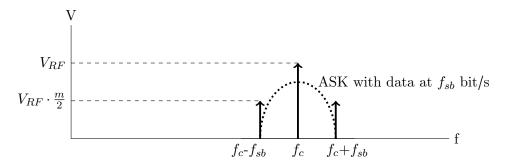


Figure 2.4: Frequency spectrum of an ASK input signal fed to the Schottky diode. The arrows represent equation (2.8), while the dotted line represents the spectrum of the data signal with data at  $f_{sb}$  bit/s.

Feeding the signal from equation (2.8) to the Schottky diode, i.e. inserting equation (2.8) into equation (2.5), provides an output current which is mathematically expressed in equation (2.9) and a spectrum depicted in figure 2.5. Similar as with equation (2.7), the output signal is composed by the same three main frequency components. Now the beatings of the modulated signal with the carrier at  $f_c \pm f_{sb}$ ,  $f_{sb} = f_{sb}$ ,  $f_{sb} = f_{sb} = f_{sb}$ , leading to an overlap of the downconverted signal and the fundamental harmonic at the ED's output. For this reason, single ended envelope detectors using one Schottky diode are limited to a maximum bitrate up to half of the carrier frequency  $f_c$  in the best case scenario [Bla+18a]. In practice, this value is smaller as shown in state of the art from table 1.1. This limitation in terms of demodulated bitrate can be overcome if the fundamental harmonic is cancelled using a balanced envelope detector.

$$I(V) = I_{bias} + v_{in}(t) G_d + \frac{1}{2} v_{in}^2(t) G_d' + \varepsilon$$

$$= I_{bias} + V_{RF} \cdot (1 + m \cdot \cos(2\pi f_{sb}t)) \cdot \cos(2\pi f_{c}t) G_d$$

$$+ \frac{1}{2} (V_{RF} \cdot (1 + m \cdot \cos(2\pi f_{sb}t)) \cos(2\pi f_{c}t))^2 G_d' + \varepsilon = I_{bias} +$$

$$+ V_{RF} G_d \left( \cos(2\pi f_{c}t) + \frac{m}{2} \cos(2\pi (f_{sb} + f_c)) + \frac{m}{2} \cos(2\pi (f_{sb} - f_c)) \right)$$

$$+ \frac{V_{RF}^2}{4} G_d' \left( 1 + \frac{m^2}{2} + 2m \cdot \cos(2\pi f_{sb}t) + \frac{m^2}{2} \cos(2 \cdot 2 \cdot \pi f_{sb}t) + \frac{m^2}{2} \cos(2 \cdot 2\pi f_{c}t) \right)$$

$$+ \cos(2 \cdot 2\pi f_{c}t) + \frac{m^2}{4} \cos(2 \cdot 2\pi (f_c + f_{sb})t) + \frac{m^2}{4} \cos(2 \cdot 2\pi (f_c - f_{sb})t)$$

$$+ m \left( \cos(2\pi (2f_c - f_{sb})t) + \cos(2\pi (2f_c + f_{sb})t) \right) + \varepsilon$$

$$(2.9)$$

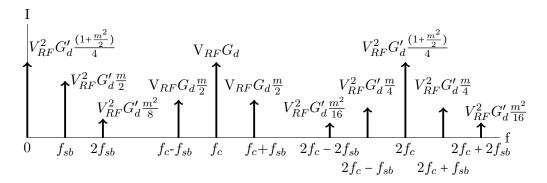


Figure 2.5: Frequency spectrum of the Schottky diode's output signal.

#### Balanced detection

In section 2.3, we have addressed the use of one Schottky diode to demodulate an ASK modulated signal. In this section we will mathematically and qualitatively discuss the use of a balance architecture, where two diodes are fed with the same signal delayed with a phase difference of  $180^{\circ}$  between both diodes. The output current for each diode,  $I_1(V)$  and  $I_2(-V)$ , are calculated using equation (2.5). The common current obtained after combining the two diodes' output can be mathematically expressed in equation (2.10).

$$I_{1}(V) = I_{bias} + v_{in}(t) G_{d} + \frac{1}{2} v_{in}(t)^{2} G_{d}' + \varepsilon$$

$$I_{2}(-V) = I_{bias} - v_{in}(t) G_{d} + \frac{1}{2} v_{in}(t)^{2} G_{d}' + \varepsilon$$

$$I_{out}(V) = I_{1}(V) + I_{2}(-V) = 2I_{bias} + v_{in}(t)^{2} G_{d}' + \varepsilon$$
(2.10)

Considering the input voltage to be the same ASK modulated signal as in the single ended version, described in equation (2.8), the combined output current from the two diodes results to equation (2.11).

$$I_{out}(V) = I_{bias} + \frac{V_{RF}^{2}}{2}G_{d}'\left(1 + \frac{m^{2}}{2} + 2m \cdot \cos(2\pi f_{sb}t) + \frac{m^{2}}{2}\cos(2 \cdot 2\pi f_{sb}t) + \frac{m^{2}}{2}\cos(2 \cdot 2\pi f_{c}t) + \cos(2 \cdot 2\pi f_{c}t) + \frac{m^{2}}{4}\cos(2 \cdot 2\pi (f_{c} + f_{sb})t) + \frac{m^{2}}{4}\cos(2 \cdot 2\pi (f_{c} - f_{sb})t) + m\left(\cos(2\pi (2f_{c} - f_{sb})t) + \cos(2\pi (2f_{c} + f_{sb})t)\right) + \varepsilon$$

$$(2.11)$$

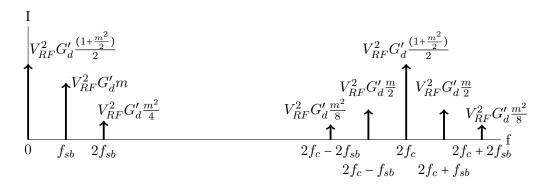


Figure 2.6: Schottky diode's demodulated output signal using a balance architecture.

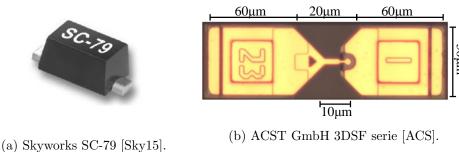


Figure 2.7: Schottky diodes used in this project.

The demodulated signal's spectrum is depicted in figure 2.6, where the main difference from figure 2.5 is the absence of the frequency components centred at the fundamental harmonic:  $f_c$  and  $f_c \pm f_{sb}$ , which are only cancelled in the frequency region where the phase difference between  $V_1$  and  $V_2$  is 180°. A balance detector will only deliver the even harmonics, cancelling the odd ones.

#### Schottky diodes for implementation

This project covers two frequency ranges as explained in chapter 1. In the UWB frequency range, we used the Skyworks SMS7621 and SMS7630 with a SC-79 package, provided as a surface mounting device (SMD), shown in figure 2.7a [Sky15]. In the W-band, ACST GmbH provided and mounted their Zero-Bias Schottky diodes from the 3DSF serie [ACS; HPC11] similar to the one depicted in figure 2.7b. The three diodes' features are summarised in table 2.1.

Figures 2.8a and 2.8b show the I-V curves of the UWB and W-band diodes and their differential resistance, defined as the first derivative from the I-V curve. Figure 2.8a is obtained using the parameters from the Skyworks' datasheet [Sky15], while figure 2.8b is depicted using the data provided by [HPC11], where the physical parameters of the diode are experimentally extracted.

Table 2.1: Schottky diodes used in this project.

Diode	$I_s$	$R_s$	$C_{j0}$	$L_s$	$C_p$	$V_{j}$	$R_{diff}$
SMS7621	$400\mu A$	$12\Omega$	$100\mathrm{fF}$	$700\mathrm{pH}$	$150\mathrm{fF}$	$0.51\mathrm{V}$	$0\Omega$
SMS7630	$5\mu\mathrm{A}$	$20\Omega$	$140\mathrm{fF}$	$700\mathrm{pH}$	$150\mathrm{fF}$	$0.34\mathrm{V}$	$0\Omega$
3DSF	$54\mu A$	$5.5\Omega$	$14.56\mathrm{fF}$	$41\mathrm{pH}$	$3.4\mathrm{fF}$	$0.22\mathrm{V}$	$402\Omega$

Figure 2.9 shows the I-V curves from the three diodes using a logarithmic scale. Besides, it compares the 3DSF and SMS7630 diodes' I-V curves with equation (2.5), which depicts the Schottky diode three term series Taylor expansion. It shows a thoroughly approximation of equation (2.5) for an input voltage below 100 mV, or -10 dBm (maximum input power a diode from ACST GmbH can handle), validating it for further calculations. When the input voltage increases above 1 V, the I-V curves tend to a piecewise-linear function [SB10], corresponding with the saturation region depicted in figure 2.3.

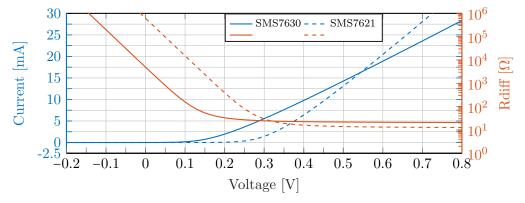
# 2.4 Balanced output signals with Rat Race and high-pass compensation architecture

The 180° phase delay to the diodes' inputs can be provided either by the interface from the device connected to the envelope detector's input, e.g. an amplifier with a differential output, or with an external device, a Balun, that transforms its input signal from single ended into a balanced output.

There are several types of Baluns that can be used in planar technology either built with transmission lines [Mar68; Zha+05a; Liu+07; Zha+05b; Ang+00] or lumped components[JK08; CC13; Kim+09; Sla]. A state of the art review can be found in [Poz12; JM14; Marb], where several trade-offs between the Baluns' features must be assessed: bandwidth or frequency coverage, phase and amplitude balance, common mode rejection ratio, insertion loss, etc. Since this topic is too broad, we will focus on the Rat Race 180°coupler [Poz12], and its variation that uses the high-pass compensation principle presented in [Sla].

#### Rat Race

The Rat Race, whose schematic is depicted in figure 2.10, is a four-port network device where each port is placed one quarter wavelength away from each other, while the transmission line between ports 2 and 4 is three quarter wavelengths in length. It splits into two 180°-phase components at ports 2 and 3, while port 1 is isolated when the input is port 4. Additionally, it can add the two input signals from ports 2 and 3 into port 1 or evenly splits the input from port 1 into two in-phase components at ports 2 and 3, while port 4 is isolated [Poz12; SB10]. These operations are summarised in the scattering matrix for an ideal Rat Race from equation (2.12).



(a) SMS7621 in dashed, SMS7630 in solid line.

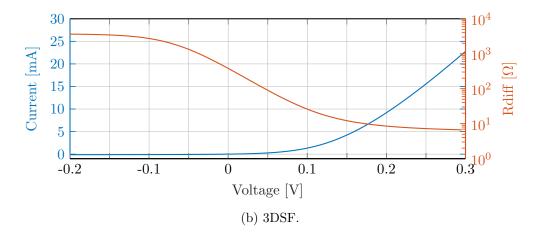


Figure 2.8: DC simulation analysis of the Schottky diodes used in the project.

$$S = -\frac{j}{\sqrt{2}} \begin{pmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & 1 \\ 0 & -1 & 1 & 0 \end{pmatrix}$$
 (2.12)

We must take into account that introducing a traditional Rat Race in an UWB ED increases its size considerably, which, for some applications can be an issue. Moreover, in the substrates used in this dissertation within the W-band EDs' design, it is not possible to use a Rat Race in this frequency region [JM14] due to the Rat Race transmission lines size's constraints, where the transmission lines' widths and lenghts become comparable.

In order to overcome these limitations, there are several approaches to design a Balun with a broad bandwidth and compact size. A thorough study of the different architectures that the author has studied can be found in [Mar68; Sla; CC99; Zha+05a; Zha+05b; Zha+14; CC13; JK08; Wal97; ZAM16; Liu+07; Ang+00; Kim+09].

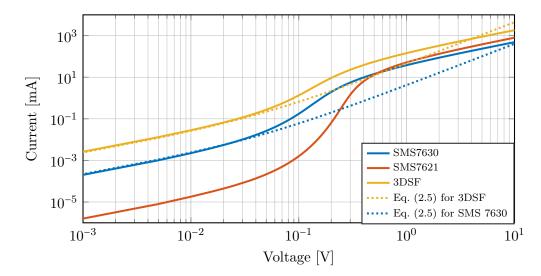


Figure 2.9: I-V curves of the Schottky diodes used in this project in double logarithmic scale.

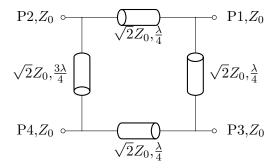


Figure 2.10: Rat Race schematic.

In this dissertation a modification of the architecture presented in [Sla] is used, which exploits the high-pass compensation principle, allowing us to have the benefits of a Rat Race without increasing the envelope detector's size from a single ended version.

#### High-pass compensation architecture

In [Sla], the long  $3\lambda/4$  arm section of the conventional Rat Race is replaced with a semi-lumped LC network using a high-pass configuration, consisting in substituting the  $3\lambda/4$  transmission line from the conventional Rat Race hybrid coupler with its equivalent LC circuit and the inductors by transmission lines as shown in figure 2.11 [GG84; Par89; SFW14]. With this technique, [Sla] achieves a size reduction of about 75% over the traditional Rat Race.

Figure 2.12 shows the schematic comparison between a conventional Rat Race,

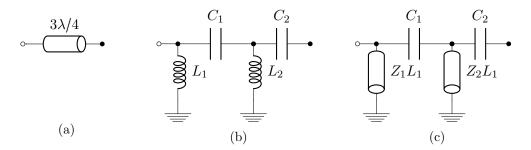


Figure 2.11: Schematic of the high pass phase compensation network which replaces the long arm of the Rat Race: (a) original  $3\lambda/4$  transmission line; (b) using inductors; (c) using transmission lines.

described in section 2.4 (figure 2.12a); the Rat Race presented in [Sla] (figure 2.12b); and the architecture proposed in [Bla+18a] (figure 2.12c). The latter is composed of a transmission line with an electrical length of 180°at the central frequency, two shorted-stubs and two Schottky diodes, which provide the capacitance for the high-pass network while at the same time demodulate the input signal. It has one input and one output in comparison with the four interfaces from the conventional Rat Race and its modified version from figures 2.12a and 2.12b. The 180°transmission line impedance is  $50\,\Omega$  in the UWB version [Bla+18a] and around  $100\,\Omega$  for the W-band versions [Bla+18b] instead of the  $\sqrt{2}Z_0$  (70  $\Omega$ ) from the standard and modified Rat Race [Poz12; Sla] due to physical and manufacturing constraints.

At the ED's output we obtain the rectified signal, which due to the balance ED architecture, does not present the fundamental harmonic which has been cancelled.

The novelty of this detector relies on the combination of two features: the ED rectifies the input signal, while simultaneously works as a Rat Race hybrid coupler inspired Balun without an isolation port. Furthermore, this architecture shows a 5x size reduction when compared to a balanced detector which uses a Rat Race as Balun [Bla+18a].

# 2.5 Bode-Fano criterion for broadband envelope detectors

Since the goal of this project is to provide high demodulation bitrates, a broadband matching is needed, simultaneously, at the input and output of the envelope detector.

The Bode-Fano criterion presents a theoretical limit on the minimum reflection coefficient,  $\rho(\omega)$ , that can be obtained with a matching network [Bod45; Fan61]. Its derivation and analysis applied to Schottky diodes can be found in [HG98; Ker95]. Nevertheless, the criterion outcome is summarised in figure 2.13 for the four RC and RL possible configurations, where  $\rho(\omega)$  is the reflection coefficient at the matching network's input.

Assuming  $|\rho(\omega)| = \rho_m$  constant within a range  $\Delta\omega$ , and having a parallel RC

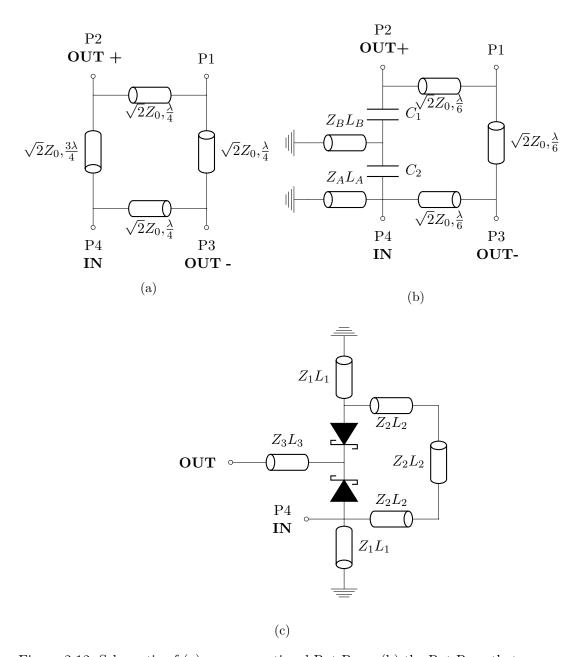


Figure 2.12: Schematic of (a) one conventional Rat Race; (b) the Rat Race that uses the high-pass compensation; (c) this work [Bla+18a].

load impedance, we could simplify the integral from the RC parallel load impedance  $\left(\int_0^\infty \ln\left(\frac{1}{|\rho(\omega)|}\right) d\omega \le \frac{\pi}{RC}\right)$  into equation (2.13), concluding that:

- 1. Increasing R or C decreases the quality of the matching, therefore, diodes with low parasitics are required.
- 2. A perfect match can only be achieved at a single frequency ( $\Delta\omega=0$ ).
- 3. Widening the matching bandwidth comes with at the cost of increasing  $|\rho(\omega)|$ . This is particularly important in this project. Since the target at W-band is a 10 GHz to 18 GHz and 5 GHz input and output bandwidth respectively, we will need a broad input and output matching. It will exist a trade-off between power transfer and matched bandwidth, which will penalise the detector sensitivity and the output power it delivers in comparison with its narrowband version.

$$\int_{0}^{\infty} \ln \left( \frac{1}{|\rho(\omega)|} \right) d\omega = \int_{\Delta\omega} \ln \left( \frac{1}{\rho_{m}} \right) d\omega = \Delta\omega \ln \frac{1}{\rho_{m}} \le \frac{\pi}{RC}$$
 (2.13)

An analogous analysis can be performed with any of the other three loads from figure 2.13.

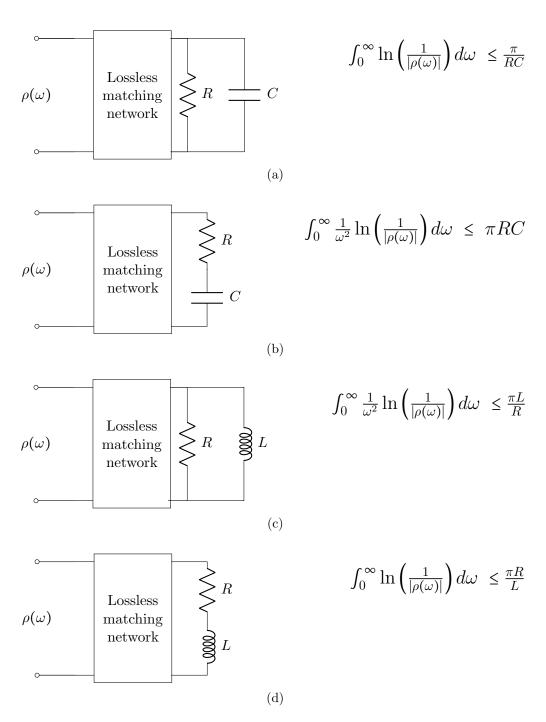


Figure 2.13: Bode–Fano limits for RC and RL loads matched with passive and lossless networks: (a) Parallel RC; (b) Series RC; (c) Parallel RL; (d) Series RL.

## 3 Envelope Detectors for Ultra-Wide Band (UWB)

In this dissertation we will show the design and simulation results of five EDs in two frequency ranges: The first two EDs which work in the Ultra-Wideband (UWB) frequency range (3.1 GHz to 10.6 GHz), are used as an initial approach to ED design, allowing to test different configurations and architecture designs handling a lower complexity and without having some manufacturing constraints and costs from higher frequency prototypes, while the three other EDs operate in the W-band (75 GHz to 110 GHz).

#### 3.1 Envelope detection principles and benchmarks

The EDs presented in this dissertation should provide a broad input bandwidth, ideally from 3.1 GHz to 10.6 GHz for UWB and 75 GHz to 110 GHz for W-band; low conversion loss; wide video bandwidth, to deliver high data rate demodulated signals at their outputs; high sensitivity, which can be boosted through an external low noise amplifier stage at their input high output power and a high ratio between the demodulated signal's bitrate and its carrier frequency, defined as  $\Delta b$ .

Although the input- and video-bandwidths depend on the technology and ED design, we need to consider that broadening them loosens the ED input's and output's matching quality according to the Bode-Fano Criterion [Bod45; Fan61], which entails a deterioration of the ED's sensitivity and the output power it delivers. The trade-off between sensitivity, power delivery and bandwidth will be constant in this chapter.

The figure-of-merit  $\Delta b$  plays a key roll in UWB envelope detectors.  $\Delta b$  must be maximised since employing an ED limits the use of phase information when transmitting a signal. In W-band EDs,  $\Delta b$  is not critical due to the broad available bandwidth (75 GHz to 110 GHz).

Section 1.2 described the current ED state of the art, where the maximum measured single-ended ED's  $\Delta b$  is 41.7% [Cim+18]. Theoretically,  $\Delta b$  can be boosted up to 50%, since the bitrate the ED can demodulate is limited to half of the carrier frequency ( $f_c$ ) in the best case scenario as demonstrated in section 2.3. This limitation is due to the presence of a fundamental harmonic spurious at  $f_c$  in the ED's output, which overlaps with the baseband downconverted signal. This overlapping introduces distortion to the output signal which cannot be removed by filtering [Poz12; Bla+18a].

In contrast, balanced EDs provide a fundamental harmonic spurious cancellation at their output as shown in section 2.3, reducing common mode noise and allowing to boost experimentally  $\Delta b$  up to 100% [Bla+17]. In addition, providing a broad phase

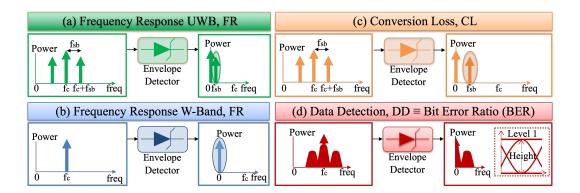


Figure 3.1: Benchmarks used to test the EDs: frequency response (FR) for: (a) UWB EDs, (b) W-Band EDs; (c) conversion loss (CL); (d) data detection (DD).

balance allows shifting the input  $f_c$  within the working frequency range while keeping the ED's performance. As a trade-off, balanced EDs provide a lower sensitivity and conversion loss with respect to single ended EDs, since the need of a balun to provide the balance signal between both diodes can introduce losses. Similarly, a behaviour mismatch between the two diodes makes the ED's matching more complex. Knowing this trade-off and prioritising to provide a high  $\Delta b$  (UWB) and demodulation bitrate (W-band) over sensitivity we decided to use balanced EDs.

The design and simulations from the planar EDs presented in this dissertation have been conducted with Keysight's Advance Design System's (ADS) circuit simulations through harmonic balance and transient analysis. The transitions' metallic blocks were designed using CST Microwave Studio simulations. This section describes the benchmarks used to measure and evaluate the five EDs' performance that will be described within this dissertation. Sections 3.2, 4.1, 4.2 and 4.3 present the design and simulation results of the UWB and W-band EDs.

The EDs features and performance are evaluated using three benchmark schemes which are summarised in the schematics from figure 3.1: frequency response (FR), conversion loss (CL) and data detection (DD).

An envelope detector's frequency response is directly linked with the input frequency range that it can demodulate, and depicts its operational bandwidth, since a broadband frequency response is needed to avoid distortion [PS08].

In this dissertation, the frequency response is obtained using two methods. In figure 3.1b we measure the envelope detector's DC output when it is excited with a sinusoidal tone with frequency  $f_c$ , which is swept within the desired frequency range. This approach will be used with the W-band EDs that use Zero bias Schottky diodes and do not have a built-in bias tee. The UWB EDs shown in this dissertation use Non Zero bias Schottky diodes which need to be biased to optimise their performance. For this reason, their frequency response must be measured in their optimum bias point, hence, it is not possible to measure directly their DC output, which leads us to the second method to measure the UWB EDs frequency response. We excite the

ED with a low frequency tone at  $f_{sb}$  in the range of MHz modulated onto a carrier with frequency  $f_c$  which is swept within the desired frequency range. The frequency response is calculated by measuring the ED's output power at  $f_{sb}$ , as depicted in figure 3.1a.

While the frequency response defines the ED's input bandwidth, the conversion loss depicts its video bandwidth. In this benchmark, the ED is fed with the same signal as the one used in the UWB ED's frequency response benchmark (figure 3.1a), the difference is that now  $f_{sb}$  is in the range of GHz, and is swept as well as  $f_c$ . The conversion loss is calculated through the difference between the downconverted signal's at  $f_{sb}$  and the input signal's powers at  $f_c \pm f_{sb}$  as shown in figure 3.1c. The video bandwidth or output bandwidth is measured using the conversion loss results. The video bandwidth is associated with the maximum bitrate an ED can demodulate, since an ASK modulated signal's bitrate ] equals its video or baseband bandwidth, which is directly represented with  $f_{sb}$ .

The frequency response and conversion loss are used to qualitatively verify if the ED under test will be able to demodulate an ASK modulated signal at a certain bitrate (CL), at which carrier frequency the sensitivity of the detector is optimal (FR) and which is the ED's range of operation (CL and FR). Demodulating high data rate ASK signals without introducing distortions can be only achieved with both a broad frequency response and a large video bandwidth. At the same time, a low conversion loss is desired. In ADS these two benchmarks are calculated using harmonic balance analysis.

Eventually, we substitute the modulating tone with frequency  $f_{sb}$  from the conversion loss setup with a data signal which carries bits with information. The ED's performance can be quantitatively measured through its Bit Error Ratio (BER), or qualitatively, through the analysis of the demodulated signal eye diagram's height and its Level of "1" bits (L1) [Bla+18b]. The BER is the ratio between the number of error bits detected and the number of transmitted bits during a selected time interval [PS08]. Similarly, in order to achieve a successful demodulation we need an open eye diagram to decide whether a "1" or a "0" was received. The eye diagram's height and Level of "1" are directly related with the ED's video bandwidth and frequency response respectively. The eye diagram parameters will be measured in simulations within this chapter, while the BER will be experimentally evaluated in chapter 3.4.

In ADS, harmonic balance uses steady state waves as input signals which does not allow to simulate the ED's behaviour during time and to plot its demodulated eye diagram. Using a transient analysis allows to overcome this limitation, and allows us to measure the signal at different points of the circuit as a function of time, and to analyse the resulting eye diagram.

### 3.2 Balanced envelope detectors for UWB

In the UWB frequency range,  $\Delta b$  together with the sensitivity are the main ED's features to focus. Achieving a high  $\Delta b$  optimises the use of the frequency spectrum

[PH03] and is our main concern in the UWB EDs design, because while the sensitivity can be boosted introducing amplifiers,  $\Delta b$  is a design parameter from the ED. [Cim+16] and [Sil+17] present two UWB single ended EDs able to demodulate up to 2.5 Gbit/s ASK modulated signals in the UWB frequency region. Their best  $\Delta b$  is 35.7% and have a sensitivity of -11 dBm. As demonstrated in chapter 2, the theoretical  $\Delta b$  maximum for a single ended ED is 50% due to the harmonics present at the EDs' output. Therefore, we investigated the use of a balanced architecture to boost  $\Delta b$ .

This section discusses two different balanced EDs' designs, which use the same technology as [Cim+16] and [Sil+17]. The first one, UWB1, was introduced in [Bla+17] and is presented in section 3.2.1. It uses an external balun to produce the balanced signal fed to a single balanced ED. The second one, UWB2, is presented in section 3.2.2 and introduced in [Bla+18a], combines the functionality of a balun while at the same time detects the input signal. Their design central frequencies are 7 GHz for UWB1 and 8 GHz for UWB2, since the requirements from Bifrost Communications were updated in between both designs.

#### 3.2.1 UWB1 with an external balun

The first UWB detector circuit's schematic is depicted in figure 3.2. It consists of a balun (Marki Bal-0010 [Mara]), and a balanced envelope detector, comprised of two Schottky diodes with a matching network at their input and low pass filter and bias tee at their output. It is implemented in microstrip technology on a Rogers 4003 substrate ( $\epsilon_r = 3.55$ , height = 32 mil and 35 µm copper layer [Rog]) and uses surface mounting devices (SMD) for the diodes, resistor, capacitor and inductor.

The Schottky diode chosen for this works was the Skyworks SMS7630, analyzed in section 2.3, which presents the features summarised in table 2.1.

The balun splits its input signal into two 180° out of phase signals, providing a phase balance bandwidth from 0.02 GHz to 10 GHz between the two diodes' inputs, which, according to equation 2.11 is needed to cancel the fundamental harmonic spurious. As a drawback, the balun introduces 8 dB insertion loss in each branch.

The output low-pass filter (LPF), placed at the two diodes' output, is a 6<sup>th</sup> order Butterworth stepped impedance filter implemented in microstrip technology with a 3.2 GHz 3 dB cut-off frequency. The filter's cut-off frequency is set to 3.2 GHz as a compromise to use the same filter in the two UWB EDs described in section 3.2.1 (UWB1) and 3.2.2 (UWB2), which can demodulate up to 4 Gbit/s and 2.5 Gbit/s ASK signals respectively. With this filter it is possible to fulfil the requirements to let going through at least 94.3% of the signal power of a 4 Gbit/s ASK signal [Max08; TS86], which is the highest bitrate that the UWB1 can demodulate according to simulations. At the same time, reducing the filter's bandwidth to 75% - 80% of the bitrate reduces the output noise.

When comparing the UWB1 with its equivalent in single ended [Cim+16], the single ended's output butterfly stub is removed in UWB1 because filter requirements can be relaxed when using a balanced detector, reducing the total output filter size

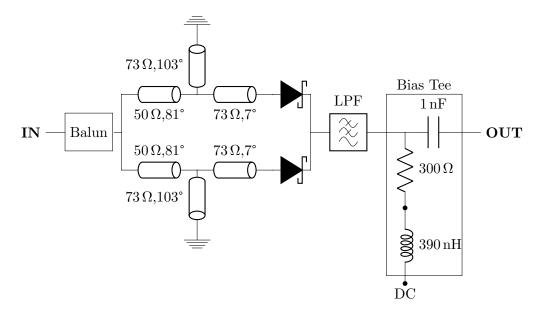


Figure 3.2: Circuit schematic of UWB1: electrical lengths are given at 7 GHz.

considerably, at the cost of introducing an external balun.

After the LPF, a bias network is placed. Setting the diodes' bias to its threshold voltage allows to optimise their rectification point, getting a better sensitivity and performance. Furthermore, it provides a DC path at the diodes' output, in order to work in their non linear region to produce the baseband harmonic.

The bias network is implemented with SMD components: one 390 nH inductor in series with a  $300\,\Omega$  resistor prevent the video signal to flow to ground through the bias tee. In parallel to the inductor and resistor a 1 nF capacitor was placed. The resistor, inductor and capacitor are implemented using SMDs components soldered on transmission lines. There is no need to design an additional DC return path at the diodes' input, since it is already provided by the matching network with the short stubs.

Finally, the input matching network, placed between the balun and the diodes adapts the diode's input to the balun's output. It is composed of two transmission lines and a shorted-stub to provide a broadband matching. The diodes' matching network must be identical to preserve the 180° Balun's phase shift.

Figure 3.3 depicts the detector circuit layout, highlighting the different elements described in this section, while figure 3.4 shows the manufactured prototype of the detector and the Marki balun Bal-0010.

#### 3.2.2 UWB2 with high-pass compensation principle

The previous ED, UWB1, uses an external balun to obtain a balanced signal, which increases size and cost of the overall circuit and introduces some losses, which decrease

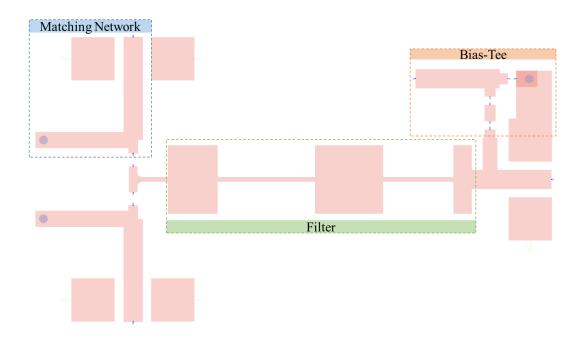


Figure 3.3: Layout of UWB1.

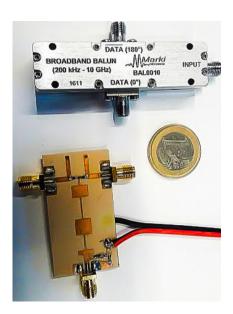


Figure 3.4: Manufactured detector circuit UWB1 with external balun Marki Bal-0010  $[\mathrm{Bla}{+}17].$ 

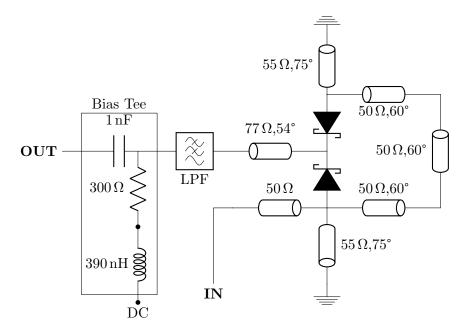


Figure 3.5: UWB2's circuit schematic: electrical lengths are given at 8 GHz.

its sensitivity. This drawback is addressed with the second UWB detector, UWB2.

The UWB2's goal is to demodulate single-ended signals adopting a balanced configuration without using an external balun. This design combines the Rat-Race hybrid coupler functionality of a balun and, simultaneously, obtains the rectified signal at the ED's output [Bla+18a]. The ED is designed following the high-pass compensation principle described in section 2.4.

The schematic of the UWB2 detector is illustrated in figure 3.5. It is composed of two Schottky diodes, two shorted-stubs, a transmission line with a 180° electrical length at 8 GHz (the central working frequency was updated in the requirement list), i.e. the ED's design frequency, where it provides the optimum phase balance, and a transmission line that delivers the downconverted signal. The same low pass filter and bias tee used in UWB1 from section 3.2.1 are placed at the ED's output, in order to be able to compare both designs without the influence of external elements aside from the ED circuits and external balun. UWB2 is implemented in microstrip technology on a Rogers 4003 substrate ( $\epsilon_r = 3.55$ , height = 32 mil and 35 µm copper layer [Rog]) and uses surface mounting devices (SMD). The Schottky diode chosen for this works was the Skyworks SMS7621 because it provides a broader phase balance bandwidth than the SMS7630. Both diodes' I-V curves and equivalent circuit have been compared and analyzed in section 2.3.

The phase balance bandwidth is measured by using harmonic balance analysis in ADS. Figure 3.6 depicts the ED's phase balance bandwidth and compares it with its equivalent Rat-Race hybrid coupler using the same microstrip technology. It

shows that both architectures provide a similar phase balance bandwidth ( $\pm 6^{\circ}$ ) of 1.5 GHz, centred at 8 GHz. This narrowed phase balance bandwidth, in comparison with UWB1 is the price to pay for having a cost effective and more compact detector circuit with a less lossy balun. The insertion loss is close to 3 dB per line [Sla], which boosts the detector sensitivity when compared with UWB1.

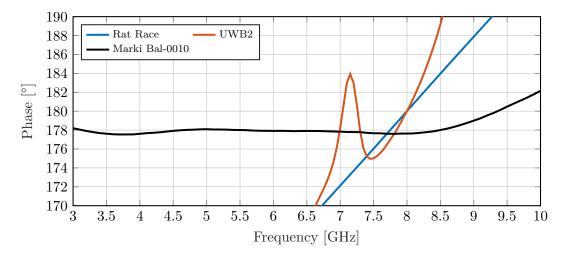


Figure 3.6: Phase balance bandwidth comparison between a Rat Race, UWB2 and the Marki Bal-0010 [Mara].

Figure 3.7 shows the detector circuit's layout and figure 3.8 displays the detector manufactured prototype. When comparing figures 3.8 and 3.4 the size comparison is evident, getting a reduction factor of 5 [Bla+18a].

#### 3.3 Simulation results

This section shows the simulation results that evaluate the two UWB envelope detectors using the three benchmarks described in section 3.1 and comparing their performance. It must be considered that their design central frequency differs, being 7 GHz for UWB1, and 8 GHz for UWB2 because the central working frequency was updated in the requirement ED's list for UWB2.

#### Frequency response

This benchmark follows the schematic depicted in figure 3.1a, where the carrier's power was set to  $0\,\mathrm{dBm}$  and the two sideband tones, separated  $100\,\mathrm{MHz}$  from the carrier to  $-10\,\mathrm{dBm}$ .

Figure 3.9 shows the frequency response simulation results of UWB1 and UWB2, which provide an operational bandwidth from 2.4 GHz to 10.2 GHz and 3.6 GHz to 10.5 GHz respectively with an average output power of -17.5 dBm for UWB1 and -13.5 dBm for UWB2. The latter's central frequency is higher because it is

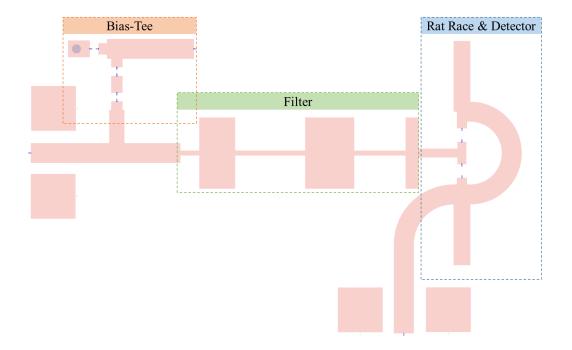


Figure 3.7: Layout of UWB2.

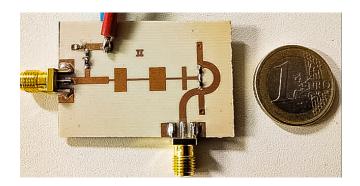


Figure 3.8: Manufactured detector UWB2 [Bla+18a].

designed with an  $8\,\mathrm{GHz}$  central frequency, in comparison with the  $7\,\mathrm{GHz}$  of UWB1. Furthermore, UWB2's output power is  $4\,\mathrm{dB}$  higher than UWB1's because it does not need of an external balun, which in the case of the Marki BAL0010 model accounts for  $8\,\mathrm{dB}$ .

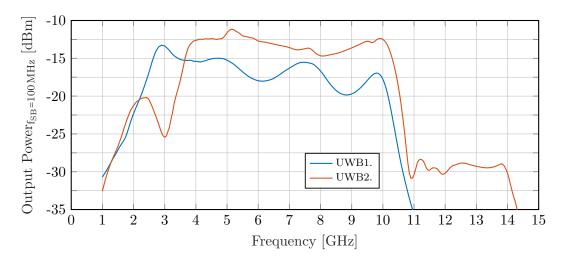


Figure 3.9: Frequency response simulation results of the envelope detectors UWB1 [Bla+17] and UWB2 [Bla+18a].

#### Conversion loss

The ED is fed with an ASK signal, composed of a 0 dBm carrier with frequency  $f_c$ , which is swept from 3 GHz to 10 GHz, modulated by two -10 dBm sidebands swept from  $f_{sb} = 0.1$  GHz to 4 GHz, placed at  $f_c \pm f_{sb}$ . The ED's conversion loss is calculated by measuring the difference between the obtained downconverted signal at  $f_{sb}$  and the input power at  $f_c \pm f_{sb}$ .

Figure 3.10 depicts the conversion loss simulation results from UWB1 (figure 3.10a) and UWB2 (figure 3.10c). UWB1's and UWB2's 3dB bandwidth matrices are sketched in figures 3.10b and d, where each element of the  $f_c$  -  $f_{sb}$  matrix is painted on white if that  $f_{sb}$  is within the 3dB bandwidth or black if it is not.

Both envelope detectors provide a a 3 dB video bandwidth up to 2 GHz in their design frequency and adjacent frequencies (7 GHz and 8 GHz for UWB1 and UWB2 respectively). At the same time, the two detectors are able to keep a broad video bandwidth within the UWB frequency range. Similar to the frequency response, UWB1 provides a higher conversion loss with respect to UWB2 due to the insertion loss of the external balun.

#### **Data detection Measurement**

Figure 3.11 shows the demodulated eye diagram's height and Level 1 (L1) when the EDs are fed with a 0 dBm ASK signal at 2.5 Gbit/s (a) and 4 Gbit/s (b), with a

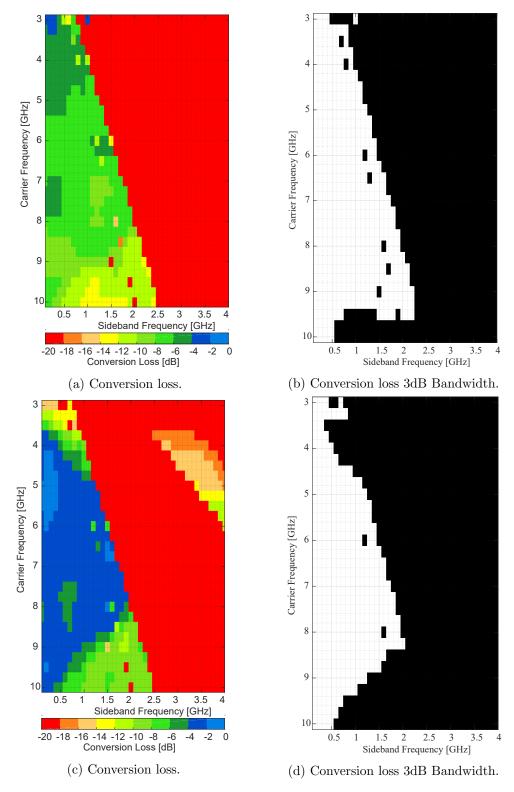


Figure 3.10: Conversion loss simulation results comparison of the UWB envelope detectors:(a) UWB1, (b) UWB1  $3\,\mathrm{dB}$  video bandwidth, c) UWB2, (d) UWB2  $3\,\mathrm{dB}$  video bandwidth.

carrier frequency swept from 1 GHz to 15 GHz.

UWB1's outcome is depicted in figure 3.11a. When demodulating a 2.5 Gbit/s ASK signal, its best performance is achieved when  $f_c$  is 3.5 GHz and 7 GHz (its design frequency), where the frequency response reaches two of its maximum peaks. In addition, the eye is opened for every  $f_c$  between 2.5 GHz and 9.5 GHz. Increasing the bitrate to 4 Gbit/s broadens the input ASK signal's spectrum. Since the L1 is directly related to the FR, the L1 lines for 2.5 Gbit/s and 4 Gbit/s almost overlap. On the other hand, the eye's height is directly proportional to the detector's video bandwidth, therefore, the carrier frequencies where the ED can operate are reduced to those with broader video bandwidth shown in figure 3.10a ( $f_c = 4.5 \,\text{GHz} - 9.5 \,\text{GHz}$ ). According to simulation results, this ED will be able to demodulate ASK signal at bitrates up to 4 Gbit/s.

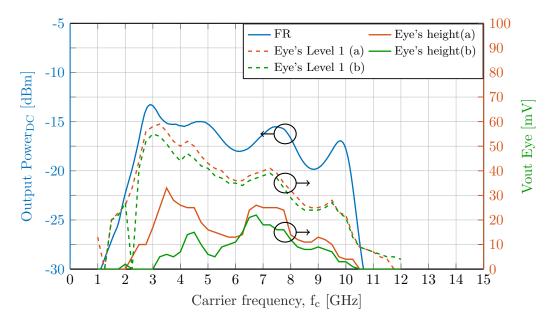
Figure 3.11b describes UWB2's DD simulation results. Its design frequency is 8 GHz, therefore, the UWB2 provides its best performance in the range for  $f_c$  between 6.5 GHz and 9 GHz when the ASK signal's bitrate is set to 2.5 Gbit/s, obtaining a higher and more open eye diagram than with UWB1. When the bitrate increases to 4 Gbit/s, the demodulated signal's eye diagram is closed for every  $f_c$  outside the 6 GHz - 8.5 GHz region, where the eye is only slightly open. Similarly as with UWB1, the L1 lines for 2.5 Gbit/s and 4 Gbit/s almost overlap when the eye diagram is not distorted ( $f_c = 6$  GHz - 8.5 GHz). Even if the UBWB2's Level 1 is higher than UWB1's due to the lower insertion losses of the UWB2's balun, the eye diagram's height is lower due to its narrower phase balance bandwidth, and therefore a 4 Gbit/s ASK signal demodulation will not be successful, allowing the demodulation of ASK signals up to 2.5 Gbit/s.

#### Summary and discussion

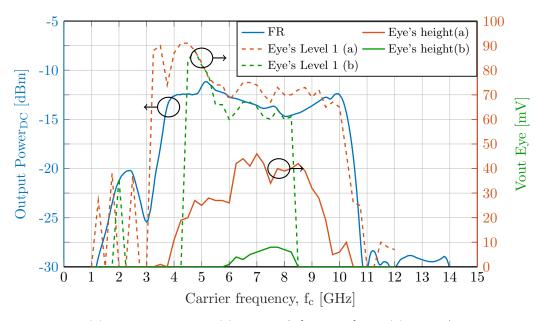
Section 3.2 has presented the design of the two UWB balanced envelope detectors. They have been characterised through simulations, using the three benchmarks in section 3.1.

UWB1 employs an external balun to obtain the balanced signal fed into the ED, while UWB2 uses the detector circuit as a balun, taking advantage of the high-pass compensation principle, while simultaneously provides the demodulated input signal at its output.

Using a balanced architecture in UWB1, allowed us to increment the demodulated bitrate from 2.5 Gbit/s to 4 Gbit/s when compared with its equivalent single ended version from [Cim+16] and [Sil+17], at the cost of reducing the ED's sensitivity. The UWB2 provides a higher sensitivity than UWB1, lower size and reduces the cost of the detector circuit (the Marki BAL-0010 costs \$735 in [Mic]). As drawback, UWB2 is only able to demodulate up to 2.5 Gbit/s signals in comparison with the 4 Gbit/s from UWB1 due to its lower phase balance bandwidth. As a result of its balanced architecture, UWB2's output LPF requirements are reduced when compared with [Cim+16] and [Sil+17], allowing a more compact LPF with less elements. For all these reasons, after evaluating the trade-offs, the architecture presented with UWB2



(a) UWB1 for bitrate (a)  $2.5\,\mathrm{Gbit/s}$  and (b)  $4\,\mathrm{Gbit/s}$  [Bla+17].



(b) UWB2 for bitrate (a)  $2.5\,\mathrm{Gbit/s}$  [Bla+18a] and (b)  $4\,\mathrm{Gbit/s}$ .

Figure 3.11: Data detection simulation results of the UWB envelope detectors: eye diagram, height and Level 1 (L1).

is the one chosen to design the W-band envelope detectors from next section.

The experimental results for both UWB EDs are shown and compared in the next section.

#### 3.4 Bit Error Rate (BER) measurements

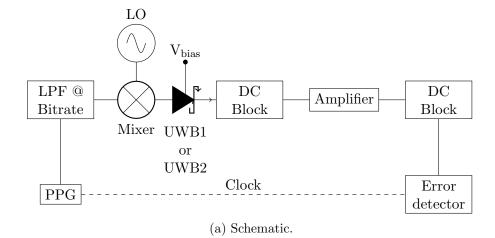
This section shows the experiments used to evaluate UWB1 and UWB2 using the data detection benchmark. Instead of measuring the height and Level 1 from the demodulated signal, we measured the Bit Error Ratio (BER) which is the ratio between the number of bit errors and the number of transferred bits. The BER result can be classified into three regions: the first one, referred as error free, befalls when there is less than 1 error in  $10^9$  transmitted bits (-Log(BER) > 9), meaning that the demodulation has been successful. The second region occurs when there is 1 error in between  $10^3$  to  $10^9$  transmitted bits (3 < -Log(BER) < 9); the BER is below the limit of 7% overhead forward error correction (FEC) [CC81; ITU04], where the information can still be retrieved. When we find more than 1 error per 1000 transmitted bits (-Log(BER) < 3), we assume that the demodulation contains too many errors and has failed.

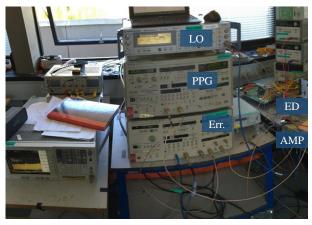
This section will not experimentally evaluate UWB1's and UWB2's frequency response and conversion loss, because they could not measured due to time constraints. Moreover, the frequency response and conversion loss are used to qualitatively verify if the ED under test will be able to demodulate an ASK modulated signal at a certain bitrate (conversion loss), at which carrier frequency the sensitivity of the detector is optimal (frequency response) and which is the ED's range of operation (conversion loss and frequency response). The BER gives a quantitative measurement of these parameters, and will be the benchmark used to evaluate the two EDs.

In the UWB frequency region, the BER is measured in real time using the setup depicted in figure 3.12. The Pulse Pattern Generator (PPG) generates a NRZ coded  $2^{31}$ -1 PRBS signal which is mixed with a Local Oscillator (LO). The LO sets the ASK signal's carrier frequency,  $f_c$ , which is directly fed into the ED. The EDs output power is boosted with a baseband amplifier due to the low sensitivity of the Error Detector to which is connected. The Error Detector measures the BER of the demodulated signal.

The ASK's carrier frequency was swept from  $4\,\text{GHz}$  to  $8\,\text{GHz}$  for UWB1 and from  $7\,\text{GHz}$  to  $9\,\text{GHz}$  for UWB2, while the ASK's power was set from  $-16\,\text{dBm}$  to  $-3\,\text{dBm}$  in steps of  $1\,\text{GHz}$  and  $1\,\text{dB}$  respectively for both EDs.

Figures 3.13 and 3.14 show the -Log(BER) versus the ASK input power to UWB1 at six carrier frequencies from 4 GHz to 9 GHz, and a bitrate of 2.5 Gbit/s and 4 Gbit/s respectively; together with the demodulated ASK signals' eye diagrams. The external balun provides 10 GHz phase balance bandwidth [Mara], hence ASK signals with higher frequency carriers are not considered in this experiment, since there is an uncertainty if the ED's performance would be limited by the balun or by the ED's architecture or design.





(b) Experimental setup [Bla+17].

Figure 3.12: BER experimental setup used with UWB EDs.

When demodulating  $2.5\,\mathrm{Gbit/s}$  ASK signals, the best performance is obtained at  $7\,\mathrm{GHz}$  and  $8\,\mathrm{GHz}$  carrier frequencies, i.e. the ED's design frequency, achieving error free with a sensitivity of  $-6\,\mathrm{dBm}$  and  $-3\,\mathrm{dBm}$  respectively. At  $6\,\mathrm{GHz}$  and  $9\,\mathrm{GHz}$  carrier frequencies the BER is below the limit of 7% overhead FEC, but error free demodulation was not possible due to an error floor.

When setting the bitrate to  $4\,\mathrm{Gbit/s}$ , error free demodulation is achieved at all tested carrier frequencies, providing a sensitivity between  $-9\,\mathrm{dBm}$  and  $-5\,\mathrm{dBm}$ . The external balun's broad bandwidth allows having a similar performance at the five carrier frequency, suffering only from a small power penalty. Demodulating a  $4\,\mathrm{Gbit/s}$  ASK signal with a  $4\,\mathrm{GHz}$  carrier frequency yields to a  $\Delta b = 100\,\%$ , which as shown in table 1.1, is to the author's knowledge, this parameter's World Record.

If we compare figures 3.13 and 3.14, we can appreciate that the performance is worse for 2.5 Gbit/s than for 4 Gbit/s, while it should be the opposite as shown

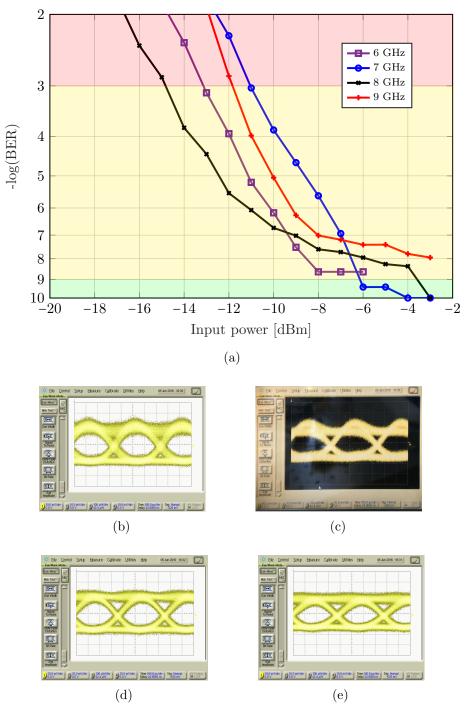


Figure 3.13: BER results of UWB1: (a) Experimental BER curves for ASK signals with bitrate =  $2.5\,\mathrm{Gbit/s}$  and eye diagrams of the demodulated signal with an input power of -7 dBm and carrier frequency at (b)  $6\,\mathrm{GHz}$ , (c)  $7\,\mathrm{GHz}$ , (d)  $8\,\mathrm{GHz}$  and (e)  $9\,\mathrm{GHz}$ .

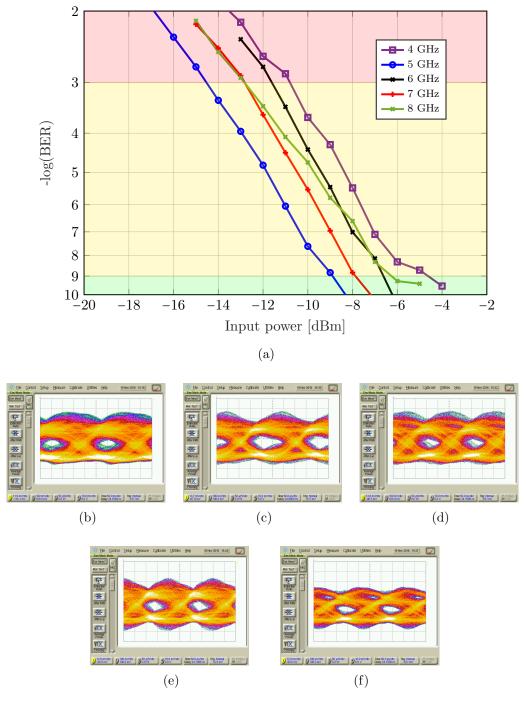


Figure 3.14: BER results of UWB1: (a) Experimental BER curves for ASK signals with bitrate =  $4\,\mathrm{Gbit/s}$  and eye diagrams of the demodulated signal with an input power of -7 dBm and carrier frequency at (b)  $4\,\mathrm{GHz}$ , (c)  $5\,\mathrm{GHz}$ , (d)  $6\,\mathrm{GHz}$ , (e)  $7\,\mathrm{GHz}$  and (f)  $8\,\mathrm{GHz}$  [Bla+17].

in figure 3.11. This difference is the result of conducting the two measurements in different places and time, changing part of the equipment, e.g. the mixer and baseband amplifiers are not the same, both results should not be directly compared. Better results are expected for the 2.5 Gbit/s curves when using the new setup used to measure the 4 Gbit/s curves of UWB1. Nevertheless, the 2.5 Gbit/s measurements were performed in the same procedure and equipment for UWB1 and UWB2, allowing us to compare both architectures in equal conditions in section 3.5.

A BER measurement was performed as well for UWB2 using the setup from figure 3.12. The equipment and settings used in this experiment are the same one as in the 2.5 Gbit/s BER measurement from UWB1 to be able to compare both architectures in equal conditions. The ASK signal's input power was swept from -17 dBm to -3 dBm while its carrier frequency was set at 7 GHz, 8 GHz and 9 GHz.

The experimental results are depicted in figure 3.15. Error free demodulation is only achieved for the 8 GHz carrier, providing a sensitivity of  $-12 \,\mathrm{dBm}$  and  $\Delta b = 31.75\,\%$ . Although using the carrier frequencies of 6 GHz, 7 GHz and 9 GHz does not provide an error free demodulation, UWB2 can produce an open eye diagram, as shown in figure 3.15, being able to retrieve the received information when introducing forward error correction coding.

These results agree with the simulations from figure 3.6, where the phase balance bandwidth, centred at  $f_c = 8 \,\text{GHz}$ , was reduced to 1.5 GHz, contrasting with the external balun's 10 GHz phase balance bandwidth. A poor fundamental harmonic cancellation for  $f_c = 6 \,\text{GHz}$ , 7 GHz and 9 GHz, results into some eye diagram distortion that can be appreciated in the eye diagrams from figure 3.15, and provoke more errors, avoiding that the UWB2 reaches error free demodulation at the these carrier frequencies.

It must be mentioned that UWB2's single ended equivalent version presented in [Cim+16] features -12 dBm of sensitivity as well as UWB2 when demodulating a 2.5 Gbit/s ASK signal. Considering that UWB2 needs of a smaller and less complex output low pass filter, and that UWB2's balanced architecture cancels part of the fundamental harmonic and common mode noise; strengthens and supports the decision of choosing this architecture when designing the W-band EDs over using a single ended one.

When the ASK signal's bitrate was increased to 4 Gbit/s using the same setup as with 2.5 Gbit/s, the obtained results were poor and are not worth to be mentioned, in accordance with the simulation results shown in figure 3.11b.

We expect that using the new BER setup used with UWB1 to measure the 4 Gbit/s BER curves will improve the UWB2's results at 2.5 Gbit/s and 4 Gbit/s as well, being able to get error free demodulation at other carrier frequencies and improving UWB2's sensitivity, since the new setup improved the results from UWB1.

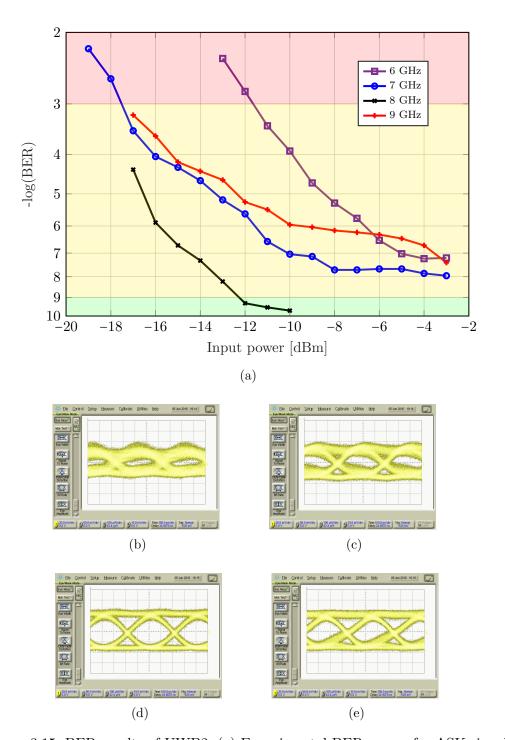


Figure 3.15: BER results of UWB2: (a) Experimental BER curves for ASK signals with bitrate =  $2.5\,\mathrm{Gbit/s}$  and eye diagrams of the demodulated signal with an input power of -7 dBm and carrier frequency at (b)  $6\,\mathrm{GHz}$ , (c)  $7\,\mathrm{GHz}$ , (d)  $8\,\mathrm{GHz}$  and (e)  $9\,\mathrm{GHz}$ .

#### 3.5 Comparison and discussion

Section 3.2 explained the design of the two UWB EDs designed in this dissertation. Their experimental results has been shown in detail in section 3.4.

UWB1 uses an external balun to provide the 180° out of phase signals to the two Schottky diodes, needed to suppress the fundamental harmonic at the ED's output. It shows a consistent performance for carrier frequencies from 4 GHz to 8 GHz when demodulating a 4 Gbit/s ASK signal, achieving a maximum  $\Delta b = 100\%$  for  $f_c = 4$  GHz ( $\Delta b = 50\%$  - 100% for  $f_c = 8$  GHz - 4 GHz), which is the current world record in the state of the art to the author's knowledge.

UWB2 combines the functionality of a balun while, simultaneously, rectifies the input signal, providing the suppression of the fundamental harmonic as well as UWB1. In comparison with UWB1, it provides a more cost effective solution and a size reduction; and introduces less insertion loss, which translates into a 6 dB - 8 dB better sensitivity than UWB1. As a drawback, it has a narrower phase balance bandwidth, which reduces the carrier frequency range which the UWB2 is able to demodulate error free.

## 4 Envelope Detectors (EDs) for W-band

This chapter presents three W-Band (75 GHz - 110 GHz) Schottky diode based balanced envelope detectors built in planar microstrip topology providing a WR-10 waveguide input interface through a WR-10 waveguide to microstrip line (MSL) transition. To connect the planar envelope detector with the waveguide feeding network output, a WR-10 to microstrip line (MSL) transition is needed.

In the W-band it is not possible to keep  $\Delta b$  as high as in the UWB, where the best  $\Delta b$  value found in the SoTA accounts to 26.9% [Kuo+12]. Due to the broad bandwidth from high data rate signals in this frequency region, it is crucial that the ED demodulates all the input signal's frequency components with a similar conversion loss, in order to prevent from distortions in the output signal [Bla+18a; Poz12]. Sensitivity is also important, since free space losses are higher and amplifiers are more costly and complex than in lower frequency ranges, therefore, the WR-10 waveguide to microstrip transition insertion losses must be minimised.

Table 4.1 summarizes the state of the art of W-band WR-10 waveguide to microstrip transitions. The Bode-Fano criterion [Bod45; Fan61] establishes the existing trade off between the transitions' S-parameters (return and insertion losses) and operational bandwidth, defined as the portion of the W-band where the transition works. In the transitions that we will present in the next section, we prioritised the operational bandwidth over S-parameters optimization, keeping low losses and manufacturing complexity, since the project's goal is designing an envelope detector operating within the whole W-band.

### 4.1 ED1 with Printed Circuit Board (PCB) substrate

The first W-band ED is composed of a W-band Schottky diode based balanced detector circuit, designed in microstrip technology on a 10 mil Rogers RT-Duroid 5880 substrate with 35 µm copper layer, presented in [Bla+18b; Bla+19] and a WR-10 waveguide WR-10 to microstrip transition described in [BJP17].

#### 4.1.1 WR-10 rectangular waveguide to microstrip line transition

This section describes the design, manufacturing and testing of an E-plane WR-10 waveguide to microstrip transition covering the full W-band as presented in [BJP17].

Figure 4.1 shows the transition CAD drawings, which can be divided into a waveguide and a microstrip section. The microstrip is placed inside the waveguide

Ref	$\begin{array}{c} \textbf{Insertion} \\ \textbf{loss} \\ [\text{dB}] \end{array}$	$\begin{array}{c} \textbf{Return} \\ \textbf{loss} \\ [\text{dB}] \end{array}$	$\begin{array}{c} \textbf{Operational} \\ \textbf{Bandwidth} \\ [\%] \end{array}$	Results	Measured
[LW99]	1.15	20	n/a	Experiment	Back to Back
[LTN13]	1	20	170	Simulation	Back to Back
[LTN13]	1.8	15	> 100	Experiment	Back to Back
[Reb+14]	0.55	15	100	Simulation	MSL to $WR-10$
[RGE15]	2.5	15	100	Experiment	Back to Back
[Zam+16]	3.26	12.7	65.7	Experiment	Back to Back
[Per+16]	0.55	15	100	Simulation	$\operatorname{MSL}$ to WR-10
[Zam+17]	0.8	13.5	85.7	Experiment	Back to Back
[Pér+18]	< 1	15	100	Simulation	WR-10 to $MSL$
[Pér+18]	0.63	8	100	Experiment	WR-10 to $MSL$

Table 4.1: WR-10 to MSL transitions state of the art.

metallic block, resulting on a dielectric filled rectangular waveguide (DFRW) as intermediate step between the WR-10 waveguide and the microstrip. The microstrip section of the transition and the envelope detector use Rogers RT-Duroid 5880 ( $\epsilon_r = 2.2$ , height = 0.254 mm and 35  $\mu$ m copper layer [Rog]) as substrate.

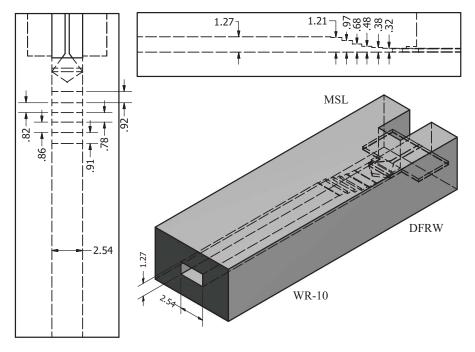
The metallic block feeds the TE<sub>10</sub> mode from the WR-10 waveguide into the DFRW through a multisection waveguide quarter wavelength Chebyshev transformer. The waveguide Chebyshev transformer matches the 1.27 mm height WR-10 waveguide with the 0.324 mm from the microstrip's height. After a mathematical analysis using Matlab applying the formulas described in [OS03; Per+16] and software simulations in CST Microwave Studio, it was concluded that a 5<sup>th</sup> order transformer was the best trade-off between performance (obtaining a flat insertion loss within the full W-band) and manufacture complexity.

The impedance needed at each section of the transformer is computed using the equivalent electric waveguide impedance,  $Z_{WR-10}$ , from equation (4.1) [Esh+05].

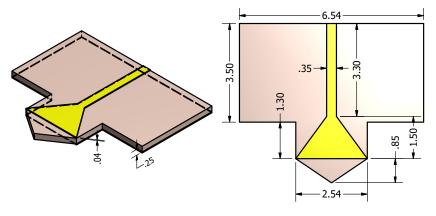
$$Z_{WR-10} = 2\frac{b}{a} \frac{\eta}{\sqrt{\epsilon_r}} \tag{4.1}$$

where a and b are the width and height of the waveguide respectively,  $\eta$  is the free space wave impedance (120 $\pi$ ) and  $\epsilon_r$  is the relative permittivity of the waveguide filling medium, equal to 1 in the WR-10 waveguide and to 2.2 in the DFRW.

For the standard air filled WR-10 waveguide (a = 2.54 mm, b= 1.27 mm) the impedance accounts for  $Z_{WR-10} = 376.7 \,\Omega$ . When the waveguide is filled with the Rogers substrate, leading to a DFRW (a = 2.54 mm, b= 0.254 mm,  $\epsilon_r$  =2.2), the impedance  $Z_{DFRW} = 67 \,\Omega$ . From equation (4.1), we know that the impedance is inversely proportional to the waveguide width and  $\epsilon_r$ , therefore, in order to decrease the abrupt impedance change from the air filled waveguide to the DFRW, we decided to include a substrate taper at the DFRW to increase the section impedance as shown in figure 4.1.



(a) Waveguide section.



(b) Microtstrip section.

Figure 4.1: Design of the WR-10 to MSL transition for ED1. Dimensions are in mm.

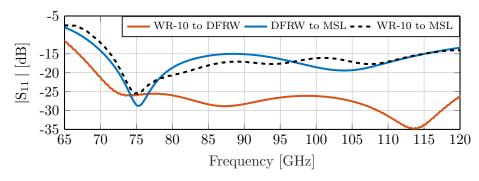
At this point we can calculate each section's height using equation (4.2), derived from equation (4.1), which relates the section height with its impedance and the sections length which is 810 µm, since  $\lambda/4$  equals to for the central W-band frequency, 92.5 GHz.

$$b_n = \frac{Z_{WR-10}a\sqrt{\epsilon_r}}{2\eta} \tag{4.2}$$

Later, the TE<sub>10</sub> mode from the DFRW is coupled into the quasi-TEM mode of the microstrip line keeping the same field propagation direction [Sim+18; Bou+09; Pér+18].

A microstrip line taper matches the DFRW to the  $50\,\Omega$  microstrip line. The reason for choosing a taper over a Chebyshev impedance transformer was that simulation results and bibliography, [Pér+18], proved a slightly better performance of the taper line, without increasing the manufacturing complexity.

The final dimensions of both sections, summarised in figure 4.1, were calculated through software optimization using CST Microwave Studio.



(a)  $|S_{11}|$  simulation results.

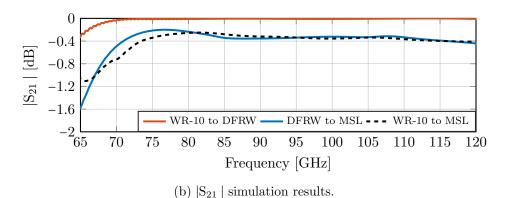


Figure 4.2: Simulated ED1's WR-10 to MSL transition S-parameters.

Figure 4.2 depicts the return and insertion loss results for the WR-10 waveguide to DFRW, DFRW to microstrip and WR-10 waveguide to microstrip transitions,



Figure 4.3: Manufactured back to back transition of ED1.

considering the waveguide interface as port 1 and the microstrip as port 2.

From these results we conclude that insertion and return loss from the WR-10 waveguide to DFRW transition are negligible, having almost no influence in the final result. The DFRW to MSL transition provides more than 15 dB return loss and less than 0.4 dB insertion loss, which is the main contribution to the full transition's insertion and return losses. Furthermore, the insertion loss is flat within the full W-band, avoiding distortion in the signal. These results outperformed in [BJP17] the state of the art simulation results from table 4.1.

#### Transition manufacturing and experimental validation

The transition was manufactured in brass at the TU Darmstadt in the Hans Busch Institut's facilities, at the Werkstatt für Feinmechanik. The metallic blocks were fabricated through micro-machining and the microstrip using a photolithographic process. WR-10 flanges and screws were added to the CAD drawing from figure 4.1.

The waveguide blocks were cut in the H-plane in order to reduce the possible field leakages since the electromagnetic field is confined in the central region of the wide WR-10 waveguide section. The slit between the blocks is negligible after introducing surface walls at the border of the inner waveguide, and having several screws which tighten firmly the upper and lower blocks. Four dowel pins are used to guarantee the alignment of the metallic blocks with respect to each other and the microstrip line held in their inside.

We tested the transition performance using the Agilent PNA N5222A with W-band waveguide extensions, which provides WR-10 waveguide interfaces. In order to connect the transition to the PNA, we needed to manufacture one back to back transition, i.e. WR-10 waveguide to microstrip to WR-10 waveguide, depicted in figure 4.3. This back to back transition is the result of joining two of the transitions depicted in figure 4.1, having a 9.6 mm  $50\,\Omega$  microstrip line in the middle. The transition S-parameters results are depicted in figure 4.4.

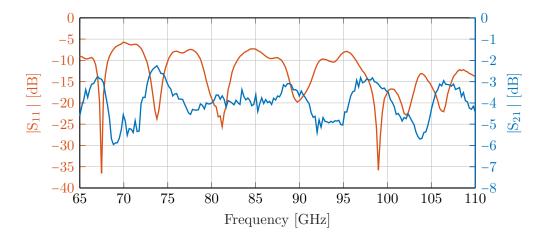


Figure 4.4: Experimental back to back S-parameters from the WR-10 to MSL transition.

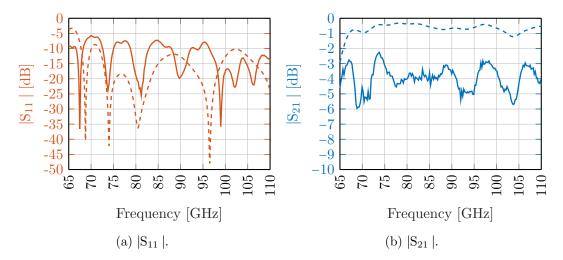


Figure 4.5: Full WR-10 to MSL to WR-10 transition back to back S-parameters comparison between experimental (solid) and simulation (dashed) results.

Figure 4.5 compares the experimental results with the simulations of the back to back transition. The measured return loss follows a similar trend as in the simulation within the lower half of the W-band. In the upper half, only the notch at 96 GHz is shifted to 99 GHz. The average return loss decreases from 18.2 dB in the simulation results to 11.6 dB on the lower W-band half and to 15.9 dB in the upper one, presenting a total average difference of 4.4 dB when comparing the experimental results with the simulation.

The insertion loss increases as well to the range between  $-2.3\,\mathrm{dB}$  and  $-5.7\,\mathrm{dB}$  within the W-band, having an average insertion loss of  $3.96\,\mathrm{dB}$  which is slightly below the performance of the state of the art experimental results from table 4.1.

The average difference between the experimental characterization and the simulation results is  $3.3\,\mathrm{dB}$  .

It has been experimentally demonstrated that the Rogers RT-Duroid 5880 presents a dielectric loss tangent of 0.01 within the W-band, with the  $\epsilon_r$  remaining at 2.22 [Reb15]. Applying equation (4.3) [Poz12], we can calculate that the substrate introduces 0.13 dB/mm of losses, which are not considered by the CST Microwave Studio within the simulation results. Considering that, the losses in the microstrip account to 1.25 dB on average in the 9.6 mm microstrip line and having two transition blocks, we can estimate the insertion loss of one manufactured WR-10 waveguide to microstrip transition is 0.5 dB to 2.2 dB within the W-band, with an average loss of 1.4 dB, which is only 1 dB more than calculated in simulations:

$$\alpha_d = \frac{27.3 \cdot \sqrt{\epsilon_r} \cdot f \cdot \tan(\delta)}{c} \tag{4.3}$$

## 4.1.2 Envelope detector circuit

The first W-band envelope detector, ED1, is based on the architecture described in section 3.2.2, which exploited the high-pass compensation principle to rectify a single ended ASK signal using a balanced demodulation scheme through its Rat-Race hybrid coupler balun functionality, allowing to cancel the fundamental harmonic at the ED1's output and hence, relaxing the ED1's output filter.

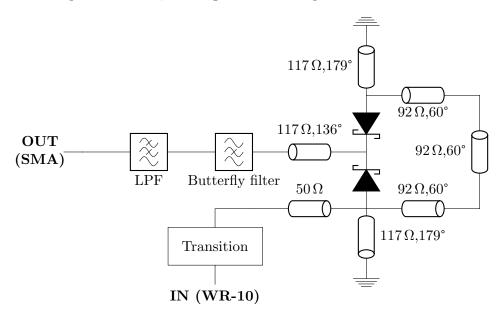
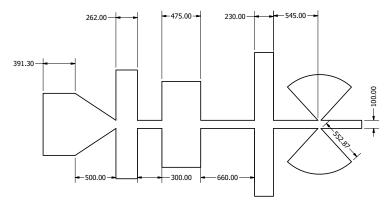
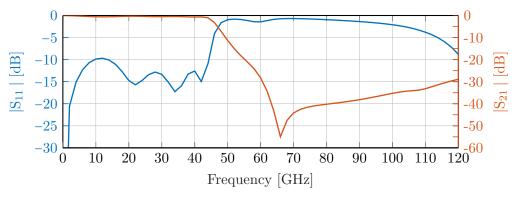


Figure 4.6: Circuit schematic of ED1: electrical lengths are measured at 92.5 GHz (W-band's central frequency).

Figure 4.6 describes the ED1's schematic, which is composed of two Schottky diodes



(a) Filter layout. Dimensions are in μm.



(b)  $|S_{11}|$  and  $|S_{21}|$  of the filter.

Figure 4.7: Output filter of ED1. Simulation results.

with two shorted stubs placed at their anodes, a semicircular shaped transmission line with an electrical length of 180° at 92.5 GHz. The diodes' cathodes are connected through a transmission line to a butterfly filter and a 6<sup>th</sup> order 45 GHz cut-off frequency stepped impedance low pass filter (LPF). Figure 4.7 shows the filter layout and its S-parameters. The two filters reject the fundamental harmonic spurious frequency components, which were not cancelled using the balanced architecture principle. At the LPF's output an SMA connector is placed to provide the output interface. In order to provide a DC path at the diodes' output, an external bias tee can be connected when necessary. Being able to place an external bias tee presents the advantage of enabling to experimentally measure the ED1's DC output in the frequency response benchmark in section 4.5, following the schematic depicted in figure 3.1b.

The detector circuit is built using the same microstrip technology as in the WR-10 to MSL transition, i.e., on a 10 mil Rogers RT-Duroid 5880 substrate [Rog] with 35 µm copper layer. The Schottky diodes from the 3DSF serie were provided by

ACST GmbH [ACS], analyzed in section 2.3 presents the features summarised in table 2.1.

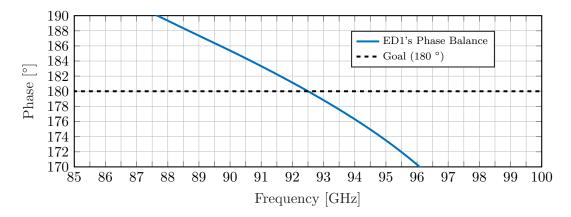


Figure 4.8: Phase balance bandwidth of ED1.

Similar to section 3.2.2, the phase balance bandwidth is measured using harmonic balance analysis in ADS. Figure 4.8 depicts ED1's phase balance bandwidth ( $\pm 6^{\circ}$ ) which accounts of 5.2 GHz (89.6 GHz - 94.8 GHz). At the W-band central frequency, 92.5 GHz, the phase balance bandwidth is 180°.

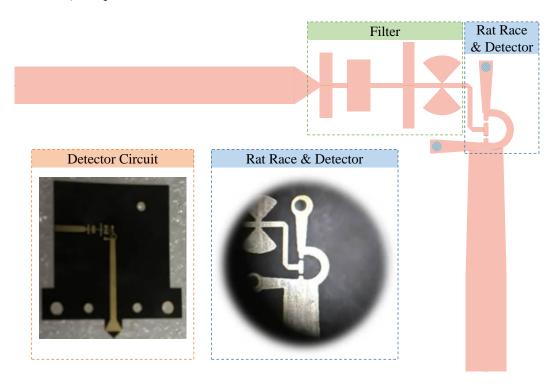
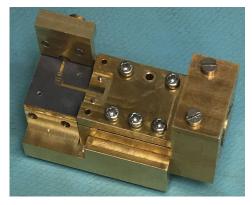


Figure 4.9: Layout of ED1.





(a) Envelope detector [Bla+19].

(b) Mounted diodes.

Figure 4.10: Manufactured ED1.

Figure 4.9 depicts the layout of the detector circuit, while figure 4.10 shows the manufactured ED mounted on the metallic blocks, obtained from cutting the transition block from figure 4.3 in half and the mounted diodes. A new metallic block was fabricated to hold the detector circuit when it is inserted into the transition.

#### 4.1.3 Simulation and experimental results mismatch for ED1

ED1's experimental characterization is thoroughly analyzed in section 4.5. It will show that the manufactured ED1 presents outstanding results in terms of conversion loss and is able to demodulate up to 14 Gbit/s ASK signals. Nonetheless, its performance is limited due to its frequency response (it will be shown in figure 4.40), which is lower on the upper W-band half region than calculated in simulations. This roll-off, which appears at 100 GHz in simulations, experimentally shows up at 92.5 GHz.

Three causes were investigated to explain this frequency shift in the roll-off: a possible mismatch in the diode model when using the Rogers 5880 substrate, since the diode was modelled mounted on fused silica [HPC11]; manufacturing tolerances either in the PCB or in the metallic block production; and the wrong substrate characterization in the simulation software, either CST Microwave Studio or ADS Momentum.

In order to check if the mismatch comes from the Rogers 5880 substrate, we decided to build a new W-band ED version, ED2, presented in section 4.2, using fused silica quartz Corning 7980 [Cor14].

After checking the PCB in detail under the microscope, we could only find small manufacturing deviations, which could not influence the observed behaviour. Regarding the metallic blocks, figure 4.5 shows that the transition insertion loss is flat in the W-band, and the difference between simulation and experimental results is only 1.6 dB on average, therefore, they cannot cause such a pronounced roll-off.

In section 4.1, the metallic block together with the  $6.3\,\mathrm{mm}$   $50\,\Omega$  transmission line used as input interface to ED1 were simulated using CST Microwave Studio, while

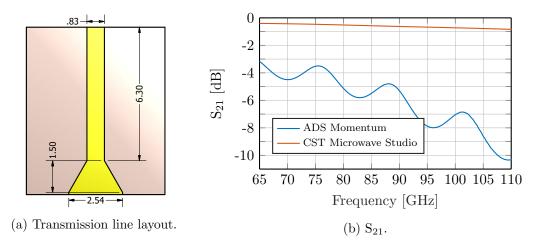


Figure 4.11: ED1's microstrip transmission line simulation results. Comparison between CST Microwave Studio and ADS Momentum.

the ED1's planar structure was simulated using ADS Momentum. In order to check if the mismatch between simulation and experimental results from figure 4.32 arises from the software, we compared the results when simulating the transmission line depicted in figure 4.11a in CST Microwave Studio and ADS Momentum, obtaining the results depicted in figure 4.11b. This transmission line is the input to the ED1's input shown in figure 4.9, and was simulated in CST Microwave Studio during the design of ED1.

According to the results depicted in figure 4.11b, CST does not consider some frequency dependant losses occurring in the 1.5 mm taper and in the 6.3 mm  $50\,\Omega$  transmission line, which account up to  $10\,\mathrm{dB}$  in the upper W-band. Although this loss value is higher than what it was calculated in section 4.1.1, where we assumed  $\tan(\delta)$  constant and equal to 0.01 in the full W-band, [Reb15] shows that  $\tan(\delta)$  increases up to 0.03-0.05 in the higher W-band region, therefore, we believe that the results obtained with CST in figure 4.11b are too optimistic in terms of losses, and that ADS provides a better estimation. We decided to construct a third W-band envelope detector, ED3, using the Rogers 5880 substrate, and correcting the ED1's experimental frequency response roll-off by reducing ED1's input transmission line.

We checked if this same issue happened with the ED2, and verified that the fused silica model provided within CST Microwave Studio was more consistent and agreed with the ADS Momentum simulations, therefore, we did not need to modify ED2's design.

#### 4.2 ED2 with fused silica substrate

The second W-band ED presented in this dissertation, ED2, counts with a W-band Schottky diode based balanced detector circuit, and a new designed WR-10 waveguide

WR-10 to microstrip transition. In this second ED, we chose a new substrate, fused silica quartz Corning 7980 with a thickness of 150 µm,  $\epsilon_r = 3.75$  and  $\tan(\delta) = 0.0001$  at 1 GHz [Cor14], which is well known within the author's research group at TU Darmstadt. Furthermore, this substrate has already been tested in this frequency range with the diodes provided by ACST [Hoe+13; Hoe+14; Hoe+15] and was used to obtain the diode model included in the simulations [HPC11]. Although the PCB fabrication process is more complex in comparison when using the Rogers RO5880, the manufacturing tolerances decrease, allowing to design a more precise circuit. Moreover, with the microstrip manufacturing process performed in the clean room, we can also fabricate thinner transmission lines if needed.

The first goal of this ED2 will be flattening the upper W-band region's frequency response from ED1 by increasing the input bandwidth. In addition, we pursue to have the optimum performance for carrier frequencies around 85 GHz, which is the working frequency within the CELTA beamformer demonstrator.

This section will follow the same structure as section 4.1. It will start with a WR-10 waveguide to microstrip transition and then show the ED's design.

## 4.2.1 WR-10 rectangular waveguide to microstrip line transition

ED2 provides a WR-10waveguide input interface similarly as the ED1. In order to connect the planar detector with the waveguide interface, a WR-10 waveguide to microstrip line transition is needed. This section describes the design, manufacturing and testing of an E-plane WR-10 waveguide to microstrip line transition covering the full W-band.

In the previous version a quarter wavelength Chebyshev transformer matched the WR-10 waveguide and the substrate heights, which showed a slightly better performance in simulations as using a linear taper. After measuring the manufactured back to back prototype, simulation and experimental results differed in  $3.3\,\mathrm{dB}$  on average in the  $|S_{21}|$ . In the transition from WR-10 waveguide to microstrip, section 4.1.1 justifies that this difference is reduced to  $1\,\mathrm{dB}$  on average in the manufactured ED circuit, after considering the losses in the microstrip line.

In this version we decided to use a double linear taper to match the 1.27 mm WR-10 waveguide to the 0.156 mm substrate. By doing this, we are able to check if the previous 1 dB mismatch can be reduced, since the manufacturing tolerances are reduced when using a taper in comparison with the Chebyshev transformer.

Figure 4.12 depicts the transition CAD drawing, divided into two sections: the metallic block encompassing the waveguide and its taper and the microstrip. The latter is placed inside the waveguide block as shown in figure 4.12a. Now, due to constraints in the microstrip fabrication process, the transition occurs directly by coupling the TE<sub>10</sub> mode from the WR-10waveguide into the microstrip line quasi-TEM mode, without having a DFRW intermediate step, since the microstrip peak is metallize on the top and ground layers. In addition, the substrate height is now 0.16 mm instead of the 0.32 mm from ED1, which makes the design a little more challenging.

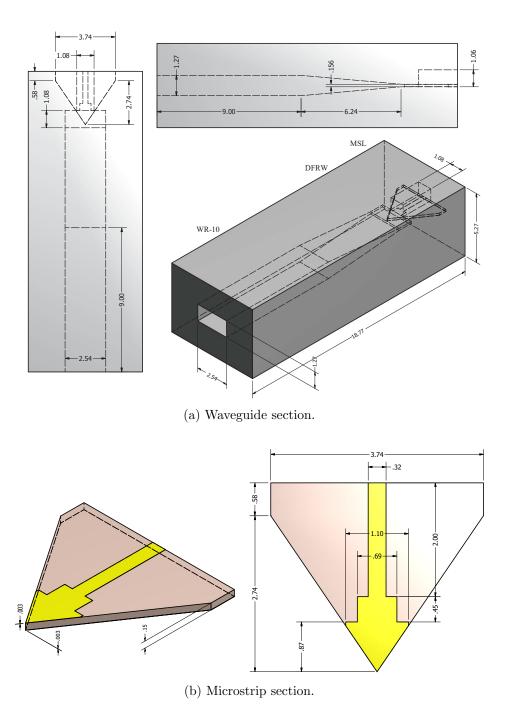


Figure 4.12: Design of the tapered waveguide to microstrip transition for ED2. Dimensions are in mm.

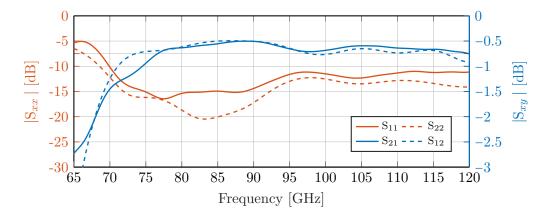


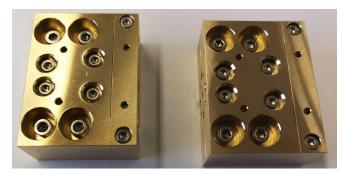
Figure 4.13: Simulated WR-10 waveguide to microstrip line transition S-parameters.

As an advantage, using a linear taper instead of the Chebyshev transformer reduces the mathematical complexity in the metallic block design. In this transition, the only parameter to optimise is the taper length, since the heights are fixed. We optimised this length through CST Microwave Studio software, in order to have a height transition as smooth as possible to feature low and flat insertion loss, while keeping the length short to have a compact block.

The microstrip section is composed of a 0.87 mm taper that confines the  $TE_{10}$  mode into the microstrip and a quarter wavelength transformer, which matches the taper impedance to a  $50\,\Omega$  microstrip line. The trade-off between the taper width and length (1.1 mm and 0.87 mm respectively), the number of elements in the transformer and the total length from the microstrip tip to the  $50\,\Omega$  transmission line was calculated using CST Microwave Studio.

The microstrip presents an arrow shape due to the substrate-cutting limitations arising from using fused silica, which is cut using a dicing saw. The final PCB cannot have inside corners because once the saw starts dicing, it cannot stop in the middle of the cut, hence the only design shapes that can be used are using straight lines.

Figure 4.13 shows the return and insertion loss simulation results for the WR-10 waveguide to microstrip transition depicted in figure 4.12, considering the waveguide interface as port 1 and the microstrip as port 2. The transition introduces between 0.5 dB and 0.8 dB insertion loss in the full W-band, while keeping the return loss above 11 dB, which are acceptable features for this project. When compared with the previous transition's results from figure 4.2, it can be noticed that the lack of the intermediate transition from WR-10 waveguide to DFRW, the larger height difference and the design constraints in the microstrip cutting reduce the transition performance (in the previous version, the return and insertion losses were above 15 dB and below 0.4 dB respectively).





(a) Metallic blocks.

(b) Microstrip line.

Figure 4.14: Manufactured back to back transition for ED2.

### Transition manufacturing and experimental validation

The transition was manufactured in brass at the TU Darmstadt in the Hans Busch Institute's facilities, at the Werkstatt für Feinmechanik, adding WR-10 flanges and screws to the CAD drawing from figure 4.12. The microstrip was manufactured by the author, using a photolithographic process in the Institute's clean room obtaining the result shown in figure 4.14b.

The waveguide blocks were cut in the H-plane in order to reduce the possible field leakages, because the electromagnetic field is confined in the middle of the wide WR-10 waveguide section. The slit between the blocks is negligible after introducing surface walls at the border of the inner waveguide, and having several screws which tighten firmly the upper and lower blocks. Eight dowel pins are used to guarantee the alignment of the metallic blocks with respect to each other. The microstrip is aligned using a slot dug into the lower metallic block as shown in figure 4.14b.

Instead of building the back to back transition and later cutting it as we did with ED1, we decided to build the transition separated into blocks: two transitions (which can be placed back to back when evaluated in the VNA) and two ED blocks, where the ED2 detector circuit will be mounted. The main reasons to separate the blocks from the beginning are to be able to reassemble the transition again if needed, even after having mounted the ED, and to increase the manufactured prototype accuracy. In the previous transition the back to back prototype was cut after measuring it, which could provide some inaccuracies in the resulting metallic blocks dimensions. This tolerances are acceptable when using the Rogers RO 5880 substrate because it can be slightly deformed applying pressure, or cut quite easily if necessary. If a fused silica substrate is pressed, it will break due to its fragility, and it is not possible to cut it as easily once the diodes are mounted, since the dicing saw may damage the diodes.

We used an Agilent PNA N5222A with W-band waveguide extensions to measure the S-parameters of the back to back transition, where we placed a  $4\,\mathrm{mm}$   $50\,\Omega$  microstrip, as shown in figure 4.14b, obtaining the results depicted in figure 4.15.

Figure 4.16 compares these experimental results, with the back to back simulation

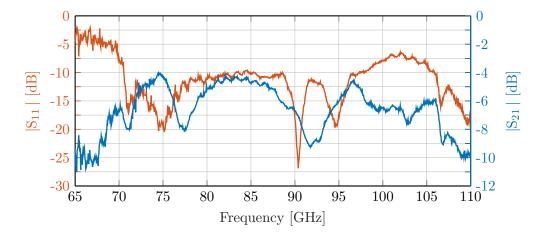


Figure 4.15: Experimental back to back S-parameters from the WR-10 waveguide to microstrip line to WR-10 waveguide transition for ED2.

results. The return loss follows a similar trend in both simulation and experimental results, being below  $-6\,\mathrm{dB}$  in the full W-band in both cases. The mean return loss difference between simulation and experimental results accounts only for  $1.13\,\mathrm{dB}$ , compared with the  $4.4\,\mathrm{dB}$  in ED1.

When evaluating the insertion loss, the experimental and simulation results difference becomes larger, obtaining a 5.74 dB average difference within the full W-band. In addition, the insertion loss is not flat in the experimental results, where its values are comprised between 4 dB and 10 dB. Furthermore, the experimental results do not follow the simulation results shape. This mismatch is due to the soft or nonexistent contact between the microstrip and the top part of the metallic block. In ED2, if the contact between the metallic block's top section and the fused silica microstrip is too strong, there is the risk that the microstrip breaks. Nevertheless, if there is an air gap in between, the  $TE_{10}$  mode cannot be fully confined into the microstrip, and part of the field is radiated outside. This effect leads to an increment of the insertion loss while keeping the same return loss as depicted in figure 4.16, because the input signal is radiated, not reflected.

In order to fill the airgap between the microstrip and the top metallic block, we added some conductive silver glue at the microstrip's bottom as shown in figure 4.17b. This glue should not modify the microstrip behaviour, since it is placed below its ground plane, lifting the microstrip to provide a contact and close the airgap.

Figure 4.18 compares the experimental S-parameter results when applying the glue with the previous ones without glue from figure 4.16. The return loss presents a similar value as before, but the insertion loss is now flatter in most of the W-band, getting rid of the previous 91.5 GHz notch.

We tested the structure after using acetone to remove the glue, and applied it again. We also tried adding more glue on top of the dry one to lift up the microstrip. Moreover, we changed the microstrip because we had two samples with the same

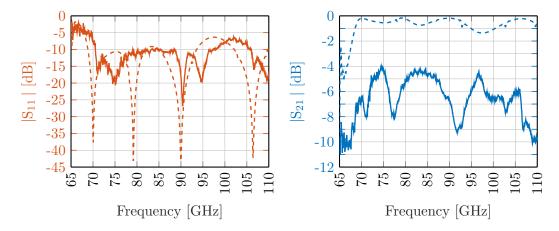


Figure 4.16: Full ED2 transition back to back S-parameters comparison between experimental (solid) and simulation (dashed) results.

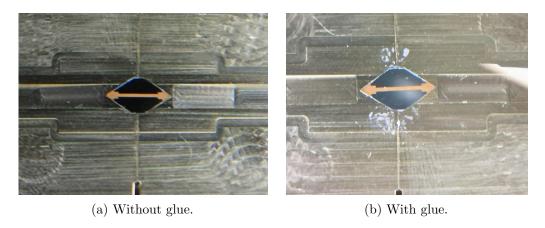


Figure 4.17: Microstrip line mounted on the back to back transition.

features available for testing. All this changes and tests lead to the results depicted in figure 4.19. The best achieved results have been shown in figure 4.18b.

From this experiment, it can be concluded that the ED2 is very sensitive to small changes when placing the fused silica substrate into the metallic blocks. Furthermore, the manufacturing tolerances are critical and they reduce the transition performance significantly in contrast to the previous version where the tolerances were negligible, e.g. in this transition, if the metallic blocks slightly press the substrate, it would break, therefore, there is a higher possibility of having an airgap between the substrate and the metallic blocks. Although this limitation can be compensated using a conductive glue, figure 4.19 proved that applying the glue must be done carefully and the circuit must be tested afterwards. The advantage is that if the glue has been applied wrongly, it can be removed and added it again.

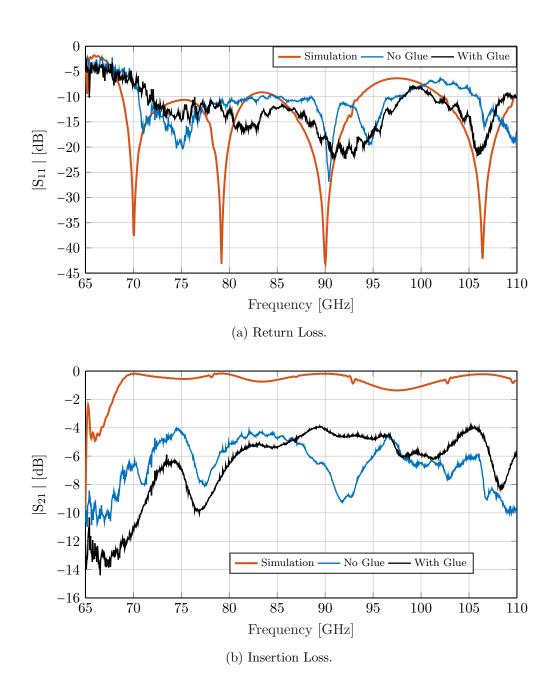


Figure 4.18: Full ED2 transition back to back S-parameters comparison between simulation and experimental results, before and after applying glue.

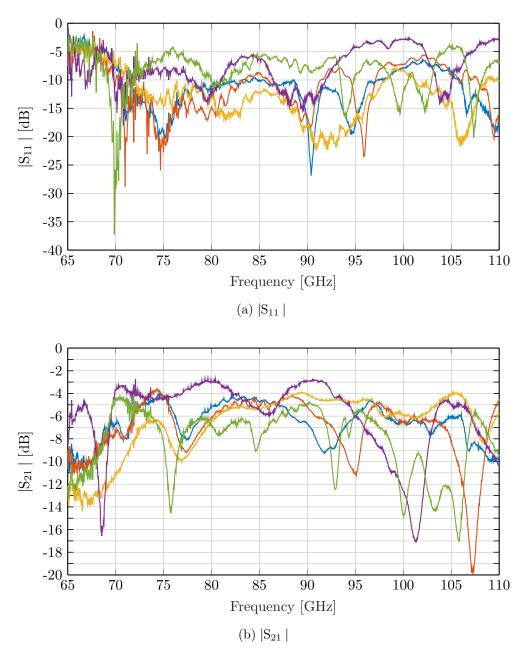


Figure 4.19: Full ED2 transition back to back S-parameters test run using two different transition PCBs and after applying glue several times.

Table 4.2: Transmission line S-parameters used in the W-band envelope detectors' design: electrical lengths are measured at 92.5 GHz.

	Substrate	$Z_{1}$	$L_{1}$	$Z_{2}$	$L_{2}$	$Z_{3}$	$L_{3}$
ED1	Rogers 5880	$100\Omega$	$125^{\circ}$	$115\Omega$	60°	$130\Omega$	220°
ED2	Fused Silica	$117\Omega$	$179^{\circ}$	$92\Omega$	$60^{\circ}$	$117\Omega$	$136^{\circ}$

## 4.2.2 Envelope detector circuit

Figure 4.20 shows the schematic of ED2, which follows the same architecture as ED1. The transmission lines have been modified optimising the phase balance bandwidth, input frequency response and conversion loss, considering that we can introduce thinner transmission lines than before. The transmission lines values for ED1 and ED2 are summarised in table 4.2. One big difference between the two EDs yields in the shorted stubs' grounds: while in the Rogers substrate it was possible to have via holes, in the fused silica substrate it is not possible to drill and metalise this holes with the available technology. Therefore, it was decided to implement the grounds by connecting two pads to the metallic block housing. Next to the pads we placed a radial stub, which behaves as an RF choke, avoiding that the input W-band signal leaks to ground.

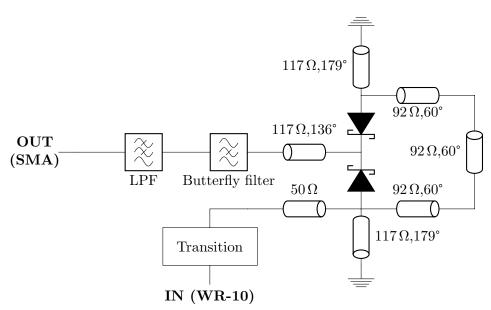
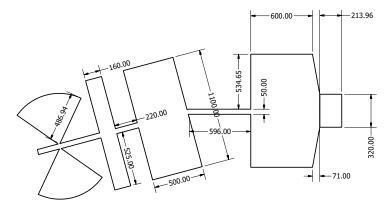
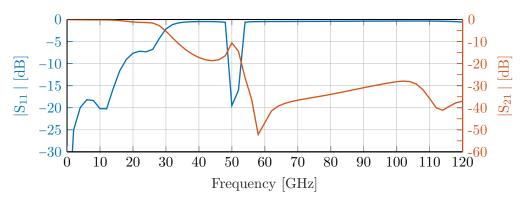


Figure 4.20: Circuit schematic of ED2: electrical lengths are measured at 92.5 GHz (W-band's central frequency).

The output filter shares the same topology as in the previous version. It consists of a butterfly filter and a  $6^{\rm th}$  order 25 GHz cut-off frequency stepped impedance



(a) Filter layout. Dimensions are in μm.



(b)  $|S_{11}|$  and  $|S_{21}|$  of the filter.

Figure 4.21: Output filter of ED2. Simulation results.

low pass (LPF) filter. The LPF cut-off frequency was reduced in order to filter the noise from the frequency band between 25 GHz and 45 GHz. The filter layout and its S-parameters are shown in figure 4.21. At the LPF's output, an SMA connector is placed to provide the ED2's output interface. Similar to ED1, this detector circuit does not count with a built in bias tee in order to measure the ED2's DC output in the frequency response benchmark.

The ED is built in microstrip technology on a 150  $\mu$ m fused silica quartz Corning 7980 [Cor14] with 3  $\mu$ m top gold layer. The Schottky diodes, provided by ACST GmbH [ACS], have the same features as in ED1 .

Figure 4.22 shows the ED's phase balance bandwidth measured through ADS harmonic balance analysis in ADS. In this version, the phase balance bandwidth  $(\pm 6^{\circ})$  accounts for 5.9 GHz, between 89.2 GHz and 95.1 GHz. At the W-band central frequency, 92.5 GHz, which is the design frequency, the phase balance bandwidth is 180°.

When compared with ED1, the phase balance bandwidth has been improved

by 13.5%, due to the possibility of shrinking down the shorted stubs, which was previously not possible due to manufacturing constraints.

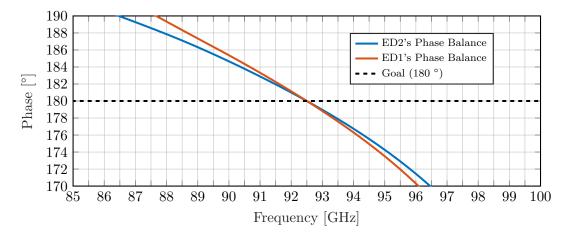


Figure 4.22: ED2's and ED1's phase balance bandwidth comparison.

Finally, figure 4.23 depicts the full detector circuit's layout.

#### Manufacturing

The substrate of ED2 was first processed by the author in the Hans Busch Institute's clean room, obtaining the results shown in figure 4.24.

When mounting the Schottky diodes at ACST GmbH facilities, on figure 4.25c, the diodes could not be glued to the substrate. Therefore we decided to manufacture a second version, where ACST GmbH would not only mount the Schottky diodes on the substrate as they did in ED1, but also process the PCB using photolithography in order to improve the manufactured ED2's quality. The resulting prototype is depicted in figure 4.25. When compared with figure 4.24, it can be noticed that the manufactured PCB improved considerably.

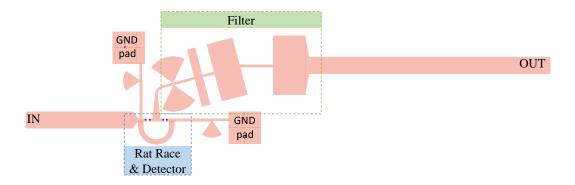
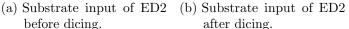


Figure 4.23: ED2's Layout.







after dicing.



(c) Substrate central area of ED2

Figure 4.24: Fused silica manufactured substrate of ED2.

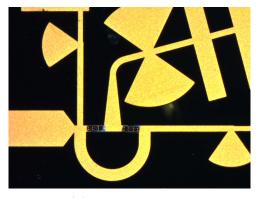
After gathering the metallic blocks and the substrate with the diodes on them, the next step is to mount the substrates on the metallic blocks and installing the grounds for the shorted stubs on the ED's pads at the Schottky diodes' inputs through bonding wires connected to the metallic blocks. Placing the bonding wires was not possible due to some calibration mismatch with the machine used to place them, which could break the substrate with the diodes mounted. Not having a ground means that the experimental results of ED2 would not be those for which it was designed, since without grounding the diodes' input, there is no DC path through the diodes, and the downconverted signal at baseband frequencies cannot be generated. Moreover, figure 4.19 shows that a small change in the substrate placement leads to significantly different results in the transition's S-parameters. For these reasons, we decided to leave the ED2 mounting and characterization for the future. This tasks together with solving the issues arising from the metallic blocks transition shown in figure 4.19 could be addressed in a PhD or Master thesis.

# 4.3 ED3 improved detector with Printed Circuit Board (PCB) substrate

As explained in section 4.1.3, we want to address ED1's experimental roll-off with a redesign of ED1 to widen the detector's input bandwidth to 35 GHz, i.e. the full W-band. Figure 4.11 justified that the reason for this shrinking is the input transmission line's length of ED1, which introduces frequency dependant losses. In order to solve them, in this new version, ED3, the input transmission line was shortened to just a taper line, and its width was reduced to preserve its input bandwidth as shown in figure 4.26. This transmission line width-shrink is possible because most of the electromagnetic  $TE_{10}$  field is confined in the central region of the WR-10 waveguide, and with this taper the field is transferred to the microstrip transmission line. The other ED1's components, such as filter and detector's structure remain the same. Simulations of the planar structure were conducted using ADS Momentum, including the input transmission line, while CST Microwave Studio was used exclusively to simulate the metallic blocks and the WR-10 waveguide to DFRW



(a) ED2.



(b) Mounted diodes.

(c) Substrate input of ED2 after dicing.

Figure 4.25: ED2's fused silica in-house manufactured substrate by ACST GmbH.

transition. Figure 4.26a shows the final layout of the ED and figure 4.26b compares it with the previous version. Since we had built a backup version of ED1 with the second half of the back to back WR-10 to MSL transition, the previously manufactured metallic blocks could be used to build ED3 by applying small adjustments to build ED3, ending up having one prototype of ED1 and another of ED3.

## Manufacturing

Once we received ED3's PCB, the next step was to mount the Schottky diodes at ACST GmbH, similar as it was done with ED1. Due to the big work load at the company, they were not able to mount the diodes before the end of this dissertation, nonetheless, they offered us generously the unmounted diodes so that we could mount them at TUDa. As a result of the Coronavirus crisis we were not able to mount the diodes and characterise ED3, since the recommendation from the authorities was to remain at home at the time we had booked to mount the diodes. Nevertheless, if in the period of time between this dissertation's hand in and its defence we are able to accomplish the two tasks, the final results will be presented in the defence and

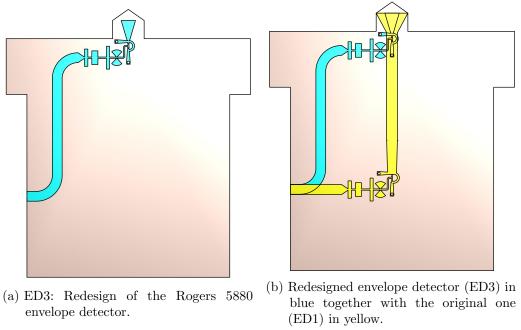


Figure 4.26: Layouts of the two ED's versions using Rogers 5880 substrate.

attached to the dissertation in an appendix.

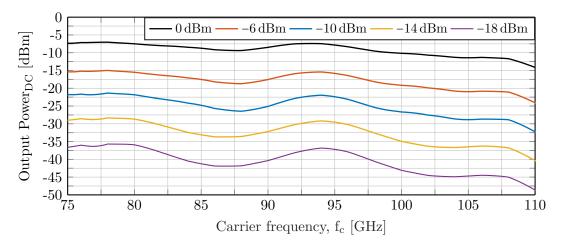
#### 4.4 Simulation results

This section describes the simulations accomplished to evaluate ED1, ED2 and ED3 using the three benchmarks described in section 3.1: frequency response, conversion loss and data detection measurement. The simulations were conducted using CST Microwave Studio for the waveguide section and the transition, including the input transmission line of each envelope detector (one taper for each detector and a  $50\,\Omega$  input transmission line of 6.3 mm for ED1 and of 2 mm for ED2); while ADS harmonic balance analysis was used for the planar structure, where the transition simulation results were included.

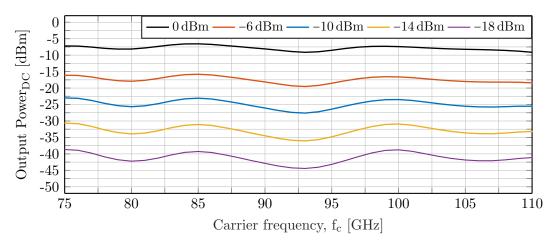
#### Frequency response

As explained in figure 3.1, the frequency response in a W-band envelope detector is calculated by measuring its DC output after being fed with a single tone, which is swept from  $75\,\mathrm{GHz}$  to  $110\,\mathrm{GHz}$  with a power set from  $0\,\mathrm{dBm}$  to  $-18\,\mathrm{dBm}$ . In contrast, the UWB detectors were fed with a low frequency modulated ASK signal composed of a carrier and its two sidebands because they were DC fed.

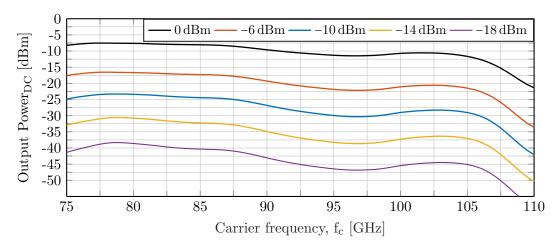
Figure 4.27a displays the frequency response simulation results of the ED1. It provides 25 GHz of 3 dB bandwidth, from 75 GHz to 100 GHz for a 0 dBm input



(a) Frequency response simulation results of ED1.



(b) Frequency response simulation results of ED2.



(c) Frequency response simulation results of ED3.

Figure 4.27: Frequency response simulation results of the W-band envelope detectors.

power. Moreover, its frequency response in the  $100\,\mathrm{GHz}$  -  $110\,\mathrm{GHz}$  range can be used for communication purposes, since the output power only reduces  $5\,\mathrm{dB}$  -  $7\,\mathrm{dB}$  when compared with the lower region of the W-band.

When decreasing the input power, the input bandwidth shrinks down as well, and the frequency response has more ripples.

Figure 4.27b depicts the frequency response results of ED2. It provides 35 GHz of 3 dB input bandwidth for a 0 dBm input power, covering the full W-band, from 75 GHz to 110 GHz. ED2's output power is similar to the one from ED1 for frequencies below 105 GHz when they are fed with a 0 dBm input tone. Furthermore, ED2 provides a higher output power for frequencies above 105 GHz.

When decreasing the input power, the input bandwidth shrinks down and the frequency response has more ripples than in ED1. Moreover, when fed with an input tone with power below  $-10\,\mathrm{dBm}$ , ED2's output power is reduced in comparison with ED1. This agrees with the Bode-Fano criterion explained in section 2.5: the bandwidth of the ED can be increased using a broader matching, at the cost of decreasing the power delivered to the Schottky diodes, and hence the output power of ED2 is lower. In addition, the insertion loss introduced by the ED2's transition are slightly higher than ED1's, which means that the detector circuit receives a lower input power.

The frequency response results of ED3 are shown in figure 4.27c. ED3 provides 29 GHz (from 75 GHz to 104 GHz) of 3 dB input bandwidth for a 0 dBm input power tone, which is broader than in ED1, either if ED1's input transmission line was simulated in CST or ADS. The roll-off still occurs, but it now starts at 105 GHz instead of at 92.5 GHz. When decreasing the input power, the input bandwidth shrinks down as well to 14 GHz for a -18 dBm input power.

The CELTA project's requirements requested 5 GHz to 10 GHz of input bandwidth, which is fulfilled at every input power from 0 dBm to -18 dBm by the three detectors: ED1, ED2 and ED3.

#### Conversion loss

Similar to the UWB EDs, the W-band envelope detectors are fed with an ASK signal, composed of a  $-17\,\mathrm{dBm}$  carrier with frequency  $f_c$ , which is swept from 75 GHz to 110 GHz, modulated by two  $-37\,\mathrm{dBm}$  sidebands swept from  $f_{sb} = 0.5\,\mathrm{GHz}$  to 30 GHz, placed at  $f_c \pm f_{sb}$ . The power values are chosen in accordance with the experimental ones, to be able to compare them in equal conditions. The conversion loss of each detector is calculated by measuring the difference between the obtained downconverted signal at  $f_{sb}$  and the input power at  $f_c \pm f_{sb}$ . The results are plotted in two graphs for each detector. In the first one,  $f_{sb}$  is plotted in the x-axis and  $f_c$  in the y-axis. The conversion loss value is represented with a colour bar. The second one shows the 3 dB bandwidth of the detector, where each element of the  $f_c$  -  $f_{sb}$  matrix is painted on white if that  $f_{sb}$  is within the 3 dB bandwidth or black if it is not.

Figure 4.28a depicts the simulated ED1's conversion loss results, obtaining a minimum of  $5.3\,\mathrm{dB}$ . The ED1's  $3\,\mathrm{dB}$  bandwidth results, shown in figure 4.28b, can

be divided into three areas: the lower, middle and upper side W-Band.

For carrier frequencies up to 81 GHz and  $f_{sb}$  < 5 GHz, the conversion loss remains below 8 dB. When  $f_{sb}$  is higher than 6 GHz, the conversion loss increases rapidly. Moreover, the waveguide cut-off frequency can be reached by the lower sideband  $(f_c - f_{sb})$  for sufficiently high  $f_{sb}$ , which result into a low conversion loss value.

In the W-band central frequencies the conversion loss is in the range of 5 dB to 12 dB for  $f_{sb}$  frequencies up to 15 GHz, furthermore, the ED's 3 dB bandwidth increases considerably, up to 20 GHz for  $f_c = 100$  GHz. The conversion loss reaches its lowest values between 91 GHz and 95 GHz, which is the ED's design frequency.

For carrier frequencies higher than  $102 \,\text{GHz}$ , the conversion loss starts to increase for all  $f_{sb}$  frequencies while remaining flat, therefore, the  $3 \,\text{dB}$  video bandwidth is still broad, but the ED1's sensitivity is reduced considerably due to the lower ED1's frequency response.

From the simulation results displayed in figure 4.28a, we can expect the ED1 to be able to demodulate ASK signals up to 20 Gbit/s, finding its best sensitivity in the W-band central frequencies, which is the ED1's design frequency.

The conversion loss of ED2 is shown in figure 4.28c, obtaining a minimum of 7.6 dB. Similar as with the frequency response, broadening ED2's input and output matching and introducing more losses in its HW to MSL transition increases ED2's minimum conversion loss with respect to ED1. The ED2's 3 dB bandwidth is depicted in figure 4.28d, where the results can be divided into three areas, attending to  $f_c$ : the lower, middle and upper side of the W-Band.

In the lower W-band, the video bandwidth has been increased in comparison to ED1, up to 13 GHz for  $f_c < 81$  GHz. In this region the conversion loss remains below 10 dB. The reason for increasing the video bandwidth in this  $f_c$  range is that in the CELTA demonstrator meeting held in December 2017, the final requirements for the demonstrator were agreed, choosing to place the  $f_c$  in the range of 80 GHz - 85 GHz. During ED1's design phase this feature was unknown, and therefore the video bandwidth was optimized for the central W-band frequencies.

In the W-band central frequencies the conversion loss is in the range of 8 dB to 12 dB for  $f_{\rm sb} < 16$  GHz. The ED2's 3 dB video bandwidth increases up to 22 GHz for  $f_c = 94$  GHz, which is an increment of 7 GHz compared to ED1 in this  $f_c$  range. The conversion loss value decreases in this  $f_c$  region because the frequency response has a valley in this region.

In the range of  $f_c = 98 \,\text{GHz}$  to  $104 \,\text{GHz}$ , the ED's  $3 \,\text{dB}$  bandwidth is reduced to  $18 \,\text{GHz}$ , and down to  $12 \,\text{GHz}$  for  $f_c = 110 \,\text{GHz}$ . Although this  $3 \,\text{dB}$  bandwidth may seem lower than in the ED1, the conversion loss is kept in the range of  $9 \,\text{dB}$  to  $12 \,\text{dB}$  in the upper W-band carrier frequencies, while in the ED1 the conversion loss increased to the range of  $10 \,\text{dB}$  to  $17 \,\text{dB}$ . The reason for maintaining this performance is the broader input bandwidth from the ED2, which, in comparison with the roll-off found at the upper W-band carrier frequencies in ED1, results on a broader video bandwidth.

From the simulation results displayed in figure 4.28c, we can expect that the ED2 will be able to demodulate ASK signals up to 25 Gbit/s. The ED2's sensitivity is flat

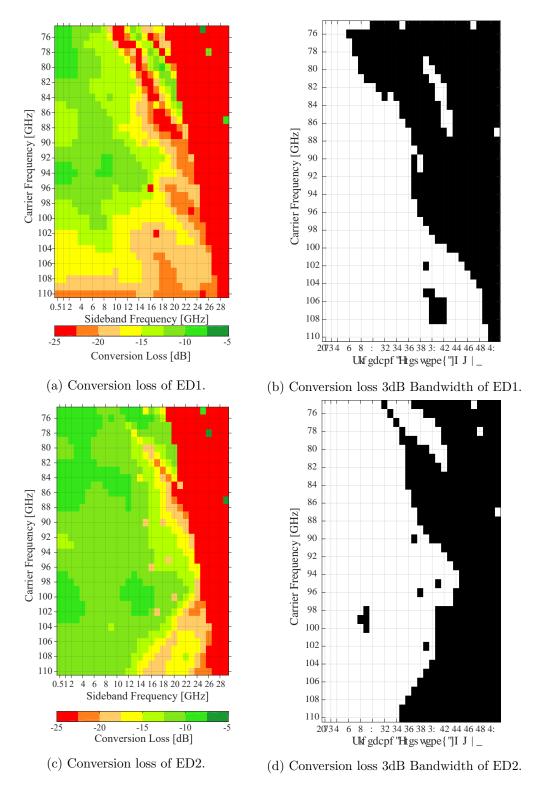


Figure 4.28: Simulated conversion loss results of the W-band detectors.

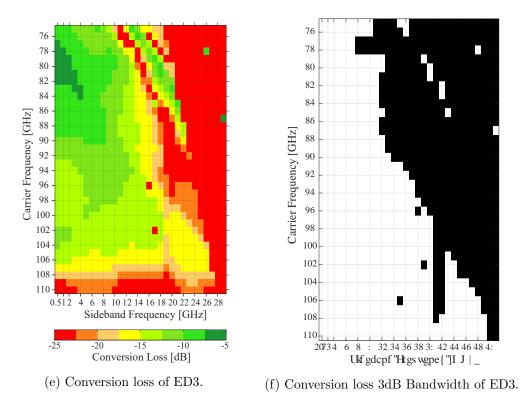


Figure 4.28: Simulated conversion loss results of the W-band detectors.

and uniform for every  $f_c$  within the full W-band when  $f_{sb} < 12 \,\text{GHz}$ .

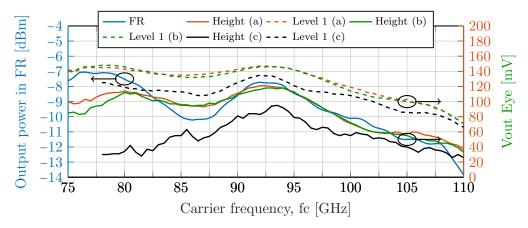
The conversion loss of ED3 is shown in figure 4.28e, obtaining a minimum of 6.6 dB. Figure 4.28f shows the ED's 3 dB bandwidth. The ED3's 3 dB bandwidth results can be divided into two areas, attending to  $f_c$ : the lower and the upper W-Band halves.

When fed with ASK signals having carrier frequencies below 91 GHz, ED3 provides up to 10 GHz of 3 dB-video bandwidth. In this frequency region the conversion loss remains below 10 dB.

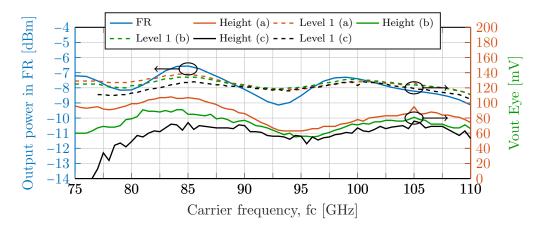
For the upper W-band carrier frequencies up to  $108\,\text{GHz}$ , the conversion loss remains in the range of  $15\,\text{dB}$ , while the ED's  $3\,\text{dB}$ -video bandwidth increases up to  $18\,\text{GHz}$ . For  $f_c$  above  $108\,\text{GHz}$  the conversion loss increases considerably, up to  $25\,\text{dB}$ .

#### **Data detection Measurement**

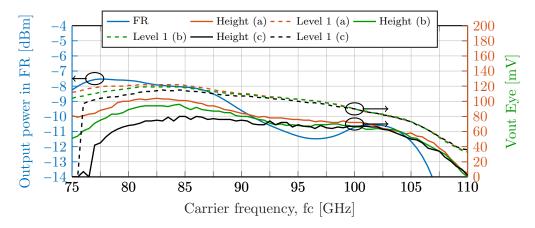
In this benchmark, similarly as with the UWB EDs, the detectors are fed with an ASK modulated signal with 0 dBm input power at carrier frequencies between 75 GHz and 110 GHz, and three bitrates: 15 Gbit/s, 20 Gbit/s and 25 Gbit/s, obtaining the demodulated signal's eye diagram, which is then analyzed to check the EDs' performance. Figure 4.29 shows for each detector its height and Level 1 (L1) at each bitrate (15 Gbit/s, 20 Gbit/s and 25 Gbit/s) and its frequency response in blue.



(a) Simulated frequency response, eye diagram, height and Level 1 (L1) of the ED1 for bitrate (a) 15 Gbit/s [Bla+18b]; (b) 20 Gbit/s; (c) 25 Gbit/sfor 0 dBm input power.



(b) Simulated frequency response, eye diagram, height and Level 1 (L1) of the ED2 for bitrate (a)  $15\,\mathrm{Gbit/s}$ ; (b)  $20\,\mathrm{Gbit/s}$ ; (c)  $25\,\mathrm{Gbit/s}$  for  $0\,\mathrm{dBm}$  input power.



(c) Simulated frequency response, eye diagram, height and Level 1 (L1) of the ED3 for bitrate (a)  $15\,\mathrm{Gbit/s}$ ; (b)  $20\,\mathrm{Gbit/s}$ ; (c)  $25\,\mathrm{Gbit/sfor}$   $0\,\mathrm{dBm}$  input power.

Figure 4.29: Simulated frequency response and eye diagram of the W-band EDs.

Figure 4.29a shows that with ED1's a successful demodulation is possible for 15 Gbit/s, 20 Gbit/s and 25 Gbit/s. The best performance for the three bitrates is achieved for carrier frequencies between 90 GHz and 95 GHz, i.e. the ED1's design frequency, where the phase balance bandwidth is optimal, as shown in figure 4.8.

In the lower W-band half, the eye diagrams' heights decrease for the three bitrates when  $f_c$  is set at a frequency where the frequency response reaches a minimum. Moreover, below 85 GHz, 90 GHz or 95 GHz carrier frequencies, the lower frequency region of the 15 Gbit/s, 20 Gbit/s and 25 Gbit/s ASK signals respectively falls outside the W-band. At a certain point, the ASK signals' spectrum region falling below the WR-10 waveguide 59 GHz cut-off frequency [Poz12] is not transmitted through the waveguide, it will not reach the microstrip and hence, it will not be downconverted, which shutters the demodulated eye diagram. Since the frequency response gets a maximum around 75 GHz or 80 GHz, the power loss from not downconverting part of the ASK signal is slightly compensated, therefore the height and Level 1 for 15 Gbit/s or 20 Gbit/s is flat in the 75 GHz - 95 GHz frequency region.

Figure 4.29b shows that ED2's best performance for 15 Gbit/s and 20 Gbit/s is found when  $f_c$  is set to 85 GHz, corresponding with a maximum in the frequency response and CELTA beamformer demonstrator's goal. In the W-band central frequencies (90 GHz - 97 GHz), the performance is slightly reduced due to the lower frequency response in this frequency region. Nonetheless, since the optimum phase balance bandwidth is found within this frequency region as shown in figure 4.22, the ED2's performance in this benchmark does not decay as much as in the frequency response benchmark. In the upper W-band region, the ED2 is also able to demodulate 15 Gbit/s and 20 Gbit/s ASK signals. When the bitrate is increases to 25 Gbit/s, ED2 offers a flat performance for carrier frequencies between 80 GHz and 110 GHz.

Figure 4.29c depicts the results of ED3. The performance is similar for 15 Gbit/s and 20 Gbit/s bitrates and is uniform up to 105 GHz carrier frequencies, where it decays due to the lower ED3's frequency response. Analogous to ED1, the optimum phase balance bandwidth is found within this frequency region between 89.2 GHz and 95.1 GHz as shown in figure 4.8, therefore, even if the frequency response decays in this frequency region, the eye's height does not shrinks as much, since there are less distortion coming from the output fundamental harmonic. When increasing the bitrate to 25 Gbit/s, the working frequency range narrows down and the eye closes for carrier frequencies below 80 GHz.

If a small part of the ASK signal frequency components are not downconverted in any of the three detectors, either because they fall below the 59 GHz waveguide cut-off frequency [Poz12], or above the input bandwidth of the detector (100 GHz for ED1, 110 GHz for ED2 and 104 GHz for ED3), the eye diagram will be open as long as most of the ASK signal power is demodulated (94% of an ASK signal's power is contained in the 80% of its bandwidth centred around the carrier frequency [TS86]). Besides, since an ASK signal is symmetric with respect to the carrier frequency, therefore, when following a single sideband demodulation (SSB) scheme, we only need to downconvert one of the two ASK signal's halves to obtain a high quality eye diagram, suffering only from an output power penalty [OWH96].

Table 4.3: Design features and simulation results from the W-band detectors presented in this dissertation.

	Substrate	Input BW [GHz]	Video BW [GHz]	Min. CL [dB]
ED1	Rogers 5880	25	20	5.3
ED2	Fused Silica	35	25	7.6
ED3	Rogers $5880$	29	18	6.6

Moreover, it must be taken into account that the next mode's cut-off frequency in a rectangular WR-10 waveguide is 118 GHz [Poz12]. Frequencies higher than 118 GHz will excite higher order modes, therefore, we should avoid using frequencies above 118 GHz. When connected to an antenna, the antenna filters the undesired higher frequencies, therefore frequencies above 118 GHz will not be an issue in the wireless system.

For 25 Gbit/s, the ASK signal spectrum falls outside either the W-band or the waveguide's cut-off frequency much faster than with the other two bitrates in the three detectors, therefore the eye diagrams close much faster than with the other two bitrates. Nevertheless the Level 1 is maintained in the three detectors since it is directly related with the frequency response.

#### Summary and discussion

This section has described the design of three envelope detectors. It has also shown their simulation results, summarised in table 4.3, following the three benchmarks described in 3.1 to test their performance. The detectors prove the scalability in frequency of the architecture presented in section 3.2.2, which combines the functionality of a Balun and, simultaneously, rectifies the input ASK signal [Bla+17]. The simulation results prove that the three detectors fulfil all the CELTA project's requirements.

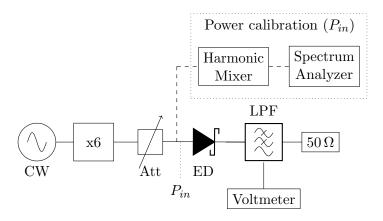
## 4.5 Envelope detection benchmark measurements

This section presents the experiments accomplished to evaluate the performance from ED1, which will be tested using the three benchmarks. Since it was not possible to finish the manufacture of ED2 and ED3, experimental results can not be presented. In this section, the data detection benchmark is performed through a Bit Error Ratio (BER) measurement, instead of measuring the height and Level 1 from the demodulated signal, analogous to the UWB envelope detectors.

#### Frequency response

When evaluating ED1, the frequency response was measured using two setups. Figure 4.30 depicts the one used at the Technical University of Denmark (DTU) and

figure 4.31 the one from the TU Darmstadt (TUDa).



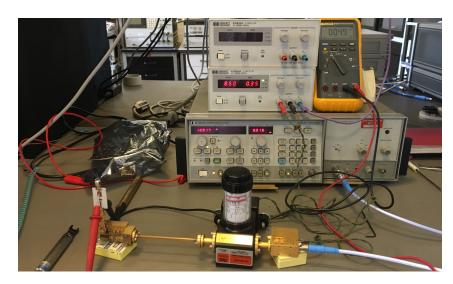


Figure 4.30: W-band frequency response experimental setup at DTU.

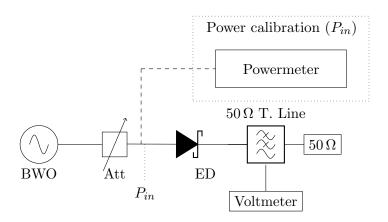
In the setup from DTU, an RF tone at lower frequency (12 GHz to 18.33 GHz) produced by a continuous wave's (CW), is upconverted to W-band with a 6x multiplier and fed into the ED1. A power calibration at the attenuator's output was needed to verify the fed power to the ED1. At the ED1's output, a low pass filter terminated in a  $50\,\Omega$  load is placed in order to measure the ED's output voltage without damaging neither the ED's PCB board, nor the Schottky diodes when the connectors contact the filter's microstrip. The ED's input signal's power was set to  $-6\,\mathrm{dBm}$  and  $-18\,\mathrm{dBm}$  in  $4\,\mathrm{dB}$  steps. The reason for not reaching  $0\,\mathrm{dBm}$  as in simulations is that ACST recommended not to feed the diodes with more than  $-10\,\mathrm{dBm}$  input power. This setup from DTU was only used to test ED1

The simulation results plotted in this section are the ones that use ADS Momentum to model the ED's input transmission line. In [Bla+19], we compared the experimental results with the ones where the transmission line is simulated using CST Microwave

Studio, which section 4.1.3 claimed that it was the wrong approach.

Figure 4.32a depicts the frequency response experimental results measured at DTU. ED1 provides 15 GHz of 3 dB bandwidth, from 75 GHz to 90 GHz for a -6 dBm input power. When fed with lower input powers, the ED1's input bandwidth is narrowed to 5 GHz - 10 GHz. The CELTA beamformer demonstrator's requirements requested 5 GHz to 10 GHz of input bandwidth, which is fulfilled experimentally at every input power from -6 dBm to -14 dBm. For a -18 dBm input power the input bandwidth accounts for 4 GHz.

From 75 GHz to 90 GHz, experimental results provide 7 dB more output power than simulations for every frequency. Above 92.5 GHz, both results match for every frequency and input power. In the full W-band, the frequency response features the same shape for every input signal's power in simulation and experimental results, suffering only of a power penalty in the ED's output power in the lower W-band, with no other effects deteriorating the demodulated signal. The manufactured ED1 provides 20 GHz of input bandwidth within W-band [Bla+19].



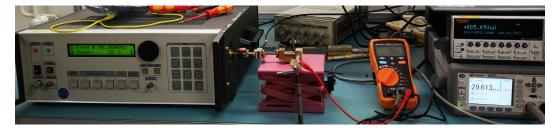


Figure 4.31: W-band frequency response experimental setup at TU Darmstadt.

We wanted to replicate the results using the equipment available at TUDa using the setup depicted in figure 4.31, where ED2 and ED3 would be tested as well. In this new setup we employed a powermeter to measure the input power to the ED instead of the harmonic mixer and spectrum analyser combination. Moreover, the W-band signal was directly generated with a Backward Wave Oscillator (BWO) instead of using a CW source connected to a multiplier. The setup also has a voltage controlled

variable attenuator [ELV] which sets the ED's input power. This time we decided to use a  $50\,\Omega$  microstrip transmission line terminated in a  $50\,\Omega$  load with a small pin to connect the voltmeter, instead of a filter, which for DC measurements is equivalent.

The ED1's input signal's power was set to  $-6\,\mathrm{dBm}$  and  $-18\,\mathrm{dBm}$  in  $4\,\mathrm{dB}$  steps, to be able to compare these results with the ones obtained at DTU. Figure 4.32b compares the measured DC output power in dashed lines with the simulation results in solid lines for each signal power. From  $80\,\mathrm{GHz}$  to  $107.5\,\mathrm{GHz}$  simulation and experimental results match thoroughly slightly differing only at some frequency for the  $-18\,\mathrm{dBm}$  input power tone. From  $75\,\mathrm{GHz}$  to  $80\,\mathrm{GHz}$  experimental results are  $5\,\mathrm{dB}$  -  $10\,\mathrm{dB}$  lower than simulations, but they shape a flatter frequency response. At  $110\,\mathrm{GHz}$  the experimental output power is  $5\,\mathrm{dB}$  higher than in simulations.

According to these new measurements, the manufactured ED1 provides 20 GHz of input bandwidth within W-band as well, and fulfils the CELTA beamformer demonstrator's requirements. Moreover, the frequency response is flatter than in the experiment performed at DTU.

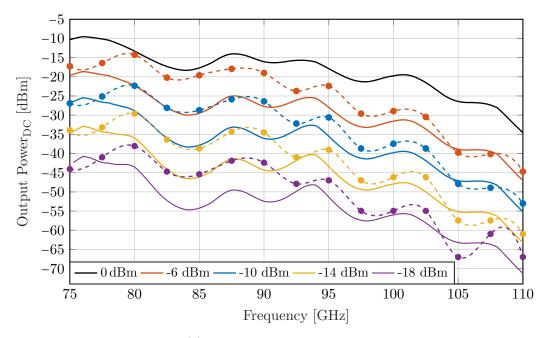
The two measurement results presented in figure 4.32 agree in the upper W-band half, presenting a mismatch only in the lower half. We believe that the experiment accomplished at TUDa is more accurate than the one from DTU. Instead of using an harmonic mixer and a spectrum analyser, which can introduce more uncertainty when calculating the input power, we used a digital power meter. In addition, we expect the TUDa's source output power to be more stable than the one from DTU, even though in [Bla+19] we presented the results from DTU.

In section 3.4, the signal was generated by mixing a data signal from a PPG with a carrier using a mixer. The resulting signal was fed into the UWB envelope detectors to perform the data detection benchmark.

When transmitting ASK signals with carriers at W-band, there are several ways to generate the RF signal. Three of the most used are: electronic generation or upconversion using multiplieres, which has been used in the frequency response setup at DTU or with mixers and oscillators, which is the approach followed in section 3.4 [Kob+99; Xu+15; CAZ15; San+10]; using non-linear optics [ZX10]; and employing photomixing [Mor+17; Rom+16b; Wun+14]. Since this dissertation's focus is not the W-band signal generation, but the design, manufacture and test of a W-band envelope detector; we decided to use the photomixing approach in the conversion loss and data detection experiments, since the equipment we needed for the experiments was available at TU/e during the author's secondment in 2018.

Figures 4.33 and 4.34 show the experimental setup that has been used to perform the conversion loss and the data detection experiments, consisting of optical and electrical components.

The output of an External Cavity Laser (ECL) is modulated using a Mach-Zehnder Modulator (MZM) driven with a tone with a  $f_c/2$  frequency from a Vector Signal Generator (VSG) while it is biased at its minimum transmission point, obtaining two optical tones with a suppressed carrier, which are separated by a frequency distance of  $f_c$ . Both tones are cranked up and separated by an Erbium Doped Fibre Amplifier (EDFA) and Wavelength Selective Switch (WSS) respectively. One of the tones is



(a) Results measured at DTU.

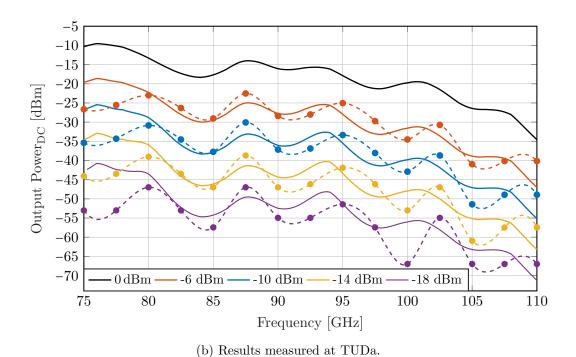


Figure 4.32: Frequency response simulation (solid) and experimental (dashed) results from  $P_{in} = -6 \, \text{dBm}$  to  $-18 \, \text{dBm}$ .

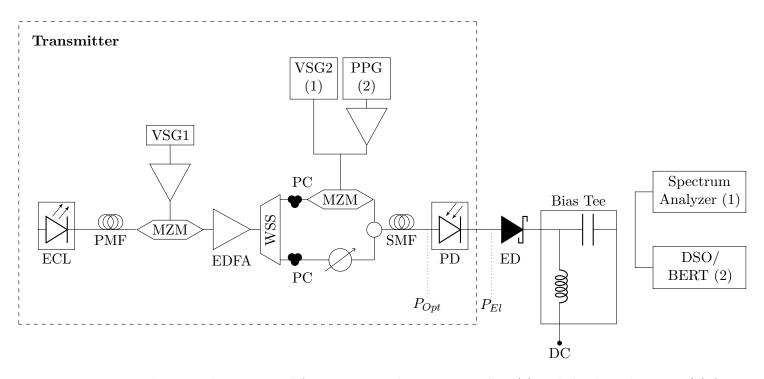


Figure 4.33: Experimental setup schematic used for measuring the conversion loss (a) and the data detection (b) from ED1.

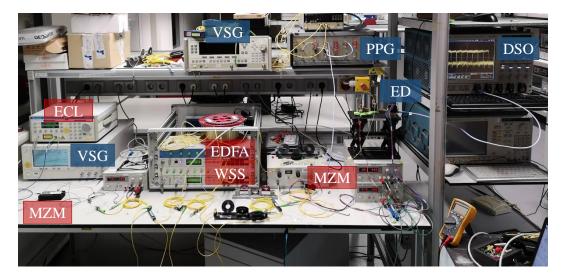


Figure 4.34: Experimental setup used for conversion loss and data detection benchmarks from ED1.

modulated with a second vector signal generator when evaluating the conversion loss benchmark or with a Pulse Pattern Generator's (PPG) output, which provides a Non-Return-to-Zero (NRZ) signal for the data detection benchmark. The NRZ signal is based on a Pseudo-Random Bit Sequence (PRBS 31) that has a length equal to  $2^{31}$ -1 bits. At the output of the PPG a driver amplifier is connected providing a boost to the electrical signal in order to achieve enough voltage swing to drive the MZM [Bla+19].

Between the wavelength selective switch's output branch and the second MZM, a Polarisation Controller (PC) is responsible for the polarisation stability of the optical signal at the input and the optical power maximisation at the output of the MZM. One Variable Attenuator (VOA), connected to the second wavelength selective switch's output through a polarisation controlled fibre, regulates the power of the Co-Propagating Tone (CT), that is combined with the Optical Signal (OS) from the MZM's output using a 3 dB coupler. The second polarisation controller ensured the polarisation coherence between the Optical Signal and Co-Propagating Tone maximising the PhotoDiode's (PD) output power. The combination of both signals is fed into a second EDFA which computer-controls the signal power at the 2 km optical fibre span's input. The fibre's termination is connected to a high-speed photodiode [Fin14], featuring 90 GHz of bandwidth, generates the electrical RF signal at W-band through heterodyne beating. The generated RF power,  $P_{El}$ , is directly proportional to  $P_{Opt}$  and depends on the PD's responsivity (0.5 A/W).

The photodiode's output is then connected through a coax to waveguide adaptor to the envelope detector. At a next step, the downconverted signal goes through a bias tee which removes its DC component and provides a DC path at the envelope detector's output. Finally, the demodulated baseband signal is fed into a spectrum analyser in the conversion loss benchmark or in the data detection to a Bit Error Ratio Tester (BERT) that measures the BER through a 29 dB power amplifier due to the low BERT sensitivity. The clock is directly synchronised to the BERT from the PPG because the goal of the data detection benchmark is to characterise the ED1 in a communication system.

#### Conversion loss

The Conversion Loss, CL, is measured using the setup from figure 4.33. The ASK modulated electrical signal that is fed to the ED1 is composed of a  $-17 \,\mathrm{dBm}$  carrier with frequency  $f_c$ , which is swept from 75 GHz to 88 GHz, modulated by two  $-37 \,\mathrm{dBm}$  sidebands swept from  $f_{sb} = 0.5 \,\mathrm{GHz}$  to 19 GHz, placed at  $f_c \pm f_{sb}$ , similar to section 4.4. The carrier frequency,  $f_c$ , was swept from 75 GHz to 88 GHz because the first MZM placed after the ECL features a 40 GHz bandwidth, which produces the two optical tones separated  $f_c$  GHz, as shown in figure 4.33. As shown in chapter 3, an ED's conversion loss accounts for the difference between the obtained downconverted signal at  $f_{sb}$  and the input power at  $f_c \pm f_{sb}$ .

Figure 4.35a depicts the experimental conversion loss results from ED1 and figure 4.35b its 3dB bandwidth. The y- and x-axis represent the ASK input signal's carrier frequency,  $f_c$ , and its sideband frequency,  $f_{sb}$  respectively. The conversion loss value is quantified with a colour bar, and each element from the 3dB bandwidth matrix is painted on white if that  $f_{sb}$  is within the 3dB bandwidth or black if it is not.

In figure 4.35a we can distinguish three well limited regions:  $f_c$  below 78 GHz, the central region for  $f_c$  between 78 GHz and 83 GHz, and  $f_c$  above 83 GHz.

ED1's minimum conversion loss value is 11.1 dB, achieved for the carrier frequency range from 78 GHz to 83 GHz, obtaining 2 GHz of 3 dB video bandwidth within this  $f_c$  range, due to the low conversion loss for  $f_{sb}$  < 2 GHz. For carrier frequencies below 78 GHz, the video bandwidth increases up to 4 GHz because the ED1 provides a higher conversion loss than in the 78 GHz to 83 GHz  $f_c$  range for low  $f_{sb}$  frequencies. When  $f_c$  is above 83 GHz, the 3 dB video bandwidth increases up to 6 GHz for  $f_c$  = 86 GHz, since the conversion loss at  $f_{sb}$  < 2 GHz increases as well. The main reason for this conversion loss increment can be found in figure 4.32, where the ED's experimental frequency response presents a bigger roll-off than expected for frequencies higher than 90 GHz, which leads to a loss of output power and an increment of the conversion loss when the ASK carrier or any of the sidebands fall above 90 GHz.

In summary, ED1 features a conversion loss below 24 dB for  $f_{sb}$  below 16 GHz in the full measured  $f_c$  range (75 GHz - 88 GHz), except for  $f_{sb} = 7$  GHz and 8 GHz at  $f_c = 81$  GHz and 82 GHz [Bla+19]. The experimental strict 3 dB video bandwidth is between 2 GHz and 6 GHz, finding a maximum at  $f_c = 86$  GHz.

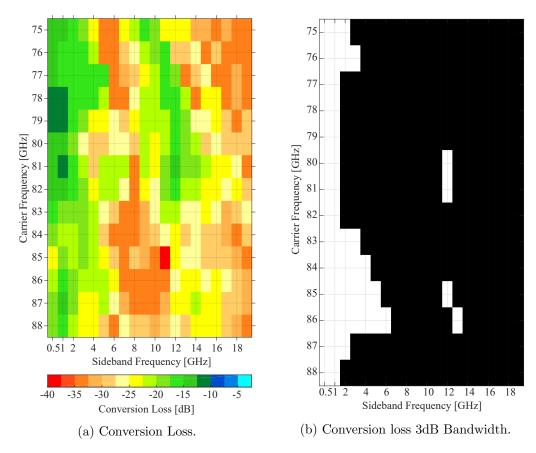


Figure 4.35: ED1 experimental Conversion Loss.

#### Data detection

Section 4.4 analyzed the ED1's performance through simulations when demodulating an input signal at 15 Gbit/s, 20 Gbit/s and 25 Gbit/s at carrier frequencies between 75 GHz and 110 GHz measuring the eye openness and its Level 1. In this section, similar to section 3.4, we measure the Bit Error Ratio (BER) of the demodulated signal, instead of analysing the eye diagram, which is the ratio between the number of bit errors and the number of transferred bits. The BER result can be classified into three regions: error free (-Log(BER) > 9), meaning that the demodulation has been successful; error free with 7% overhead forward error correction (FEC) [CC81; ITU04] (3 < -Log(BER) < 9), where the information can still be retrieved; and failure (-Log(BER) < 3).

Figures 4.34 and 4.33 show the setup used to measure the BER in real time, which is similar to the one used to measure the conversion loss in the previous section. When measuring the BER, we substituted the second Vector Signal Generator with a Pulse Pattern Generator (PPG) and the spectrum analyser with a BER tester (BERT), allowing to run real-time BER measurements. The ASK input signal's

carrier frequency was swept from 78 GHz to 92 GHz and its power ( $P_{El}$  in figure 4.33) from -27 dBm to -7 dBm.

The results are depicted in figure 4.36 showing the BER vs electrical input power to the ED1  $(P_{El})$  and bitrate. On the right side of the figure, the colorbar sorts the BER into error free, with BER >  $10^{-9}$  coloured in green; in orange and yellow when error free demodulation is possible using a 7% overhead Forward Error Correction (FEC) [ITU04], i.e. BER >  $10^{-3}$  and a detection with errors when BER <  $10^{-3}$  painted in red.

The ED1 demodulates ASK signals up to 14 Gbit/s with  $f_c = 90$  GHz and 92 GHz at a BER of  $2 \cdot 10^{-5}$  and  $8.4 \cdot 10^{-7}$  respectively. Moreover, error free demodulation is possible for bitrates up to 12 Gbit/s with  $f_c = 82$  GHz, which is the  $f_c$  that offers the best sensitivity. For every other carrier frequency, demodulation is possible up to 10 Gbit/s using FEC.

These results agree with the previous ones from figures 4.32 and 4.35. The 82 GHz carrier frequency provides the flattest and broadest video bandwidth in figure 4.35, therefore the ED1 is able to demodulate error free the highest bitrate at this carrier frequency. Likewise, carrier frequencies with lower video bandwidth lead to lower demodulation bitrates.

Similarly, the frequency response results from figure 4.32 are directly related with the ED1's sensitivity from figure 4.36. For  $f_c = 78 \,\text{GHz}$  and  $80 \,\text{GHz}$ , ED1 features its highest FR, therefore, it also achieves the best sensitivity at these  $f_c$ 's when demodulating  $4 \,\text{Gbit/s}$  ASK signals as shown in figure 4.36. Nevertheless, due to ED1's lower video bandwidth at these  $f_c$ 's, the maximum demodulated bitrate is limited.

Although error free transmission is not reached for  $f_c = 90\,\mathrm{GHz}$  and 92 GHz due to the lower output power that ED1 delivers as depicted in the frequency response results from figure 4.32, the ED1 achieved its highest demodulation bitrates for these two carrier frequencies because it is design to offer its best performance in the W-band central frequencies [Bla+18b]. At these  $f_c$ 's, the ED1's phase balance bandwidth is optimal, leading to a cancellation of the fundamental harmonic spurious at its output. Section 4.1.3 justified why ED1 provides a lower output power when  $f_c$  is within the central W-band, and therefore error free cannot be reached. Boosting the ED1's frequency response would lead to error free demodulation for these  $f_c$ 's, and could allow to increase the maximum demodulated bitrate.

In contrast, lower  $f_c$ 's without an adequate phase balance bandwidth work following a single ended architecture, and therefore they are only able to demodulate lower bitrates. Since these  $f_c$ 's have a greater FR, error free demodulation is possible. These results confirm the statements from section 2.4 proving experimentally the benefits of this architecture in comparison with a single ended one.

The PD used in this experiment provides 90 GHz of 3 dB bandwidth [Fin14], therefore, it should be considered that this setup's restriction may limit the quality of the W-band signal fed into the ED1 for the higher  $f_c$ 's, since the upper half of the signal will present lower power at ED1's input than the lower half due to the photodiode's roll-off.

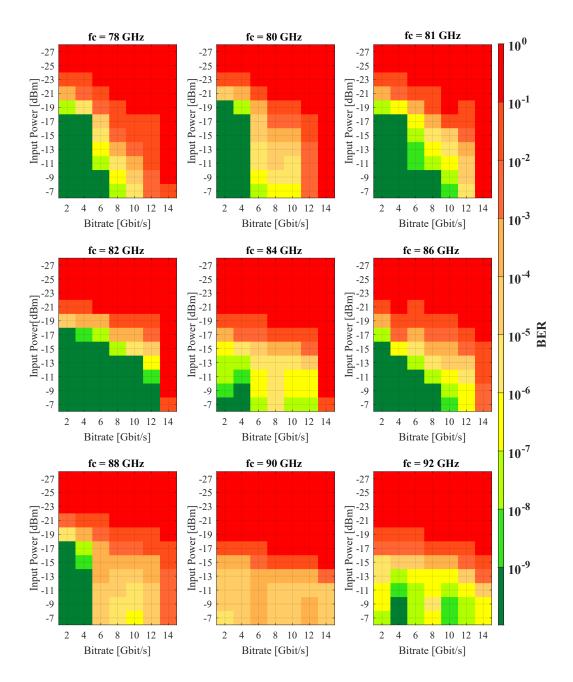


Figure 4.36: Experimental BER results for carrier frequencies between 78 GHz and 92 GHz, data rates between 2 Gbit/s to 14 Gbit/s and input powers -27 dBm and -7 dBm [Bla+19].

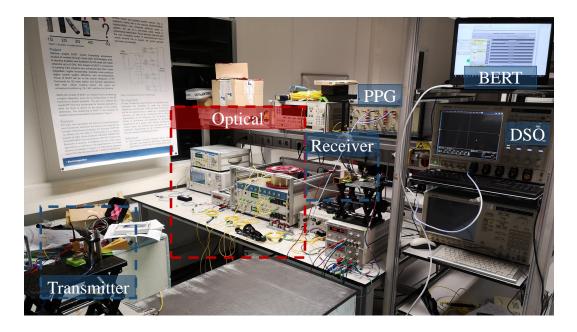


Figure 4.37: Experimental wireless setup and link budget.

# 4.6 Wireless communication experiment

Once we have tested the stand alone ED1's performance, we wanted to evaluate its behaviour in the proposed wireless communication scenario, which is the final goal of the beamformer CELTA demonstrator. ED2 and ED3 were not tested within the CELTA demonstrator because they had not been manufactured during the experiment performed during TU/e secondment.

#### Wireless transmission with horn antennas

We tested ED1's performance in a point to point wireless communication system using the setup shown in figure 4.37 with the schematic depicted in figure 4.38. We decided to perform only the data detection benchmark through a real time signal transmission, since due to time constraints, the frequency response and conversion loss benchmarks could not be tested. The transmitter schematic used in this experiment is the same one from figure 4.34 for the data detection benchmark, i.e. using the PPG. The W-band signal is generated at the PD's output through heterodyne beating and transmitted after being amplified with a 10 dB gain medium power amplifier (MPA) through a pair of horn antennas with 24 dBi gain each.

At the receiver side the signal is amplified with a 22 dB gain Low Noise Amplifier (LNA) before feeding the W-band ASK signal to the ED1. Similarly as in the back to back experiment, the ED1's output is connected to the BERT through a bias tee and a baseband amplifier.

Since the wireless experiment is exclusively a validation before using beamformer

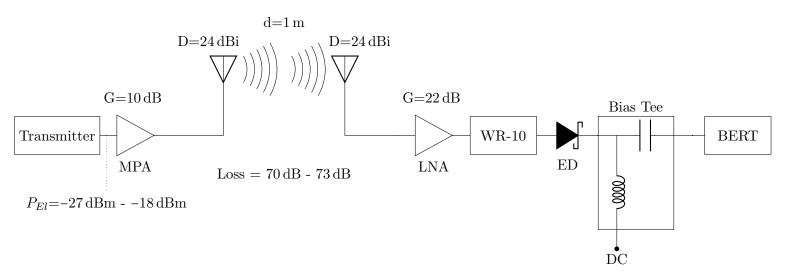


Figure 4.38: Experimental wireless setup schematic.

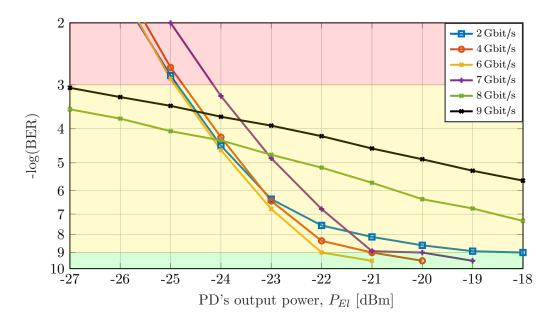


Figure 4.39: Experimental BER results the wireless experiment with ED1.

antennas, which were not available at the moment of the experiment, and due to the time constraints to perform all the W-band experiments from this chapter, we decided to test the ED1 with only one carrier frequency. Considering that the beamformer demonstrator carrier frequency was agreed to be in the range of  $80\,\mathrm{GHz}$  -  $85\,\mathrm{GHz}$ , and after evaluating the best compromise between sensitivity and demodulated bitrate from figure 4.36, we decided to test ED1 with an ASK signal with  $f_c = 82\,\mathrm{GHz}$ , transmitted through 1 m wireless distance. Testing more carrier frequencies could have been possible with more time, but due to equipment availability, it was not possible. Nonetheless, the results would not provide a better understanding of the ED1's performance, thoroughly analyzed in section 4.5, which is the goal of this dissertation.

Figure 4.39 shows the BER vs the electrical power at the photodiode's output  $(P_{El})$  and table 4.4 shows  $P_{El}$ 's relation with the ED1's input power. Error free demodulation is achieved for bitrates up to 7 Gbit/s. Moreover, it is possible to demodulate ASK signals up to 9 Gbit/s with a BER of  $2.4 \cdot 10^{-6}$ . In addition, it can be presumed that increasing the signal's power at the transmitter would allow to reach error free for 9 Gbit/s.

With this experiment, we conclude the suitability of the ED1 to work in the

Table 4.4: Relation between PD's output and ED1's input powers.

Dt [ ]		_				-22				
ED's Input power [dBm]	-15	-14	-13	-12	-11	-10	-9	-8	-7	-6

CELTA beamformer demonstrator. Further tests can be accomplished to introduce the beamforming scheme in the wireless system described in chapter 1, e.g. introducing the LC antenna in the receiver instead of the current horn antenna or substituting the current transmitter with the beamformer photonic chip. These modifications will not change the ED1's performance, nonetheless they have not been introduced because the LC antenna and photonic chip had not been manufactured during the author's secondment at TUE.

# 4.7 Analysis and comparison

This chapter has described the design of three W-band envelope detectors and has shown the simulation results following the three benchmarks described in 3.1 to test their performance. Moreover, ED1 has been experimentally characterised in section 4.5. This section compares the simulation and experimental results of ED1 and analyses the statements from section 4.1.3.

### Frequency response

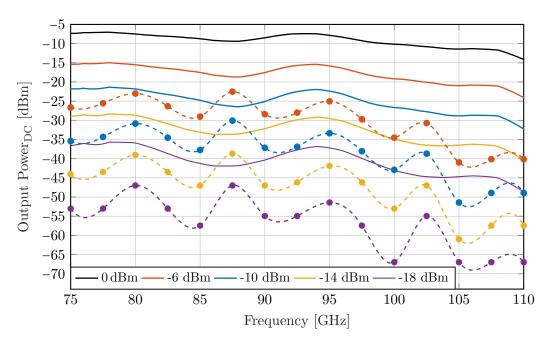
Figure 4.40 compares the frequency response simulation results when the input transmission line is simulated either using CST Microwave Studio (a) or ADS Momentum (b) with the experimental results obtained at TU Darmstadt, presented in figure 4.32. The ED's input signal's power was set between  $-6\,\mathrm{dBm}$  and  $-18\,\mathrm{dBm}$  in 4 dB steps. The experimentally measured DC output power is depicted using dashed lines in figure 4.40 and compared with the simulation results in solid lines for each signal power. The WR-10 waveguide to dielectric filled rectangular waveguide (DFRW) transition was simulated in CST for both scenarios.

When using the input transmission line model from CST Microwave Studio, there is a big difference between simulation and experimental results as shown in figure 4.40a. However, simulating the input transmission line model in ADS Momentum leads to the simulation results displayed in figure 4.40b, which match thoroughly with the experimental results within the full W-band.

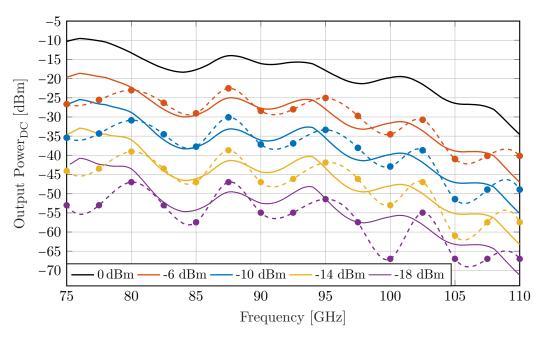
### Conversion loss

Figure 4.41a shows a zoom of figure 4.28a, which depicts the simulated conversion loss using harmonic balance analysis in ADS, where the input transmission line is simulated using CST Microwave Studio. Figure 4.41b results from comparing the simulation (figure 4.41a) and experimental results (figure 4.35a), by subtracting both conversion loss value matrices. Figure 4.41b's analysis can be found in [Bla+19] and is skipped in this dissertation since section 4.1.3 concluded that CST provided wrong simulation results to the ED1's input transmission line.

Figure 4.41c depicts the simulated conversion loss of ED1 when modelling the input transmission line with ADS Momentum, as presented in section 4.1.3. Similarly



(a) Input transmission line simulated in CST Microwave Studio.



(b) Input transmission line simulated in ADS Momentum.

Figure 4.40: Frequency response of ED1: simulation (solid) and experimental (dashed) results measured at TU Darmstadt from  $P_{in}$ =-6 dBm to -18 dBm.

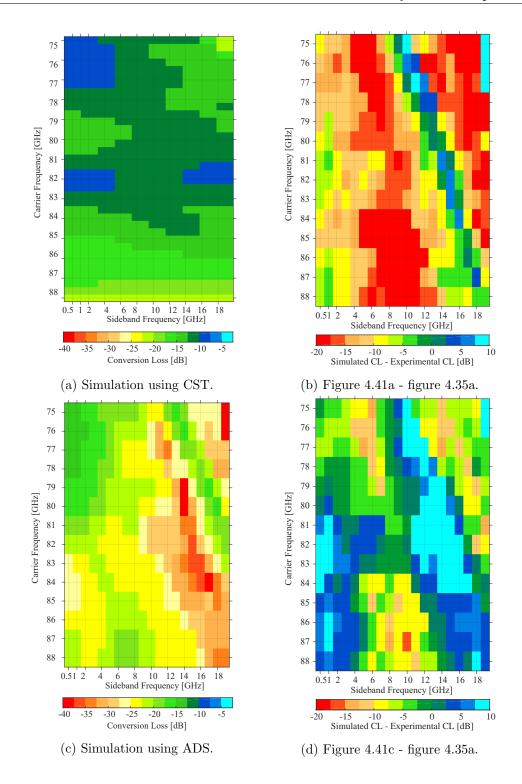


Figure 4.41: Comparison of conversion loss of ED1. Input transmission line simulated with CST Microwave Studio or ADS Momentum.

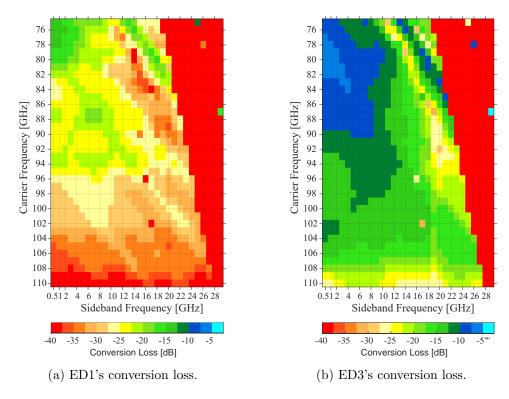


Figure 4.42: Conversion loss simulation results comparison.

as before, figure 4.41d compares these simulation results with the experimental from figure 4.35a by subtracting both conversion loss value matrices.

The results can be divided into two regions separated at  $f_c$  81 GHz. For  $f_c = 75$  GHz - 81 GHz and low  $f_{sb}$ , simulation and experimental results match thoroughly. For  $f_c = 81$  GHz - 88 GHz, experimental results show a slightly lower conversion loss than simulation's. When the lower sideband tone falls outside the W-band, i.e.  $f_{sb} > 4$  GHz for  $f_c < 79$  GHz, the simulation results from figure 4.41c are not an accurate estimation, therefore, the difference in figure 4.41d increases for those matrix elements. This mismatch is not relevant, since the frequency range outside the W-band will not be used.

While in figure 4.41b the average difference between simulation and results accounts to 11.4 dB, when using the ADS Momentum input transition line simulated model, this difference reduces to only 0.4 dB in figure 4.41d, confirming the conclusions from section 4.1.3, which stated that simulating the input transmission line to ED1 with CST instead of ADS was the wrong approach when designing ED1.

Figure 4.42a shows ED1's simulated Conversion Loss performance when its input transmission line is simulated in ADS Momentum. When comparing figures 4.42a (ED1) and 4.42b (ED3), it can be seen that the redesign version does not only provide a higher video bandwidth at the upper W-band half, but also improves the Conversion Loss in its lower half. In the previous simulation results from ED1 and

ED2, the Conversion Loss color bar minimum was set at  $-25\,\mathrm{dB}.$  Due to the higher Conversion Loss values found in  $4.42\mathrm{a},$  the colorbar range needed to be increased up to  $-40\,\mathrm{dB}.$ 

# 5 Conclusions and Outlook

# 5.1 Conclusions

The growth in the demand of wireless communication services and data rates requires the research and development of novel RF systems, leading into a migration to higher frequencies to grant broader bandwidths to end users. The beamformer demonstrator conceived in the EU CELTA project operates at W-band (75 GHz to 110 GHz) and enables high bitrate wireless indoor communications using high directive antennas and beamforming to align the antennas beams between the transmitter and receiver. Within this EU project, one transmitter and two receiver blocks are developed. The second receiver block, produced fully at TU Darmstadt is composed of a liquid crystal (LC) antenna array and a zero bias Schottky diode based envelope detector (ED) built in planar technology.

This PhD dissertation has reviewed five Schottky Diode based envelope detectors. Two of them are designed for UWB  $(3.1\,\mathrm{GHz}$  -  $10.6\,\mathrm{GHz})$  which use the Skyworks SMS7630 and SMS7621 Schottky diodes [Sky15], and three for W-band  $(75\,\mathrm{GHz}$  -  $110\,\mathrm{GHz})$  which use the 3DSF Schottky diodes from ACST GmbH [ACS].

The UWB detectors have been used to test and compare different Schottky diode based ED architectures, to later apply that knowledge to this dissertation final goal: building a W-band ED for the CELTA beamformer demonstrator. These two detectors use a balanced architecture, and they mainly differ in the method they use to obtain the balanced signal which is fed into the ED circuit. UWB1 uses an external Balun to produce the balanced signal and UWB2 combines the functionality of a Rat Race hybrid coupler Balun to obtain the balanced signal, while at the same time rectifies the input signal, suppressing the output fundamental harmonic. UWB1's and UWB2's single ended version, presented in [Cim+16], is able to demodulate up to 2.5 Gbit/s ASK modulated signals. Despite of using a bigger and more complex output low pass filter than UWB1 and UWB2, [Cim+16] does not cancel common mode noise due to its single ended architecture. UWB1 is able to demodulate up to 4 Gbit/s ASK modulated signals and provides a broad phase balance bandwidth at the cost of introducing higher losses and increasing the ED's size and cost. On the other hand, UWB2 demodulates up to 2.5 Gbit/s ASK modulated signals, provides a better sensitivity and offers a less complex, more compact, and better cost effective architecture than UWB1, therefore, we decided to use UWB2's architecture to design three W-band EDs: ED1, ED2 and ED3.

ED1 has been designed using the Rogers 5880 substrate. According to the results presented in chapter 4, ED1 experimentally provides 20 GHz of input bandwidth, a minimum conversion loss of 11 dB, and features up to 6 GHz video bandwidth.

Moreover, ED1 achieves real time error free demodulation of signals up to 12 Gbit/s using a 82 GHz carrier. Besides, for 90 GHz to 92 GHz carriers a BER below the limit for 7% overhead FEC for 14 Gbit/s signals was measured [Bla+19]. Section 4.5 shows that ED1 suffers from a roll-off in its experimental frequency response for frequencies above 92.5 GHz, which in simulation results appeared at 100 GHz. For this reason, we decided to design two additional W-band EDs. ED2 pursues to shift up the roll-of by substituting the Rogers substrate with a fused silica one, which has been tested for long time when using the 3DSF ACST Schottky diodes, and was the substrate use for their characterisation. ED3 attempts to check the roll-off's origin and shift it to higher frequencies.

ED2 uses fused silica quartz Corning 7980 as substrate. It provides 35 GHz of input and 22 GHz of video bandwidth, introducing a minimum conversion loss of 7.6 dB. These results could only be calculated in simulations, since its assembly could not be finished due to technical issues at TU Darmstadt facilities' equipment to install the connect the grounds to the detector's package.

In section 4.1.3 we proved that ED1's roll-off arises from a simulation inaccuracy from CST Microwave Studio, which has been the software used to simulate the WR-10 waveguide to microstrip transition, the microstrip taper and the  $50\,\Omega$  input transmission line to ED1 and ED2. We observed, using ADS Momentum, that ED1's microstrip taper and its  $50\,\Omega$  input transmission line provide higher frequency dependent losses than what CST Microwave Studio calculated. For this reason, we decided to design ED3, a redesigned version of ED1, where its input transmission line was shortened and shrunk with respect to ED1's, reducing the high frequency losses. We checked that CST Microwave Studio's miscalculation is negligible in ED2.

ED3 is built in Rogers 5880 and features 29 GHz of input and 18 GHz of video bandwidth, improving ED1's simulation results depicted in section 4.1.3. ED3 could be assembled, but the diodes could not be mounted, therefore, only simulation results are presented.

Recalling the state of the art analysed in the introduction, table 5.1 and figure 5.1 add the experimental results from the envelope detectors presented in this dissertation, and compares them with the previous state of the art and the goals pursued in the CELTA's beamformer demonstrator and in this dissertation. Tables 5.2 and 5.3 summarise the five envelope detectors' features, their simulation and experimental results. Comparing UWB1 and UWB2 in table 5.1 with its single ended version, [Cim+16], justifies the use of a balanced architecture for this project. Only ED1 was experimentally tested, using the frequency response and conversion loss benchmarks due to time constraints for UWB1 and UWB2, and because ED2 and ED3 were not fully mounted. Nevertheless, UWB1, UWB2 and ED1 were measured using real time data transmission measurements, i.e. the data detection benchmark.

UWB1 outperforms considerably the state of the art of UWB envelope detectors, increasing  $\Delta b$  and the demodulated bitrate. UWB2 provides the same performance as the previous best result, while it proves the feasibility of a new ED architecture introduced in [Bla+18a].

As confirmed in section 4.5, ED1 experimentally fulfils all the goals set for this

Table 5.1: UWB and W-band envelope detectors state of the art.

#	Ref	$f_c$ [GHz]	Bitrate [Gbit/s]	$\Delta \mathbf{b}$ [%]	Connection	Architecture
1	[Cim+16]	7	2.5	35.7	Coaxial	Single Ended
2	[Sil+17]	7	2.5	35.7	Coaxial	Single Ended
3	[Cim+18]	6	2.5	41.7	Coaxial	Single Ended
4	[SO07]	5.5	1	18.2	Probe tip on chip	Single Ended
5	UWB1	4-8	4	100-50	Coaxial	Balanced
6	$\mathbf{UWB2}$	8	2.5	31.3	Coaxial	Balanced
7	[TMA15]	101	26	25.7	Probe tip on chip	Balanced
8	[Kuo+12]	93	25	26.9	Wireless $(0.3 \mathrm{m})$	n/a
9	[Tho+14]	108	24	22.2	Probe tip on chip	n/a
10	[Pan+11]	93	20	21.5	Wireless $(20  \text{cm})$	n/a
11	[Lee+16]	84	20	23.8	Probe tip on chip	Single Ended
12	[Lee+15]	80	12	15	Wireless $(1.2  \text{cm})$	Single Ended
13	[Nak+09]	85.5	10	11.7	Probe tip on chip	Single Ended
14	[Nak+14]	80	12.5	15.6	Wireless $(2  \text{cm})$	Balanced
15	[Nak+14]	100	7.6	7.6	Wireless $(2  \text{cm})$	Balanced
16	[Guz+19; Ali+18]	81	3	3.7	Wireless $(0.5 \mathrm{m})$	Single Ended
17	ED1	75-92	14	15.5	WR-10 (IN) Coaxial (OUT)	Balanced
18		82	7	20.7	Wireless (1 m)	Balanced

Table 5.2: Design features, simulation (sim) and experimental (exp) results (frequency response and conversion loss) from the EDs presented in this dissertation.

	Architecture	Substrate	Input BW [GHz]	$egin{aligned}  ext{Video BW} \ [ ext{GHz}] \end{aligned}$	$egin{aligned}  ext{Min. CL} \ [ ext{dB}] \end{aligned}$
UWB1 (Sim)	Ext. Balun & balance ED	Rogers 4003	7.8	2	3.2
UWB2 (Sim)	Rat Race & ED	Rogers 4003	6.9	2	1.2
ED1 (Sim)	Rat Race	Rogers 5880	20	20	13.2
ED1 (Exp)	&	Rogers 5880	20	6	11.1
ED2 (Sim)	ED	Fused Silica	35	25	7.6
ED3 (Sim)	ED	Rogers 5880	29	18	6.6

Table 5.3: Data detection experimental results from the envelope detectors described in this dissertation.

	Max. Bitrate (Error Free) [Gbit/s]	Working fc [GHz]	Sensitivity (Error Free) [dBm]	Best $\Delta \mathbf{b}$ [%]
UWB1	4	4-8	-9	100
UWB2	2.5	4-9	-12	31.75
ED1	12	78-92	-9	14.63

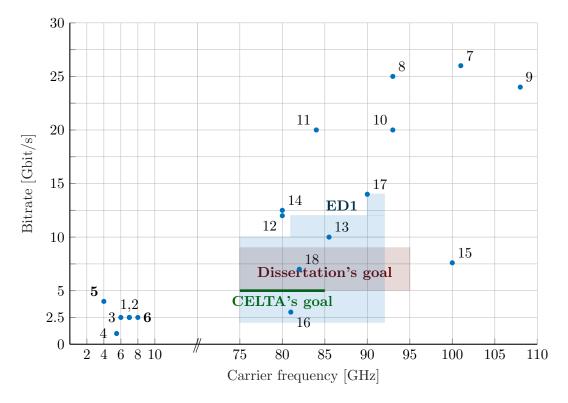


Figure 5.1: UWB and W-band envelope detectors state of the art. References in table 5.3

dissertation in chapter 1 and the CELTA's beamformer requirements. Moreover, it is able to demodulate higher bitrates than proposed in chapter 1, despite of its slightly lower carrier frequency operational range as shown in figure 5.1.

When compared with the state of the art, some detectors measured using probe tips on chip show a better performance. Nevertheless, when connected to an antenna featuring a WR-10 interface they would need to add a packaging, adapter or transition which may limit their performance and increase cost and complexity, while ED1 allows the possibility to be plugged in most of commercial W-band antennas, and in particular in the LC antenna designed for the CELTA's demonstrator without the need of any extra device. Some authors have overcome this limitation introducing short range antennas (up to 2 cm), which is too limited for the project's requirements. [Kuo+12] provides a higher bitrate, 25 Gbit/s at a reasonable distance (0.3 m), but still less than 1 m.

Comparing ED1 and [Guz+19] is more fair because both use the same Schottky diodes from ACST GmbH and Rogers RT-Duroid 5880 substrate [Ali+18]. The comparison proves that ED1 improves the state of the art significantly: while [Guz+19] demodulates up to 3 Gbit/s with 0.5 m of distance, ED1 boost it up to 7 Gbit/s with 1 m.

When experimentally measured, we believe that ED2 and in particular ED3 will

improve ED1's performance in terms of bitrate and carrier frequency operational range due to their broader input and video bandwidths. Moreover, their sensitivity should improve, since the lossy input transition line has been shortened in both detectors.

# 5.2 Outlook

Future work can be addressed from two perspectives: as an improvement of the work presented in this dissertation; or by using the knowledge obtained from this work to research new techniques and paths to introduce sub-THz and THz Schottky diode based envelope detectors in next generation communication systems.

The two UWB envelope detectors can be upgraded in different ways since they complement to each other. UWB1 has been able to demodulate high data rate signals, while presenting a lower sensitivity than UWB2. UWB1's sensitivity can be boosted by replacing the Marki Balun Bal-0010 with another Balun. The BAL-0212 from Marki introduces 4 dB insertion loss instead of 8 dB, nevertheless, it was not used since in it was out of stock at the purchase moment. UWB2 addresses the loss of sensitivity with a new envelope detector architecture which reduces the size and cost of the detector circuit, at the cost of providing a lower phase balance bandwidth. This bandwidth can be either widened, or optimised for another application with a redesign of the detector circuit's shorted stubs or by choosing other Schottky diodes.

Due to their higher design and manufacturing complexity, the W-band envelope detectors have more room for improvement. The first enhancement has been presented in section 4.1.3, where we pursued to shift ED1's frequency response roll-off to higher frequencies. Although ED2 and ED3 were developed to solve this effect, a better characterization of the Rogers RO 5880 at W-band through measuring several transmission lines with different lengths and widths would be interesting. This experiment can help to correlate its outcome with the simulation software's model (CST Microwave Studio and ADS Momentum), investigating which software estimates the results best and introducing the substrates features into them to obtain more accurate simulation results. This is the path to follow if it is found that ED3 experimental results do not match simulations.

Fabricating ED2 has been very challenging, and the final prototype suffers from manufacturing tolerances which are critical in the design. Inaccuracies in the metallic block prototypes implied obtaining unexpected results in the WR-10 waveguide to microstrip line transition's S-parameters. This mismatch in the blocks dimension could be solved by improving the milling process. Besides, as explained in section 4.2.2, the ground pads must be connected.

ED3 is the most promising detector in the author's opinion. It combines the metallic blocks from ED1, which experimentally proved a good performance; with the new redesign discussed in sections 4.1.3 and 4.3, which should provide a broader input bandwidth. Diode mount and ED3's experimental characterization is the next step to follow, to compare its performance with ED1 and confirm the assertions

expounded in section 4.1.3.

Both UWB and W-band EDs can benefit of introducing a low noise amplifier (LNA) at their input to enhance their sensitivity or at their output to increase the delivered power.

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# Erklärungen laut Promotionsordnung

# § 8 Abs. 1 lit. c PromO

Ich versichere hiermit, dass die elektronische Version meiner Dissertation mit der schriftlichen Version übereinstimmt.

# § 8 Abs. 1 lit. d PromO

Ich versichere hiermit, dass zu einem vorherigen Zeitpunkt noch keine Promotion versucht wurde. In diesem Fall sind nähere Angaben über Zeitpunkt, Hochschule, Dissertationsthema und Ergebnis dieses Versuchs mitzuteilen.

#### § 9 Abs. 1 PromO

Ich versichere hiermit, dass die vorliegende Dissertation selbstständig und nur unter Verwendung der angegebenen Quellen verfasst wurde.

# § 9 Abs. 2 PromO

Die Arbeit hat bisher noch nicht zu Prüfungszwecken gedient

Darmstadt, 30. November 2020