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# Algorithmic Tracking Scheme Analog-to-Digital Converter

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Zur Erlangung des akademischen Grades Doktor-Ingenieur (Dr.-Ing.)  
Genehmigte Dissertation von Oliver Bachmann aus Gelnhausen  
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Algorithmic Tracking Scheme Analog-to-Digital Converter

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*Diese Dissertation widme ich  
meiner Ehefrau Jennifer und  
danke ihr für ihre geduldige  
Unterstützung*



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# Zusammenfassung

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Informationen stellen in der heutigen Welt einen immer bedeutenderen Faktor dar. Insbesondere die Erfassung physikalischer Parameter und deren Verarbeitung sind für moderne Anwendungen unerlässlich. Jedes technische Gerät liefert Benutzern immer genauere Informationen über die Umgebung. Der Bedarf an noch detaillierteren Informationen wächst jedoch stetig. Ein Analog-Digital-Wandler (ADC) übersetzt die physikalischen Signale in Informationen zur computerstützten Verarbeitung auf dem Endgerät des Anwenders. Jedoch gelangt die technische Realisierung dieser entscheidenden Komponente an ihre Grenzen. Infolgedessen müssen Forscher neue Wege finden um den Bedarf an wachsenden Informationen zu decken. Heutige ADCs quantisieren die Informationen normalerweise eindimensional innerhalb eines äquidistanten Zeitverlaufs. Bei diesem Ansatz wird jedoch die Zweidimensionalität physikalischer Signale vernachlässigt - Variationen in Größe und Zeit. Eine detaillierte Wandlung beider Dimensionen impliziert jedoch eine höhere Informationsdichte. Ungleichmäßig abgetastete Signale stellen durch den Erhalt der Beziehung zu einer dynamischen Variation des physikalischen Signals eine Alternative dar. Der Algorithmic Tracking Scheme ADC präsentiert eine Lösung auf Basis völlig neuer Methoden zur Umwandlung einer hohen Informationsdichte mittels ungleichmäßiger Abtastung. Das vorgeschlagene ADC Konzept vergleicht das physikalische Eingangssignal mit einer dynamischen Referenz, die durch algorithmische Implementierungen erzeugt wird. Dieser Vorschlag führt zu grundlegenden Forschungsfragen: Welche Bedeutung hat das Referenzsignal? Welche Konstitution des Referenzsignals beeinflusst die Informationsdichte? Wie werden technische Ansätze realisiert? Die Analyse der Informationsdichte beantwortet diese Fragen. In diesem Zusammenhang leitet eine mathematische Beschreibung die Grundlagen für das Studium der Informationsdichte her. Mögliche Abtastalgorithmen werden aus diesen Gleichungen abgeleitet und definieren eine dynamische Implementierung der ADC-Topologie. Im Rahmen der Konzeptbewertung wurden die Algorithmen mit zusätzlicher Funktionalität analoger Elemente auf einem FPGA implementiert. Zusätzlich wurde der ADC-Prozess auf drei ASIC-Prototypen übertragen und validiert. Dabei kamen sowohl State-of-the-Art als auch High-Performance-Computing Technologien (65 nm, 65 nm, 28 nm) zum Einsatz. Die hergeleiteten Gleichungen als auch die Messergebnisse bestätigen sich gegenseitig. Als Resultat wird dem ADC-Designer ein funktionales Entwicklungswerkzeug auf Basis von Gleichungen und Designmethodik zur Verfügung gestellt.



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## Abstract

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Information is an increasingly important factor in today's world. In particular, the acquisition of physical parameters and their processing are essential for modern applications. Every technical device provides users with ever more precise information about the environment. However, the demand for even more detailed information grows steadily. An Analog-to-Digital Converter (ADC) translates the physical signals into computer-processable representations to provide this information to the consumer's application. Representing a more detailed version of the environmental information is now limited by the technical realization of this crucial component. As a result, researchers need to establish new ways to meet the demand for growing information. Today's ADCs usually quantize the information in a one-dimensional way within an equidistant sampling. However, this approach neglects physical signals in two dimensions - in magnitude variations and time variations. While ADCs realize the magnitude quantization with high accuracy, the representation for the resolution in time is usually insufficient. However, a detailed conversion of both dimensions implies a higher information density. Non-uniformly sampled signals represent an alternative, as these retain the relationship to a dynamic variation in the physical signal. As a solution, a completely new method for a high information density conversion based on non-uniform sampling presents the Algorithmic Tracking Scheme ADC. The conceptual basis proposes an ADC that compares the physical input signal to a dynamic reference generated by algorithmic implementations. This proposal leads to fundamental research questions: What is the significance of the reference signal? Which constitution of the reference signal influences the information density? How to realize technical approaches? The analysis of the information density answers these questions. In this context, a mathematical description derives the fundamentals for the study of information density. Possible sampling algorithms are derived from these equations and initialize a dynamic implementation of the ADC topology. As part of the concept evaluation, an FPGA configuration with analog element functionality implements the algorithms. Additionally, the ADC process was transferred and validated on three ASIC prototypes using state-of-the-art technologies and high-performance-computing technologies (65 nm, 65 nm, 28 nm). Both the derived equations and the measurement results mutually confirm each other. Thus, the proposed mathematical equations and design methodology provide a functional development tool for ADC designers.



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## Abbreviations

<b>ADC</b>	Analog-to-Digital-Converter
<b>ALU</b>	Arithmetic-Logic-Unit
<b>ASGA</b>	Accelerated-Step-Generation-Algorithm (BE-Algorithm)
<b>ASIC</b>	Application-Specific-Integrated-Circuit
<b>ATS ADC</b>	Algorithmic-Tracking-Scheme ADC
<b>BEA</b>	Bandwidth-Extended-Algorithm
<b>CIC</b>	Cascaded-Integrator-Comb
<b>DAC</b>	Digital-to-Analog Converter
<b>DDR</b>	Double-Data-Rate
<b>DMA</b>	Direct-Memory-Access
<b>DNL</b>	Differential-Non-Linearity
<b>DSP</b>	Digital-Signal-Processing
<b>ENOB</b>	Effective-Number-of-Bits
<b>FFT</b>	Fast-Fourier-Transform
<b>FMC</b>	FPGA-Mezzanine-Card
<b>FOM</b>	Figure-of-Merit
<b>FPGA</b>	Field-Programmable-Gate-Array
<b>FSM</b>	Finite-State-Machine
<b>HPC</b>	High-Performance-Computing
<b>IC</b>	Inverse-Conversion-Compensation
<b>ICMR</b>	Input-Common-Mode-Rejection
<b>ILA</b>	Integrated-Logic-Analyzer
<b>INL</b>	Integral-Non-Linearity
<b>JASGA</b>	Jump-Accelerated-Step-Generation-Algorithm (RE-Algorithm)
<b>LDO</b>	Low-Drop-Out
<b>LSB</b>	Least-Significant-Bit
<b>LVDS</b>	Low-Voltage-Differential-Signal
<b>MSB</b>	Most-Significant-Bit
<b>PCB</b>	Printed-Circuit-Board
<b>PCU</b>	Process-Control-Unit
<b>PLL</b>	Phase-Locked-Loop
<b>PVT</b>	Process-Voltage-Temperature
<b>REA</b>	Resolution-Enhancement-Algorithm
<b>RMS</b>	Root-Mean-Square
<b>SAR</b>	Successive Approximation Register

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<b>SINAD</b>	Signal-to-Noise-and-Distortion Ratio
<b>SNR</b>	Signal-to-Noise Ratio
<b>SoA</b>	State-of-the-Art
<b>SST</b>	Source-Series-Terminated
<b>T&amp;C</b>	Tracking-and-Correction-Compensation

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## Nomenclature

$A$	Sinusoidal input signal amplitude.
$V_{\text{ref}}$	Dynamic analog reference signal based on digitally generated level.
$V_{\text{in}}$	Continuous analog input signal. Assumed as a sine wave.
$\tau_{\text{d}}$	Total delay of the ADC feedback configuration.
$T_{\text{sample}}$	Constant time for equidistant sampling for uniform conversion.
$T_{\text{samp}}$	Sampling interval for step validation of the Tracking ADC.
$A_{\text{v}}(0)$	Comparator DC voltage gain.
$\Gamma_{\text{crest}}$	Crest ratio: crest factor ratio between sine and a triangular function.
$\Delta_{\text{s}}(t)$	Sampling function as time delta between consecutive sampling steps.
$\delta\tau$	Uncertainty in time.
$\delta\tau_{\text{clk}}$	Uncertainty in time caused by the clock generating the reference.
$E[f(t)^2]$	Power density of the input signal function.
$\varepsilon_{\text{a}}$	Error in amplitude/magnitude.
$\varepsilon_{\text{t}}$	Error in time.
$E[\delta\tau^2]$	Power density of the uncertainty in time.
$E[(t \rightarrow q)^2]$	Power density of the time error translated to a magnitude error.
$f_{\text{bw}}$	Absolute bandwidth limitation of tracking scheme ADCs.
$f_{\text{clk}}$	ADC system clock.
$f_{\text{conv}}$	Average conversion rate (reciprocal of the conversion time $T_{\text{conv}}^{-1}$ ).
$f_{\text{in}}$	Input frequency of a sinusoidal signal.
$f_{\text{max}}$	Maximum representable input frequency.
$f_{\text{max}_{\text{bw}}}$	Normalized frequency limit for the absolute bandwidth.
$f_{\text{max}_{\text{res}}}$	Resolution-related bandwidth limitation. $N_{\text{max}} - 1$ Bit.
$f_{\text{ref}}$	Reference step generation rate (frequently equal to $f_{\text{clk}}^{-1}$ ).
$f_{\text{samp}}$	Sampling frequency (reciprocal of the sampling interval $T_{\text{samp}}^{-1}$ ).
$f_{\text{sig}}$	Sinusoidal input signal frequency.
$q$	Least-Significant-Bit related to ADC resolution.
$M_{\text{jump}_{\text{t}}}$	Total number of jumped resolution steps by the reference signal.
$M_{\text{skip}_{\text{a}}}$	Total number of skipped amplitude/magnitude resolution steps.
$N$	ADC resolution.
$N_{\text{amp}}$	Representable resolution by the input signal amplitude.
$\mathcal{N}_{\text{conv}}$	Power density conversion noise portion.
$N_{\text{delay}}$	Number of CIC-Interpolator delay elements.
$N_{\text{disp}}$	Number of overdrive/underdrive ref. steps due to dispersion effect.
$N_{\text{int}}$	Number of additional interpolated resolution steps.

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$N_{R2R}$	Resolution R2R voltage scaling network.
$N_{ref}$	Power density reference noise portion.
$\omega_c$	-3 dB frequency of the single (dominant) comparator pole.
$\sqrt{E [\varepsilon_{tot}^2]}$	RMS total error per sample.
$\sqrt{E [\varepsilon_a^2]}$	RMS quantization error in amplitude/magnitude.
$\tau_{cmpd}$	Propagation delay of a comparator.
$\tau_{dacd}$	Propagation delay of a digital-to-analog converter.
$T_{conv}$	Average conversion time for non-uniform sample schemes.
$t_c$	Comparator cutoff delay (reciprocal of -3 dB frequency $\omega_c$ ).
$t_p$	Comparator transition propagation delay.
$t_{pf}$	Comparator falling transition propagation delay.
$t_{pr}$	Comparator rising transition propagation delay.
$T_{ref}$	Reference step generation time (reciprocal step generation rate $f_{ref}^{-1}$ ).
$T_{sig}$	Sinusoidal input signal period.
$V_{IH}$	High voltage level at comparator input terminal.
$V_{IL}$	Low voltage level at comparator input terminal.
$V_{max}$	Maximum output voltage level of the comparator.
$v_n$	Voltage at negative comparator input terminal.
$v_o$	Voltage at comparator output terminal.
$V_{OH}$	High voltage level at comparator output terminal.
$V_{OL}$	Low voltage level at comparator output terminal.
$v_p$	Voltage at positive comparator input terminal.
$V_{pk}$	Periodical signal peak voltage
$V_{rms}$	Periodical signal RMS voltage



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# 1 Introduction

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In 1948 Claude Shannon published his masterpiece "A Mathematical Theory of Communication" [1]. As the founder of modern information theory, Shannon created the basis for any communication system such as smartphones or computers and thus laid the foundation for today's technological world. The information describes organized or classified data about one system to be processed by another system. Shannon defined the basic principle of a "bit" as the smallest representable unit to quantify information. The approach to quantify any information, in turn, paved the way for modern communication based on the translation of a physical property into a processable representation for digital systems. Digital data processing has arisen.

Shannon described the basic principle of communication systems by a transmitter, a channel, and a receiver. In this context, the transmitter encodes the message of the input signal into quantized information. This information is transmitted via the channel and decoded by the receiver. The encoding of the physical input signal by binary information defines a conversion technique to the most basic representation of signals – '1' or '0'. This approach enables the stable transmission of information as a message over a channel. Furthermore, binary data represents a reliable method within today's digital signal processing. In this context, the transmitter converts the message of the real-world analog system to a processable binary representation. The process follows the rules adapted to the behavior of the analog system. In the broader sense - a comparator device. According to the current state of technology, a comparator represents this analog module and performs the translation procedure. However, further applications are imaginable. For instance, the concept of voltage to frequency translation by a voltage-controlled oscillator and a subsequent digital sampling of the frequency [2]. In any case, the transmitter defines an analog interface that can convert the message into quantized binary information. Thereby, the conversion is related to the binary encoding property described by Shannon. In today's technical applications, this system is known as the Analog-to-Digital-Converter (ADC).

In the context of the most common ADC topologies, the analog comparator defines the actual conversion system. It acts as a '1' bit quantizer that detects the event of a level

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crossing between the analog input signal and a reference signal. The reference signal, in turn, is generated by the ADC. Thus the relation between the analog input signal and the reference signal describes the encoding scheme for the input message of the transmission system. The level crossing detection by the comparator validates the event, thus that the corresponding information of the reference signal represents the analog signal. The most straightforward procedure implements the topology of a Flash ADC [3]. In this process, the comparison between the input signal and a constant reference signal whose binary correspondence is known to the system realizes the encoding of the ADC. If an input signal crosses the reference, the comparator establishes the "1" bit quantization functionality and declares the corresponding binary representation as valid. Ideally, the assignment of the corresponding binary representation establishes immediately. Therefore, this type of ADC is called Flash ADC and generates the fastest conversion response. A drawback of this topology is the requirement of a further comparator for each comparison level. Concerning the binary correspondence, the number of comparators increases exponentially to the base 2 with the desired resolution. As a result, this procedure significantly increases the hardware complexity of the system. Therefore, the comparator reuse established as a basic idea to overcome this drawback situation. Contrary to an immediate level-crossing detection, the reference signal is varied until it crosses the input signal. In these terms, the number of comparators is no longer the determining magnitude. However, the duration until detection validation determines the accuracy of representing the message of the analog input signal. If the input signal is represented by a constant, the message has no time-dependent component and constitutes single event information. However, in a time-variant input signal, the meaning between the duration and the magnitude describes the total message. This dependency describes the terminology of the information density of a signal.

The approach of Shannon's information theory to quantize a message into several unit portions defined as "bit" considers the entire exploration space of the physical world concerning the dimensions. In a figurative sense, this implies that the physical signal carries a subdividable message. These portions describe the dimensions in which the signal exists. For example, our perceptible world represents four dimensions: three space dimensions (x,y,z) and the time dimension. The description of an accurate event in this exploration space requires the information of the three dimensions in space and the information of the time dimension. The message of this context, in turn, is described by the concatenation of the respective information. In translation to an analog input signal concept, two physical dimensions are present - the magnitude and the time. Both are required to determine the message of the input signal. Thus, in quantization, the information of magnitude and the information in time is decomposed to provide a binary representation. As described by

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Shannon: the smaller the quantization interval (bit), the more accurate the representation of the analog signal. Thus, an infinite number of quantization steps implies the most accurate representation. Because technically, an infinite quantization is impossible, the difference between the original signal and the number of quantization steps used for the representation defines as noise. In the context of an analog-to-digital converter, the number of quantization steps that represent the signal magnitude defines as resolution, and the number of quantization steps in time defines as conversion rate.

Consequently, the resolution and conversion rate are the parameters that describe the possible representable information density by the ADC. The missing information about the original input signal defines as noise. Thereby, the terminology "rate" in conversion rate indicates a repetitive representation of the same behavior. This aspect is related to the historical background of conversion and defines that a quantization result of the signal magnitude is always associated with the equidistant quantization in time. Since the quantization in magnitude and the quantization in time describe the two-dimensional message of an input signal (e.g. generated due to an analog sensor), the represented accuracy of both dimensions describes the information density of the conversion. The difference between the conversion result and the original analog signal defines the conversion noise, as already stated. Due to this fact, the various existing ADC conversion schemes relate to the ability to represent the magnitude quantization adequately and represent the time quantization adequately. Since both physical quantities play an essential role in analog-to-digital conversion, the entirety of the message refers to a tuple that describes the information density in the following.

This short introduction of a 2-dimensional point of view for analog input signals clarifies the previously explained benefits and drawbacks of the ADC topologies. In the case of the ideal Flash ADC, the immediate response to a change of the input signal considers as the ability to represent the time information close to an infinite quantization. Thus, the only remaining task is to quantize the magnitude of the input signal. Thereby, the resolution and thus the number of comparison levels determine the information density of the message. As derived, the hardware complexity of the Flash ADC system increases with the increase of the resolution. Therefore, most modern ADC topologies reduce the hardware complexity by implementing a single comparator and applying a dynamically adjustable reference signal that the ADC generates. The reference signal varies in the way to scan the analog signal, whereby each scanning needs to be evaluated by the comparator. However, this approach implies that a single analog level of the input requires a certain number of comparisons. Therefore, an accurate signal conversion requires a cumulative time based on multiple sampling times. In these terms, the introduced approach exchanges a parallelized scanning property (Flash ADC) with a sequential scanning property. Whether

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the input signal is a constant for a certain amount of time (Sample & Hold device) or not, the actual input signal continuous in time. This aspect implies that the transfer towards a sequential scanning fades out the input signal. Thus, during the scanning process, no magnitude information can be assigned by time information. In other words, the message representation is incomplete, which increases the noise portion of the conversion. However, the magnitude information converts accurately, despite a reduced hardware complexity. In summary, it is always a trade-off between tolerable noise and hardware complexity. These are the terms of today's analog-to-digital conversion schemes.

The most intuitive approach concerns a counter-based encoding scheme for the reference signal in the sequential scanning procedure. The procedure applies to a digital increase of the reference signal by a counter which generates a digital ramp. Due to this property, this kind of analog-to-digital converter generally refers to as Digital Ramp ADC or Counter ADC [3]. The digital reference is converted to an analog representation by a Digital-to-Analog Converter (DAC) in the ongoing process. Thus, the comparator can compare it. If the comparator detects the level crossing between the analog signal and the dynamic analog reference, the event is validated and processed as the conversion result. A consecutive conversion cycle is initialized by the reset of the counter, thus that the scanning procedure starts again. The result of the conversion process addresses the 2-dimensional tuple of the message as an exact representation of the magnitude quantization. Based on the digital update rate of the reference signal, an additional statement about the time for the event detection assigns to the result of the quantized input signal magnitude. However, due to a linear update of the reference signal, the time information varies with the level-crossing detection and is therefore directly related to the input signal magnitude. This process implies that the higher the input signal magnitude, the longer the duration for a level crossing detection and vice versa. Therefore, the converted information density represents a constant message. Consequently, because portions of information are faded out, the noise increases. Because the level-crossing event generates the moment of validation for the conversion result, the duration for this event varies with the input signal. This kind of scheme generally refers to asynchronous or non-uniform conversion. If exclusively this event determines the conversion rate, synchronous receiver systems may have difficulties processing the signal. On the other hand, this kind of conversion scheme has an event detection that varies between  $1 \rightarrow 2^N$  clock cycles, which implies that the average noise portion increases dramatically.

The Successive Approximation Register (SAR) ADC overcomes the drawbacks of the simple counter-based ADC [3]. The topology replaces the digital counter with the successive approximation register, which scans the analog input signal for each possible binary

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constitution. Instead, to compare each single level representation within the resolution scope, it addresses the actual binary result by the division of 2. This procedure implies that the number of scanned levels reduces to the actual resolution of the ADC. Since the scanning process includes every possible level, the duration for a conversion result validation always takes the same amount of time. As a result, the duration of a conversion cycle is constant. So this procedure represents synchronous or uniform conversion schemes. Due to the synchronous nature, a conversion results within a specific time and therefore defines a "rate". The constant conversion rate, in turn, is processable by synchronous receiving systems. Concerning the information density, a deterministic fading out establishes, which implies a constant noise portion.

Nevertheless, the assignment of the time to magnitude quantization within the conversion time relates to an error. Because, due to the binary nature of the scanning process, the loss of the information distinctly reduces compared to the simple counter ADC approach. As a result, there is always a trade-off between the resolution (N) and the time information. Thus, application areas for this kind of ADC in its basic topology relate to moderate magnitude resolution where the conversion time is subject to a tolerable information loss.

As examined, the relation between time quantization accuracy and magnitude quantization accuracy of a 2-dimensional input signal defines the representative message. Besides the magnitude resolution, the SAR conversion scheme exhibits a loss in time information related to the fade-out property during the conversion cycle. It is present as noise for the case that the input signal changes during the conversion period. Due to this fact, a higher conversion rate implies a more accurate ability to "track" a varying signal in time. Indeed, this procedure applies to the process of time interleaving of a multichannel ADC [4]. However, the Tracking ADC [3] represents a more fundamental approach that can provide a close to immediate response behavior like the Flash ADC.

Contrary to the Flash ADC, the tracking scheme applies a derived sequential scanning process. Thus, the hardware complexity likewise reduces to a single comparator. Unlike the Digital Ramp ADC and the SAR ADC conversion scheme, the Tracking ADC procedure constitutes a proximity approach. In this concept, the change in magnitude of the analog input signal behaves in the proximity of the preceded magnitude. Thereby, the difference in time and the difference in magnitude between consecutive conversion cycles describe a delta function. Since the digital reference and thus the analog reference never resets, rapid level-crossing event detection enables. In the ideal case, the level-crossing validates within a subsequent update of the reference signal. Indeed, the level-crossing event detection depends on the relation between the slope of the input signal and the slope of the analog reference signal. Thereby, the magnitude of the bit (resolution) and the update rate constitute the slope of the analog reference signal.

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The topology of the Tracking ADC belongs to the type of counter-based ADCs as likewise the Digital Ramp ADC and the SAR ADC. However, compared to the Digital Ramp ADC, the encoding scheme of the Tracking ADC is extended by an up-counting and down-counting property. The procedure concerns the level-crossing events, which establish a binary control signal for the up/down-counter due to the comparator. So the level-crossing event indicates the change of the counting polarity. A level-crossing above the input signal ensures that the counter turns its state from up-counting to down-counting. The level-crossing below the input signal ensures the contrary behavior. In this way, this kind of ADC "tracks" the input signal, which derives the name from this property. As typical for counter ADCs, the Tracking ADC converts the 2-dimensional tuple of time and magnitude. Thus, the conversion represents the message of the analog input in both dimensions. Since the level-crossing detection declares the validation event of the conversion, the tracking scheme relates to an asynchronous or non-uniform conversion scheme.

Besides the counting scheme-based ADCs, there are various implementation possibilities like the  $\Delta\Sigma$ -ADC or the Single-Slope/Dual-Slope ADC [3]. However, the functionality differs from counter-based ADCs since the conversion event of the magnitude is translated to a timed event signified by the comparator. Therefore, a reconstruction of the magnitude information concerns filtering and sampling processes of a '1'-bit quantized signal. These concepts realize a synchronous conversion rate which applies to standard receiver systems. Indeed, most of the current State-of-the-Art (SoA) ADCs consider the pure conversion results in the magnitude. However, the brief introduction of the 2-dimensional nature of analog signals and the conversion ability of non-uniform sampling schemes illustrate the potential, covered by additional information of the entire analog message. ADCs based on a counter scheme carry information about the magnitude and the time, which cover the entire scope of the 2-dimensional message. An asynchronous or non-uniform conversion scheme represents this aspect.

The idea of non-uniform sampling is relatively new. Conventionally, an additional overhead of signal processing is required to decode the time information into representative magnitude information based on an asynchronous conversion signal [5]. Nevertheless, as illustrated by the Tracking ADC, the temporal information of a completed conversion leads to the initialization of a new conversion cycle. This aspect implies that a higher number of quantized magnitudes establishes within the same time than synchronous designs. As a result, the higher number of conversion cycles results in a higher information density. Various publications that describe the application of asynchronous ADC techniques realized the art of non-uniform sampling. The SAR ADC topology is one of the most popular conversion techniques nowadays and is improved continuously. Likewise, there was the

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realization about the dependency between information density and ADC performance. Related to the binary search nature of the SAR algorithm, the conversion cycle requires a predefined time. Thus, it limits the possible number of detection cycles.

Contrary to the approach of a more accurate conversion in time, the asynchronous SAR ADCs belong to the idea that a low varying signal carries less information in the time dimension. Based on this fact, the asynchronous SAR implementations consider that sampling is only necessary if the input signal is changing. Therefore, the general approach concerns a reduced sampling activity in order to reduce the power consumption. Since the demand for low-power ADC applications growth with emerging portable devices, the first approaches to reduce power consumption started a decade ago [6, 7, 8]. These first attempts had moderate resolutions and low conversion rates. However, modern telecommunication systems demand high speed, low power in conjunction with a moderate resolution. Thus, the development in the second half of the past decade concentrated on improvement and the design of new approaches for asynchronous SAR systems. The design methodology for asynchronous was refined [9] towards ADC designs for application-specific environments where low power is the primary concern. The procedure belongs to low resolution but high conversion rates [10, 11] or high resolution and low conversion rate [12, 13] implementations, as this is always a trade-off for SAR topologies. Indeed, also the concept for a more accurate temporal conversion was prosecuted in the scope of the SAR ADCs. The approach concerns an adjustment of the binary search algorithm characteristic for a procedure that shortens the sampling interval. In these terms, strategies to improve the actual conversion algorithm enabled faster conversion rates as in [14]. Another strategy applies to the topology of the sampling circuit and the comparator. Multiplication of these analog components initialize the conversion process during the acquisition cycle and thus perform pseudo parallel [15, 16]. Additionally, the sub-range of the SAR conversion scheme based on sequential low-bit order processing of two separated conversion cycles achieves this kind of parallelism. The initialization of the respective conversion cycle arranges during the current conversion cycle process [17].

Related to the fact that the basic SAR algorithm processes a synchronous conversion scheme, the described approaches preserve this property even if the sampling can be acquired asynchronously. Also, the property of an objective asynchronous conversion can be provided and summarizes under the term non-uniform. These implementation techniques modify either the encoding approach of the SAR ADC by the modification of the search algorithm or modify the decoding of asynchronous SAR implementations. In these terms, the asynchronous SAR implementation provides a non-uniform temporal response which can be converted by a time-to-digital converter as proposed in [18]. The modification of the encoding, in turn, concerns the binary search algorithm and supports a non-uniform objective conversion. [19] describes a method to track the input signal's change to provide

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a reference about the current information density. In this way, the conversion rate adjusts to meet the minimum requirement to represent the input signal message. [20] proposes a non-uniform quantization scheme for high-speed SAR ADC architectures. The binary search scheme of the SAR ADC was reorganized to a non-uniform quantization scheme and combined with a random sampling strategy. This approach allows higher conversion rates based on an asynchronous sampling sequence.

The brief insight in the theory of application techniques for asynchronous SAR ADC illustrates the demand and possible advantages that asynchronous or non-uniform sampling schemes can achieve. However, the theory and the applications are not restricted to the field of SAR ADCs and their derivatives. Instead, there is a wide field of possible ADC topologies in the extended scope of counter algorithm-based analog-to-digital conversion techniques. This area includes the described SAR ADC, the Digital Ramp ADC, the Tracking ADC, or their derivatives. For example, a non-uniformly sampled ADC, based on a parallel digital ramp architecture, applies the temporal conversion information by a pulse position modulation. It is presented in [21] and describes a new technique to convert the quantization information in time.

Common to all of the asynchronous sampling schemes is the ability to quantize the information in time. In order to achieve temporal quantization, the basic topology constitutes a comparing device that detects an event of level crossing between the analog input signal and a generated reference signal. This procedure is the central fact for the classification of the counter-based ADCs into asynchronous conversion topologies. However, the counter-based ADCs belong to the parent group of level-crossing ADCs. The classical level-crossing problem was presented first in 1981 by J.W. Mark et al. [22] as a non-uniform sampling approach for data compression. They evaluated the benefits of established systems. However, the first idea for implementing the level-crossing concept as a non-uniform ADC topology was by N. Sayiner et al. in 1996 [23].

Additionally, a mathematical approach was proposed that derives a definition of the total quantization error. Thereby, the combination of errors as an error in time and a magnitude error enables the determination of a system-related noise portion. Thus, this approach establishes a mathematical basis for the class of level-crossing converter. Based on the fundamentals of level-crossing ADCs, E. Allier et al. identified the relationship between the level-crossing approach and an asynchronous system design in 2003 [24]. They proposed a new class of A/D converter that uses level-crossing events to generate an asynchronous signal. The proposed topology based on an up/down-counter, a digital-to-analog converter, and a comparator constitutes a feedback configuration. The system has no global clock but increases or decreases the reference signal related to the level-crossing events. As a

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result, the "1"-bit binary output stream of the comparator is distributed non-uniformly in time by the detection events. In order to convert the non-uniformly sampled information into a binary representation, a timer realizes the quantization in time by the detection of the duration between individual level-crossing events. Based on the asynchronous application of the level-crossing ADC, the mathematical approach extended the timer sampling and related the total quantization error to the expression of the signal-to-noise ratio (SNR). Based on this approach, E. Allier et al. [25] published an improved version of asynchronous level-crossing ADC in 2005.

Further developments in level crossing ADCs led to improvements such as a more accurate sampling for constant signals. In this context, the systematic introduction of triangular dither achieved this improvement [26]. The nature of level-crossing ADCs traces back to the primary approach of an intersection between the analog input signal and a reference. A non-uniform signal in the time domain encodes the result of the level-crossing event detection. Therefore, the initial approach is not restricted to the topology suggestion of E. Allier et al. but instead extends to any level-crossing behavior. In this way, the idea was implemented in the scope of Flash ADCs as described in [27]. However, the proposed strict quantization in time neglects the basic information of the magnitude. Therefore, the consideration of both information-bearing dimensions enables a more accurate description of the input signal message. The application of this property to ADC systems requires an input signal quantization in the voltage domain and in the time domain. [28] proposes a system design based on the traditional level-crossing approach and provides a voltage quantization based on a sawtooth-formed reference. The time quantization, in turn, is provided by the sampling of the level-crossing events with a time-to-digital converter. Alias-free asynchronous filter techniques perform the suppression quantization noise effects in the time domain. A comparable approach was also proposed by [29]. However, the level-crossing event detection refers to a Flash-based non-uniform sampling characteristic. In general, specific to these ADCs is a method to convert both the temporal information and the magnitude information of the input signal. As a result, the information density of the converted signal increases distinctly compared to uniformly sampled ADC approaches.

Based on the aspect that, in general, any input signal for ADCs is represented by time and by the magnitude, and a level-crossing approach enables the revelation of this property, a re-examination of ADC topologies can identify these characteristics. In the scope of the Flash topology, the state-of-the-art already performed this step. Besides the Flash topology, the counter-based topologies also exhibit the property of level-crossing. Contrary to the SAR ADC, the Digital Ramp ADC and the Tracking ADC generate an asynchronous conversion scheme. Level quantization converts the information in magnitude, but the

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information in time is unused so far. However, these topologies provide the property to enable possible conversion information of the time. While the Digital Ramp ADC resets the reference signal with the validation of an intersection event, the Tracking ADC carries on the scanning process for a consecutive intersection moment from the current state. This ability has the side effect that a magnitude conversion of consecutive conversion samples is always relative to the intersection moments. Thus, this aspect implies that the time information is represented as the delta between consecutive detection moments and carries the basic information of the message. Related to the fact that the tracking scheme always updates the reference signal based on the quantization step in magnitude and the quantization step in time, a 2-dimensional reference develops. However, the traditional tracking scheme approach keeps this relation unused.

Nevertheless, the non-uniformly constituted time information provides the possibility to be quantized by a distinct higher resolution (e.g. by a TDC). The insight in this relation illustrates the 2-dimensional ability of tracking- scheme-based algorithms. However, the restriction of the step detection for Tracking ADCs led to the disregard of this topology. Due to this fact, the central area of Tracking-ADC applications nowadays merely covers the field of power supply monitoring where an event detection system is required. Since the conversion scheme of the Tracking ADCs is suitable for the quantization in magnitude and time, recent Tracking ADC approaches illustrate an impression about the SoA and inform about potential improvement strategies simultaneously.

As mentioned, the field of power management functionality concerns the applications of Tracking ADCs. Thereby, the main focus relies on power consumption since the ADC defines an auxiliary system. Nevertheless, even in this area, the detection of input signal transients describes a crucial fact. Therefore, [30] proposes a method for DC-DC controller, which reduces the power consumption of the Tracking ADC by an intelligent clock management system. This system features a self-clocked design that can adjust the clock frequency on the demand of a faster update rate for the reference signal, which is the case for detecting input signal transients. In these terms, a modified Tracking ADC addresses this requirement as described in [31]. The basic principle of the tracking scheme approach is extended in the digital domain by the asynchronous control logic. It acts as a listener to significant changes in the input signal and triggers the conversion. Besides the solutions for an improved tracking ability by adaptive frequency control, a parallelized design enabled the detection of significant input signal changes [32]. A further set of comparators configures the ADC, and instead of listening for the event, the event converts directly. A parallel comparison by a respective comparator detects the delta of the reference signal for 1 LSB and 2 LSB concerning the current status simultaneously. In general, this approach allows the tracking of higher input signal slopes than the simple

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detection of a single step delta. However, these improvements are related to application-specific designs where the detection of events is required. Thereby, the resolution is almost peripheral, which resulted in magnitudes of 4 bit to 6 bit. Thus, to open up the tracking scheme properties for a broader field of applications, a higher resolution is required. Based on these terms, a Tracking ADC should establish the property of a high resolution and the advantage of fast conversion rates at the same time. [33] described a proposal to increase the resolution of the Tracking ADC. A modified version of the tracking scheme generates a resolution of 12 bits by a dynamic adjustment of the reference signal step size. In these terms, a digital implementation, which extends the basic up/down-counter functionality, controls the step size adjustment. This modification shifts a solution for the input slope restriction from the analog domain to the digital domain. Thus, it enables a higher degree of flexibility and controllability about the reference signal. The idea of an improvement based on digital operations was also performed in [34] to provide a higher resolution than established Tracking ADCs. A multi-bit quantizer, in a four comparator constitution, generates a multi-bit status control for the digital operation block. The methodology provides intersection event detections in parallel. Thus, the modified design has a resolution of 10 bit and provides an average conversion rate of 50 MS/s.

In summary, the modifications of the Tracking ADC designs reveal the ability to improve the basic tracking scheme and establishes applicability within the performance scope of recent ADCs. Especially the point of view for operation modifications within the digital domain reveal a wide range of performance improvement properties.

The new perspective about the digital domain opens the mind to an entirely new approach for the design of Tracking ADCs. The perspective enables problems to be solved that previously meant restrictions for the Tracking ADC. In particular, this aspect concerns the property of the non-uniform sampling problem whereby an adaptation of the tracking algorithm promises a quantization within the 2-dimensional message. The time quantization and the magnitude quantization, in turn, imply a more accurate representation of the input signal message denoted by the information density. Since the modifications of the reference signal due to the implementation of sampling schemes by digital operations modify the primary Tracking ADC significantly, a new type of conversion schemes reveals. These conversion schemes are assigned to new terminology and are referred to as **"Algorithmic Tracking Scheme"** in the following.

In these terms, the primary tracking principle remains. However, the actual sequence of the tracking scheme controls an advanced digital operation referenced to the level-crossing detection of the comparator. Based on the relation to the input signal, the resulting conversion rate is non-uniform. In this context, the non-uniformly sampled signal provides the

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information of the input signal magnitude. Additionally, the advanced digital operations enable the decoding ability of the non-uniform information in time. Thus, the concept provides a 2-dimensional reference. In concern to the tracking scheme, a digital ramp constitutes this reference due to a triangular signal. Due to the intersection moments relative to the input signal, the progressive propagation of the triangular reference signal is also relative to the input signal. In detail, this implies that the non-uniform property represents the constitution between the ADC resolution and the reference step generation rate represented as the system clock. Thereby an accurate dependency between the time and the magnitude is generated. The basic idea is simple: The reference step generation rate is faster than the allowed internal system delay. Thus, a digital ramp develops between the switching moments of the comparator, which refers to the systems propagation delay. As a result, the quantization in time generates a relation to the input signal intersection with the reference signal. It is the basic idea of an algorithmic tracking scheme approach that can quantize the 2-dimensional message.

The simple idea to maintain the Tracking ADC topology and increase the clock frequency, which represents the update rate of the reference signal, sounds like a straightforward approach. However, the real importance of this approach raises fundamental questions since it breaks with the convention that the sampling rate of ADCs results from the internal system delay. The principle creates an entirely new condition where the moments of an intersection event depend on the relation between the input signal and the generated reference signal in conjunction with the internal feedback delay of the system. The generated conversion result constitutes a composition between the ADC resolution and the intersection moments. In other words, the result is a quantized representation of the input signal in terms of the magnitude and the non-uniform time intervals which result from the intersection moments.

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The all-encompassing question is concerned to the meaning of the basic approach to modify the update behavior of the reference signal used for the comparison with the input signal. Thus the question arises:

**What is the significance of the reference signal modification for the system?**

This question primarily considers the performance of an ADC in terms of the amount of information that can be represented, known as information density. This aspect includes precisely the circumstances in which ADCs have to perform in a range close to their specification limits. This point of view mainly concerns the performance evaluation in terms of information density within the entire input signal bandwidth of the ADC. In the scope of the knowledge about the importance of a reference signal modification concerning the representable information density, another fundamental question arises:

**Which constitution of the reference signal influences the information density?**

The investigation of the question deals with the expansion of the initial idea to increase the clock frequency. In the context of digital operations, a deliberate creation or suppression of system properties is possible. This purpose maps analog properties to digital operations. The applied algorithm now determines the primary characterization of the ADC. The Algorithmic Tracking scheme ADC. In order to assign the algorithms to a specific hardware design, another general question arises:

**How to realize technical approaches of the Algorithmic Tracking Scheme ADC?**

The implementation of the proposed approach answers the question by analog and digital resource investigations. Thereby, the analog system demands cover a minimum implementation requirement. Flexible digital implementation of the algorithms concerns the system in particular. In this sense, terms of programming ability and reconfiguration ability become essential and offer a wide range of algorithmic possibilities. Thus there is no one solution but a variety of definable solutions concerning the application area.

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The fundamental questions will be addressed in detailed research to describe an entirely new perspective on converted information. The concept of information density is used as a benchmark to categorize ADC properties and evaluate various conversion algorithms. In these terms, the research scope covers the following fundamental investigations:

## **Chapter 2: Mathematical Theory of Non-uniform Sampling**

The transfer of the basic tracking scheme to a general design strategy for implementing a variety of sampling algorithms requires a mathematical background. Therefore, a set of equations is derived which describes the properties of an algorithmic tracking scheme. In order to validate the applicability of the mathematical description, a MATLAB model which implements the general behavior of tracking scheme ADCs was developed. The set of equations contains the description of the input signal bandwidth limitations related to the respective parametrization of the ADC. However, the bandwidth limitation exclusively describes a specific frequency. Thus, the general purpose of the derivation for mathematical expressions concerns the predictability of the information density within the entire bandwidth course. This aspect especially concerns the ability to represent the information density under the constraint of a non-uniform sampling in the lossy area. Thereby, the concept of the Signal-to-Noise Ratio (SNR) was applied to investigate the information density. The basic approach is that the converted information density is affected by the noise component of the system. Conversely, this means that the definition of the SNR represents a comparison criterion for the similarity of the conversion result to the input signal. The prediction ability of the derived equations represents a general approach that can perform non-uniform sampling and uniform sampling. Based on an investigation of the affection by parameter variations and the validation by the MATLAB model, a theoretical approach for the reference signal modification is derived. The chapter answers in these terms the all-encompassing question: What is the significance of the reference signal modification for the system?

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### **Chapter 3: Algorithmic Tracking Scheme ADC**

The derived set of equations enables the predictability of properties for algorithmic tracking scheme ADCs. Derived from these equations, a variety of possible algorithmic implementation patterns are imaginable. The approach of primarily digital implementation, therefore, offers the highest degree of configuration ability. Thus, the analog constitution of the proposed system reduces to the minimum amount of demands. The proposed algorithmic implementation model demonstrates the ability of digital designs in the scope of programming ability and reconfiguration ability. An investigation concerning the predictability of the derived set of equations demonstrates the applicability of the algorithmic tracking scheme approach. In order to demonstrate the design flexibility, the proposed algorithmic approaches improve the performance by modified conversion schemes. In these terms, the bandwidth limitation and the effective resolution of the ADC improve by an algorithmic approach. Analysis precedes the implementation approach and reveals the methodology to constitute the reference signal in the context of specific performance parameters. The chapter answers the second fundamental design question: Which constitution of the reference signal influences the information density?

The previous chapters answer the fundamental questions about the significance and the constitution of a reference signal modification. The derived set of equations validates the theoretical approach and offers a wide variety of theoretical implementation possibilities. In order to verify the implementation capability of the proposed system, the following chapters answer the third and general question: How can the approach of the algorithmic tracking scheme be implemented?

### **Chapter 4: Analog Hardware System Characteristics**

The reduction of the analog complexity to a minimum requirement and the determination of a dependency on the internal system delay examines the properties of the analog hardware system about non-linearity disturbances. In particular, the feedback configuration's propagation delay is the main character concerning the conversion rate. A large part of the non-linearity effects attributes to the comparator. Due to the non-clocked version, the influence of the dispersion effect is decisive for the propagation delay. This influence thus leads to non-linearity effects in the context of the conversion. Therefore, the reason for the dispersion effect is investigated and described in a mathematical model. Based on this model, two compensation methods are introduced that can eliminate non-linearity effects.

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## **Chapter 5: FPGA based ADC System Design**

The actual implementation of the Algorithmic Tracking Scheme ADC was performed on an Field-Programmable-Gate-Array (FPGA) to demonstrate the applicability. The analog resources used for the implementation constitute a voltage scaling network interfaced to the digital FPGA output ports. Thus the reference signal generation is controlled by the algorithmic implementation on the FPGA. In order to provide the feedback configuration, one of the LVDS receivers represents the functionality of the comparator. Therefore, the analysis precedes the investigation of the comparing capability of the receiver. A preliminary analysis of a wide variety of algorithmic implementations demonstrates the FPGA's ability to program and reconfigure the algorithm. Common ADC architectures like the Digital Ramp ADC, the SAR ADC, and the conventional Tracking ADC were implemented and evaluated in the scope of their respective performance. The proposed algorithmic tracking scheme implementations are compared to the common ADCs. A comparison between measurement results and the mathematical model verify the approaches.

## **Chapter 6: Mixed Signal ASIC Design**

The advantage of FPGA implementations relates to the flexibility of programming. However, compared to FPGA implementations, Application-Specific-Integrated-Circuit (ASIC) performance is distinctly better. Therefore, three different mixed-signal ASIC designs implement the algorithmic tracking scheme approach to investigate the increase in performance by integrated circuits. However, the non-linearity affection is significant for integrated circuits, as an evaluation demonstrates. Therefore, implementations of the ADC designs expand with proposed compensation methods. Two ASIC prototypes of the ADC cover the algorithmic tracking scheme and two different compensation methods in an SoA 65 nm process node. Since one of the compensation methods raises advantages compared to the other one, the third ASIC covers this compensation method in a 28 nm process node. In this context, the transfer to an 28 nm process node promised improvements based on High-Performance-Computing (HPC) technology.

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## 2 Mathematical Theory of Non-uniform Sampling

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In general, any real-world physical signal property quantizes into a tuple of time and magnitude. Analog-to-digital conversion organizes a relation between time and magnitude by fractionating the analog signal related to predefined quantization steps. The precision in time and the related precision in magnitude are decisive about the accuracy of the signal representation. An infinite number of time-magnitude tuples implies the most accurate representation of real-world analog signals in this context. However, due to the restriction based on system resources, an analog-to-digital conversion assigning an infinite number of tuples is not applicable. Instead, the assignment of valid tuple relates to the quantization properties based on the available resources. In order to recover the converted signal from its digital representation, it is beneficial to quantize the time in equidistant discrete steps. In this way, the sequence of the quantized amplitude and the discrete information of the time step is sufficient to assign the tuple. This type of system generally refers to as uniform or synchronous sampling. However, based on the equidistant discrete time steps, an error between the analog signal and the digital representation is caused. This error is related to the particular property of a finite number of quantization steps in time and magnitude. Most the state-of-the-art A/D-conversion schemes define a relation between conversion time (quantization step in time) and resolution (quantization step in magnitude). Thus, the lower the resolution, the shorter the conversion time. In this relation, the maximum number of comparative steps acts as a worst-case scenario. Thus, the maximum number of steps defines the conversion time related to uniform sampling. Regardless of current magnitude information conversion, the conversion cycle is always related to a constant duration within a sample window. Therefore, it would be beneficial to start the next sample window right after converting the magnitude information. This type of system generally refers to as non-uniform or asynchronous sampling. The procedure relates the conversion time to the adequate time required in order to detect the amplitude information. Therefore, theoretical faster conversion can provide a higher information density than synchronous A/D-conversion.

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Synchronous or uniform sampling ADCs such as SAR-,  $\Delta\Sigma$ - or Pipeline-ADCs are well known and understood. The group of asynchronous or non-uniform sampling ADCs refers to level-crossing ADCs. The conversion time depends on assigning the quantization level of the ADC to the actual signal by an intersection detection. Known applications are Flash-, or Counter-ADCs, which differ in the reference signal formation to represent the quantization level comparison to the input signal. While Flash-ADCs provide the fastest conversion time, they suffer from hardware complexity. Counter-ADCs, in turn, requires a low hardware complexity but suffer from slow conversion times. Tracking-ADCs represent a trade-off is represented, which is the advanced implementation of a counter-based ADC. Due to the tracking mode, the conversion time depends on the input signal level and the difference to the previously converted level. It provides the delta between consecutive conversion cycles. The delta function, in turn, provides information about the required time and the number of resolution steps between consecutive samples. The required time for the conversion cycle depends on the input signal level, which causes the conversion time to be non-uniform under the consideration of a time-variant input signal. Thus, a non-uniform conversion ADC like a tracking scheme ADC provides information in magnitude and time. The context leads to the aspect that non-uniformly sampled ADCs can provide a higher level of information density than uniformly sampled ADCs.

Level crossing approaches cause non-uniform conversion times by the interdependence to the analog input signal. The converted magnitude information reveals the same interdependence. Thus, the converted amount of information of both dimensions is considered relative to the input signal. However, the occurrence of a successful level crossing detection is not equidistant in time as guaranteed for uniform conversion schemes. Due to this fact, the prediction of non-uniform ADC behavior refers to as the occurrence probability of a level-crossing detection. However, compared to uniform conversion, this aspect requires a novel definition of ADC behavior. Thereby, the interaction for degrees of freedom for this kind of ADC needs to be investigated to predict rational parameters for designing a non-uniform sampling algorithm. The delta function primarily constitutes the degrees of freedom based on a relation between initial parameters for absolute resolution, conversion rate, and reference step generation rate. Based on these parameters, the SNR needs to be defined. However, the state-of-the-art SNR relates the noise power exclusively to the absolute resolution for uniform sampling. Therefore, the existing approaches need to be extended by the probability of level-crossing occurrence. In this context, the non-uniform sampling introduces further noise to the system. Because the delta function represents the direct relation between the conversion step and the input signal, it also represents the amount of system noise caused by non-uniform sampling. Therefore, the level-crossing approach represents the basis for derivation of a novel equations for non-uniform sampling.

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Based on fast conversion cycles and low hardware complexity, the application of a tracking scheme offers a basis representation for designing a non-uniformly sampled system. The provided delta function based on a single bit resolution for a single conversion time step forms the basic tracking scheme's basic structure. A comparator converts a comparative step any time the analog reference signal crosses the input signal as a 1-bit quantizer. Thus, the level crossing approach applies as a starting point for the mathematical derivation of the SNR for asynchronous analog-to-digital conversion. This chapter derives the relevant system constraints of the analog-to-digital conversion scheme and a dependency between signal and noise power within the non-uniform sampling system. The design of a MATLAB model for a tracking scheme approaches compares the mathematical model with a simulation model. The consequences regarding possibilities of system improvement by considering the results will be analyzed and demonstrated in an ideal system based on MATLAB simulations.

## 2.1 A Brief Analysis of Level-Crossing AD-Conversion Modeling

In the tracking ADC approach described in [32], the physical properties of the ADC-system based on resolution and total delay of the conversion loop (i.e., the minimum time needed for a sample) are decisive about the ability to convert the input signal. The basic tracking system in figure 2.1 constitutes a continuous counting system that provides a reference signal ( $V_{ref}$ ) proportional to the actual counter value. A comparator changes the counter polarity (i.e., up or down counting) based on whether the actual reference is higher or lower than the actual input signal ( $V_{in}$ ). The total system delay ( $\tau_d$ ), illustrated in figure 2.1, limits the maximum conversion rate of the ADC.

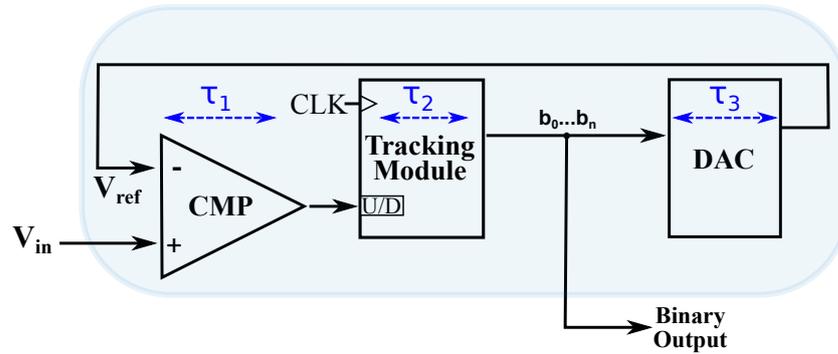
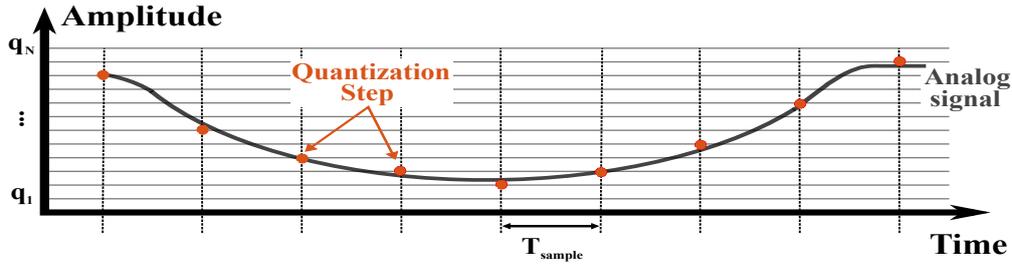


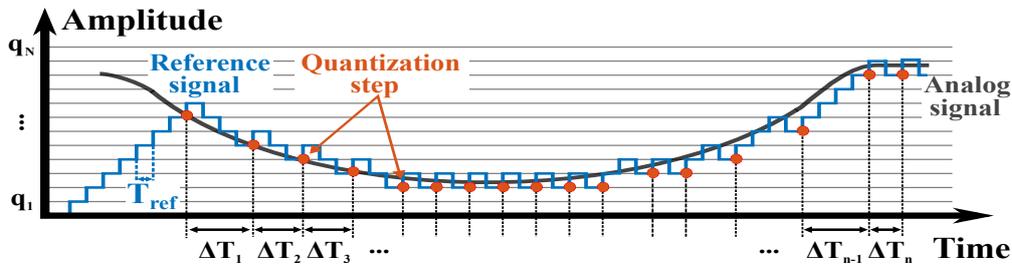
Figure 2.1: Tracking ADC system and total system delay ( $\tau_d = \tau_1 + \tau_2 + \tau_3$ ).

The tracking process of an analog signal requires that the system detects the level-crossing event. Therefore, a quantization step is valid whenever the reference signal crosses the analog signal. However, the Tracking ADC generates a continuous toggling of the conversion result in this procedure [3]. This aspect is related to the tracking behavior, which requires the classification of the analog input signal between adjacent quantization levels. Due to the level crossing dependency, the time for the generation of a sample varies ( $\Delta T_1 - \Delta T_n$ ) non-uniformly. Figure 2.2(b) demonstrates the sampling scheme of the Tracking ADC. A consideration that exclusively validates a level-crossing of the reference above the input signal simplifies the conversion process. Thus, this assumption clarifies the non-uniformity of the conversion by excluding the continuous toggling behavior of the result. In comparison, uniform sampling, as depicted in figure 2.2(a), is based on equidistant time steps ( $T_{sample}$ ). The time amplitude tuple constitutes a constant time

interval in which the amplitude quantization takes place. This fact implies that the time interval for uniform sampling is related to the number of amplitude quantization steps (resolution). Thus, uniform sampling in figure 2.2(a) requires  $N$  comparisons for the amplitude quantization. Non-uniform sampling in figure 2.2(b) can provide the amplitude quantization related to the level crossing.



(a) Uniform sampling scheme.



(b) Non-uniform sampling scheme.

Figure 2.2: Uniform sampling scheme based on equidistant time steps  $T_{\text{sample}}$  in (a) compared to non-uniform sampling based on varying time steps  $\Delta T_1$ - $\Delta T_n$  in (b). Uniform sampling (a):  $N$  comparisons for amplitude quantization. Non-uniform sampling (b): amplitude quantization by level crossing.

### 2.1.1 Mathematical Derivation of Limit Factors for Tracking Scheme ADCs

The tracking scheme requires the following of the input signal by the dynamic reference signal ( $V_{\text{ref}}$ ) as illustrated in figure 2.2(b). Therefore, the update of the dynamic reference signal depends on the parameterization of the single step. In these terms, the ADC resolution represents the single step height for an least-significant-bit ( $q$ ). The update rate equates to the reference step generation rate, the system clock in the simplest case. Thus, the reciprocal of the reference step generation rate refers to the single-step width in

time ( $T_{\text{ref}}$ ). As a limiting factor of the ADC system, illustrated in figure 2.1, the internal feedback delay defines the minimum propagation delay ( $\tau_d$ ). Therefore, the moment of the analog level crossing needs to propagate through the Comparator ( $\tau_1$ ), synchronized by a reference step in the Tracking Module ( $\tau_2$ ), and propagated through the DAC ( $\tau_3$ ) in order to apply an updated reference signal. This limitation defines the minimum sampling interval ( $T_{\text{samp}}$ ) for an ideal comparator with constant propagation delay in the following. The periodical input signal ( $V_{\text{in}}$ ) is generalized to a sine wave since any signal derives from a sine wave representation. The intersection of the input signal and the dynamic reference signal ( $V_{\text{ref}}$ ) establishes for equality of the respective signal slope. Thus, each intersection occurs if the reference slope is at least the input signal slope. Considering a sinusoidal half-wave of the input signal ( $V_{\text{in}}$ ) represents a sufficient condition for each existing slope. Figure 2.3 depicts the considerations for the level crossing approach:

$$\begin{aligned} \text{Periodical input signal } (V_{\text{in}}): & \quad f(t) = \frac{A}{2} \sin(2\pi f \cdot t) \\ \text{Sampling interval } (T_{\text{samp}}): & \quad \Delta_s(t) = T_{\text{samp}} \end{aligned}$$

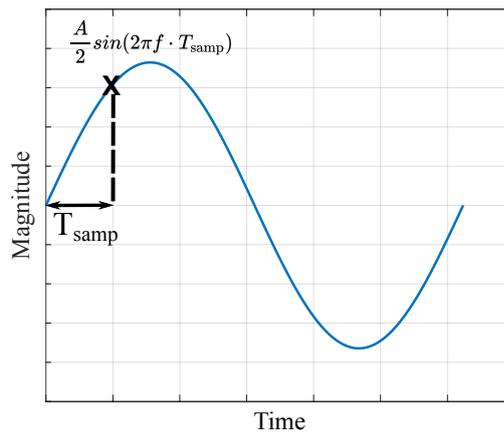


Figure 2.3: Tracking scheme intersection moment for the slope of the input signal at  $T_{\text{samp}}$  and the slope of the sample interval  $T_{\text{samp}}$ .

The approach demonstrates the relation between the slope of the dynamic reference signal and the slope of the input signal. The comparator processes the validation of the level-crossing event. In this context, the system clock selection for generating the digital reference step refers to the reciprocal value of the system delay ( $\tau_d = T_{\text{samp}} = f_{\text{clk}}^{-1}$ ).

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Since the boundaries for the level-crossing detection limit the minimum delay due to the system properties, this approach also conditions the sampling interval equality to the system delay. As a result, the continuous tracking scheme of the ADC system generates a comparison between  $V_{in}$  and  $V_{ref}$  for every clock cycle of the counter ( $f_{clk}$ ). Ideally, every comparison provides a valid sample as for the case of a static signal. However, for a dynamic input signal, the tracking ADC may need several clock cycles to validate a sample, as indicated in figure 2.2(b). The described behavior refers to the system properties regarding the internal delay ( $\tau_d$ ) and resolution to characterize the reference step. Thus, the characterization constrains the slope of the dynamic reference signal in terms of the sampling interval ( $T_{samp}$ ) and the quantization step ( $q$ ). It characterizes the ability to intersect the input signal. Furthermore, the relationship establishes mapping several sampling intervals to several quantization steps until a level intersection validates. The relation between the number of sampling steps and quantization steps is related to the actual input signal slope. Since the number of steps can vary with the actual slope, the sampling is non-uniform. The following hypothesis results:

**Hypothesis:**

Non-uniform sampling is decisive about the binary mapping. The number of effective bits depends on the number of successive samples.  $q$  relates  $T_{samp}$ .

**Approach:**

There is a resolvable quantization step at any equal slope between the input signal ( $V_{in}$ ) and the dynamic reference signal ( $V_{ref}$ ).

**Resolution related Bandwidth Limitation**

With the dependence of equal slopes at any successive sample, a transformation establishes. The transformation determines the deviation to the number of sampling steps in time and the corresponding deviation in magnitude (quantization step number referring to voltage) until a signal intersection ensures. This transformation derives from the tracking ADC scheme, which establishes a linear dependency between quantization steps and sampling times. Every increase in quantization steps is processed by the clock frequency of a counter, generating the digital reference signal, which transforms to an analog representation by the DAC. A stair-step function as depicted in figure (Fig. 2.4) develops.

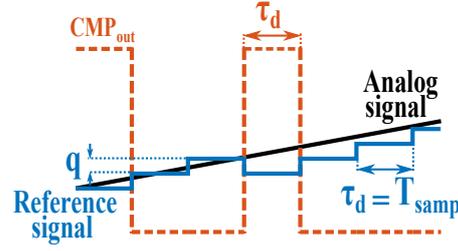


Figure 2.4: Stair-step function of the dynamic reference signal of a tracking scheme ADC. The quantization step ( $q$ ) and the sampling time ( $T_{\text{samp}}$ ) are in linear dependency. The sampling time is determined by the system delay ( $\tau_d$ ) and needs to be at least equal ( $T_{\text{samp}} = \tau_d$ ).

The transformation between the number of sampling steps and the number of quantization steps can be represented by "Bernstein's Theorem" [23]. It relates the slope of the input signal to the slope of the reference step. In this context, the ratio between a quantization step ( $q$ ) and a general sampling step function ( $\Delta_s(t)$ ), defined as a delta in time between consecutive sampling steps, represents the reference slope. It results in the transformation prescription in equation 2.1:

$$q \hat{=} \frac{d}{dt} f(t) \cdot \Delta_s(t) \quad (2.1)$$

By the application of the "Bernstein Theorem," the maximum input signal slope can be defined. The intersection between the slope of the reference step ( $q\Delta_s(t)$ ) and the maximum slope of the input signal derives a necessary condition. Therefore, to ensure the intersection, the input signal slope must be smaller than the slope of the reference step represented by  $q$  and  $\Delta_s(t)$ . To simplify the condition, the delta between consecutive sampling steps represents the sampling interval for a step validation of the Tracking ADC ( $T_{\text{samp}}$ ). It relates to the system delay limitation and the system clock, respectively. The definition of a limitation concerning the input signal slope applies to a sinusoidal assumption in the following. In these terms, the sine function represents any possible slope within a single half-wave. Thus, the input is modeled by half of the amplitude  $A/2$ . Furthermore, the input frequency declares the signal variation within a time-magnitude relation. Thus, the maximum input frequency ( $f_{\text{max}}$ ) related to the intersection represents the maximum slope. In summary, the intersection of a sinusoidal input signal and the reference signal must respect the following condition, described in [31]:

$$q \hat{=} \frac{d}{dt} f(t) \cdot \Delta_s(t) \quad \Rightarrow \quad \left| \frac{d f(t)}{dt} \right| \leq \frac{q}{T_{\text{samp}}}$$

$$\left| \frac{d}{dt} \frac{A}{2} \sin(2\pi f_{\text{in}} \cdot t) \right| \leq \frac{q}{T_{\text{samp}}} \quad (2.2)$$

In application of equation 2.2, the relation between the input signal slope and the tracking ADC system parameter results. The maximum applicable frequency of the sinusoidal input defines the bandwidth ( $f_{\text{in}} \rightarrow f_{\text{max}}$ ) and the maximum slope results for the derivative if the cosine function equates to "1":

$$|A\pi f_{\text{in}} \cos(2\pi f_{\text{in}} \cdot t)| \leq \frac{q}{T_{\text{samp}}}$$

$$\max(\cos(2\pi f_{\text{max}} \cdot t)) \leq \frac{q}{A\pi f_{\text{max}} T_{\text{samp}}}$$

$$1 \leq \frac{q}{A\pi f_{\text{max}} T_{\text{samp}}} \quad (2.3)$$

By the translation of the expression to the related ADC system parameters regarding resolution ( $N$ ) and conversion frequency ( $f_{\text{samp}}$ ), the slope approximation by "Bernstein Theorem" results in equation 2.4. Therefore, the signal amplitude ( $A$ ) is related to the ADC full-scale range by the number of bits ( $N$ ) due to  $A = q \cdot 2^N$ . Furthermore, the sampling time relates to the reciprocal by the sampling frequency ( $f_{\text{samp}} = T_{\text{samp}}^{-1}$ ). In this context, the resolution related bandwidth limitation ( $f_{\text{max, res}}$ ) results in equation 2.4.

$$f_{\text{max}} \leq \frac{q}{A\pi \cdot T_{\text{samp}}} = \frac{f_{\text{samp}}}{\pi \cdot 2^N} \quad \Rightarrow \quad \boxed{f_{\text{max, res}} \leq \frac{f_{\text{samp}}}{\pi \cdot 2^N}} \quad (2.4)$$

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### **Evaluation:**

Equation 2.4 defines the maximum frequency ( $f_{\max, \text{res}}$ ) for a selected resolution ( $N$ ) of a tracking scheme ADC. The result indicates the dependency to the sampling frequency, which boundaries derive from the inverse of the propagation delay in the feedback path of the ADC and define the sampling time ( $f_{\text{samp}} = T_{\text{samp}}^{-1}$ ). Due to the limitation of the inequality, which implies that the slope of the input signal needs to be smaller or equal to the slope of the dynamic reference signal, the maximum input bandwidth ( $f_{\max, \text{res}}$ ) has an injective relationship. So a selected resolution describes the bandwidth restricted to the maximum frequency, on the one hand. On the other hand, the inequality allows no statement about an effective resolution for frequencies differing from the bandwidth limitation.

## Absolute Bandwidth Limitation

The evaluation reveals the injective property of equation 2.4. In order to define further frequency limitations based on the level-crossing approach, the expected slope for any single resolution needs to be derived again because the effective resolution relates to the conversion frequency. However, the derivation of a dynamic system, where the effective resolution decreases with increasing input slope (frequency), obviously turns out to be complex at this time. Indeed, the absolute frequency limit of the ADC represents an apparent boundary condition. In general, the Nyquist-bandwidth characterizes the absolute frequency limitation of many uniformly sampled ADCs [3]. The Nyquist theorem states the complete reconstruction ability of a signal by a sampling rate twice the signal bandwidth [35]. Alternatively, the bandwidth represents the frequency limit until the ADC can detect an alias-free conversion result. Therefore, a similar concept applies to these boundary conditions by introducing a tracking scheme based on the linearity condition postulated by the hypothesis:  $q$  relates to  $T_{\text{samp}}$ .

Triangular reference signal:  $f(t) = \frac{2A}{T_{\text{sig}}} \cdot t$

Sampling interval ( $T_{\text{samp}}$ ):  $\Delta_s(t) = T_{\text{samp}}$

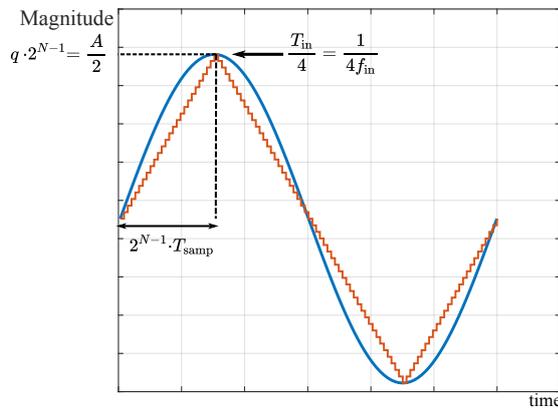


Figure 2.5: Intersection of the sinusoidal input signal and the developing triangular reference signal at  $2^{N-1} \cdot T_{\text{samp}}$ .

The maximum and the minimum of the input sine wave characterize the switching moments of the tracking ADC based on a triangular staircase function. Thus, in consideration of the absolute bandwidth, it is necessary to determine the maximum and minimum of input sine wave. Hence, the time to reach the maximum voltage level. Based on the counter clock frequency, the time until reaching the maximum voltage level by continuous counting is decisive about the "Nyquist"-related frequency. The maximum of the sine wave is present for a quarter of the period ( $T_{\text{sig}}$ ) concerning the origin. Thus the relation between the origin and the maximum results in half of the sine wave amplitude. A linear function between the number of quantization steps ( $q$ ) and sampling steps ( $T_{\text{samp}}$ ) establishes. Since binary operations characterize an ADC, a representation for the "1-bit" cross-section within the bandwidth needs to be assumed for the maximum and minimum of the sine wave as the absolute limit. Therefore, the sampling time ( $T_{\text{samp}}$ ) occurs between the two intersections of the triangular staircase function. Figure 2.5 illustrates the assumptions in which these dependencies for the first intersection derive the function for the triangular signal at a quarter of the signal period ( $T_{\text{sig}}/4$ ).

Referred to the hypothesis that the number of effective bits depends on the number of successive samples, the criterion concerns two intersections between the input signal and the dynamic reference signal. Therefore, the assumed "Bernstein Theorem" transformation between the resolution ( $q$ ) and the sampling time ( $T_{\text{samp}}$ ) can be applied with the assumption of a staircase contemplation between  $q$  and  $T_{\text{samp}}$ .

$$q \hat{=} \frac{d}{dt} f(t) \cdot \Delta_s(t) \quad \Rightarrow \quad \left| \frac{d f(t)}{dt} \right| \leq \frac{q}{T_{\text{samp}}} \quad \Leftrightarrow \quad \left| \frac{d}{dt} \frac{2A}{T_{\text{sig}}} \cdot t \right| \leq \frac{q}{T_{\text{samp}}} \quad (2.5)$$

The derived inequality represents a relationship between the maximum of the input signal and the maximum number of sampling steps. By replacing the amplitude by the linear correspondence of  $q \cdot 2^{N-1}$  steps and the equality of the conversion frequency to the sampling time ( $f_{\text{samp}} = T_{\text{samp}}^{-1}$ ) equation 2.6 results.

$$q \cdot 2^{N+1} \cdot f_{\text{bw}} \leq \frac{q}{T_{\text{samp}}} \quad \Rightarrow \quad \boxed{f_{\text{bw}} \leq \frac{f_{\text{samp}}}{2^{N+1}}} \quad (2.6)$$

### **Evaluation:**

Equation 2.6 defines the maximum input frequency ( $f_{bw}$ ) of an ADC for the limitation of an effective resolution of "1-bit" (i.e. zero level crossing). The result is related to the counter clock frequency, which boundaries refer to the inverse of the propagation delay in the feedback path of the ADC and defined as sampling time ( $f_{clk} = T_{samp}^{-1}$ ). Compared to the maximum frequency ( $f_{max_{res}}$ ) for a selected resolution, the absolute frequency ( $f_{bw}$ ) is higher by a factor of  $\pi/2$ . However, in this case, the resulting function also reveals an injective property since the limit of the "1-bit" resolution characteristic is valid for any frequency below the stated limit.

### **2.1.2 Crest-ratio Derivation based on RMS to Peak value Definition**

The "Bernstein's Theorem", derived in equation 2.1, relates the slope of one signal type referred to the input to the slope of another signal type referred to the reference signal. The proposed approach assumes a sinusoidal input signal type, which intersects by the generated reference signal. The reference signal, in turn, develops to a triangular staircase function under the assumption of an accelerated step generation rate. However, the relation between these signals introduces an error. This error is related because the ADC can not determine the exact intersection between the sine wave and the reference signal due to the sampling time ( $T_{samp}$ ). Therefore, a valid assumption to average the crossing section related to the sampling time is by determining the mean deviation from the exact intersection. The derivation of the Root-Mean-Square (RMS) for each signal depicts a common approach in signal processing [36]. Thus, the RMS value of each signal type represents an approximation for the exact intersection of the signals, which considers the average error by sampling. Equation 2.7 and equation 2.8 derive the RMS value for the sine wave and the triangular reference signal.

$$E [V_{sine}^2] = \frac{2}{\pi} \int_0^{\pi/2} [V_{pk} \sin(\Theta)]^2 d\Theta = \frac{V_{pk}^2}{2} \Leftrightarrow V_{rms_{sine}} = \sqrt{E [V_{sine}^2]} = \frac{V_{pk}}{\sqrt{2}} \quad (2.7)$$

$$E [V_{trian}^2] = \frac{2}{\pi} \int_0^{\pi/2} \left[ V_{pk} \frac{2}{\pi} \Theta \right]^2 d\Theta = \frac{V_{pk}^2}{3} \Leftrightarrow V_{rms_{trian}} = \sqrt{E [V_{trian}^2]} = \frac{V_{pk}}{\sqrt{3}} \quad (2.8)$$

To represent the intersections of the entire signal, the peak value  $V_{pk}$  of the alternating signals is decisive. As derived, the error introduced by the sampling time ( $T_{s\text{amp}}$ ) can be considered by approximating the RMS values of both signals. Since the RMS value for different signal types also differs, an additional deviation is caused related to the RMS shift between these signals. Figure 2.6 illustrates the RMS values for the sine wave and the triangular staircase function. The shift between these values is stated by  $\Delta V_{rms}$ .

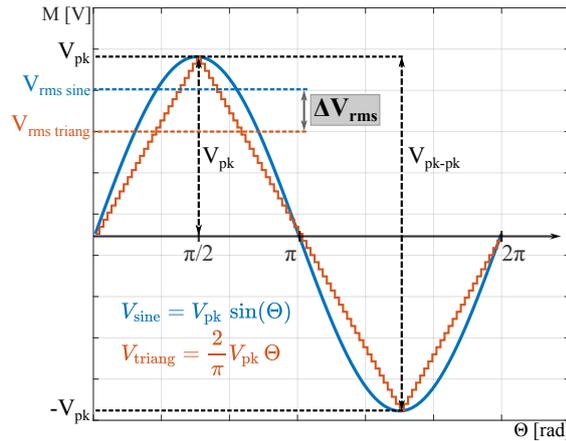


Figure 2.6: Deviation between RMS value of a sine wave ( $V_{rms\ sine}$ ) and the rms value of the triangular reference signal ( $V_{rms\ triang}$ ). The intersection based on the slope of both signals related to "Bernstein's Theorem" considers the peak value ( $V_{pk}$ ) of these signals. The derivation of the intersection is determined for the RMS value. Thus the ratio between the RMS value of the sine wave and the triangular function needs to be adjusted by the crest ratio approach.

The shift between the RMS values introduces an uncertainty which is referred to the relation between  $V_{pk}$  and  $V_{rms}$  for each signal. The conversion between peak value and RMS value as given in equation 2.7 and 2.8 of a signal is well understood and a common approach in signal processing. The technical term of the ratio between  $V_{pk}$  and  $V_{rms}$  is defined as "crest factor" in literature [37].

Related to "Bernstein's Theorem" a multiplication between the slope of the input signal and the reference signal defines the intersection moment. The introduced error based on sampling considers the signal RMS values on the one hand. On the other hand, the peak value  $V_{pk}$  represents the entire signal. Therefore, a translation between both signals is a crucial parameterization. The crest factor offers a common approach. In these terms,

it needs to be considered that the peak value of both signals is equal. Thus, the relation between the intersection moments derives from the ratio of the crest factor for the sine wave and the crest factor for the triangular wave as depicted in equation 2.9.

$$\sqrt{2} V_{\text{rms sine}} = \sqrt{3} V_{\text{rms trian}} \Leftrightarrow \Gamma_{\text{crest}} = \frac{V_{\text{rms sine}}}{V_{\text{rms trian}}} = \sqrt{\frac{3}{2}} \quad (2.9)$$

The parameter of the ratio between the RMS values of both signals are introduced as the "crest ratio ( $\Gamma_{\text{crest}}$ )" in the following and applied to any intersection assumption in this work. Besides, a scope about the validity of  $\Gamma_{\text{crest}}$  must be specified. Since it is representative to the RMS values of the signals, the simple multiplication of the "Bernstein's Theorem" function with  $\Gamma_{\text{crest}}$  normalizes the equation in consideration within the half of the sine wave amplitude (i.e.  $V_{\text{pk}}$ ). The assumption is valid for the consideration of the simple intersection by level-crossing. An example is given by the definition of the maximum bandwidth for a selected resolution in equation 2.4 since any slope is present within half of the signal period. If the signal relation applies for the entire period, the RMS value to be considered appears for the first and the second half of the period. This aspect applies to the Nyquist-related bandwidth in equation 2.6 where intersections occur for the maximum and the minimum of the signal. Therefore, the multiplication of the "Bernstein's Theorem" function with the crest ratio needs to be quadratic, thus developing the normalization factor to  $\Gamma_{\text{crest}}^2$ .

### 2.1.3 Transfer of the Mathematical Approach to Tracking Scheme ADCs

The transfer of the mathematical derivation to tracking scheme ADC systems requires the definition of technical parameters. So far, the derivation of the mathematical system was related to the sampling time, which is equal to the propagation delay of the feedback configuration ( $T_{\text{samp}} = \tau_d$ ). Furthermore, the sampling time was translated to a sampling frequency ( $f_{\text{samp}}$ ) to define a sampling/conversion rate. In this context, the terminology of the sampling frequency transfers to the clock frequency of the system ( $f_{\text{samp}} \rightarrow f_{\text{clk}}$ ). The mathematical derivation has defined frequency limitations for a tracking scheme ADC. One limitation defines the frequency limit for the specified resolution 2.1.1, and the other limitation defines the bandwidth as an absolute frequency limitation 2.1.1. Both

approaches need to be considered separately because the boundaries for intersecting slopes between input and reference differ regarding the maximum and minimum peak values  $V_{pk}$  of the input signal.

The slope for a frequency limit referred to a specific resolution is based on assuming that the reference signal can track the input signal by the specified resolution at any intersection within the signal. The representation of any slope within a quarter of the input signal period ( $T_{sig}/4$ ) claims to the consideration of the maximum slope. If the tracking for a specific system configuration is possible for the maximum slope, the parametrization enables the tracking for the entire signal. This aspect implies that the internal system delay constrains the clock frequency, which acts as the reference step generation rate. Therefore, the clock frequency ( $f_{clk}$ ) equals to the sampling rate ( $f_{samp}$ ). Figure 2.7 illustrates the concept of the translation between the sampling frequency and the clock frequency by equality of the time periods ( $T_{clk} = T_{samp}$ ).

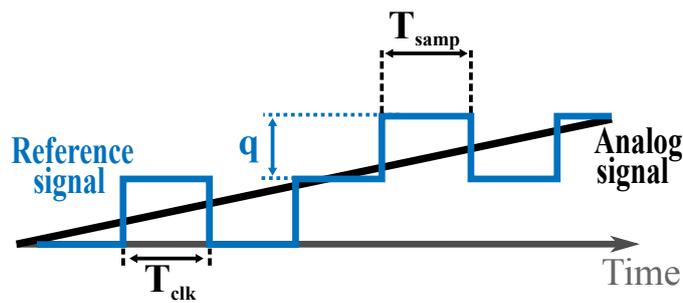


Figure 2.7: System parameter transfer between sampling time  $T_{samp}$  and digital clock period  $T_{clk}$  assumed as equal.

The derivation of the "crest-ratio ( $\Gamma_{crest}$ )" illustrates that the expressions for the bandwidth limitations are incomplete with respect to the input and reference signal relations. Thus, equation 2.4 and 2.6 require adjustments. Concerning the resolution-related bandwidth limitation, the maximum slope is located within  $T_{sig}/4$ . Therefore, the adjustment by the crest ratio applies to the simple approximation by  $\Gamma_{crest}$  as derived in section 2.1.2. Thus, the re-evaluated frequency limit based, which classifies for the tracking scheme ADC approach, arises to equation 2.10.

$$\Gamma_{\text{crest}} = \sqrt{\frac{3}{2}} \quad \Rightarrow \quad f_{\text{maxres}} \leq \sqrt{\frac{3}{2}} \cdot \frac{f_{\text{clk}}}{\pi \cdot 2^N} \quad (2.10)$$

The other limitation specifies the effective resolution limit for a "1-bit"-resolution correspondence. It describes the absolute bandwidth limitation (Eqn. 2.6) for the intersection with the maximum and minimum sinusoidal function. Thus, a triangular stair-step function develops, which slope concurrently defines the intersection between the input signal and the triangular reference signal at the ADC input frequency limit. Under the same consideration as for the resolution-related bandwidth limitation, the clock period matches the system constraints for the internal delay ( $\tau_d$ ), which again implies matching the sampling time. ( $T_{\text{samp}} = T_{\text{clk}}$ ). In this case, the signal development reveals an intersection with the signal maximum of a half-wave sinusoidal input for  $2^{N-1}$  reference steps generated by  $f_{\text{clk}}$ . Figure 2.8 illustrates the principle.

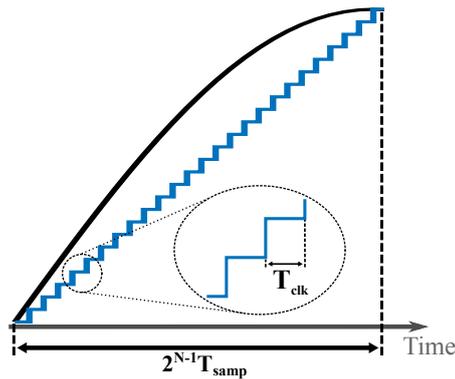


Figure 2.8: Translation between sampling time  $T_{\text{samp}}$  and digital clock period ( $T_{\text{clk}}$ ) for a tracking scheme development based on a triangular function. The intersection of the input and the triangular function is related to the slope ( $q/T_{\text{clk}}$ ). Thus the sampling time can be related to the clock period ( $f_{\text{samp}} = f_{\text{clk}}$ ).

Again, the "crest-ratio ( $\Gamma_{\text{crest}}$ )" should normalize equation 2.6 concerning the assumption of the relation between the peak value and RMS value. Based on the claim to reconstruct the input signal, two intersection moments between the developing triangular reference signal and the input signal are necessary, as illustrated in figure 2.5. In the actual input signal context, the RMS deviation refers to an intersection with the negative peak value ( $-V_{\text{pk}}$ ) and the positive peak value ( $+V_{\text{pk}}$ ). The requirement for these intersections derives from the Nyquist criterion [35]. However, this aspect implies a twofold step consideration of the normalization by the crest-ratio. Thus, the RMS value belongs to the first half and the second half of the period. Related to the "Bernstein Theorem", the normalization corresponds to a multiplication of the crest ratio factor. Thus, a squared version of this correction factor results ( $\Gamma_{\text{crest}}^2$ ). The normalized frequency limit for the absolute bandwidth ( $f_{\text{max}_{\text{bw}}}$ ) for an ADC classified by a tracking scheme arises from Equation 2.11.

$$\Gamma_{\text{crest}}^2 = \frac{3}{2} \quad \Rightarrow \quad \boxed{f_{\text{max}_{\text{bw}}} \leq \frac{3}{2} \cdot \frac{f_{\text{clk}}}{2^{N+1}}} \quad (2.11)$$

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## 2.1.4 MATLAB Simulation Model for Tracking Scheme ADCs

A MATLAB simulation model enables the verification process for tracking scheme ADCs. Application related, the model should be traced back to a simplified version of the tracking scheme ADC. Inspired by the Tracking ADC sampling scheme, the simulation model implements the required fundamental properties. The implementation implies that the basic sub-modules take the behavior of a comparator, a digital-to-analog converter (DAC), and the digital algorithmic part. Based on the Tracking ADC approach, a counter with an up-down counting option constitutes the digital algorithmic part. The individual submodules connect in a feedback configuration. Figure 2.9 illustrates the conceptual block diagram of the MATLAB simulation model. The counter generates the digital reference scheme, converted into a proportional reference voltage ( $v_{ref}$ ). The comparator module processes the task to compare the reference voltage with the analog input voltage ( $v_{in}$ ). Upon the result of the comparison ( $v_{ref}$  above or below  $v_{in}$ ), the comparator module changes its output state in a binary manner ("1-bit" digital stream) to provide the up-down signal for the counter. The counter, in turn, decides the binary counting polarity (up or down) by the reference of the comparator output and passes the updated information to the DAC to provide an updated version of the reference signal. In this way, the basic module implementation can track the continuous input signal ( $v_{in}$ ).

Additional modules are required to map the behavior of an ADC to a MATLAB simulation model. The "Sine wave generator" generates a sinusoidal signal based on the initial information of amplitude ( $A$ ) and input frequency ( $f_{in}$ ). Furthermore, a high-resolution time step ( $t$ ) is predefined. The higher the time resolution, the more accurate time steps can develop, which is necessary since the application of a tracking scheme ADC implies a non-uniform time sampling. However, MATLAB processes vectorial representations. Therefore, the non-uniform behavior adjusts to the sampling time steps related to the comparator frequency ( $f_{cmp}$ ) and the clock frequency ( $f_{clk}$ ). A "Time step Synchronizer" in each case takes on the task of synchronizing the time vector ( $t$ ) both with the clock frequency ( $f_{clk}$ ) and with the comparator frequency ( $f_{cmp}$ ). The comparator frequency represents the inverse of the averaged propagation delay of the entire feedback path from the counter over the DAC to the comparator and back to the counter. In the case of a Tracking ADC, the boundary condition of the maximum propagation delay in the feedback path determines the maximum sampling frequency ( $f_{samp}$ ), thus ( $f_{clk} = f_{cmp}$ ).

With the application of a continuous system based on the vectorial MATLAB representation, a "for-loop" updates the propagation delay ( $t_{cmp_{nxt}}$ ) and the clock period ( $t_{clk_{nxt}}$ ) with every comparison where these times are equal to the input time vector ( $t$ ). With every update ( $n$ ) the counter module is updated based on the comparator signal update ( $t_{cmp_{nxt}}$ ) and the

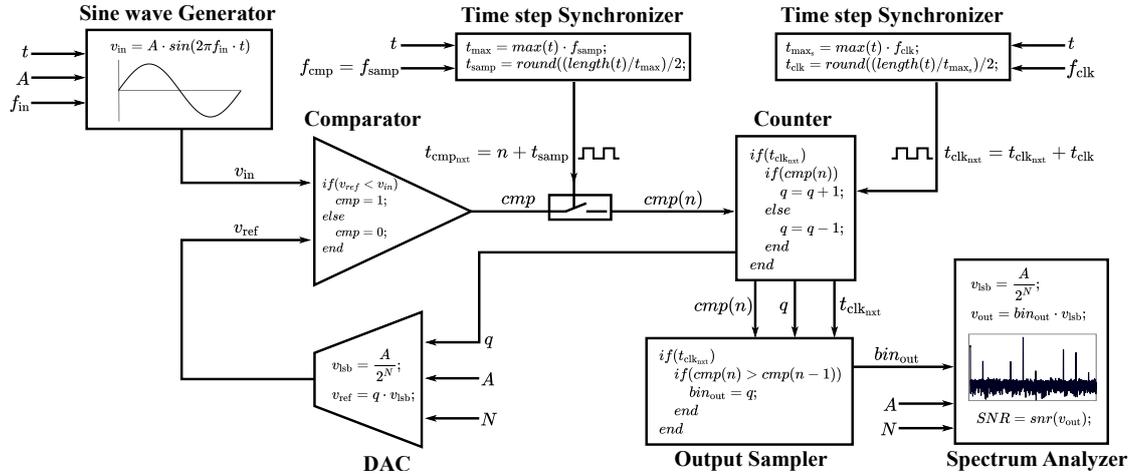


Figure 2.9: Block diagram of the MATLAB simulation model for tracking scheme ADCs. The ADC block diagram is constituted by the comparator, the counter and the digital-to-analog-converter (DAC). The basic components are connected in a feedback configuration. The comparator compares the input signal ( $v_{in}$ ) with a dynamic reference signal ( $v_{ref}$ ) and causes the counter to turn its counting direction. The counter generates the digital code which is converted into the reference signal by the DAC. Both time synchronizer represent the applied frequencies for the clock ( $f_{clk}$ ) and for the propagation delay of the comparator ( $f_{cmp}$ ). The sampled binary output ( $bin_{out}$ ) is analyzed by a spectrum analyzer regarding signal-to-noise-ratio.

clock update ( $t_{clk_{nxt}}$ ). The binary counter update ( $q$ ), generated based on the up or down counting condition, is passed to the DAC. The DAC computes the LSB voltage ( $v_{lsb}$ ) based on the input signal amplitude ( $A$ ) and the ADC resolution ( $N$ ). In order to generate the dynamic reference voltage ( $v_{ref}$ ) the LSB voltage is multiplied by the binary input ( $q$ ). The "Comparator" decides if  $v_{ref}$  is smaller or greater than  $v_{in}$  and generates a binary output stream based on this decision. The following sampling ( $t_{cmp_{nxt}}$ ) forwards the decision back to the counter via the  $cmp(n)$  signal.

This conversion process generates a continuous, binary output. Due to the application of a tracking scheme that needs to validate every conversion by a bit toggle, the direct evaluation of the binary counter stream falsifies the signal information. Therefore, the binary counter output ( $q$ ) needs to be sampled by an "Output Sampler". With every update of  $t_{cmp_{nxt}}$  the sampler compares the updated comparator signal ( $cmp(n)$ ) with

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its predecessor ( $cmp(n - 1)$ ). If a valid transition ( $cmp(n) > cmp(n - 1)$ ) related to a comparator rising edge detection was found, the binary output stream ( $bin_{out}$ ) updates the binary counter value ( $q$ ).

The MATLAB simulation model implemented in this way represents a behavioral model to simulate the binary output ( $bin_{out}$ ), the reference voltage ( $v_{ref}$ ) and the comparator output ( $cmp$ ) based on an input signal ( $v_{in}$ ) for a continuous-time tracking scheme ADC. So, the waveforms of these signals represent a transient model of the ADC, which can evaluate the static behavior of the ADC. In order to evaluate the dynamic behavior of the ADC, the spectrum of the ADC output waveform ( $bin_{out}$ ) is decisive. Therefore, the "Spectrum Analyzer" module calculates the signal-to-noise ratio of a high number of converted sine wave cycles based on the output voltage ( $v_{out}$ ). Beforehand, the binary output stream ( $bin_{out}$ ) normalizes to  $v_{out}$  related to the reference LSB voltage ( $v_{lsb}$ ). The determination of the signal-to-noise ratio also provides information about the effective resolution based on the ENOB for the ADC. This information defines the foundation to analyze the ADC model regarding input bandwidth limits.

### Simulation model uncertainty

Every modeling of the real-world behavior of a derived system is related to an uncertainty based on parametric assumptions or behavioral validation applications. In order to determine the accuracy of the behavioral ADC model, investigations regarding ADC constraints and evaluation schemes of the results were necessary. Therefore, the digital output of the ADC was evaluated by spectral properties based on the signal-to-noise ratio to derive valid statements. The basic functionality of the tracking ADC provides conversion results if the reference signal crosses the input signal. Ideally, the system is limited to the bandwidth referred to as "Nyquist". Based on the definition of "Nyquist" these assumptions are valid for a uniform sampled signal. Alias-free reconstruction is possible for a sampling rate twice the allowed input signal bandwidth [35]. Contrary, the tracking scheme conversion is non-uniform and provides a conversion result upon the crossing of signals, independently if it is within the "Nyquist"-band. However, the spectral evaluation by the Fourier-Transform refers to uniform sampling constraints concerning the "Nyquist"-rate. To enable an evaluation based on spectral analysis and thus ensure comparability, a valid statement for the evaluation considers the number of input data to the analyzer, which needs to be high enough for a close approximation. Conversely, the closer the input signal frequency to the absolute bandwidth limit, the less precise the result will be due to non-uniform conversion.

Based on these assumptions, the behavioral ADC model was evaluated regarding absolute limitations. In conclusion, the analysis revealed an imprecision of the spectral evaluation, related to a conversion caused by non-uniform sampling, below an effective resolution of 2 bits. The probability of converting a resolution below 2 bits cannot be predicted reliably by the signal-to-noise ratio. Nevertheless, to provide an analysis system that compares to the state-of-the-art for uniform sampling systems, the results for the SNR above the 2-bit limit are accurate enough. Therefore, a limitation approximates the results evaluated by the spectral analysis. The approximation considers the geometrical mean of the two-bit representation in order to include statistical deviations. As a result, the inaccuracy limit  $\text{SNR} = 6.02\sqrt{2} + 1.76 \text{ dB} = 10.27 \text{ dB}$  considers an approximation validated by simulation results. However, for exact predictions, the derivation of mathematical relations was necessary (section: 2.57). Therefore, the derived equations compare to the MATLAB simulation model under the constraint of a clipping below an effective resolution of 2 bits. Figure 2.10 illustrates the condition for this claim, which compares a simulated SNR signal to a calculated representation.

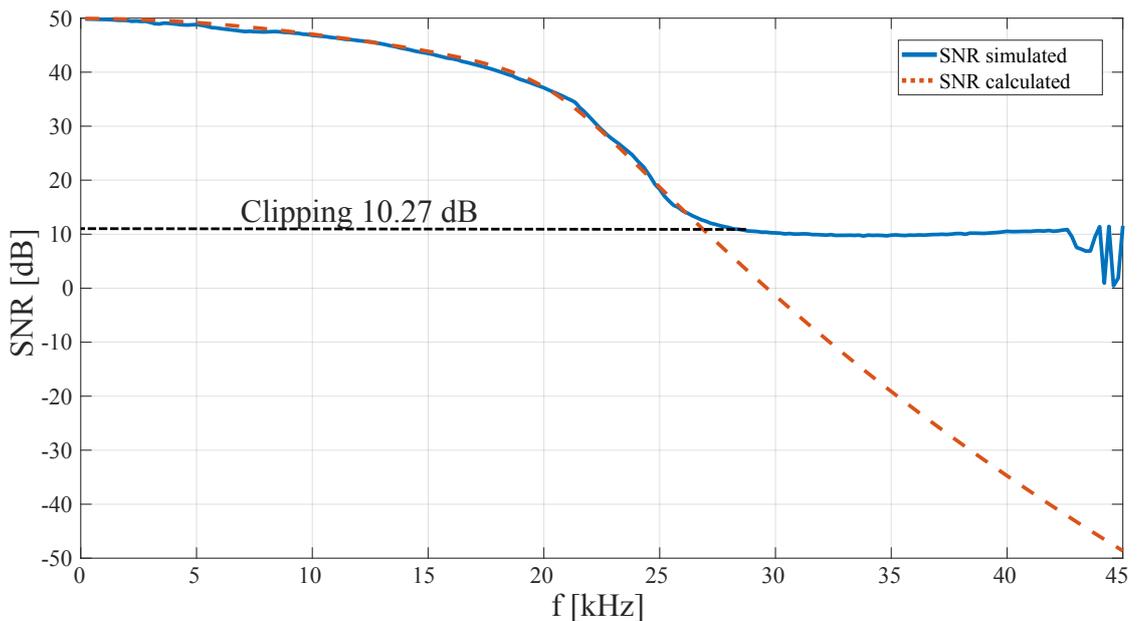


Figure 2.10: Clipping of the simulated SNR at an effective resolution of 2 bit (geometrical mean of 2 bit  $\text{SNR} = 10.27 \text{ dB}$ ) compared to a derived mathematical model (section: 2.57).

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## 2.1.5 Validation of the Mathematical Model for the Bandwidth Limitation

The validation of the derived mathematical model should be applied by the behavioral ADC MATLAB simulation model. Application related, the simulation model classifies a tracking scheme and represents the conventional Tracking ADC as a simplified version. In terms of validation, the mathematical model applied equal Tracking ADC system parameters as in the MATLAB simulation model. In order to validate the derived equations, the result of the frequency limit equation (Eqn. 2.10) referred to a specific resolution and the absolute frequency limitation predicted by equation (Eqn. 2.11) is compared to the MATLAB model. With both equations, the limits of the SNR can be predicted for two distinguished points. Example calculations show the applicability.

The selection of system parameters for the Tracking ADC refers to a resolution of  $N = 8$  bit and a digital clock frequency of  $f_{\text{clk}} = 10$  MHz. Referred to the assumptions met for the derivation of these equations, the input is a sinusoidal signal whose limiting frequencies needs to be determined. With equation 2.10 the maximum input frequency for a specific resolution ( $f_{\text{max}_{\text{res}}}$ ) results in the relation given in equation 2.12. As described in section 2.1.3, the average conversion rate corresponds to the sampling frequency ( $f_{\text{samp}}$ ) equal to the clock frequency ( $f_{\text{clk}}$ ).

Resolution:	$N = 8$ bit
Clock frequency:	$f_{\text{clk}} = 10$ MHz
Conversion rate:	$f_{\text{conv}} = f_{\text{samp}} = f_{\text{clk}} = 10$ MHz

$$f_{\text{max}_{\text{res}}} \leq \sqrt{\frac{3}{2}} \cdot \frac{f_{\text{clk}}}{\pi \cdot 2^N} \quad \Rightarrow \quad \boxed{f_{\text{max}_{\text{res}}} \leq 15.228 \text{ kHz}} \quad (2.12)$$

With equation 2.11, the maximum input frequency to determine the bandwidth ( $f_{\text{max}_{\text{bw}}}$ ) results in the relation given in equation 2.13. As described in section 2.1.3, the average conversion rate corresponds to the sampling frequency ( $f_{\text{samp}}$ ). It is equal to the clock frequency ( $f_{\text{clk}}$ ) since the slope of the generated reference signal derives from the clock frequency. The developing triangular reference signal displays the sinusoidal input.

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Resolution:	$N = 8 \text{ bit}$
Clock frequency:	$f_{\text{clk}} = 10 \text{ MHz}$
Conversion rate:	$f_{\text{conv}} = f_{\text{samp}} = f_{\text{clk}} = 10 \text{ MHz}$

$$f_{\text{max}_{\text{bw}}} \leq \frac{3}{2} \cdot \frac{f_{\text{clk}}}{2^{N+1}} \quad \Rightarrow \quad \boxed{f_{\text{max}_{\text{bw}}} \leq 29.296 \text{ kHz}} \quad (2.13)$$

In order to compare the calculated frequency limits with the simulation model, the signal-to-noise ratio of the simulation model is a crucial parameter representing the bandwidth. Therefore, the frequency of a sinusoidal input signal sweeps within a range of 1 kHz to 45 kHz. In addition, the calculation and the simulation model applied the same input parameters. A resolution of 8 bit and a sampling frequency equal to the clock frequency ( $f_{\text{samp}} = f_{\text{clk}} = 10 \text{ MHz}$ ). The amplitude of the input signal is negligible since the amplitude, and the voltage resolution ( $v_{\text{lsb}}$ ) normalize by the simulation model to investigate the dynamic behavior. This assumption is valid for an input voltage range equal to the comparator voltage range (no clipping) as for real devices. For the sake of completeness, the amplitude ( $A$ ) was selected to 1 V. In order to simulate a correct behavior of a non-uniform sampled signal by a Fast-Fourier-Transform (FFT), an accurate number of sinusoidal cycles ensures to exclude deviations. Therefore, the number of input signal cycles was chosen to 1000. Figure 2.11 illustrates the SNR result of the simulation model over the stated frequency range. Referred to the inaccuracy due to the evaluation by the FFT analysis of the MATLAB simulation model, described in section 2.1.4, the exact intersection for the zero-crossing event of the SNR curve can not be determined by the simulation model. However, as derived in later section 2.3, the mathematical model represents the exact intersection of the SNR course at the zero crossing moment in figure 2.11 and defines the bandwidth limit ( $f_{\text{max}_{\text{bw}}}$ ).

Sinusoidal input signal range ( $f_{in}$ ): [1 kHz  $\rightarrow$  45 kHz]  
 Sampling frequency ( $f_{samp} = f_{clk}$ ): 10 MHz  
 Resolution ( $N$ ): 8 bit

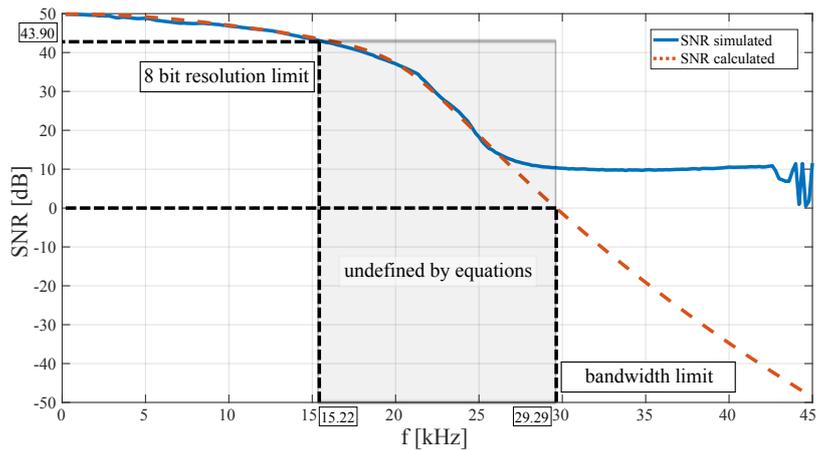


Figure 2.11: Comparison between the mathematical and the simulation model. Simulated curve of the SNR for an input signal range from [1 kHz  $\rightarrow$  45 kHz]. FFT calculation for 1000 sine wave cycle. Resolution-related bandwidth limit at 15.22 kHz (43.90 dB  $\rightarrow$  7 bit). Input signal bandwidth limit at 29.29 kHz (0 dB) which is represented by the calculation model due to simulation inaccuracy.

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The calculated resolution-related bandwidth limit by equation 2.12 of 15.22 kHz corresponds to an SNR of 43.90 dB  $\rightarrow$  7 bit. As expected, the intersection is present at a 1-bit effective resolution drop. Thus,  $N - 1$  applies as the limit for the maximum resolution. This corresponds to a value of  $6.02 \cdot (N - 1) + 1.76$  dB = 43.90 dB. The simulated MATLAB model and the calculated model depicts the exact value for predicting the maximum frequency for the resolution limit. Based on the absolute bandwidth limit at 29.29 kHz, the result is precisely at the expected zero crossing moment of the calculated model. Due to the claim of a "1-bit" sampling limit, the influence of non-uniform sampling is negligible. There are just two possibilities. Either the signal can be sampled by the reference signal slope or not. SNR values below the limit of 6.02 dB can be traced back to the continuous sampling, which implies that an intersection is possible even for higher frequency parts in any case. However, as for the case of uniform sampled ADCs, there is no meaning for these values. Related to "Nyquist", there is no possibility to regenerate the signal from the digitized binary stream.

#### **Evaluation:**

The comparison between the behavioral ADC MATLAB simulation model, the calculated SNR curve, and the derived equations for predicting the frequency limits demonstrate a high level of agreement. Thus two important corner values for designing a tracking scheme ADC classified can be defined. The resolution limit frequency ( $f_{\max_{\text{res}}}$ ) on the one hand and the absolute bandwidth limit ( $f_{\max_{\text{bw}}}$ ) on the other hand.

There is an injective behavior of both equations by defining a maximum frequency for a given resolution but no corresponding effective resolution for a given frequency. The limits define a range. Figure 2.11 illustrates this behavior by indicating a wide frequency range undefined by the equations. In consideration of a non-uniform analog-to-digital conversion, the region between the limits can change drastically. The region can be broader or more narrow depending on the selection of ADC parameters (resolution (N), sampling frequency ( $f_{\text{samp}}$ )) that act as degrees of freedom. As a result, the statement based on the evaluation:

The tracking scheme ADC provides a wide bandwidth range even if it loses a bit of effective resolution. The bandwidth limit predefines the maximum input frequency limitation.

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## 2.2 Mathematical Derivation of the Signal-to-Noise Ratio

The signal processing for ADCs is characterized by the signal-to-noise ratio (SNR) and defines the dynamic behavior. Therefore, the derivation of the signal-to-noise ratio for continuous time ADCs classified by a tracking scheme represents an important basic requirement for the design and the comparability. The assumptions regarding frequency limitation so far only describe two specific frequency analysis within the entire bandwidth. This analysis provides a closed form representation for the maximum frequency limit at the specified resolution and the maximum input frequency referred to absolute bandwidth limit. As examined, these relationships cannot provide any information about the effective resolution of the ADC in between these limits. Since the signal-to-noise ratio defines a direct dependency between the bandwidth and the effective resolution, a mathematical expression for the SNR of a non-uniform sampled ADC should be derived.

In the ideal case uniform sampling schemes consider the noise portion from quantization which only depends on the resolution of the ADC [38]. In comparison, non-uniform sampling schemes consider quantization noise based on resolution as well as quantization noise based on time for non-uniform conversion as depicted in figure 2.2. This consideration results in an error in amplitude/magnitude ( $\varepsilon_a$ ) and an additional error in time ( $\varepsilon_t$ ). Therefore, the traditional approach for the quantization error ( $\varepsilon_a$ ) needs to be extended by the error in time ( $\varepsilon_t$ ). A definition of these errors is described in [23], which combines both as rms total error per sample by

$$\sqrt{E[\varepsilon_{\text{tot}}^2]} = \sqrt{E[\varepsilon_a^2] + E[\varepsilon_t^2]} \quad (2.14)$$

where  $\varepsilon_a$  and  $\varepsilon_t$  are uncorrelated variables. Thus the error in magnitude and the error in time can be determined independently. The background for this assumption concludes from the perspective of the minimum error by quantization. So, due to the quantization nature of a binary signal, the result is determined by a stair-step function. Thus, the best scenario depicts the case if a quasi uniform sampling is applied. The limit for the quasi uniform sampling is stated by the resolution referred frequency limit which is defined by equation 2.10 for tracking scheme ADCs. Below this frequency the ideal condition can be assumed, that a conversion is valid for every sample period ( $T_{\text{samp}}$ ) and the error is reduced to the error in amplitude ( $\varepsilon_a$ ). If the frequency is higher than the resolution limitation, the total error per sample is increased by the error in time. Therefore, the quantization error ( $\varepsilon_a$ ) can be assumed as upper limit. Due to the uncorrelated nature of  $\varepsilon_a$  and  $\varepsilon_t$ , the quantization error can be expressed by the traditional approach for the

power density. The quantization sampling dependency is illustrated in figure 2.12, which relates the quantization error to a single conversion step under the ideal condition.

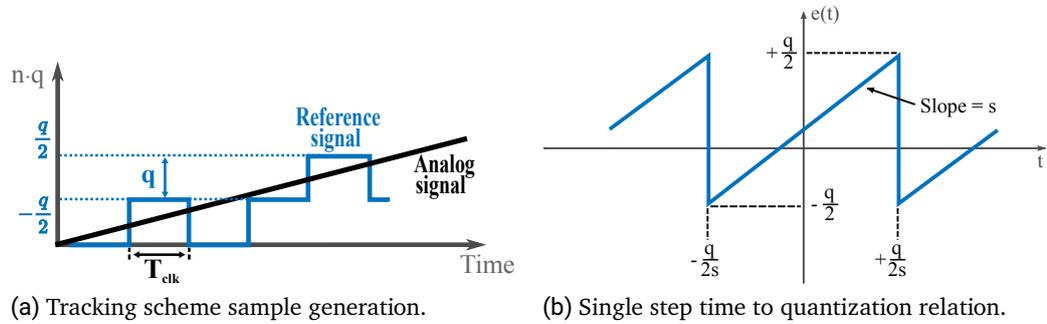


Figure 2.12: Dependency of the quantization error in magnitude ( $\varepsilon_a$ ) within a single sample step. The least significant bit is expressed as  $q$ . Thus the power density of a single step can be calculated mean free by the interval  $[-q/2, q/2]$ .

Based on the single step assumption in figure 2.12 the power density ( $E[\varepsilon_a^2]$ ) and the derived rms quantization error in magnitude ( $\varepsilon_a$ ) can be defined. The integration interval to be considered relates to a single step within  $[-q/2, q/2]$  and can be expressed for a number of steps by the definition of LSB per step to  $[-q/2s, q/2s]$ . Thus, the function of a number of linear increasing steps results in  $f(t_{\text{samp}}) = s \cdot t_{\text{samp}}$ . Equation 2.15 derives the statistical quantization error in magnitude ( $\sqrt{E[\varepsilon_a^2]}$ ) through the power density.

$$\begin{array}{ll} \text{Interval:} & [-q/2s, q/2s] \\ \text{Function:} & f(t_{\text{samp}}) = s \cdot t_{\text{samp}} \end{array}$$

$$E[\varepsilon_a^2] = \frac{s}{q} \int_{-q/2s}^{q/2s} (s \cdot t_{\text{samp}})^2 dt_{\text{samp}} = \frac{q^2}{12} \Rightarrow \boxed{\sqrt{E[\varepsilon_a^2]} = \frac{q}{\sqrt{12}}} \quad (2.15)$$

Based on the statement for the RMS total error per sample ( $\sqrt{E[\varepsilon_{\text{tot}}^2]}$ ) described in [23] the rms error in time ( $\varepsilon_t$ ) defines the noise portion for non-uniform sampling. The error is additive, since an uncorrelated relation can be assumed between the quantization in amplitude and the sampling interval. Similar to the uncertainty within the quantization interval, there is an uncertainty for the sampling interval. Due to the reference signal that is generated by a stair-step function based on  $T_{\text{ref}}$  the exact intersection between the analog input signal and the reference signal can not be determined by the ADC. Rather, an uncertainty error arises due to the time shift between the exact intersection and the samples generated by  $T_{\text{ref}}$ . Where  $T_{\text{ref}}$  is representative for the reference signal generation period of the ADC which is declared as  $T_{\text{ref}} = T_{\text{clk}} = f_{\text{clk}}^{-1}$ . Where the multiple of  $T_{\text{ref}}$  is representative for the sample period  $T_{\text{samp}} = n \cdot T_{\text{ref}}$ . Thus, the uncertainty in time ( $\delta\tau$ ) for the level crossing approach is caused when the analog signal crosses the reference signal during the time interval  $(0, T_{\text{ref}}]$ . Figure 2.13 illustrates the described behavior.

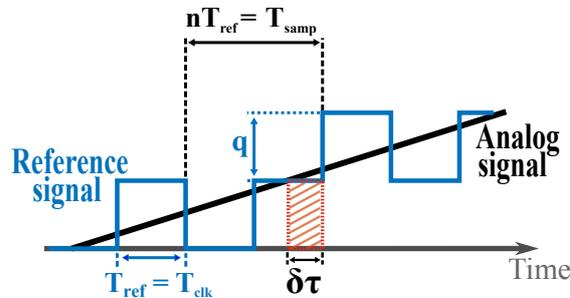


Figure 2.13: Uncertainty in time ( $\delta\tau$ ) for the level crossing approach caused when the analog signal crosses the reference signal during the interval  $(0, T_{\text{ref}}]$ .

Due to the fact that a tracking scheme ADC validates a conversion by level crossing, it is assumed, that the rms error in time can be defined by the level crossing problem described in [23]. The level crossing problem considers the hypothesis derived in section 2.1.1, that asynchronous (non-uniform) sampling is decisive about the binary mapping. The number of bits depends on the number of successive samples, thus that  $q[V]$  relates to  $T_{\text{samp}}[s]$ . Based on this hypothesis the "Bernstein Theorem" can be applied to describe the sampling error in time ( $\varepsilon_t$ ). According to the claim of uncertainty in time the "Bernstein"-relation is sampled by the variable  $\delta\tau$ . The intersection between the input signal and the reference signal relates to the slope of these signals and reveals a statistical uncertainty within the sample interval  $(0, T_{\text{ref}}]$ . Therefore, the definition for the "Bernstein Theorem" transforms to equation 2.16 in order to allow for the uncertainty in time ( $\delta\tau$ ).

$$q \hat{=} \frac{d}{dt}f(t) \cdot \delta\tau(t) \quad (2.16)$$

Related to [23], the analysis of equation 2.16 reveals that the slope of the input signal ( $d/dt f(t)$ ) is a random variable with zero mean, which is independent to the random variable  $\delta\tau$ . This assumption holds true, since the uncertainty in time ( $\delta\tau$ ) is related to the reference signal (generated by  $T_{\text{ref}}$ ) and the slope of the input signal is based on its unadulterated properties. There is no feedback or translation between both signals. Therefore, the power density and statistical deviation can be determined separately. Thus the power density of the "Bernstein Theorem" ( $E[(t \rightarrow q)^2]$ ) can be expressed as the multiplication of the power density of the uncertainty in time ( $E[\delta\tau^2]$ ) with the power density of the slope of the input signal ( $E[(f'(t))^2]$ ) by equation 2.17.

$$E[(t \rightarrow q)^2] \hat{=} E[s_{\text{in}}^2] \cdot E[\delta\tau^2] \quad \Leftrightarrow \quad E[(t \rightarrow q)^2] \hat{=} E[(f'(t))^2] \cdot E[\delta\tau^2] \quad (2.17)$$

As depicted in figure 2.13 the error of temporal uncertainty ( $\delta\tau$ ) can be expected within the sample interval  $(0, T_{\text{ref}}]$ . Therefore, the definition of the power density must refer to the single step of  $T_{\text{ref}}$ . The procedure is related to the definition of the quantization error in amplitude ( $\varepsilon_a$ ), which also considers the deviation within a single step. Based on this method the power density and the statistical error of the uncertainty in time ( $\delta\tau$ ) can be defined by equation 2.18 within the interval  $[-T_{\text{ref}}/2s, T_{\text{ref}}/2s]$ .

Interval:	$[-T_{\text{ref}}/2s, T_{\text{ref}}/2s]$
Function:	$f(t_{\text{ref}}) = s \cdot \delta_t$

$$\boxed{E[\delta_t^2] = \frac{s}{T_{\text{ref}}} \int_{-T_{\text{ref}}/2s}^{T_{\text{ref}}/2s} (s \cdot \delta_t)^2 d\delta_t = \frac{T_{\text{ref}}^2}{12}} \quad \Rightarrow \quad \boxed{\sqrt{E[\delta_t^2]} = \frac{T_{\text{ref}}}{\sqrt{12}}} \quad (2.18)$$

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While the statistical error of the uncertainty in time ( $\sqrt{E[\delta_t^2]}$ ) is based on the sample interval ( $T_{\text{ref}}$ ), the power density and the derived statistical error of the input signal slope ( $\sqrt{E[s_{\text{in}}^2]}$ ) has no related reference. The statement of the intersection between the slopes can only be derived for a range of intersections at this moment, because the exact intersection is based on the relation between the input signal curve and the derived (tracked) reference signal. But the postulation, that there exist an exact intersection can be certainly defined for an interval within the time period of the input signal ( $T_{\text{sig}}$ ). Thus, even without the exact knowledge of the intersection interval the following hypothesis can be defined.

**Hypothesis:**

If at least two intersections between the input signal slope and the reference signal slope exists, it will be in the interval  $[0, T_{\text{sig}}]$ . If it does not exist, the effective resolution is less than "1-bit" and the input signal frequency is not within the ADC bandwidth.

**Approach:**

Since the exact intersection between the input signal slope and the reference signal slope is unknown, the interval for the definition of the power density of the input signal slope extends towards the entire signal period  $[0, T_{\text{sig}}]$ .

With the stated approach it is assumed, that an intersection within the interval  $[0, T_{\text{sig}}]$  of the input signal exists. The hypothesis can be validated based on the curve of the signal-to-noise ratio related to a frequency sweep. Therefore, the noise power of the error in time based on "Bernstein Theorem" will be pursued further. Based on the claim of an existing intersection an expression for the statistical error of the input signal slope ( $\sqrt{E[s_{\text{in}}^2]}$ ) can be derived by equation 2.19. Therefore, the power is considered for the derivative of the half amplitude input signal.

Interval:  $[-T_{\text{sig}}, T_{\text{sig}}]$   
function:  $f(t) = A/2 \sin(2\pi f_{\text{sig}} \cdot t)$

$$E [s_{\text{in}}^2] = \frac{1}{2T_{\text{sig}}} \int_{-T_{\text{sig}}}^{T_{\text{sig}}} \left[ \frac{d}{dt} \frac{A}{2} \sin(2\pi f_{\text{sig}} \cdot t) \right]^2 dt$$

$$E [s_{\text{in}}^2] = \frac{1}{2T_{\text{sig}}} \int_{-T_{\text{sig}}}^{T_{\text{sig}}} [A \pi f_{\text{sig}} \cos(2\pi f_{\text{sig}} \cdot t)]^2 dt$$

$$E [s_{\text{in}}^2] = \frac{A^2 \pi f_{\text{sig}}}{8 T_{\text{sig}}} \cdot [4\pi f_{\text{sig}} T_{\text{sig}} + \sin(4\pi f_{\text{sig}} \cdot T_{\text{sig}})]$$

with  $f_{\text{sig}} = T_{\text{sig}}^{-1}$

$$\Rightarrow \boxed{E [s_{\text{in}}^2] = \frac{A^2}{2} \pi^2 f_{\text{sig}}^2} \Rightarrow \boxed{\sqrt{E [s_{\text{in}}^2]} = \frac{A}{\sqrt{2}} \pi f_{\text{sig}}} \quad (2.19)$$

Equation 2.19 depicts the power density ( $E [s_{\text{in}}^2]$ ) and the statistical error ( $\sqrt{E [s_{\text{in}}^2]}$ ) for the input signal slope. Based on equation 2.17 the relationship can be formed for the entire error in time ( $E [(t \rightarrow q)^2]$ ) which is transformed to a quantization error in magnitude related to the "Bernstein Theorem".

$$E [(t \rightarrow q)^2] \hat{=} E [s_{\text{in}}^2] \cdot E [\delta\tau^2] \Rightarrow E [(t \rightarrow q)^2] \hat{=} \frac{A^2}{24} \pi^2 f_{\text{sig}}^2 \cdot T_{\text{ref}}^2 \quad (2.20)$$

with  $A^2 = 2^{2N} q^2$  and  $T_{\text{ref}}^2 = f_{\text{samp}}^{-2}$

$$\boxed{E [(t \rightarrow q)^2] = \left( \frac{q}{\sqrt{24}} 2^N \pi \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2} \Rightarrow \boxed{\sqrt{E [(t \rightarrow q)^2]} = \frac{q}{\sqrt{24}} 2^N \pi \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)} \quad (2.21)$$

In order to derive the signal-to-noise ratio, from the noise portion defined in equation 2.14 a relation between the input signal power ( $E[f(t)^2]$ ) and the noise portion needs to be established. Therefore, the input signal power must be defined related to the constraint of half of the amplitude ( $A$ ) in order to provide a generalization. Thus, equation 2.22 develops within the entire input interval defined by  $[-T_{\text{sig}}, T_{\text{sig}}]$ .

$$\begin{aligned} \text{Interval:} & \quad [-T_{\text{sig}}, T_{\text{sig}}] \\ \text{function:} & \quad f(t) = A/2 \sin(2\pi f_{\text{sig}} \cdot t) \end{aligned}$$

$$\begin{aligned} E[f(t)^2] &= \frac{1}{2T_{\text{sig}}} \int_{-T_{\text{sig}}}^{T_{\text{sig}}} \left[ \frac{A}{2} \sin(2\pi f_{\text{sig}} \cdot t) \right]^2 dt \\ E[f(t)^2] &= \frac{A^2}{8T_{\text{sig}}} \cdot \left[ T_{\text{sig}} - \frac{\sin(4\pi f_{\text{sig}} \cdot T_{\text{sig}})}{4\pi f_{\text{sig}}} \right] \end{aligned}$$

$$\text{with } f_{\text{sig}} = T_{\text{sig}}^{-1} \quad \text{and} \quad A^2 = 2^{2N} q^2$$

$$\Rightarrow \boxed{E[f(t)^2] = \frac{A^2}{8} = q^2 2^{2N-3}} \quad \Rightarrow \quad \boxed{\sqrt{E[f(t)^2]} = \frac{q}{\sqrt{8}} 2^N} \quad (2.22)$$

The signal-to-noise ratio is based on the relation between the signal power ( $E[f(t)^2]$ ) and total noise power ( $E[\varepsilon_{\text{tot}}^2]$ ). Related to equation 2.14, the total noise power allows for the error on magnitude ( $\varepsilon_a$ ) based on quantization and the error in time ( $\varepsilon_t$ ) which timing uncertainty is transformed to an magnitude representation by the application of the "Bernstein Theorem". Using this relationship the signal-to-noise ratio (SNR) for a tracking scheme based ADC results in equation 2.23.

$$E[\varepsilon_{\text{tot}}^2] = \sqrt{E[\varepsilon_a^2] + E[\varepsilon_t^2]}^2 = \sqrt{E[\varepsilon_a^2] + E[(t \mapsto q)^2]}^2 = E[\varepsilon_a^2] + E[(t \mapsto q)^2]$$

$$SNR = 10 \log \left[ \frac{E[f(t)^2]}{E[\varepsilon_{\text{tot}}^2]} \right] = 10 \log \left[ \frac{q^2 2^{2N-3}}{\frac{q^2}{12} + \frac{q^2}{3} 2^{(2N-3)} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2} \right]$$

$$\Rightarrow \boxed{SNR = 10 \log \left[ \left( \frac{1}{3 \cdot 2^{2N-1}} + \frac{1}{3} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \right)^{-1} \right]} \quad (2.23)$$

### Crest-ratio Normalization for the SNR based on Bernstein Approach

Related to the "Bernstein Theorem" translation an error between the rms values of both intersecting signals is present which is based on the rms value to peak value relation as derived in section 2.1.2. This error is normalized by the relation of the crest factors of both signals and defined as "crest-ratio". At this moment, the derivation and dependencies of the "crest-ratio" within the Bernstein definition assumed in section 2.1.2 becomes clearer. In the formation of the signal-to-noise ratio the power of the signals is considered. As described, the "Bernstein Theorem" relates the power of the signal slope and the power of the sampling time slope to a power at the corresponding intersection moment and transfers the relation to an equivalent power of quantization. The square root of the power defines the root-mean-square (rms) of the signal (i.e.  $V_{\text{rms}}$ ). Thus, the multiplication of the signal power by the application of the "Bernstein Theorem" can be traced back to the multiplication of the signal rms values. However, since the rms values of both signal types differ, an shift of the signal intersection occurs and leads to an additional error. Based on the claim, that the intersection exists for the equivalence of both signal slopes, the intersection can be considered for the peak values of both signals. In the ideal case, they are also equivalent whereby a normalization between the values is represented by the introduced "crest-ratio" ( $\Gamma_{\text{crest}}$ ).

Since it is clarified, that the simple consideration of the Bernstein relation introduces an uncertainty between the rms values of the signals, the relation for the noise power in time characterized by the noise power in magnitude needs to be normalized by the "crest-ratio". Thus, the completely described noise portion sampling results in equation 2.24. It is representative in order to define the normalized signal-to-noise ratio (SNR) in equation 2.25.

$$E_{[(t \mapsto q)^2]} = \Gamma_{\text{crest}} \cdot \left( \frac{q}{\sqrt{24}} 2^N \pi \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 = \sqrt{\frac{3}{2}} \cdot \left( \frac{q}{\sqrt{24}} 2^N \pi \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \quad (2.24)$$

$$SNR = 10 \log \left[ \left( \frac{1}{3 \cdot 2^{2N-1}} + \Gamma_{\text{crest}} \cdot \frac{1}{3} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \right)^{-1} \right]$$

$$SNR = 10 \log \left[ \left( \frac{1}{3 \cdot 2^{2N-1}} + \frac{\pi^2}{\sqrt{6}} \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \right)^{-1} \right] \quad (2.25)$$

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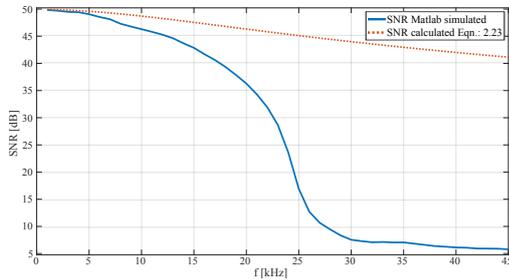
## 2.2.1 Evaluation of the Basic Mathematical SNR Model

The evaluation and validation of the derived mathematical model for the signal-to-noise ratio should be referred to the behavioral ADC MATLAB simulation model. To compare the models, the mathematically determined SNR has the equal parametrization as the tracking scheme ADC developed in the behavioral MATLAB simulation model. Based on the signal course, the applicability and the made hypothesis of the mathematical model can be validated and the absolute bandwidth limitation can be evaluated.

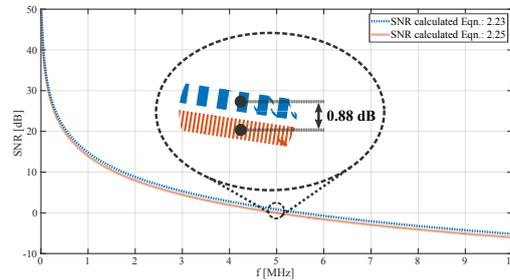
The initial system parameters for the tracking scheme ADC are selected for a resolution of  $N = 8$  bit and a digital clock frequency of  $f_{\text{clk}} = 10$  MHz. The input is defined as sinusoidal signal and ( $f_{\text{in}}$ ) is swept over the expected input range. The average conversion rate corresponds to the sampling frequency ( $f_{\text{samp}}$ ) and equals the clock frequency ( $f_{\text{clk}}$ ).

Figure 2.14(a) shows the course of the simulated and the mathematical signal-to-noise ratio over a considered frequency range of 1 kHz to 45 kHz. The signal courses reveal, that there is a high deviation between both models. The curves only match each other for high signal-to-noise ratios at low frequencies. Obviously, the calculated approach does not match the simulation system. This can be explained by the statement the hypothesis made. So the limitation claimed by the hypothesis is a generalized statement which assumes that an intersection exist within the input signal period. If there is no intersection, the signal is out of bandwidth. However, the hypothesis does provide information about how often and at what intervals these intersections can occur. But this statement is restricted to the single step relation, which assumes that for any time sample ( $T_{\text{samp}}$ ) there is a possible conversion related to the number of bits  $N$ . Therefore, the bandwidth for this kind of structure is limited to the number of samples that can be applied to the input signal, where the number of possible samples is defined by the ratio between signal period and sample time ( $T_{\text{sig}}/T_{\text{samp}}$ ). In order to reconstruct the input signal, the bandwidth is limited by  $f_{\text{sig}_{\text{max}}} = f_{\text{samp}}/2$  which corresponds to the "Nyquist"-frequency.

The generalization made under the hypothesis results in a high probability that the sampling time is included in the signal period. The resolution refers to the number of sampling steps. This property explains the course of the SNR in figure 2.14(b), which shows a rapid drop at the beginning and a flatter course towards the bandwidth limit. At  $f_{\text{sig}_{\text{max}}} = f_{\text{samp}}/2$  the bandwidth limit is reached by the zero crossing moment of the SNR curve. Related to the applied frequency of  $f_{\text{clk}} = 10$  MHz, the limiting frequency reveals in  $f_{\text{max}} = 5$  MHz. Figure 2.14(b) illustrates the bandwidth limit with and without "crest-ratio"-normalization. The deviation corresponds exactly to the missing "crest-ratio"-factor, where  $10 \log(\sqrt{3/2}) \approx 0.88$  dB.



(a) SNR comparison between simulated MATLAB model and calculated equation model.



(b) Calculated equation models: Deviation of the bandwidth limit by the "crest-ratio".

Figure 2.14: SNR comparison between the MATLAB simulation model and the calculated model by equation 2.23. Deviation between the simulated MATLAB model and calculated equation model related to the assumption of existing intersections in the interval  $[0, T_{\text{sig}}]$ , which defines an initial approach. The assumption is comparable to uniform sampling for a bandwidth of  $f_{\text{samp}}/2$ . The deviation between the calculated models by Eqn. 2.23 and Eqn. 2.25 corresponds the crest-ratio by  $10 \log(\sqrt{3/2}) \approx 0.88$  dB.

### **Evaluation:**

The comparison of the signal-to-noise ratio course between the behavioral ADC MATLAB simulation model and the equation based model demonstrates, that there are high deviations between the models. The only match is present for high signal-to-noise ratios at low frequencies. The background regarding the deviation is related to the assumptions made by the hypothesis which provides information about how often and at what intervals intersections can occur. Based on this hypothesis it is assumed, that there exists a valid sample with the maximum resolution at any sampling time ( $T_{\text{samp}}$ ). If the input frequency is higher than the Nyquist frequency, the input signal is out of bandwidth. Under these constraints the investigated behavior can be attributed to any uniform sampled ADC (i.e. Nyquist-rate ADCs). Thus, the derived expression for the signal-to-noise ratio in equation 2.25 can be attributed to any Nyquist-rate ADCs. But the generalization made by the hypothesis is not completely representative for non-uniformly sampled ADCs like tracking scheme ADCs. Due to the non-uniform sampling there are a variety of sampling times which can be a multiple of the minimum sampling time ( $T_{\text{samp}}$ ). Therefore, the generalized hypothesis needs to be adjusted by restrictions in order to reveal a high level of agreement referred to a mathematical equation for non-uniformly sampled conversion schemes.

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## 2.3 Mathematical SNR Derivation for Non-uniform Sampling

The mathematical derivation of the signal-to-noise-ratio based on the hypothesis made in section 2.2 revealed, that the assumed generalization is not completely representative for non-uniformly sampled ADCs but for uniformly sampled ADCs. The generalization excludes a variety of possible samples within the signal period ( $T_{sig}$ ) which are based on a multiple of the minimum sampling time ( $T_{samp}$ ). This background becomes clear if the chosen approach of the "Bernstein theorem" is considered. Due to the choice of a fixed minimum sampling period ( $T_{samp}$ ) the intersection signal is represented for a single bit conversion. But the tracking scheme approach also allows intersections between the slope of the input signal and a multiple of the reference signal period. As a side note, even the multiple of ( $T_{samp}$ ) has the same slope as the minimum reference period because of the linear dependency between magnitude quantization ( $q$ ) and time quantization ( $T_{samp}$ ). However, the difference of the new approach considers the number of possible samplings which is the ratio of  $T_{sig}/T_{samp}$  in the ideal case as for the uniformly sampled signals. In case of non-uniformly sampled signals, the probability of occurrence of a number of valid samples is not predetermined and depends on the signal course of the input signal. The meaning of individual samples is given by figure 2.15, demonstrating the non-uniformly sampled input signal for multiple numbers of the minimum sampling periods.

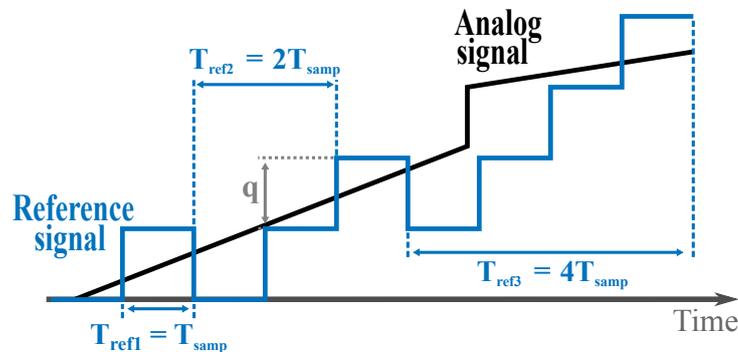


Figure 2.15: Input signal tracking by reference samples  $T_{ref}$  based on a multiple of minimum sampling steps ( $T_{samp}$ ). The number of reference steps refers to the current input signal slope.

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Based on the considerations of the probability of occurrence for a number of valid samples within the signal period and the clarification of the sample scheme development illustrated in figure 2.15 the previously existing hypothesis can be adjusted regarding a non-uniformly sampled signal. The procedure considers, that any possible signal intersection between the input signal and the sampling period reference step introduces a noise portion to the total noise, thus that equation 2.26 is valid.

$$\text{Noise}_{\text{total}} = \text{Noise}(T_{\text{ref}(1)}) + \text{Noise}(T_{\text{ref}(2)}) + \dots = \sum_{i=0}^n \text{Noise}(T_{\text{ref}(i)}) \quad (2.26)$$

Therefore, the hypothesis is extended by the statement, that a variety of sample portions ( $T_{\text{ref}}$ ) as a multiple of the minimum sample time ( $T_{\text{samp}}$ ) can exist within the sample period ( $T_{\text{sig}}$ ). Every sample portion is referred to the input signal slope and introduces noise. The sum of every noise portion defines the total noise which is introduced by sampling. Related to these considerations, the hypothesis for non-uniformly sampled signals can be defined.

**Hypothesis:**

Suppose at least two intersections between the input signal slope and the reference signal slope exist. In that case, it will be in the interval  $[0, T_{\text{sig}}]$  as a variety of sample portions based on the minimum sample time ( $T_{\text{samp}}$ ). If it does not exist, the effective resolution is less than "1-bit" and the input signal frequency is not within the ADC bandwidth.

**Approach:**

The interval for the definition of the power density of the input signal slope is still considered for the entire signal period  $[0, T_{\text{sig}}]$ . The total noise portion is based on the sum of the single noise portions weighted by the number of occurrences within the entire signal period. This approach is valid due to a linear relation between magnitude quantization ( $q$ ) and time quantization ( $T_{\text{samp}}$ ), referred to as the triangular reference signal development. Related to the derived signal-to-noise ratio based on "Bernstein theorem", the maximum number of samples develops with the statement that there is a valid sample for any sample time. Thus, also the maximum power is defined by a uniform assumption. In order to define a non-uniformly sampled approach, the intersection assumption for the derivation of the total noise power needs to be decomposed.

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In the following two methods based on the made hypothesis and the basic approach are presented. Method 1 (described in subsection 2.3.1) considers a special case, which generalizes the sampling time ( $T_{\text{samp}}$ ) to the clock period ( $T_{\text{clk}}$ ) thus that the signal intersection is always present for the clock period. Method 2 (described in subsection 2.3.3) relates the "Bernstein Theorem" to the decomposed power assumption of the hypothesis, thus that the sampling time ( $T_{\text{samp}}$ ) not restricted to the clock period. The advantage of method 2 is the ability to consider alternating feedback delays due to comparator non-linearities or even if the digital reference clock is higher or lower than the maximum feedback delay of the ADC system. A summary of the two methodical approaches regarding the applicability for real devices is given in the following.

**Method 1: SNR for Multi-bit Sampling with Equal Time Variants ( $T_{\text{samp}} = T_{\text{clk}}$ )**

This approach considers that the sampling time is equal to the reference step generation time ( $T_{\text{ref}}$ ) which is the clock for digital systems ( $T_{\text{samp}} = T_{\text{clk}}$ ). Related to an analog-to-digital converter the demand is valid if the comparator propagation time (i.e. switching ability) and the digital reference generation time (i.e. clock frequency of a counter) is equal. These considerations corresponds to the sample behavior of a common Tracking ADC. The made approach simplifies the derivation of the noise power and can be derived without the Bernstein relation.

**Method 2: SNR for Multi-bit Sampling with Various Time Variants ( $T_{\text{samp}} \neq T_{\text{clk}}$ )**

This approach considers that the reference step generation time ( $T_{\text{ref}} = T_{\text{clk}}$ ) which is the clock for digital systems is unequal to the sampling time, thus that  $T_{\text{samp}} \neq T_{\text{clk}}$  is valid. In case of an analog-to-digital converter the demands are met, if the step generation time ( $T_{\text{ref}}$ ) of the digital source is higher than the comparator propagation time (i.e. switching ability) allows. This technical approach leads to the ability, that an ADC is able to quickly generate a reference signal which is able to be adjusted during the propagation time. Thus, the technical limits of the comparator can be achieved and in addition, the sampling scheme can be adjusted based on the demand. The inaccuracy between the slope of the step generation function and the maximum allowed slope by the comparator are considered based on the Bernstein relation.

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### 2.3.1 Method 1: SNR for Multi-bit Sampling with Equal Time Variants

The mathematical derivation of the signal-to-noise ratio in section 2.2 has demonstrated, that the assumptions made by the hypothesis were not accurate enough and just provided the ability to predict the frequency behavior based on SNR investigations for uniformly sampled signals. In order to derive an expression for the non-uniformly sampled tracking schemes, the hypothesis was extended by the claim, that the uniformly sampled power relation acts as a maximum limit for the power. Related to non-uniform sampling the new hypothesis claims that the non-uniform noise power introduced can be expressed by a multiple of the proportionally total noise power. Thus the hypothesis follows, that the equation for the noise portion can be decomposed regarding the non-uniform sampling weights. The relation that will be established converts a multiple of time samples into a multiple of quantization samples instead as for the already derived SNR function which is related to a single step conversion. The resulting function can then be defined as a multi-bit approach for the signal-to-noise ratio.

As described, the basic consideration for the presented method is the simplification, that the sampling time ( $T_{\text{samp}}$ ) equals the reference step generation time ( $T_{\text{ref}}$ ) represented by the clock period of the digital signal ( $T_{\text{ref}} = T_{\text{clk}}$ ). Therefore, the time variant is considered to be equal, thus that ( $T_{\text{ref}} = T_{\text{samp}}$ ). Upon this assumption a further hypothesis can be made which is based on the assumption of a variety of sample portions within the total signal period.

#### **Hypothesis:**

Suppose there is an intersection between the input signal and the reference signal at a sample time ( $T_{\text{samp}}$ ) under the constraint that the step generation time  $T_{\text{ref}} = T_{\text{samp}}$ , the intersection can be located at the input signal moment of the sampling time. The total noise is based on the sum of the noise portions for a variety of sampling times.

#### **Approach:**

In the ideal case, there is a direct dependency between the input signal and the sampling time under the assumption of  $T_{\text{ref}} = T_{\text{samp}}$ . Thus, the noise power evaluated at each sampling moment ( $N T_{\text{ref}}$ ) provides an overall impression for the derivation of a noise function. Due to the proportionality, the relation between the quantization and the sampling time will still be met ( $N q \propto N T_{\text{ref}}$ ).

The proposed approach for the system approximation provides a method to derive the noise portion, which is generated by sampling, straight from the input signal power. By the formation of the indefinite integral the assumption made in the hypothesis is obvious. In order to define the considered range, the integral limits will further be defined by the relation, that an increase in binary weights are proportional to the time weights as described by  $N_q \propto N T_{ref}$ . The input signal type to be evaluated is a sinusoidal function and the power density is expressed by the variance ( $\sigma^2 = E[f(t)^2]$ ) in equation 2.27.

Function:  $f(t) = A/2 \sin(2\pi f_{sig} \cdot t)$

$$E[f(t)^2] = \int \left[ \frac{A}{2} \sin(2\pi f_{sig} \cdot t) \right]^2 dt = \frac{A^2}{4} \cdot \left[ \frac{t}{2} - \frac{\sin(4\pi f_{sig} \cdot t)}{8\pi f_{sig}} \right] \quad (2.27)$$

Based on the result of the input signal power in equation 2.27 the coherences of the single noise portions can be established. The power density is based on two portions:

- Power density of the input signals full period which is defined by  $\frac{A^2}{8} t$
- Delta of the power density caused by the sample step  $-\frac{A^2}{4} \frac{\sin(4\pi f_{sig} \cdot t)}{8\pi f_{sig}}$

The result of  $A^2/8$  is well known as the full period power of a sinusoidal signal. The second portion of the power density is caused by sampling. So, if the full input signal period as a reciprocal of  $f_{sig}$  is considered, the noise portion related to sampling is zero. Thus, it follows that if there is a sampling noise introduced, it can be subtracted from the full period. In case of the SNR consideration the full signal power is divided by the sampling noise power.

This approach becomes clearer, if the integral limits for the power density are defined. Due to the proportionality of  $N q \propto N T_{\text{ref}}$  the full amplitude of the signal can be expressed in proportional time steps of  $T_{\text{ref}} = T_{\text{samp}}$ . Since the half of the input signal amplitude is considered the integral limits are also halved and relation 2.28 results for the interval to be considered. Based on the integral limits the power ( $E [f(t)^2]$ ) evaluates to equation 2.29.

$$\text{Proportional relation: } \frac{A}{2} = 2^{N-1} q \propto 2^{N-1} T_{\text{ref}} \quad (2.28)$$

$$\begin{aligned} \text{Interval: } & [-2^{N-2} T_{\text{samp}}, 2^{N-2} T_{\text{samp}}] \\ \text{Function: } & f(t) = A/2 \sin(2\pi f_{\text{sig}} \cdot t) \end{aligned}$$

$$E [f(t)^2] = \frac{1}{2^{N-1} T_{\text{samp}}} \int_{-2^{N-2} T_{\text{samp}}}^{2^{N-2} T_{\text{samp}}} \left[ \frac{A}{2} \sin(2\pi f_{\text{sig}} \cdot t) \right]^2 dt$$

$$E [f(t)^2] = \frac{A^2}{8} \cdot \left[ 1 - \frac{\sin(\pi f_{\text{sig}} 2^N T_{\text{samp}})}{\pi f_{\text{sig}} 2^N T_{\text{samp}}} \right]$$

$$E [f(t)^2] = \frac{A^2}{8} \cdot [1 - \text{sinc}(\pi f_{\text{sig}} 2^N T_{\text{samp}})] \quad (2.29)$$

By the analysis of the result for the power described over the entire number of samples within half of the input signal amplitude ( $2^{N-1} T_{\text{samp}}$ ) the entire signal power and the noise power portion due to sampling are obvious again. The scaling by  $A^2/8$  relates the amplitude to the resolution. In turn, this implies, that the noise portion defined by the sinc-function is related to the single bit event and scaled by  $2^N$ , thus that  $q^2 2^{2N}/8$ . Therefore, the signal-to-noise ratio can be derived by the ratio of the maximum signal power and the noise power by sampling in equation 2.30.

$$SNR = 10 \log \left[ \frac{\frac{A^2}{8}}{\frac{A^2}{8} \cdot \text{sinc}(\pi f_{\text{sig}} 2^N T_{\text{samp}})} \right] = 10 \log \left[ \frac{1}{\text{sinc}(\pi f_{\text{sig}} 2^N T_{\text{samp}})} \right] \quad (2.30)$$

The function derives the noise power by  $\text{sinc}(\pi f_{\text{sig}} 2^N T_{\text{samp}})$  for a single bit event with  $2^N$ -scaling (i.e.  $q \mapsto A/2^N$ ). Therefore, the signal-to-noise ratio defines the single bit event. In order to define a multi-bit function related to the made hypothesis, that the total noise depends on the sum of the noise portions for a variety of sampling times, the sinc-function needs to be decomposed and depicted as polynomial definition. The depiction as polynomial function ensures, that the proportionately noise is related to any bit within the  $2^N$ -range and the  $T_{\text{sig}}/T_{\text{samp}}$ -relation.

### Taylor Series Expansion of the Sinc-function

In order to consider the noise portions introduced by the sinc-function for every subdivision of bits and sample portions (related to  $T_{\text{samp}}$ ), the sinc-function needs to be expressed as a polynomial representation. Therefore, the background for the polynomial representation is given by the linear weighting of each polynomial subsection. Thus, the sample portions, which also show the linear weighting based on the coefficient scaling of  $q$  and  $T_{\text{samp}}$  can be expressed in any order. The "Taylor series expansion" can be used to decompose the sinc-function and thus for the definition of the influence by sub-sampling related to various steps predefined in the hypothesis. In this case the development base of the "Taylor series expansion" is assumed around zero ( $t_0 = 0$ ) for the simple sampling step  $T_{\text{samp}}$ . Thus, the noise portion for the sinc-function is represented by its "Taylor series expansion" with equation 2.31. The characterized relation defines the conversion between the sampling noise power and the magnitude quantization noise power ( $E_{[(t \mapsto q)^2]}$ ) as derived for the Bernstein-relation in section 2.2. Thereby every series part of the sinc-function represents the quantization related power weight, which is normalized to  $q^2$ .

$$E_{[(t \mapsto q)^2]} = q^2 \cdot \text{sinc}(\pi f_{\text{sig}} 2^N T_{\text{samp}}) = q^2 \cdot \sum_{k=0}^{\infty} (-1)^k \frac{(\pi f_{\text{sig}} 2^N T_{\text{samp}})^{2k}}{(2k+1)!} \quad (2.31)$$

Based on the "Taylor series expansion" by equation 2.31 the sinc-function can be considered related to a variety of sampling possibilities as predicted by the hypothesis. Related to the expanded hypothesis, the intersection between the input signal and the reference signal can be located at the input signal moment of the sampling time ( $T_{\text{samp}}$ ). This statement is valid so far the proportionality relation ( $N q \propto N T_{\text{samp}}$ ) between quantization steps and time sample steps requirement is met. As figure 2.15 illustrates, the proportionality relation maps the number of quantization steps to a number of sampling steps in a linear dependency. Since the "Taylor series expansion" is necessary to decompose the sinc-function, the meaning for each polynomial section of the series expansion is referred to a binary scaled portion of the noise. The polynomial sections are defined as base of the series expansion. Each base of the sinc-function relate to a number of steps. this means, the value of  $T_{\text{samp}}$  also needs to be related to the resolution step. As an example: If the base is squared, the error is caused by a single time step ( $T_{\text{samp}}$ ). If the base is related to the power of four, the error is caused by two time steps ( $2 T_{\text{samp}}$ ). Since the intersection is determined in a linear constitution the example can be continued. However, the result of the continuing example shows, that in order to define the corresponding power definition for each base of the sinc-series expansion the sampling time ( $T_{\text{samp}}$ ) needs to be multiplied by the number of steps. The weight for these steps is a direct relation to the base of the sinc-series expansion, which leads to the relation  $k \cdot T_{\text{samp}}$ . Since the intersection of the input signal and the reference signal is related to a staircase function with an resolution of minimum sampling step ( $T_{\text{samp}}$ ) the statistical mean value of the intersection can be determined by equation 2.32. It relates the sinc-series weight factor to a statistical mean. Furthermore, this approach results in the complete mathematical description of the noise power for the sinc-function given in equation 2.33 which is representative for the sum of each noise portion within the ADC resolution.

$$E [k T_{\text{samp}}] = \int_0^{k T_{\text{samp}}} t^2 dt = \frac{k T_{\text{samp}}}{2} \quad (2.32)$$

$$E_{[t \rightarrow q]^2} = q^2 \cdot \sum_{k=0} (-1)^k \frac{(\pi f_{\text{sig}} 2^{N-1} k T_{\text{samp}})^{2k}}{(2k + 1)!} \quad (2.33)$$

## Step Number and Size of the Taylor Series Expansion

In order to display the entire power of the noise portion summation, predicted by the hypothesis, the number of sufficient steps considered by the series expansion needs to be defined. As derived, the relation for the number of sufficient steps depends on the proportionality condition ( $N q \propto N T_{\text{ref}}$ ). Therefore,  $N - 1$  steps can be mapped to the half of the input signal amplitude. Referred to the consideration of the power depicted by the series expansion, a quadratic function is resolved, thus that the number of sufficient steps needs to be twice the minimum requirement. It follows  $2(N - 1)$ . This claim is also decisive about the negative sign of the series expansion  $(-1)^k$ . The number of steps decides about the sign. Since the power is considered, the absolute of each noise portion is of interest. So, the sign has no mean and determines the deviation from the original input signal. It states if the deviation is positive or negative.

Since the number of steps depicted by the series expansion is representative for the resolution, the value "zero" can be excluded. As an opposite example, if the step size is related to "zero" the noise portion is at the same magnitude as the input signal power. No resolution, no conversion. This consideration validates the previous assumptions. Based on the consideration of a sufficient number of resolution steps, the noise power per bit develops to equation 2.34. Furthermore, the accuracy of the noise power appraisal per binary step can be improved by halving the step width. Therefore, the range of the sum is doubled and the run variable  $k$  is divided by 2 as illustrated in equation 2.35.

$$E_{[(t \rightarrow q)^2]} = q^2 \cdot \sum_{k=1}^{2(N-1)} (-1)^{4k} \frac{(\pi f_{\text{sig}} 2^{N-1} k T_{\text{samp}})^{2k}}{(2k + 1)!} \quad (2.34)$$

$$E_{[(t \rightarrow q)^2]} = q^2 \cdot \sum_{k=2}^{4(N-1)} (-1)^{2k} \frac{(\pi f_{\text{sig}} 2^{N-2} k T_{\text{samp}})^k}{(k + 1)!} \quad (2.35)$$

---

## Proof of Concept based on the Relationship to the Bernstein Approach

The "Bernstein"-relation which transforms the error in time to an error in magnitude was used to derive the frequency limitations for tracking scheme ADCs and the signal-to-noise ratio for a uniformly sampled approach. The verification of the Bernstein approach was guaranteed by a behavioral MATLAB simulation model. Since the Bernstein approach corresponds to the simulation model and the made hypothesis based on this model, the sampling noise for a multi-bit sampling with equal time variants must be traceable to the verified approaches. Therefore, in order to validate that the multi-bit sampling solution is correct, the multi-bit noise power derived by the Taylor series expansion is compared to the noise power derived by the "Bernstein"-relation. If the step width of the multi-bit version is considered to be reduced to the first step, thus that  $k = 2$ , the series expansion of the noise power by sampling reduces to equation 2.37.

$$E_{\text{bern}[(t \rightarrow q)^2]} = \frac{q^2}{3} \cdot 2^{2N-3} \cdot \pi^2 \cdot f_{\text{sig}} \cdot T_{\text{samp}} \quad (2.36)$$

$$E_{\text{mult}[(t \rightarrow q)^2]}|_{k=2} = q^2 \cdot (-1)^{2k} \frac{(\pi f_{\text{sig}} 2^{N-2} k T_{\text{samp}})^k}{(k+1)!} \quad (2.37)$$

$$\Leftrightarrow q^2 \frac{1}{24} 2^{2N} \pi^2 f_{\text{sig}} T_{\text{samp}} = \frac{q^2}{3} \cdot 2^{2N-3} \cdot \pi^2 \cdot f_{\text{sig}} \cdot T_{\text{samp}} \equiv E_{\text{bern}[(t \rightarrow q)^2]} \quad (2.38)$$

In comparison to equation 2.36 of the Bernstein assumption the reduced multi-bit approach for equal time variants (i.e.  $T_{\text{samp}} = T_{\text{ref}} = T_{\text{clk}}$ ) corresponds exactly. If one derives the meaning of the first base in the polynomial summation, the agreement can be explained by the uniformly sampling which was the assumption of the noise power equation derived by Bernstein theorem. So, the first base of the sum of the sinc-function determines the case if the input signal is sampled uniformly which implies that there is a valid conversion for every time sample  $T_{\text{samp}}$ . The higher order bases of the sinc-function series expansion are decisive about the additional noise portions if a multiple of time steps are missing.

## Signal-to-Noise Ratio for Multi-bit Sampling Approaches

The noise of the quantization step error derived in section 2.2 ( $\sqrt{E[\varepsilon_a^2]}$ ) is the upper limit for the effective resolution. The input signal power is considered for the half of the amplitude and the period  $T_{\text{sig}}$ , thus that the derived function  $\sqrt{E[s_{\text{in}}^2]}$  in equation 2.19 is valid again. Based on these boundary conditions the signal-to-noise ratio for a non-uniformly sampled tracking scheme ADC can be defined within the restriction of the hypothesis, that the sampling time is equal to the reference step generation time. Related crest-ratio assumptions (section: 2.1.2) by the RMS consideration of the Bernstein function, the relationship to the sampling noise derived in this section also needs to be considered. Thus, the factor for the crest-ratio is present for the sampling noise power again. Since the definition for the noise power related to the Taylor series expansion of the sinc-function also shows a quadratic property, the crest-ratio also needs to be squared ( $\Gamma_{\text{crest}}^2$ ). This property can be evaluated from the derivation of the noise function which was defined by the full period  $T_{\text{sig}}$  of the input signal. Therefore, it relates the RMS value for the maximum and the minimum of the sine wave and the triangular reference. From these dependencies evaluates the normalized equation 2.39. It defines the signal-to-noise ratio of non-uniformly sampled ADC schemes under the condition of equal time variants ( $T_{\text{samp}} = T_{\text{ref}} = T_{\text{clk}}$ ).

$$\text{Sampling noise power: } E[(t \rightarrow q)^2] = q^2 \cdot \sum_{k=2}^{4(N-1)} (-1)^{2k} \frac{(\pi f_{\text{sig}} 2^{N-2} k T_{\text{samp}})^k}{(k+1)!}$$

$$\text{Quantization noise power: } E[\varepsilon_a^2] = \frac{q^2}{12}$$

$$\text{Signal power: } E[f(t)^2] = \frac{q^2}{8} 2^{2N}$$

$$\Rightarrow \text{SNR} = 10 \log \left[ \frac{2^{2N-3}}{\frac{1}{12} + \Gamma_{\text{crest}}^2 \cdot \sum_{k=2}^{4(N-1)} (-1)^{2k} \frac{(\pi f_{\text{sig}} 2^{N-2} k T_{\text{samp}})^k}{(k+1)!}} \right] \quad (2.39)$$

---

### 2.3.2 Evaluation of the Mathematical SNR Model for Non-uniform Sampling

The derived equation for the signal-to-noise ratio of non-uniformly sampled ADC schemes under the condition of equal time variants ( $T_{\text{samp}} = T_{\text{ref}} = T_{\text{clk}}$ ) was validated by the comparison with the mathematical model of the Bernstein relation. The proof of concept has demonstrated, that the non-uniformly sampled ADC approach under the simplification of equal time variants can be traced back to the basic system. However, the proof of concept is incomplete, since no statement about the multi-bit behavior of the mathematical model was made. Therefore, the mathematical signal-to-noise ratio needs to be validated by the behavioral MATLAB simulation model. The simulations are based on a range of input signal frequencies ( $f_{\text{in}} = 10 \text{ kHz}$  to  $200 \text{ kHz}$ ), ADC resolutions ( $N = 8$  and  $9$  bit) and sampling frequencies equal to the clock frequencies by  $f_{\text{clk}} = f_{\text{samp}} = 10, 20, 30$  and  $50 \text{ MHz}$ . The figures 2.16 and 2.17 illustrate the individual simulation results compared to the predicted calculation results.

Based on the simulation results of the behavioral MATLAB model the course of the signal-to-noise ratio predicted by equation 2.39 can be verified. The accordance of the mathematical model to the behavioral simulation model demonstrates a high accuracy over the entire investigated input frequency range under the consideration of a variety of parametrization. So, it is shown that the derived equation not only covers a particular case but covers the entire scope of the degrees of freedom in a relationship of non-uniform sampling. The resolution ( $N$ ) and the conversion rate ( $f_{\text{samp}}$ ) characterize degrees of freedom.

The made hypothesis, which claims the statement of an existing intersection between the input signal and the reference signal at a sample time ( $T_{\text{samp}}$ ) can be located at the input signal moment of the sampling time. Thus, it is proven. The extended constraint that the step generation time equals the sampling time ( $T_{\text{ref}} = T_{\text{samp}}$ ) is considered by the equality of the clock frequency and the conversion rate, thus that  $f_{\text{clk}} = f_{\text{samp}}$ . Therefore, the total noise is based on the sum of the noise portions for a variety of sampling times. Deviations between the simulated and the calculated model, could be explained by the uncertainty of the MATLAB evaluation system by FFT (section: 2.1.4). Thus, the analysis needs a high number of samples in order to generate a high accuracy. In relation to non-uniformly sampled signals, the SNR calculated is representative for a sufficient number of samples. The highest accuracy is generated for infinite non-uniform signals. However, the demonstration illustrated in figure 2.16 and 2.17 shows an accurate accordance between the simulation model and the mathematical model.

In summary, the made hypothesis is valid within the defined scope, that an intersection can be located at the input signal moment of the sampling time, if the step generation time equals the sampling time ( $T_{\text{ref}} = T_{\text{samp}}$ ). Therefore, this approach can be applied to the conventional Tracking ADC, where the tracking scheme is based on this requirement. If the tracking scheme should be extended by a further degree of freedom, the step generation time needs to be independent of the sampling time, thus that  $f_{\text{clk}} \neq f_{\text{samp}}$ . This implies, that the hypothesis would be invalid and an extended approach needs to be defined.

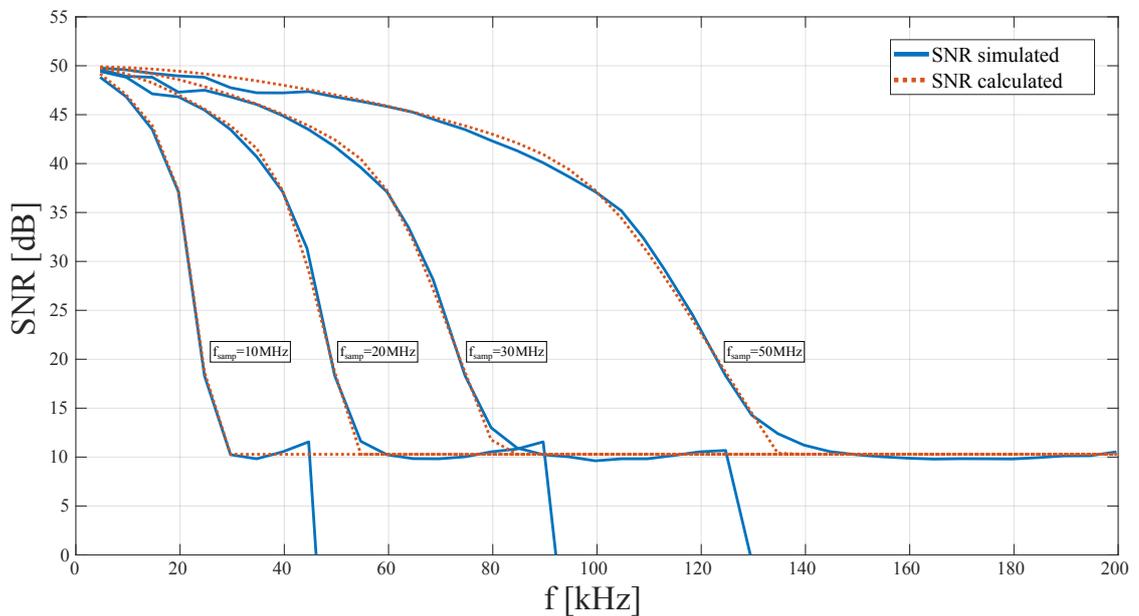


Figure 2.16: Comparison between the behavioral MATLAB simulation model and the signal-to-noise ratio (SNR) calculated by equation 2.39. Parameters:  $N = 8$ ,  $f_{\text{in}} = [10 \text{ kHz to } 200 \text{ kHz}]$  and  $f_{\text{clk}} = f_{\text{samp}} = 10, 20, 30$  and  $50 \text{ MHz}$ . The mathematical expression corresponds to the MATLAB simulation model. The uncertainty of the simulation due to evaluation by FFT explains deviations.

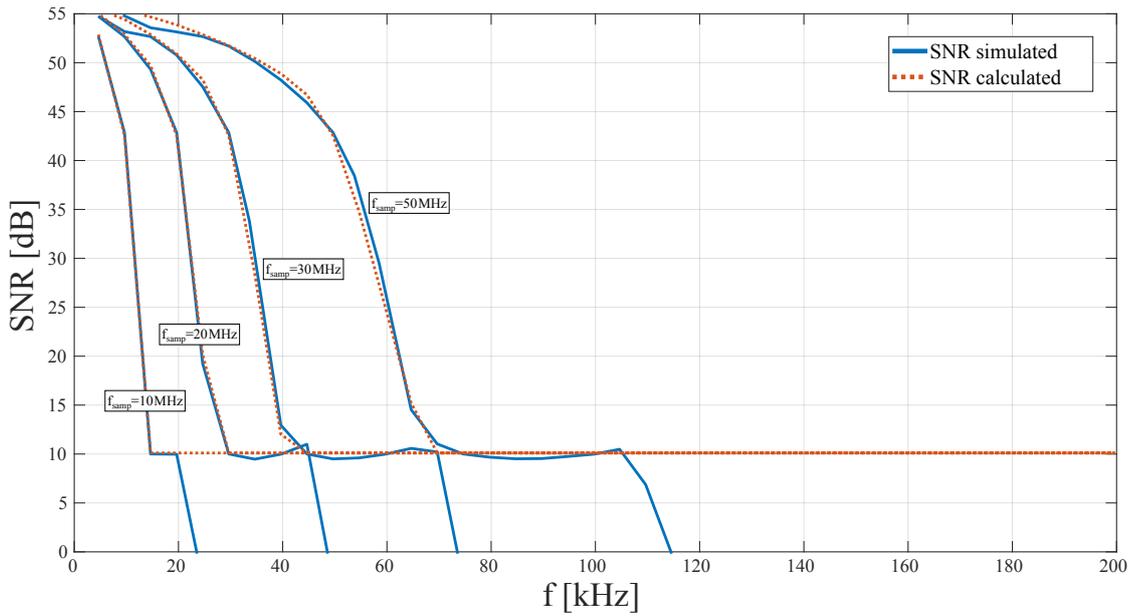


Figure 2.17: Comparison between the behavioral MATLAB simulation model and the signal-to-noise ratio (SNR) calculated by equation 2.39. Parameters:  $N = 9$ ,  $f_{\text{in}} = [10 \text{ kHz to } 200 \text{ kHz}]$  and  $f_{\text{clk}} = f_{\text{samp}} = 10, 20, 30$  and  $50 \text{ MHz}$ . The mathematical expression corresponds to the MATLAB simulation model. The uncertainty of the simulation due to evaluation by FFT explains deviations.

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### 2.3.3 Method 2: SNR for Multi-bit Sampling with Various Time Variants

The mathematical derivation of the signal-to-noise ratio in section 2.2 describes the frequency behavior for uniformly sampled signals. It has turned out, that the assumptions made by the hypothesis are not accurate enough for the prediction of non-uniformly sampled tracking schemes. Therefore, the basic approach defined by the hypothesis was extended towards the statement, that the non-uniform sampling is based on various sample time intervals and consists of a multiple of the initial sampling time ( $T_{\text{samp}}$ ). The total noise by sampling is the sum of each noise component. This hypothesis was investigated and validated in method 1. However, the initial hypothesis was extended by the condition, that the step generation time is equal to the sampling time  $T_{\text{ref}} = T_{\text{samp}}$ . Thus, the intersection could be located at the input signal moment of the sampling time. The evaluation based on behavioral MATLAB simulations demonstrated, that the hypothesis including the extended version is valid and predict the signal-to-noise ratio for non-uniformly sampled signals under the condition of equal time variants. Technically, this claim corresponds to the conventional Tracking ADC.

The approach of various time variants postulates a consideration for the fact, that the sampling time  $T_{\text{samp}}$  is not equal to the reference step generation time  $T_{\text{ref}}$ . Indeed, this fact corresponds to any non-uniformly sampled ADC. The Tracking ADC defines a special form of non-uniform sampling ADCs where the conversion limits are defined by the maximum feedback delay (i.e.  $T_{\text{samp}}$ ). Based on this fact, the reference signal generation of Tracking ADCs is not flexible. The generalized version of non-uniformly sampled ADCs promises a higher degree of control about the reference signal, since it postulates a further degree of freedom. Thereby, the possibility of a faster reference step generation than the total feedback delay allows, exists. As a result the sampling time is unequal to the reference step generation time  $T_{\text{samp}} \neq T_{\text{ref}}$ . In the broader sense, unequal time variants also allow, the consideration of various feedback delays of tracking scheme ADCs, that can not be transferred to the digital step generation property of the clock frequency ( $f_{\text{clk}}$ ). Based on this consideration the extension of the hypothesis made in method 1 can be generalized to any possible time composition between  $T_{\text{samp}}$  and  $T_{\text{ref}}$ .

#### **Hypothesis:**

If there is an intersection between the input signal and the reference signal at the moment of composition between the times  $T_{\text{samp}}$  and  $T_{\text{ref}} = T_{\text{clk}}$ , the statistical error related to that moment can be defined as noise portion. The total noise depends on the sum of the noise portions for a variety of sampling times.

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### **Approach:**

The hypothesis extends the validated claim for the "Bernstein"-relation, that the intersections between the input signal slope and the reference signal slope exists in the interval  $[0, T_{\text{sig}}]$ . This claim is verified and reveals the limit for a uniformly sampled signal. In this context, the sample time intervals are equal by the minimum step. The investigation in method 1 concerning non-uniformly sampled signals has verified the claim of noise portions based on various time intervals, which can be composed by the sum of each noise portion. The derivation relates to the Taylor series expansion of the noise portion. Thus, each noise portion predicts a weighted time to quantization noise. Based on the generalized hypothesis, the noise portion for various time compositions between  $T_{\text{samp}}$  and  $T_{\text{ref}}$  should be derived with the "Bernstein"-relation because it predicts a validated noise portion due to the slope consideration independently of the slope constraints as for method 1. The decomposition of the Bernstein noise portion refers to as method 1. Thus, the noisy proportion is decomposed by the "Taylor series expansion" to consider the proportional noise of the various intersection intervals. The relation converts multiple time samples into multiple magnitude quantization samples.

The described derivation of the signal-to-noise ratio for multi-bit sampling with equal time variants in method 1 represents a special form of the "Bernstein" time to resolution error translation. The special form is established by the condition of the proportionality of  $Nq \propto NT_{\text{samp}}$  based on the sampling time ( $T_{\text{samp}}$ ). This assumption results in a quadratic representation of the signal intersection error. Related to method 1 the multi-bit sampling could be derived from the power of the input signal and its noise introduced by the sampling time ( $T_{\text{samp}}$ ). The relation  $Nq \propto NT_{\text{samp}}$  is based on the "Bernstein Theorem". Since it is valid for the quadratic representation of the time error within the specialized form, it is also valid for the general time error based on level-crossing. It can be concluded, that the time error of level-crossing is equal to the sampling error of the input signal. This assumption was validated in consideration of the first base section for the Taylor series expansion of the sinc-function and the simple Bernstein related noise power. But if the sampling time is different to the reference generation time, thus that condition  $T_{\text{samp}} \neq T_{\text{ref}}$  is met, the proportionality argument is not valid any more ( $Nq \not\propto NT_{\text{samp}}$ ). However, the proportionality is translated to the reference generation time ( $T_{\text{ref}}$ ) by  $Nq \propto NT_{\text{ref}}$ , which is based on the clock frequency by  $T_{\text{ref}} = f_{\text{clk}}^{-1}$ . The relation between the degrees of freedom (i.e  $N$ ,  $T_{\text{samp}}$  and  $T_{\text{ref}}$ ) is based on the reference signal slope generated for these variables within successive samples. Therefore, a successive sample can be expected within the averaged sample time which corresponds to the internal feedback delay ( $T_{\text{samp}} = \tau_d$ ). Thus, a system response can be expected in

conjunction with  $\tau_d$  and  $T_{\text{ref}} = \tau_{\text{clk}}$ . As shown in figure 2.18, it turns out that the sample property is also limited by the system delay. The conjunction between the step generation time ( $T_{\text{ref}}$ ) and the system delay ( $\tau_d = T_{\text{samp}}$ ) still introduces an uncertainty in time ( $\delta\tau_{\text{clk}}$ ) based on level crossing which defines the deviation from the sampling interval ( $\Delta T_{\text{ref}} = \Delta T_{\text{samp}}$ ). It is constituted by the relation between the input signal slope and the reference signal generated by  $T_{\text{clk}}$ . The concept is illustrated in Fig. 2.19.

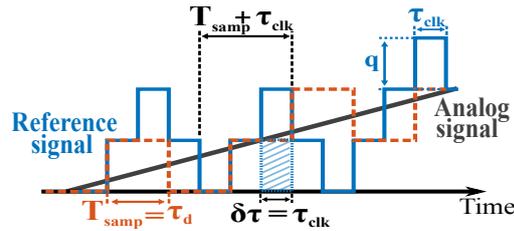


Figure 2.18: Uncertainty in time ( $\delta\tau = \tau_{\text{clk}}$ ) for the level crossing approach caused when the analog signal crosses the reference signal during the interval  $(0, T_{\text{ref}}]$ .

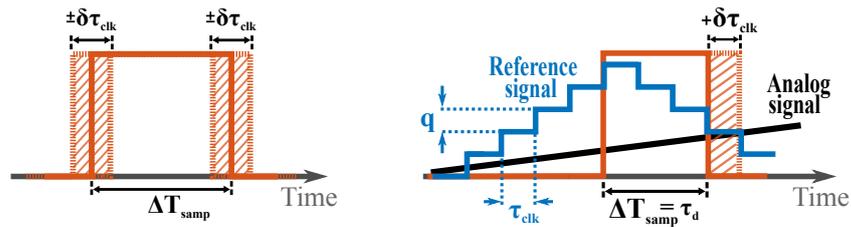


Figure 2.19: The influence of a faster clock frequency ( $f_{\text{clk}} = \tau_{\text{clk}}^{-1}$ ) introduces an uncertainty to the sampling interval ( $T_{\text{samp}}$ ). The uncertainty is constituted by the relation between the analog signal slope and the ADC reference signal.

In order to extend the quantization error in time ( $\varepsilon_t$ ) mathematically, a new relation between the sampling interval  $\Delta T_{\text{samp}} = \tau_d$  and  $T_{\text{ref}} = \tau_{\text{clk}}$  needs to be established. Therefore, the accuracy of the reference step generation  $T_{\text{ref}}$  varies as a function of the input signal, thus that the condition  $f(t_{\text{ref}})$  is met within the interval  $[-\delta\tau_{\text{clk}}, +\delta\tau_{\text{clk}}]$ . Furthermore, the Bernstein condition is further related to the sampling interval  $T_{\text{samp}}$  by  $\varepsilon_t \cong s(T_{\text{ref}}) \cdot \partial t_{\text{samp}}$  in the interval  $(0, T_{\text{samp}}]$ . Therefore, the rms quantization error in time results from the extension as a composition of the uncertainty  $\delta\tau_{\text{clk}}$  and the average sample time ( $T_{\text{samp}}$ ) as  $\Delta T_{\text{ref}} = T_{\text{samp}} \circ \delta\tau_{\text{clk}}$ .

Related to the depiction of an exact result the "Bernstein"-relation in equation 2.40 is used for the consideration of a general noise power version. As for the derivation of the input signal power decomposition the Bernstein related noise power is derive in the most general representation as the indefinite integral of the power density slope. The decomposition of the Bernstein noise power can be derived from the result given in equation 2.41.

Bernstein relation: 
$$q \hat{=} \frac{d}{dt} f(t_{ref}) \cdot \Delta_s(t_{samp}) \quad (2.40)$$

function: 
$$f(t_{ref}) = \frac{A}{2} \sin(2\pi f_{sig} \cdot t_{ref}) \Rightarrow \frac{d}{dt_{ref}} f(t_{ref}) = A \pi f_{sig} \cos(2\pi f_{sig} \cdot t_{ref})$$

$$E [f'(t_{ref})^2] = \int [f'(t_{ref})]^2 dt_{ref} = \int [A \pi f_{sig} \cos(2\pi f_{sig} \cdot t_{ref})]^2 dt_{ref}$$

$$\Rightarrow E [f'(t_{ref})^2] = A^2 \pi^2 f_{sig}^2 \cdot \left[ \frac{t_{ref}}{2} + \frac{\sin(4\pi f_{sig} T_{ref})}{8\pi f_{sig}} \right] \quad (2.41)$$

As for the derivation of method 1 the coherences of the noise portions can be established by the result of the Bernstein related sampling power in equation 2.41. Again, the power density is based on two portions:

- Power density related to the full period: 
$$\boxed{A^2 \pi^2 f_{sig}^2 \cdot \frac{t_{ref}}{2}}$$

- Density of the sampling power: 
$$\boxed{A^2 \pi^2 f_{sig}^2 \cdot \frac{\sin(4\pi f_{sig} T_{ref})}{8\pi f_{sig}}}$$

Based on the derivation of the signal-to-noise ratio for uniformly sampled ADCs in section 2.2 the noise portion  $A^2 \pi^2 f_{sig}^2 \cdot t_{ref}/2$  in contemplation with the sampling time  $T_{samp}$  is known as the noise introduced by uniform sampling.

Further evaluations by the definite integral show that this part is independent of the reference step generation rate ( $T_{\text{ref}}$ ). The second portion of the power density depends on  $T_{\text{ref}}$  and is the proportionately noise introduced by sampling. Whereby, it can be derived, that the noise portion is reduced to the uniform sampling portion if no reference step is generated, which leads to continuous uniform sampling by  $T_{\text{samp}}$ .

The definite integral of the input signal slope evaluates the proportional noise introduced by the reference generation time which equates with the digital clock. Again, half of the input signal amplitude is considered, thus that the interval to be observed is limited by the relation  $A/2=2^{N-1}q \Rightarrow T_{\text{sig}}/2=2^{N-1}T_{\text{ref}}$ . Therefore, the resulting interval (Eqn. 2.42) corresponds to  $[-2^{N-2}T_{\text{ref}}, 2^{N-2}T_{\text{ref}}]$  in order to define a mean zero relation for the power derivation in equation 2.43.

$$\text{Proportional relation: } \frac{A}{2} = 2^{N-1}q \propto 2^{N-1}T_{\text{ref}} \quad (2.42)$$

$$\text{Interval: } [-2^{N-2}T_{\text{ref}}, 2^{N-2}T_{\text{ref}}]$$

$$\text{function: } f(t_{\text{ref}}) = \frac{A}{2} \sin(2\pi f_{\text{sig}} \cdot t_{\text{ref}}) \Rightarrow \frac{d}{dt_{\text{ref}}}f(t_{\text{ref}}) = A\pi f_{\text{sig}} \cos(2\pi f_{\text{sig}} \cdot t_{\text{ref}})$$

$$E [f'(t_{\text{ref}})^2] = \frac{1}{2^{N-1}T_{\text{ref}}} \int_{-2^{N-2}T_{\text{ref}}}^{2^{N-2}T_{\text{ref}}} [A\pi f_{\text{sig}} \cos(2\pi f_{\text{sig}} \cdot t_{\text{ref}})]^2 dt_{\text{ref}}$$

$$E [f'(t_{\text{ref}})^2] = \frac{A^2}{2} \pi^2 f_{\text{sig}}^2 \cdot \left[ 1 + \frac{\sin(\pi f_{\text{sig}} 2^N T_{\text{ref}})}{\pi f_{\text{sig}} 2^N T_{\text{ref}}} \right]$$

$$E [f'(t_{\text{ref}})^2] = \frac{A^2}{2} \pi^2 f_{\text{sig}}^2 \cdot [1 + \text{sinc}(\pi f_{\text{sig}} 2^N T_{\text{ref}})] \quad (2.43)$$

As predicted, a portion of the definite integral is independent of the reference step generation time and thus independent of the digital clock period ( $T_{\text{clk}}$ ). However, this proportion is defined by the actual sampling time ( $T_{\text{samp}}$ ) as assumed by the hypothesis.

It claims that if an intersection between the input signal and the reference signal exists at the moment of a composition between the times  $T_{\text{samp}}$  and  $T_{\text{ref}}$ , the statistical error related to that moment can be defined as noise portion. In order to define that error for each possible intersection the second noise portion, which is based on the sinc-function needs to be decomposed and represented as polynomial function by the "Taylor series expansion" as already described in method 1. The Taylor series expansion of the sinc-function for the Bernstein slope approximation is defined by equation 2.44.

$$\text{sinc}(\pi f_{\text{sig}} 2^N T_{\text{ref}}) = \sum_{k=0}^{\infty} (-1)^k \frac{(\pi f_{\text{sig}} 2^N T_{\text{ref}})^{2k}}{(2k+1)!} \quad (2.44)$$

Also in this case, the "Taylor series expansion" by equation 2.44 of the sinc-function can be considered related to a variety of sampling possibilities as predicted by the hypothesis. But related to the hypothesis in this section, the intersection between the input signal and the reference signal is located for the composition of  $T_{\text{samp}}$  and  $T_{\text{ref}}$ . However, the proportionality relation ( $N q \propto N T_{\text{ref}}$ ) between quantization steps and reference steps requirement is met. Therefore, the proportionality relation maps the number of quantization steps to a number of sampling steps in a linear dependency. As already derived in the previous section for method 1, the number of generated reference time steps are related to each base section of the series expansion. So, the generation time ( $T_{\text{ref}}$ ) needs to be multiplied by the number of steps, thus that the reference for each base section is defined by  $k \cdot T_{\text{ref}}$ . Referred to the intersection of the input signal and the staircase reference signal the statistical mean value of the intersection can be determined by equation 2.32 again. By  $k \cdot T_{\text{ref}}/2$  the sinc-series weight factors are related to the statistical mean. Based on these relationships, the multi-bit power density caused by various sampling times (i.e. non-uniform sampling) can be defined for the slope, which is the first part of the "Bernstein" development. Thus equation 2.45 results.

$$E \left[ f'(t_{\text{ref}})^2 \right] = \frac{A^2}{2} \pi^2 f_{\text{sig}}^2 \left[ 1 + \sum_{k=0}^{\infty} (-1)^k \frac{(\pi f_{\text{sig}} 2^{N-1} k T_{\text{ref}})^{2k}}{(2k+1)!} \right] \quad (2.45)$$

The second part of the "Bernstein" development requires the relation to the sampling time ( $T_{\text{samp}}$ ) of the ADC. It defines the ability of the ADC system to sample the input signal and defines the probability of occurrence of an intersection between the input and the reference signal. Therefore, it is decisive about the frequency of intersection and in this way defined as the sample or conversion rate. The "Bernstein Theorem" defines a connection between the reference signal and the sample rate. Thereby, the power density determines a crucial role in order to estimate the noise of the non-uniform sample scheme. The basic assumption of the hypothesis in section 2.2 are still valid for the Bernstein derivation of the hypothesis made in this section for a multi-bit sampling dependency. Again, it can be assumed, that the power density of the signal which is subdivided by  $T_{\text{ref}}$  is independent of the power caused by the conversion rate ( $T_{\text{samp}}$ ). The assumptions are still valid, because the digital clock frequency is independent of the statistical conversion rate. Thus, referred to equation 2.18 the entire error in time related to an error in magnitude by Bernstein evaluates to equation 2.46.

$$E[(t \rightarrow q)^2] \hat{=} E[f'(t_{\text{ref}})^2] \cdot E[\delta\tau^2] \quad \Rightarrow \quad E[(t \rightarrow q)^2] \hat{=} E[f'(t_{\text{ref}})^2] \cdot \frac{T_{\text{samp}}^2}{12}$$

$$\text{with } A^2 = 2^{2N} q^2 \quad , \quad T_{\text{samp}}^2 = f_{\text{samp}}^{-2} \quad \text{and} \quad T_{\text{ref}}^2 = f_{\text{ref}}^{-2} = f_{\text{clk}}^{-2}$$

$$E[(t \rightarrow q)^2] = \frac{q^2}{3} 2^{2N-3} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \cdot \left[ 1 + \sum_{k=0}^{\infty} (-1)^k \frac{(\pi f_{\text{sig}} 2^{N-1} k T_{\text{ref}})^{2k}}{(2k+1)!} \right] \quad (2.46)$$

### Scope of Validity Considerations for Time Error Definition by Bernstein

The definition of the time error translation to an error in magnitude by Bernstein is specified in equation 2.46. As stated by the hypothesis, the total noise depends on the sum of the noise portions for a variety of sampling times. The individual noise portion of the timing uncertainty due to sampling  $T_{\text{samp}}$  and reference step generation time  $T_{\text{ref}}$  are specified by the "Bernstein"-relation. It is obvious, that the first portion is basically the noise portion based on uniform sampling as derived in equation 2.21. The second noise portion based on the Taylor series expansion is related to the composition between the sampling time  $T_{\text{samp}}$  and the reference  $T_{\text{ref}}$ . In this way each individual segment of

the series expansion defines an error which is linearly related to the resolution portion ( $N = 2 \mapsto x^2, N = 3 \mapsto x^3, \dots$ ). Related to the described contemplation, the series expansion needs to be considered based on the covered equation scope. The basic element of the series expansion is referred to a quadratic function, which is obviously based on the consideration of the noise power. This is the reason for the uniform sampling time expression (Eqn. 2.47) which is squared as well as for the composition between the sampling time and the step generation time which is defined by the basic expression in equation 2.48. The composition also describes the quadratic property, where variable "k" is representative for the individual resolutions. If the composition between  $T_{\text{ref}}$  and  $T_{\text{samp}}$  is representative, the series expansion needs to be defined regarding the scope of the variable. Thus, under consideration of equation 2.49 the step generation time is equal to the sampling time  $T_{\text{ref}} = T_{\text{samp}}$ . By this means the same valence as for equation 2.34 should arise. In comparison of both equations the statement is true except for the context, that the Bernstein relation in 2.49 is shifted by "1" and multiplied by the mean value ratio of 1/12. This fact demands, that the contemplation of the series expansion is overdetermined. Thereby, the over-determination depends on the considered scope of validity of the time error definition by Bernstein.

Sampling time expression:

$$\frac{q^2}{3} 2^{N-3} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \quad (2.47)$$

Composition between  $T_{\text{ref}}$  and  $T_{\text{samp}}$ :

$$\frac{q^2}{3} 2^{N-3} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \cdot \sum_{k=0} (-1)^k \frac{(\pi f_{\text{sig}} 2^{N-1} k T_{\text{ref}})^{2k}}{(2k+1)!} \quad (2.48)$$

Composition between  $T_{\text{ref}} = T_{\text{samp}}$ :

$$\frac{q^2}{12} \cdot \sum_{k=0} (-1)^k \frac{(\pi f_{\text{sig}} 2^{N-1} k T_{\text{samp}})^{2k+2}}{(2k+1)!} \quad (2.49)$$

Based on these assumptions the scope of the time error definition within the series expansion needs to be related. The context of the series expansion defines the weight of the mean value for the step generation time in relation to the Taylor faculty. If the valence of the Taylor series is shifted by "1", the relation is out of scope. Therefore, an adjustment is necessary in order to relate the scope to the individual context of the series elements. Based on the relation between the mean value weight for  $T_{\text{ref}}$  and the faculty of the Taylor series the scope shifting factor can be determined as inverse function as demonstrated in equation 2.50.

$$\left( \frac{(k/2)^{2k}}{(2k+1)!} \Big|_{k=1} \right)^{-1} = \left( \frac{1}{4} \cdot \frac{1}{3!} \right)^{-1} = 24 \quad (2.50)$$

Related to the scope shifting factor that shifts the series expansion by "1", the valance can be adjusted by the static value defined in equation 2.50. Since the influence by shifting the series expansion out of the relation defines a crucial interdependence between  $T_{\text{samp}}$  and  $T_{\text{ref}}$ , the derived approach needs to be redetermined by shifting the Taylor series expansion coefficients. A further aspect to be considered by the scope shift concerns to the sign of the series expansion defined by  $(-1)^k$ . The scope shift by "1" leads to the contemplation, that the sign is defined by its squared value. This fact becomes more obvious if the complete Taylor series is developed. Due to the periodical development of the sine function a shift by "1" corresponds to the skip of the negative signed parts. Furthermore, due to the consideration of the sum as total power the absolute deviation is of interest. Based on these relations the final expression for the noise power evaluates to equation 2.51.

$$E[(t \rightarrow q)^2] = q^2 2^{2N} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \cdot \left[ \frac{1}{24} + \sum_{k=0} (-1)^{2k} \frac{(\pi f_{\text{sig}} 2^{N-1} k T_{\text{ref}})^{2k}}{(2k+1)!} \right] \quad (2.51)$$

---

## Step Number and Size of the Taylor Series Expansion

As a basic assumption the number of sufficient steps considered by the Taylor series expansion can be traced back to the assumptions of method 1. In order to display the entire power of the noise summation, predicted by the hypothesis, the number of sufficient steps again depends on the proportionality condition ( $N q \propto N T_{\text{ref}}$ ). Therefore,  $N - 1$  steps can be mapped to the half of the input signal amplitude which resolves a quadratic function thus that  $2(N - 1)$  follows. In addition, "zero" needs to be excluded, since the reference generation would be constant. This context would be valid from the technical side of view, but there are no statements about the targeted dynamic behavior defined by the signal-to-noise ratio.

The actual definition about the sufficient number of steps varies by the relation between the two reference times  $T_{\text{ref}}$  and  $T_{\text{samp}}$  referred to the arising intersection. Since the number of sufficient steps describe the accuracy of the series expansion the number of average reference steps within the sample period  $T_{\text{samp}}$  can be resolved. Thus, the higher the number of resolved steps, the less is the number of required steps for the series expansion. The squared value of the relation between the sampling time and the step generation time defines the additional required steps. In turn, the higher the ratio between the clock frequency ( $f_{\text{clk}} = T_{\text{ref}}^{-1}$ ) and the average conversion rate, described by the sampling rate, ( $f_{\text{samp}} = T_{\text{samp}}^{-1}$ ) the less steps are required for a sufficient resolution of the series expansion. Therefore, the number of reduction steps is determined by the maximum possible occurrence, which is defined by the ratio between clock rate and conversion rate ( $f_{\text{clk}}/f_{\text{samp}}$ ). Thus, the relation  $[2(N - 1) - f_{\text{clk}}/f_{\text{conv}}]$  acts as upper limit of the series expansion. Replaced by the frequency relations for  $f_{\text{samp}}$  and  $f_{\text{clk}}$  results equation 2.52 for the noise portion of the time uncertainty.

Upper limit series definition:  $limit = 2(N - 1) - f_{\text{clk}}/f_{\text{samp}}$

$$E[(t \rightarrow q)^2] = q^2 2^{2N} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \cdot \left[ \frac{1}{24} + \sum_{k=1}^{limit} (-1)^{2k} \frac{(\pi 2^{N-1} k \cdot f_{\text{sig}}/f_{\text{clk}})^{2k}}{(2k + 1)!} \right] \quad (2.52)$$

The accuracy of the Taylor series expansion depends on the step resolution in time. A further possibility to improve the noise relation from equation 2.52 is revealed by the mean value consideration. Since the expected intersection between the input signal and

the reference signal is predicted to be located at the statistical mean of a single reference step, the mean of the step generation time ( $T_{ref}$ ) identifies the crossing. The Taylor series expansion was defined for a natural number of steps in the minimal order of magnitude of "1". In contemplation of the statistical mean, the assumption of an intersection located at the half of each step generation time promises an more accurate statistical approximation. This approach was already applied to method 1, which enabled a higher accuracy. But in comparison to method 1 the scope of validity is not quadratic, which implies, that a shift of the discrete events of the series expansion requires an adjustment of the scope of validity for the time error definition by Bernstein. In the course of this section it was already explained how the discrete events of the Taylor series are adapted. Related to this dependencies, the normalization for a shift of "1" was determined by equation 2.50. In consideration to allow the accuracy to be 1/2, the initial start consideration for the discrete event of "1" needs to be extended to "1/2". In this terms, the start value, and also the consideration of reduction steps, of the series expansion is subject to this condition, thus that the initialization and the limit is shifted by "1". Therefore, the step resolution for the series expansion evaluates to  $[2 : 1/2 : 2 (N - 1) - (f_{clk}/f_{samp} + 1)]$ . Related to that claim, the normalization factor develops to equation 2.53.

$$\left( \frac{(k/2)^{2k}}{(2k+1)!} \Big|_{k=1/2} \right)^{-1} \cdot \left( \frac{(k/2)^{2k}}{(2k+1)!} \Big|_{k=1} \right)^{-1} = 192 \quad (2.53)$$

Based on the derivation of the normalization factor in equation 2.53 the initialization and the limit of the Taylor series expansion can be reevaluated. Thus, the total series range results in  $[4 : 1 : 4 (N - 1) - 2 (f_{clk}/f_{samp} + 1)]$ . Rewriting the relation for the Bernstein time-to-magnitude relation results in equation 2.54.

Upper limit series definition:  $limit = 4 (N - 1) - 2 (f_{clk}/f_{samp} + 1)$

$$E[(t \rightarrow q)^2] = q^2 2^{2N} \pi^2 \left( \frac{f_{sig}}{f_{samp}} \right)^2 \cdot \left[ \frac{1}{24} + 2^3 \cdot \sum_{k=4}^{limit} \frac{(-1)^k (\pi 2^{N-2} k \cdot f_{sig}/f_{clk})^k}{(k+1)!} \right] \quad (2.54)$$

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## Proof of Concept for the Extended Bernstein Approach

Based on the Bernstein approach, a general relation for non-uniformly sampled signals was derived related to the hypothesis made in this section. Method 1 has demonstrated that a restricted hypothesis is valid for the case that the sample time corresponds to the step generation time ( $T_{\text{samp}} = T_{\text{ref}}$ ). The claim of this hypothesis was validated by the back tracing to the general Bernstein approach of section 2.2. The hypothesis made for method 2 about the existence of an intersection between the input signal and the reference signal at the moment of a composition between the times  $T_{\text{samp}}$  and  $T_{\text{ref}}$  and farther the definition as a noise portion based on a statistical error related to that moment are a generalized version of method 1. In order to validate this claim, the evaluated Bernstein time-to-magnitude relation needs to be traced back to the basic claim of section 2.2 and method 1. Therefore, the dependency of method 1 that  $T_{\text{samp}}$  corresponds to  $T_{\text{ref}}$  needs to be applied to the result. As a starting point, the simplified version is considered for the proof of concept. Therefore, equation 2.47 and 2.49 evaluated in this section already considered these approach. In summary, it can be concluded, that the derived time-to-magnitude relation for Bernstein is based on two separated portions. The one defined in equation 2.47 corresponds exactly to the result from section 2.2. For the second portion, the derived scope of validity needs to be adjusted regarding a shift of "1" which leads the normalization to be equal. Under these constraints the derived general equation 2.53 corresponds to the claim of method 1 which is restricted to  $T_{\text{samp}} = T_{\text{ref}}$ . The dependencies are depicted in the following equations 2.55 and 2.56.

In comparison of method 1 in equation 2.34 the multi-bit approach for various time variants (i.e.  $T_{\text{samp}} \neq T_{\text{ref}}$ ) of method 2 can be translated to an exact correspondence. Therefore, the dependency for the scope of validity of the time error was applied in order to shift the Taylor series expansion towards a comparable relation, thus that equation 2.56 demonstrates the equality. The equality of the sampling time expression (Eqn. 2.55) is obvious and can be directly attributed to the uniform sampling relation of equation 2.21.

Sampling time expression:

$$\frac{q^2}{3} 2^{2N-3} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \equiv E_{\text{bern}[(t \mapsto q)^2]} \quad (\text{Eqn. 2.21}) \quad (2.55)$$

Composition between  $T_{\text{ref}}$  and  $T_{\text{samp}}$  (Eqn. 2.52):

$$q^2 2^{2N} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \cdot \sum_{k=1}^{\text{limit}} (-1)^{2k} \frac{(\pi f_{\text{sig}} 2^{N-1} k T_{\text{ref}})^{2k}}{(2k+1)!}$$

Composition between  $T_{\text{ref}} = T_{\text{samp}}$  and shift related to Eqn. 2.50:

$$q^2 12 \sum_{k=1}^{2(N-1)-1} (-1)^k \frac{(\pi f_{\text{sig}} 2^{N-1} k T_{\text{samp}})^{2k+2}}{(2k+1)!} \Rightarrow q^2 \sum_{k=1}^{2(N-1)} (-1)^{2k} \frac{(\pi f_{\text{sig}} 2^{N-1} k T_{\text{samp}})^{2k}}{(2k+1)!}$$

Method 1  $T_{\text{ref}} = T_{\text{samp}}$ :

$$q^2 \cdot \sum_{k=1}^{2(N-1)} (-1)^{2k} \frac{(\pi f_{\text{sig}} 2^{N-1} k T_{\text{samp}})^{2k}}{(2k+1)!} \quad (\text{Eqn. 2.34})$$

Comparison Method 1 and method 2:

$$E_{[(t \mapsto q)^2]}(\text{method 1}) \equiv E_{[(t \mapsto q)^2]}(\text{method 2}) \quad (2.56)$$

## General SNR Approach for Non-uniform Sampling

The hypothesis postulates a scope for the derivation of a general expression for the signal-to-noise ratio of non-uniformly sampled signals. Therefore, the hypothesis postulates, that any individual intersection between the input signal and the reference signal can be expressed as a noise portion. The summation of each noise portion defines the total noise which is introduced by sampling. Compared to uniformly sampled signals, where each noise portion offers the same weight, each individual noise portion of non-uniformly sampled signals is weighted by the probability of occurrence and the related binary weight of the actual intersection. Again, the quantization noise determines the upper limit of resolution and thus depicts an additional noise portion.

Related to the misalignment assumption in section 2.1.2 based on the rms consideration of the Bernstein function, the normalization to the peak values of the intersecting signals needs to be applied. Again, the definition for the total noise power is derived from each individual element of the Taylor series expansion and describes the quadratic relationship. Therefore, the crest-ratio also needs to be defined for a quadratic relationship, thus that the crest-ratio  $\Gamma_{\text{crest}}^2$  is valid. Based on the derivation and the validation of the expression for the individual noise factors of non-uniformly sampled signals the expression for the signal-to-noise ratio can be evaluated to equation 2.57.

Sampling noise power [ $limit = 4(N - 1) - 2(f_{\text{clk}}/f_{\text{samp}} + 1)$ ]:

$$E[(t \rightarrow q)^2] = q^2 2^{2N} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \cdot \left[ \frac{1}{24} + 2^3 \cdot \sum_{k=4}^{limit} (-1)^k \frac{(\pi 2^{N-2} k \cdot f_{\text{sig}}/f_{\text{clk}})^k}{(k+1)!} \right]$$

Quantization noise power:  $E[\epsilon_a^2] = \frac{q^2}{12}$

Signal power:  $E[f(t)^2] = \frac{q^2}{8} 2^{2N}$

$$SNR = 10 \log \left[ \left( \frac{1}{3 \cdot 2^{2N-1}} + \Gamma_{\text{crest}}^2 \cdot \left( \frac{\pi f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \left[ \frac{1}{3} + 2^6 \sum_{k=4}^{limit} (-1)^k \frac{(\pi 2^{N-2} k \cdot f_{\text{sig}}/f_{\text{clk}})^k}{(k+1)!} \right] \right)^{-1} \right] \quad (2.57)$$

---

### 2.3.4 Evaluation of the General Mathematical SNR Model

The derived equation for the general expression of the signal-to-noise ratio for non-uniformly sampled ADC schemes includes the condition of various time variants ( $T_{\text{samp}} \neq T_{\text{ref}} = T_{\text{clk}}$ ). The general mathematical model can be traced back to the mathematical derivation of a uniformly sampled ADC scheme and a non-uniformly sampled ADC scheme where the conversion time equals the digital clock ( $T_{\text{samp}} = T_{\text{clk}}$ ) as derived for method 1 (sec.: 2.3.1). The proof of concept has demonstrated, that the general approach of the hypothesis can be validated and suggests that the derived mathematical model is able to predict the SNR for every degree of freedom provided by the ADC. The sample rate ( $f_{\text{samp}}$ ), the reference step generation rate ( $f_{\text{clk}}$ ) represented by the digital system clock and the absolute resolution (N) of the ADC define the possible degrees of freedom and can be supervised by the mathematical model as well as by the behavioral MATLAB simulation model. Especially the sample rate is an important factor, since it is representative for a dynamic conversion time, which can be either assigned to a fixed clock rate or represents the dynamic propagation delay of the ADC feedback system.

In order to validate the proof of concept, both mathematical models need to be compared. Therefore, the constraint of equal time variants ( $T_{\text{samp}} = T_{\text{clk}}$ ) needs to be applied to method 2, thus that the hypothesis made for method 1 is valid. The comparison is evaluated for a parametrization  $f_{\text{clk}} = f_{\text{samp}} = 10 - 50$  MHz and applied to resolutions of  $N = 6, 7, 8$  and  $9$  bit. Figure 2.20 illustrates the calculated results of method 1 and method 2 for a resolution of  $N = 8$  bit. It can be validated, that both mathematical models predict the same results, which implies that the assumptions are correct and both models can be converted into each other. However, the illustrated deviations between the results of the methods are caused by inaccuracy related to the number of iteration elements of the Taylor series expansion. The evaluation results revealed that the influence of the iteration number decreases with the resolution. As a result, the more accurate the non-uniform models represent the combination of sampling steps and the resolution, the more accurate are the correspondences between the models. The ability to predict the bandwidth limitation describes a further property concerning both mathematical models. Contrary, the ability of the MATLAB simulation model to predict the bandwidth is restricted due to the evaluation process.

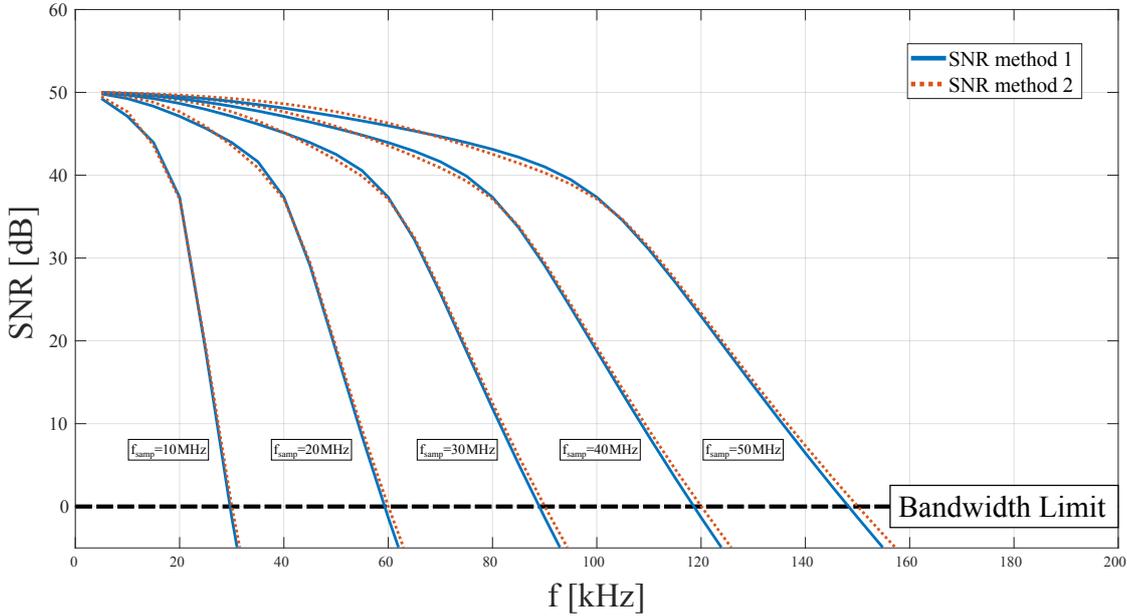


Figure 2.20: Comparison between the derived mathematical models of method 1 (Eqn. 2.39) and method 2 (Eqn. 2.57) for non-uniform sampling. The comparison is conditioned for the normalization of model 2 by the assumption that the clock frequency equals to the sampling rate, thus that  $f_{\text{samp}} = f_{\text{clk}} = 10 - 50$  MHz. Accordance of both models illustrated by an evaluation that is parametrized for  $N = 8$  bit. Deviations are caused due to accuracy related to the number of iteration elements of the Taylor series expansion.

In order to verify the generalized method 2 the independence between the sampling time and the step generation time needs to be considered as independent degrees of freedom, thus that  $f_{\text{clk}} \neq f_{\text{samp}}$ . Again, by the application of the behavioral MATLAB simulation model the prediction property of the derived mathematical model in method 2 can be validated based on the course of the signal-to-noise ratio of the ADC models. The simulations are based on a range of input signal frequencies ( $f_{\text{in}}$ ), ADC resolutions ( $N$ ), clock frequencies ( $f_{\text{clk}}$ ) and sampling frequencies ( $f_{\text{samp}}$ ). The initial system parameters for the tracking scheme ADC are selected for resolutions of  $N = 7, 8$  and  $9$  bit and a digital clock frequency range of  $f_{\text{clk}} = 10, 20, 30$  and  $50$  MHz. The input is defined as sinusoidal signal and ( $f_{\text{in}}$ ) is swept over the expected input range of  $10$  kHz to  $200$  kHz. The average conversion rate corresponds to the sampling frequency and is fixed to  $f_{\text{samp}} = 10$  MHz.

In addition a simulation for a combination of worst case parameter demonstrates the applicability of the mathematical model. Therefore, the parameter choice is defined by  $f_{\text{clk}} = 50 \text{ MHz}$ ,  $f_{\text{samp}} = 20$  and  $30 \text{ MHz}$  and a resolution of  $N = 8$  and  $9$  bit. Thus, these combinations have no even divisor within the mathematical model, which relates to the assumption of a worst case scenario due to the accuracy of the Taylor series expansion. The results are illustrated in figure 2.21.

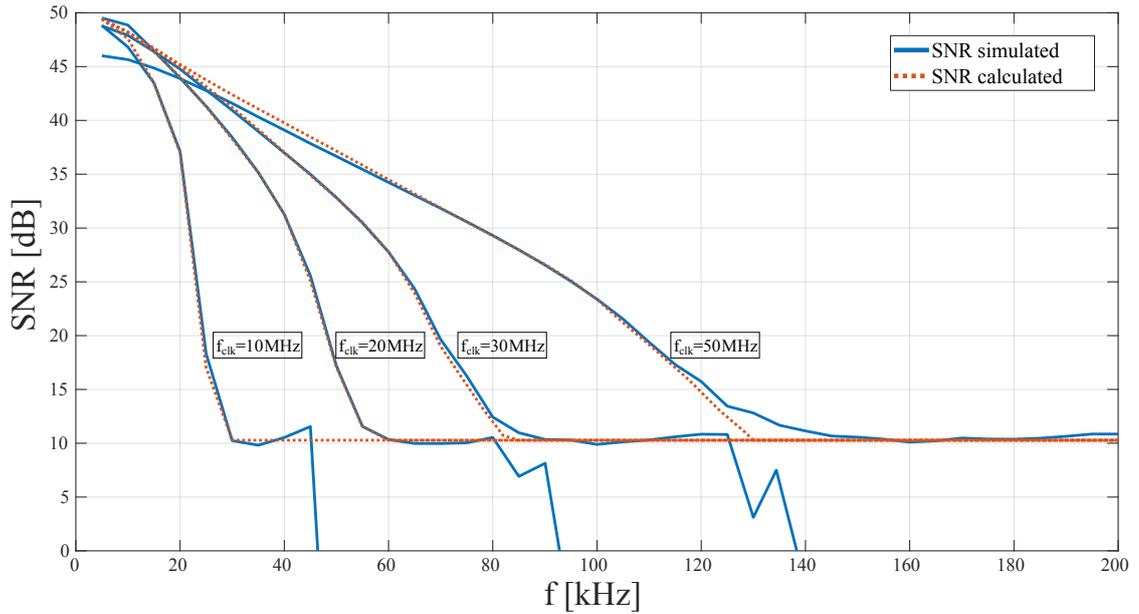


Figure 2.21: Comparison between the behavioral MATLAB simulation model and the calculated model by equation 2.57. Parameters:  $f_{\text{in}} = [10 \text{ kHz to } 200 \text{ kHz}]$ ,  $f_{\text{clk}} = 10, 20, 30$  and  $50 \text{ MHz}$ ,  $N = 8$  bit and  $f_{\text{samp}} = 10 \text{ MHz}$ . An uncertainty of the simulation due to evaluation by FFT explains deviations.

The analysis of the comparison between the behavioral MATLAB simulation model and the mathematical derivation of the SNR for method 2 reveals a high degree of accordance. The further degree of freedom defined by the independence of the sample rate and the clock frequency ( $f_{\text{samp}} \neq f_{\text{clk}}$ ) can be established according to the made hypothesis. Thus the generalized statement of an existing intersection between the input signal and the reference signal at the moment of a composition between the times  $T_{\text{samp}}$  and  $T_{\text{ref}}$  relates the statistical error to that moment and defines the noise portion. In addition, the total noise is based on the sum of the noise portions for a variety of sampling times.

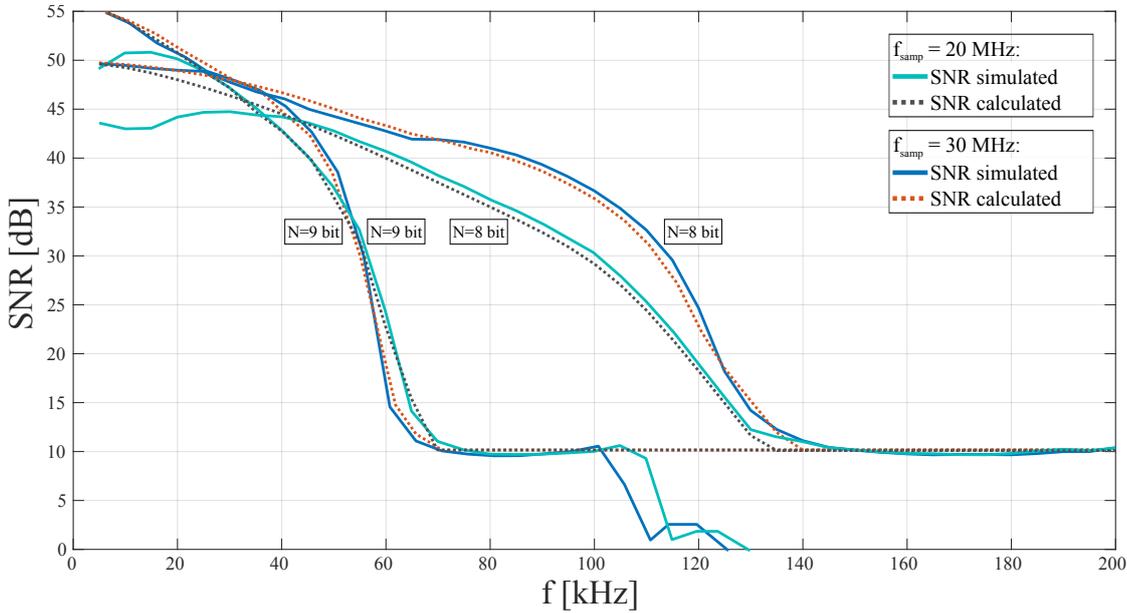


Figure 2.22: Comparison between the behavioral MATLAB simulation model and the calculated model by equation 2.57. Parameters:  $f_{\text{in}} = [10 \text{ kHz to } 200 \text{ kHz}]$ ,  $f_{\text{clk}} = 50 \text{ MHz}$  and  $f_{\text{samp}} = 20, 30 \text{ MHz}$  and a resolution of  $N = 8$  and  $9$  bit. An uncertainty of the simulation due to evaluation by FFT explains deviations. The effect increases for higher rates of non-uniformly generated reference signals. The greater the difference between  $f_{\text{samp}}$  and  $f_{\text{clk}}$ , the less precise is the simulation model.

In order to examine boundary conditions, the validity of equation 2.57 is verified by a parameter combination, which relates a worst case scenario based on the accuracy of the Taylor series expansion. The results are illustrated in figure 2.22 and verifies the mathematical expression even for boundary conditions. Thus, the mathematical expression corresponds to the MATLAB simulation model. Deviations could be explained by the uncertainty of the simulation due to evaluation by FFT. The aspect becomes apparent close to the limitations of the evaluation process for a clock frequency of  $f_{\text{clk}} = 50 \text{ MHz}$ . The effect increases for higher rates of non-uniformly generated reference signals. Thus, the inaccuracy by simulation corresponds to the composition between the sample rate and the clock rate as ratio of  $f_{\text{clk}}/f_{\text{samp}} = 5$ . The greater the difference between  $f_{\text{samp}}$  and  $f_{\text{clk}}$ , the less precise the simulation model. Thereby, the dependency can be explained by

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the uncertainty of the evaluation process, which increases for an increasing number of non-uniform sampling steps. As illustrated in figure 2.22, the decrease of the ratio towards  $f_{\text{clk}}/f_{\text{samp}} = 50/30 = 1.\bar{6}$  stabilizes the evaluation process by reducing the number of non-uniform sampling steps.

Based on the comparison between the MATLAB simulation model and the mathematical derivation of the SNR for method 1 and for method 2, it can be concluded that the hypothesis is valid. Therefore, equation 2.57 of method 2 provides a general mathematical expression to determine the signal-to-noise ratio of non-uniformly sampled signals converted by an ADC.

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## 2.4 Summary on Behavioral and Mathematical Modeling

The non-uniformity of a conversion scheme based on the tracking required a novel mathematical definition of the ADC behavior. The interaction for described degrees of freedom to be parametrized by the ADC sampling algorithm had to be derived in these terms. The degrees of freedom apply to a sampling algorithm based on a delta function. It describes a relation between target parameters for absolute resolution, conversion rate, and sampling generation rate (digital clock rate). Besides the quantization noise, the non-uniform sampling introduces further noise to the system, defined as sampling noise. The amount of the system noise caused by non-uniform sampling is a direct relation to the delta function. Characteristics as absolute resolution and input signal bandwidth are fundamental parameters in order to compare ADCs. These characteristics are related to the conversion rate and the digital clock rate of ADCs. The approach to compare these characteristics in terms of information density of the converted signal is based on the signal-to-noise ratio (SNR). Therefore, this chapter relates the evaluation process of non-uniformly sampled ADCs to the SNR.

A MATLAB simulation model (section 2.1.4), parametrized by the described degrees of freedom, provides information about the expected ADC behavior. The behavioral model converts an analog input signal into its binary correspondence. Thereby, the simulation model processes a sinusoidal input signal. In this procedure, the SNR analysis of the binary ADC output considers a fast-Fourier transform (FFT) provided by the MATLAB SNR tool. Since MATLAB requires a uniform signal for an accurate representation, the amount of data points needs to be high enough in order to satisfy a close approximation for the SNR of non-uniformly sampled signals. Nevertheless, the accuracy of the SNR may vary. In addition, the simulation time increases with the amount of data needed for an accurate representation.

The derivation of the mathematical expression for the definition of boundary conditions and the signal-to-noise ratio provides an accurate SNR prediction method for a non-uniformly sampled ADC. A stepwise derivation with the goal of a general expression for the SNR was pursued to approach the problem. Therefore, initial boundary conditions for non-uniform sampling schemes were derived, and an initial hypothesis, which relates the number of effective bits to the number of successive samples, was made. Based on the hypothesis, the expression for the maximum resolution bandwidth and the overall bandwidth limit were derived. The verification process was based on the SNR results of the MATLAB simulation model, which has demonstrated that the expressions are valid. Since the expressions for the bandwidth limits are two central points within the SNR

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course over the input frequency band of interest, no statement about the SNR course between these points can be made. Due to this fact, a mathematical equation for the SNR was derived based on a new hypothesis. This hypothesis claims that if at least two intersections between the input signal slope and the reference signal slope exist, it will be in the interval of the input signal period. If it does not exist, the effective resolution is less than "1-bit" and the input signal frequency is not within the ADC bandwidth. Related to this hypothesis, an expression for the SNR was defined based on the "Bernstein Theorem". It relates the intersection of the input signal slope and the reference signal slope as a magnitude quantized value. The expression is representable as sampling noise. The total noise derives in combination with the quantization noise.

Due to the claim made by the hypothesis that there needs to exist an intersection, the derived SNR is related to a uniformly sampled signal, which depends on the sampling frequency. This behavior was verified by the MATLAB simulation model. The results and the evaluation of the hypothesis statement revealed that the hypothesis needs to be more specified to describe the SNR as an expression for non-uniformly sampled signals. In general, the made hypothesis was extended by the addition of the claim that the existence of any intersection within the input signal period is related to a variety of sample portions based on the minimum sample time. The condition arises for the intersection assumption that the derivation of the total noise power needs to be decomposed. Based on this assumption, two methods were derived that describe the mathematical model for non-uniform sampling. Method 1 specifies the condition if the degrees of freedom of the sampling frequency and the clock frequency are equal, which is the definition for the conventional Tracking ADC approach. Method 2 generalizes this specification by the assumption of inequality between the sampling frequency and the clock frequency. It derives a general expression for the SNR and considers all degrees of freedom independently and without restrictions.

First of all, method 1, which specifies the equality of the sampling frequency and the clock frequency, was considered. Therefore, the hypothesis was specified to the claim that if there is an intersection between the input signal and the reference signal at a sample time under the constraint that the step generation time equals the sample time, the intersection can be located at the input signal moment of the sampling time. The total noise depends on the sum of the noise portions for a variety of sampling times. The proposed approach for the system approximation provides a method to derive the noise portion generated by sampling straight from the input signal power. The mathematical decomposition of the noise portion as a portion of the unconstrained input signal power resulted from a Taylor series expansion. Based on this approach, the resulting expression for the SNR

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relates to non-uniform sampling. The validation of the specified hypothesis was based as a proof of concept on the one hand and by the MATLAB simulation model on the other hand. The backtracing of the mathematical expression within the proof of concept for the non-uniform SNR to the expression of the uniform SNR revealed the uniform sampling as a particular case of non-uniform sampling. The proof of concept demonstrated the tracing back the mathematical expression for the non-uniform SNR to the expression of the uniform SNR revealed the uniform sampling as a particular case of non-uniform sampling. Furthermore, the entire course of the signal-to-noise ratio could be predicted by the non-uniform model of method 1. The validation was evaluated by the MATLAB simulation model and demonstrated a high degree of accordance.

Method 2 introduced a further development, representing a generalized expression for the SNR. It enables an independent consideration for all degrees of freedom. To consider the sampling frequency independently of the clock frequency by method 2 extends method 1 and leads to a generalized form of the hypothesis. The hypothesis claims that if there is an intersection between the input signal and the reference signal at the moment of composition between the times for sampling and reference step generation, the statistical error related to that moment can be defined as noise portion. The total noise depends on the sum of the noise portions for a variety of sampling times. The hypothesis extends the validated claim for the "Bernstein"-relation referred to intersections between the input signal slope and the reference signal slope, where the SNR expression for uniform sampling was derived. Compared to method 1 the noise portion for uniform sampling was decomposed by the Taylor series expansion to determine the individual noise portions. This approach satisfies the conditions for non-uniform sampling, where the statistical error is related to the moment of composition between the sampling and reference step generation time. Based on the made hypothesis, the resulting expression for the SNR is related to non-uniform sampling in a generalized form. Within a proof of concept, the expression was traced back to the uniform SNR expression and the expression derived in method 1. It reveals that the generalized form can be converted to the specialized form and thus demonstrates that the expression of method 2 is the general representation of the non-uniform signal-to-noise ratio. Furthermore, under the constraint of sampling and clock frequency equality, both methods were compared by their mathematical models, which reveals high accordance, already investigated through the proof of concept. In addition, the validity of the general non-uniform equation was determined by the comparison to the behavioral MATLAB simulation model. Under consideration of any degree of freedom (i.e. sampling rate, clock frequency, and resolution), the general SNR expression was evaluated by various combinations that include edge cases. The comparison between the simulation model and the mathematical model demonstrates high accordance.

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In summary, this chapter derives a set of mathematical expressions for the description of the bandwidth and SNR course of uniformly sampled ADCs and non-uniformly sampled ADCs. These models can represent the proposed tracking scheme. Furthermore, these basic equations provide a method to predict the signal-to-noise ratio based on non-uniformly sampled ADC algorithms. The general expression illustrates the ability to characterize the SNR by the resolution, the sampling rate, and the digital clock rate concerning degrees of freedom. Non-linearities of the feedback configuration of ADCs due to varying system delays can be considered a statistical mean or dynamic function of the sampling time. Furthermore, algorithmic properties like reference level jumps can be related to a ratio between resolution and sampling time by redefining the resolution related to the portion of uniform sampling. Based on these properties, the equation provides the ability to predict the signal-to-noise ratio for a new set of sampling algorithms. These open the way to digitally adjust the entire conversion algorithm of an ADC to an application-specific area in a dynamic manner.

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## 3 Algorithmic Tracking Scheme ADC

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In the previous chapter 2 mathematical expressions for the description of non-uniformly sampled ADCs were derived based on physical interrelationships. The derived equations provide a general description of the signal-to-noise ratio for this kind of ADCs. It could be demonstrated that the general expression for the non-uniform sampling scheme can be traced back to a restricted version related to uniform sampling, as for most of the state-of-the-art ADCs. The equations could define the description of essential degrees of freedom for the design of ADCs regarding bandwidth, resolution, and conversion rate. Furthermore, the derived general expressions consider the approach to separate the conversion rate from the digital reference generation rate (i.e. the digital clock). The individual consideration of these parameters enables a farther degree of freedom within the ADC design.

Nowadays, a variety of individual ADC schemes exist. The SoA relates the applicability of the individual ADC schemes to a specific application area [39]. Thereby, each ADC scheme has its advantages and disadvantages. Thus, the demands of the application area determine the selection of the respective ADC. The suitability of these ADCs assesses in a direct comparison. For example,  $\Delta\Sigma$ -ADCs generally perform high resolutions and fewer samples per second (conversion rate), which implies a bandwidth restriction. SAR-ADCs (commonly classified as Nyquist rate ADCs) are used for moderate conversion rate applications under moderate resolutions but can operate with a high input bandwidth. The Flash ADC provides the highest conversion rate and thus the highest bandwidth. However, because of a complex analog hardware structure, the resolution is low. Figure 3.1 depicts a comparison between common ADC topologies classified in categories for resolution and samples per second. The analog hardware implementation of these ADCs primarily determines the specific characteristics. Therefore, to implement a specific sampling scheme, the analog part of the ADC must be designed to meet the requirements of the sampling scheme. There is no flexibility in terms of adjusting or changing the sampling scheme. This factor is the main reason for the restriction of an ADC to the specific application area.

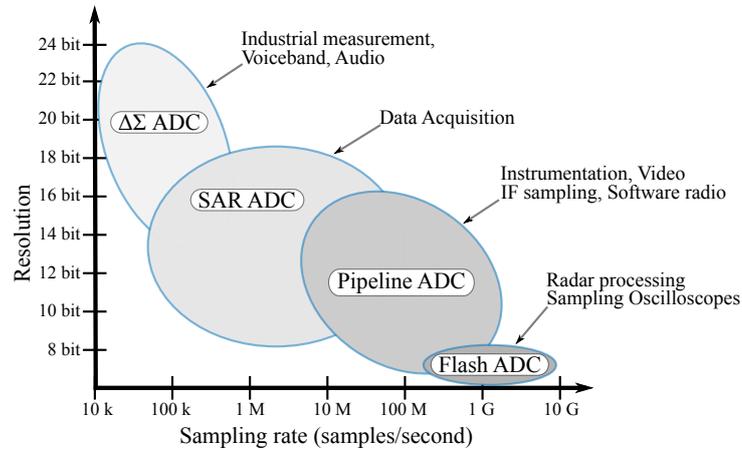


Figure 3.1: Comparison for common ADC topologies classified in approximated state-of-the-art categories based on resolution and samples per second and example application areas. Inspired by [40].

Since nowadays, ADCs are inflexible in terms of a dynamic and hardware-independent sampling algorithm, the ADC scheme introduced in this work should overcome this bottleneck. Therefore, the hardware complexity of the proposed approach reduces to a minimum, and digital operations establish the main operations. The resulting benefit relates to the configuration or even reconfiguration of the sampling algorithm regarding desired characteristics. Therefore, the possible algorithms to be implemented can either define a uniform or a non-uniform sampling scheme. Related to the derived equations in chapter 2 the non-uniform expression (Eqn. 2.57) is the general mathematical form in order to predict the signal-to-noise ratio under certain degrees of freedom. As a demonstrated result, the uniform sampling is a subset of the non-uniform sampling. These relations enable the prediction of the behavior for a new set of sampling algorithms for ADCs. Thus, the proposed ADC topology in this work classifies as algorithmic ADC. In order to implement those sampling algorithms, the analog hardware is reduced to the main basic operations of digital-to-analog conversion and compare. Figure 3.2 illustrates the fundamental schematic of the proposed topology based on the comparator and the DAC as basic components. The Arithmetic-Logic-Unit (ALU) represents the processing component for the sampling algorithm and connects to the analog components in a feedback configuration. The DAC converts digital reference steps defined by the algorithm into an analog representation to specify a dynamic analog reference level. The comparator functions as a 1-bit quantizer and compares the reference level to the analog input signal.

A 1-bit digital stream is generated and indicates the reference signal's direction relative to the input signal. For example, the information about the relative position of the direction is "UP" if the reference is higher than the input signal. Contrary, the information about the relative position of the direction is "DOWN" if the reference is lower than the input signal. The algorithm can react to the status of the digital comparator and process further decisions to provide updated reference steps.

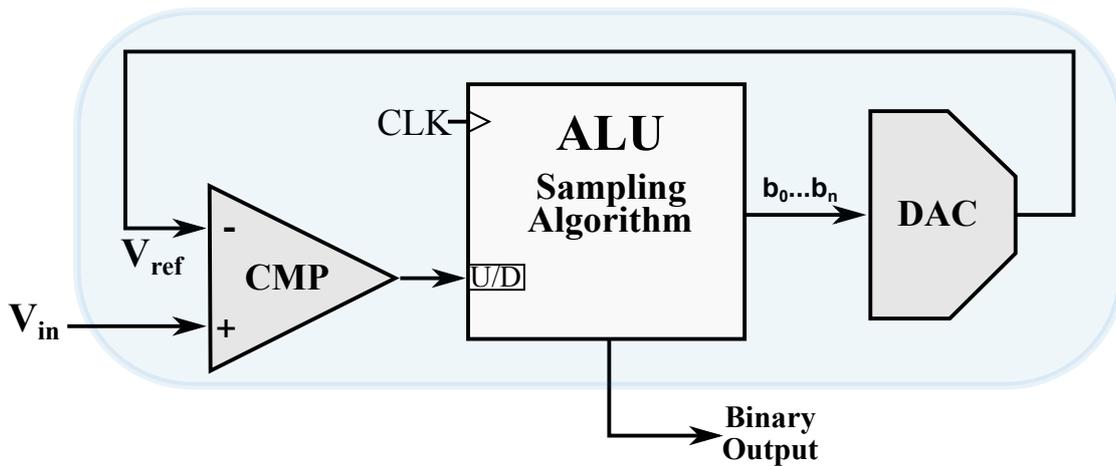


Figure 3.2: Algorithmic ADC schematic based on the main basic analog components for hardware-independent processing of the sampling algorithm. Components: Comparator (CMP), Digital-to-Analog Converter (DAC) and Arithmetic Logic Unit (ALU).

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### 3.1 Application-Specific Algorithm

The proposed ADC methodology describes a general purpose algorithmic ADC. In this terms, the hardware effort is reduced to the main basic properties of digital-to-analog conversion and compare. Therefore, the topology is characterized by a digital-to-analog converter (DAC) and a comparator. The specific operations of the ADC are implemented by a sampling algorithm, which defines the properties of the reference step generation. The hardware component that provides the algorithm is characterized as arithmetic-logic-unit (ALU). So far the ALU is not further specified, but provides the algorithm specific digital operations. The general purpose is enabled by the algorithmic implementation and can either be static for a specialist purpose or even reconfigurable (i.e. programmable). Based on this background, an application specific sampling algorithm is characterized in this chapter.

In general, an algorithm is an unambiguous operating instruction. The individual tasks must therefore determine deterministic results based on the respective input values. The processing time of the algorithm is decisive for the sampling speed of an ADC. The faster the input data is processed by the algorithm, the faster the update rate of the reference steps, which are compared to the analog input. Fast data processing, in turn, can be established for small data sets. In case of the proposed ADC methodology the 1-bit digital stream of the comparator is informative about the direction of the reference signal in relation to the input signal. If one refers to the fact that the algorithm creates a delta between consecutive samples, the calculation time is reduced enormously. In the best case, an "actio-reactio" property of the algorithm is achieved within the next possible sample period defined by the ADC feedback delay. Furthermore, the generation of deltas between consecutive reference steps enables a continuous scanning of the input signal. This property is commonly referred to as tracking. However, the tracking scheme presupposes, that a generation of deltas in magnitude quantization also means the generation of deltas in time. These deltas in time are characteristic for a non-uniform sampling scheme, which is the base for the tracking scheme. As derived in chapter 2, the non-uniform sampling establishes the ability to quantize a signal as well as in magnitude as in time. In relation of the delta in time and in magnitude, the general information density (i.e. information per step) can be higher compared to uniform sampling where exclusively magnitude quantization in a fixed time interval is decisive about the information density. Therefore, it can be advantageous to convert a signal in a non-uniform scheme. Furthermore, due to the concrete information in time between consecutive samples, a sample and hold device is not necessary. This type of converter is understood as continuous time ADC and reduces the hardware complexity. Based on these considerations, the tracking scheme seems to be advantageous in order to derive an algorithm, which is defined by a sequential processing.

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A Tracking ADC is the most basic form of implementing a tracking scheme. The conventional Tracking ADC is able to perform the afore defined algorithmic requirements. Nowadays its application in the field of signal monitoring is widespread [30, 31]. However, it is hardly used in the traditional analog-to-digital conversion. This has the background, that the Tracking ADC indeed processes a signal quasi immediately due to a conversion based on the delta time property, but the delta magnitude property is restricted to 1-bit. This implies, that the event of an alteration is determined quickly, but the amount of the alteration in magnitude is related to the slope of the input signal. Therefore, the higher the slope of the input signal, the protracted the conversion time. As a result with higher input frequencies less conversion steps can be resolved. In this terms, the conventional Tracking ADC is bandwidth limited. With increasing resolution of the ADC, the lower the bandwidth becomes. This leads to the fact, that the conventional implementation of a Tracking ADC is not suitable for the classical analog-to-digital conversion.

There are a variety of useful possibilities for implementing an algorithm for the general purpose ADC. The rationality is related to the specific area of application. Based on the postulated advantages of a non-uniformly sampled tracking scheme, this section transfers the algorithm of the general purpose ADC to the tracking scheme. In order to derive rational algorithms and thus define an application area, the sampling properties of the conventional Tracking ADC act as a basic approach. Related to the disadvantages of the Tracking ADC referred to the bandwidth limitation, the proposed tracking scheme is reconfigured. Therefore, the derived algorithm in this section should demonstrate how a combination of the degrees of freedom (i.e. resolution, sampling rate and clock rate) needs to be configured in terms of bandwidth expansion. A prediction of the bandwidth and the related signal-to-noise ratio course within the bandwidth of interest are referred to the SNR equations derived in chapter 2. Based on this approach, the configuration and combination for the degrees of freedom is investigated and the effects for the effective resolution determined. Thus, the reconfiguration parameter of the new tracking scheme algorithm are defined. The tracking scheme algorithm is then configured in order to enhance the effective resolution for the bandwidth expanded approach.

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### 3.1.1 Algorithmic Expansion of the Bandwidth Limitation

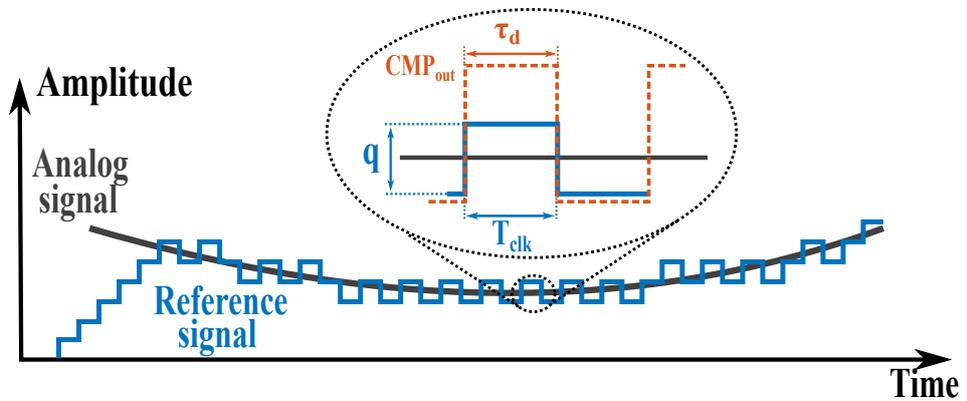
An application specific algorithm for the general purpose ADC is based on the tracking scheme procedure. Herby, the conventional Tracking ADC algorithm should serve as a starting point. Related to the bandwidth limitations of this kind of ADC, the basic tracking scheme algorithm should be reconfigured in terms of bandwidth expansion. Therefore, the degrees of freedom defined in chapter 2 should be parameterized to meet this demand. In order to characterize the parametrization of the resolution, sampling rate and digital clock rate, the conventional Tracking ADC scheme is analyzed in advance. Therefore, the ADC schematic in figure 3.2 serves as reference for the conventional approach, since the configuration already provides the required hardware components. The Tracking ADC is constituted by a comparing device (Comparator) and a digital-to-analog converter (DAC). The sampling algorithm for the tracking scheme is implemented on the ALU. In case of the conventional Tracking ADC the algorithm is constituted by an up-down counter, whereby the comparator state is connected to the up-down switch of the counter. The digital counter state is connected to the DAC as binary input, which is converted in an analog representation. This is the reference signal which is processed by the comparator. The comparator, in turn, acts as one bit quantizer upon the decision if the reference signal is above or below the input signal. Thus, a level crossing between these signals can be detected. The interface to the up-down switch of the counter causes the counter to invert the counting direction. Based on this principle, the Tracking ADC is connected in a feedback configuration which is constraint by the feedback delay ( $\tau_d$ ) of this loop. The maximum feedback delay determines the sampling time. In case of the conventional Tracking ADC it is defined as the average sampling rate or conversion rate. The update rate of consecutive reference steps and thus the clock rate is also limited to this constraint (i.e.  $f_{\text{samp}} = \tau_d^{-1} = f_{\text{clk}}$ ).

In order to track the analog input signal for the first time, the counter counts up periodically until the level crossing between the dynamic reference signal and the analog signal is detected by a binary bit inversion of the comparator. This procedure causes the counter to invert the counting direction. The count down process is executed until the level crossing is detected again and the order to invert the counting direction is caused by the comparator again. In this way, the tracking ADC can track the analog signal using the reference signal. The conversion scheme of the conventional Tracking ADC algorithm under the constraint of ( $f_{\text{samp}} = \tau_d^{-1} = f_{\text{clk}}$ ) is illustrated in figure 3.3(a).

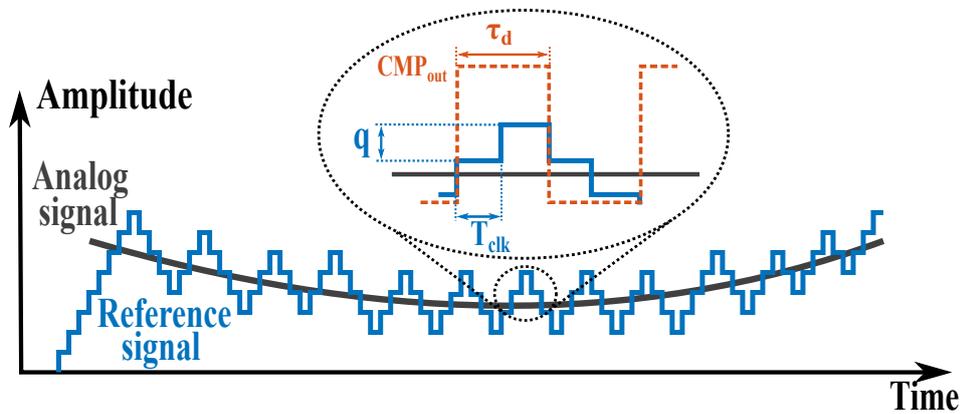
As derived in chapter 2 a tracking scheme approach is related to level crossing. The level crossing, in turn is determined by the intersection between the reference signal and the analog input signal. Therefore, the intersection moment is determined for the slope equality of both signals. The slope of the reference signal is defined by the single step consideration. It is established for a single quantization step within a single generation time, thus that the relation  $q/f_{\text{clk}}$ . Whereby the step generation time is equal to the sampling time as constraint for the Tracking ADC. Based on the level crossing approach, equation 2.11 defines the absolute bandwidth. Therefore, it is decisive about the ability to extend the absolute bandwidth of the tracking scheme. Related to the degrees of freedom for the resolution  $N$  and the step generation rate ( $f_{\text{clk}}$ ) as given in equation 2.11, the parametrization of these variables decides about the absolute bandwidth. Based on the fact that the bandwidth improvement should not result in a deterioration of the remaining ADC parameters, decreasing the resolution is not applicable. In this term, the reference step generation rate ( $f_{\text{clk}}$ ) needs to be increased, as demonstrated concerning 3.1.

$$f_{\text{max}_{\text{bw}}} \leq \frac{3}{2} \cdot \frac{f_{\text{samp}}}{2^{N+1}} \Rightarrow \boxed{\text{decouple: } f_{\text{clk}}, f_{\text{samp}}} \Rightarrow \uparrow f_{\text{max}_{\text{bw}}} \leq \frac{3}{2} \cdot \frac{\boxed{\uparrow f_{\text{clk}}}}{2^{N+1}} \quad (3.1)$$

Referred to the conventional Tracking ADC constraint of  $f_{\text{samp}} = \tau_{\text{d}}^{-1} = f_{\text{clk}}$ , the step generation rate needs to be decoupled from the sampling rate. Thus, the algorithmic generation of reference steps is faster than the internal feedback system delay  $\tau_{\text{d}}$  allows. However, the slope of the reference signal within a sampling time period increases, which allows to detect a higher input signal slope. In turn, the bandwidth of ADC is increases due to the reconfiguration of the tracking scheme. Compared to the conventional approach a bandwidth expansion is established using a higher clock frequency ( $f_{\text{clk}}$ ). Related to equation 3.1, the bandwidth increases linearly with the clock frequency. The evolving tracking scheme of the proposed algorithm based on a 2 times faster step generation rate ( $f_{\text{clk}}$ ) is shown in figure 3.3(b). In general, the basic principle of the proposed algorithm, is to generate a triangular staircase function whose switching moments are specified by the comparator.



(a) Conversion scheme of the conventional Tracking ADC algorithm ( $f_{\text{samp}} = \tau_d^{-1} = f_{\text{clk}}$ ).



(b) Conversion scheme of the proposed tracking algorithm ( $f_{\text{samp}} = \tau_d^{-1} = 2f_{\text{clk}}$ ).

Figure 3.3: Comparison between the conversion scheme of the conventional Tracking ADC (a) and the conversion scheme of the proposed tracking algorithm (b). Improved tracking ability of the proposed approach by a higher slope of the reference signal. Based on a 2 times faster step generation rate ( $f_{\text{clk}}$ ), the absolute bandwidth is doubled. For a 3 times faster rate, the bandwidth is tripled and for a 4 times faster rate the bandwidth quadrupled  $\rightarrow$  linear dependency.

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The average number of sampling steps during a sampling period, can be approximated by the ratio between sampling time and reference step generation time ( $f_{\text{clk}}/f_{\text{samp}}$ ). The term average defines the ratio which is set for a constant signal. Due to the dynamic property of the input signal the actual sampling time needs to be considered as a relation of the composition of  $f_{\text{clk}}$  and  $f_{\text{samp}}$ . This fact explains the ability to follow the input signal with the maximum resolution, although a large number of steps are formed which, in this way, are skipped. The sequence of conversion steps (determined by the comparator inversion) is based on the relation between the input signal and the reference signal. The resulting delta is the difference between consecutive steps in time (subdivided in quantized time steps by  $f_{\text{clk}}$ ) and at the same time the difference in magnitude (subdivided in quantization steps). Thus, the delta between conversion events is formed by the relation between a current step and the previous step. Therefore, the proposed tracking scheme is a Delta scheme based on relative conversion steps. This relative relationship allows the algorithm to account for a level crossing event for the ascending reference signal (above the analog signal) as well as for the descending reference signal (below the analog signal) of the evolving triangular staircase function. Finally, the mean value can be formed from two consecutive conversion results, which determines the total result close to the analog origin. In the ideal case, the conversion of the total result is related to twice the minimum feedback delay ( $\tau_d$ ), since the entire reference signal formation is generated during this dead time. While the dead time, no system response can be generated by the comparator. Therefore, the reference signal can be formed in any rational way on the one hand. On the other hand, the dead time acts as low pass filter due to the fade-out property. Although these considerations can also be related to the conventional approach, but there are significantly fewer variations between successive values which is based on the slower reference step generation. Nevertheless, it would be advantageous to determine the mean value for consecutive conversion results for the conventional Tracking ADC, since the never stable toggle of the binary reference signal is suppressed when it is used as general conversion result. The comparison between the conventional tracking scheme in figure 3.4(a) and the proposed tracking scheme in figure 3.4(b) reveals the described properties. The numerical output values are presented in an exemplary conversion cycle under the consideration of equal input signal slopes for both conversion schemes. Due to the ability of the proposed approach to detect a higher slope in relation to a higher variety of reference steps, the generated mean of the conversion results demonstrates a higher accuracy (i.e. number of divers results) of the converted value. The situation of the exemplary conversion cycle explains the absolute bandwidth expansion predicted by equation 3.1 due to the fact, that a larger number of different values per time describe a higher information density. So, if the information density of the proposed approach is higher for equal slopes, than the conversion can be established for a higher input frequency.

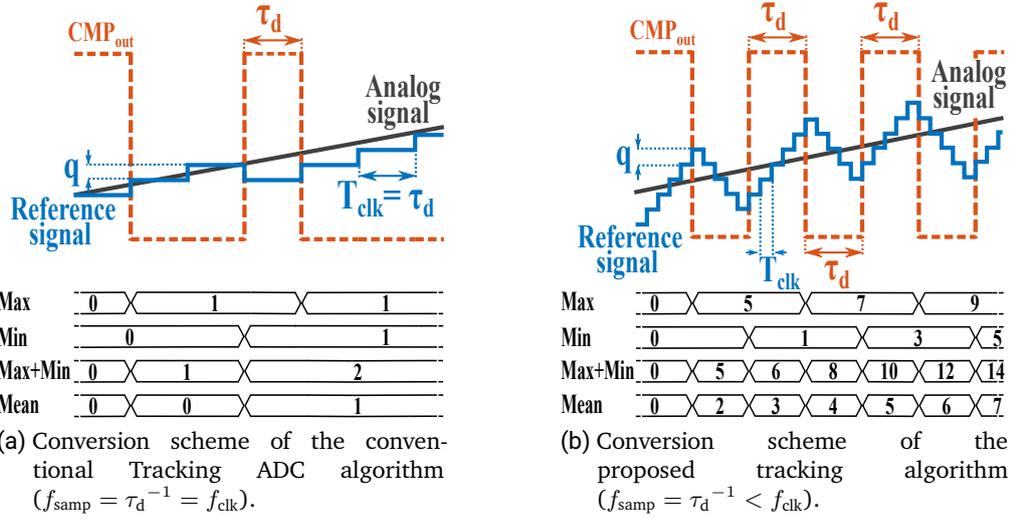


Figure 3.4: Numerical comparison of the conventional tracking scheme (a) and the proposed tracking scheme (b) for an equal input signal slope. Sample development of the tracking schemes based on an exemplary conversion. Mean calculation of the converted values in order to illustrate the output generation of the schemes.

### Evaluation of the Bandwidth Expansion Algorithm

The theoretical assumptions of the bandwidth extension approach should be verified by the course of the signal-to-noise ratio (SNR). Therefore, the application of the general expression for the SNR of non-uniformly sampled signals (Eqn. 2.57) derived in chapter 2 is applied for the validation. As demonstrated, the general expression is able to predict the absolute bandwidth as well as the maximum resolution bandwidth. Based on this property, the absolute bandwidth in terms of extension can also be predicted by the SNR equation. The condition is determined for a SNR value of "0" at the crossing section of the bandwidth limitation. However, as demonstrated by simulations the re-evaluation of the equation would reveal in the same results as predicted in equation 2.11. In addition, since the SNR expression defines the total signal-to-noise ratio course within the bandwidth of interest, also the limit for the maximum resolution can be determined. This case would reveal, that the SNR value of the maximum resolution limit is dropped by 6.02 dB (i.e. 1-bit effective resolution). So it is possible to define a bandwidth where the maximum resolution can be resolved. However, in consideration of equation 2.57 the

expression illustrates the dependencies of the sampling frequency ( $f_{\text{samp}}$ ) as well as for the clock frequency ( $f_{\text{clk}}$ ). In comparison the absolute bandwidth allows for a simplified consideration of the intersection moment of the reference signal slope related to the clock frequency which is exclusively generated from  $f_{\text{clk}}$ . The resolution limited bandwidth, in turn, considers the sampling in addition. Equation 2.4 was derived for the case, that the reference generation frequency ( $f_{\text{clk}}$ ) equals to the sampling frequency ( $f_{\text{samp}}$ ). In order to derive an expression for the bandwidth of the maximum resolution either the SNR equation can be rearranged as described, or equation 2.4 adapted. Based on the fact, that the series expansion for the SNR equation is based on the number of series elements, a closed equation form can not applied. Therefore, the proposed approach is by theoretical assumptions for the adaption of equation 2.4 which are then validated by the SNR course of the general expression.

In order to adapt the limitation of the maximum resolution for equation 2.4 to the composition between the sampling frequency ( $f_{\text{samp}}$ ) and the step generation rate ( $f_{\text{clk}}$ ), the relationship between these parameters is decisive. Besides the level crossing the initial feedback delay ( $\tau_d$ ) of the system is decisive, since this time is described as dead time where no processing can be detected. If the dead time is passed a detection can be processed upon the relation between the input signal and the reference signal. Since the generation of the reference signal is related to  $f_{\text{clk}}$  two probabilities of occurrence needs to be distinguished. The conversion case if the multiple of  $T_{\text{clk}}$  is exactly the dead time (assumed as  $T_{\text{samp}}$ ) and the other case if the next detectable transition is scheduled for  $T_{\text{samp}} + T_{\text{clk}}$ . This conversion behavior is illustrated in figure 3.5.

Related to the fact, that the limitation of the maximum resolution is based on the two probabilities of occurrence a relation for the proportional appearance must be derived. The possibility of a conversion step equals the dead time by  $T_{\text{samp}}$  is already represented by equation 2.4. Therefore, the expression needs to be extended in terms of the case  $T_{\text{samp}} + T_{\text{clk}}$ . Thus, the relation between  $T_{\text{clk}}$  the arithmetic mean of  $T_{\text{samp}} + T_{\text{clk}}$  should be considered, since it determines the proportional deviation from dead time ( $T_{\text{samp}}$ ). Under these conditions the expression for the bandwidth limitation related to the maximum resolution equation 3.2 evolves.

So far it was considered, that the feedback delay ( $\tau_d$ ), represented as dead time, is defined as the sampling time ( $T_{\text{samp}}$ ) and constraint to the conversion time ( $T_{\text{conv}}$ ). Based on the consideration, that the actual conversion time of a sampling algorithm can be different to the sampling time, the simplification that these times equal, needs to be defined separately now. This enables the ability to define the algorithm based on its sampling properties, but still related to the system delay. In order to decouple the physical system parameter of

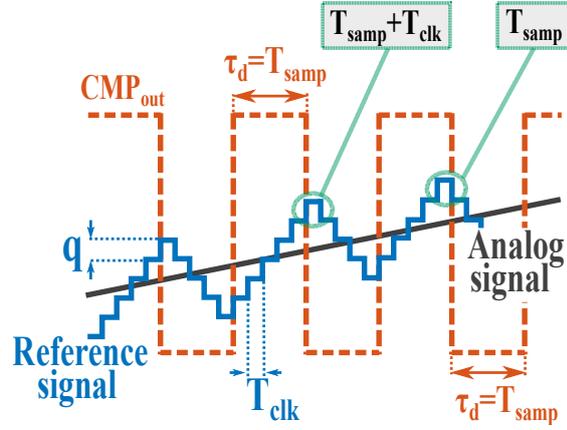


Figure 3.5: Consideration of the proposed conversion step generation. Due to the composition between the sampling time ( $T_{\text{samp}}$ ) and the step generation time ( $T_{\text{clk}}$ ) the time for the conversion step can either be  $T_{\text{samp}}$  or  $T_{\text{samp}} + T_{\text{clk}}$ . The decision depends on the relation between the analog input signal and the initial feedback delay.

the feedback delay ( $\tau_d = T_{\text{samp}}$ ) from the system related parameter of the conversion time ( $T_{\text{conv}}$ ), the parameter  $f_{\text{samp}}$  from the initial expression is now defined as  $f_{\text{conv}}$ , which is caused by the comparator switching moments. The parameter which is decisive for the dead time or the minimum time for a sample is constrained for  $f_{\text{samp}_{\text{min}}} = \tau_d^{-1}$ . Thus, the resulting expression for the determination of the bandwidth limitation related to the maximum resolution is rearranged to equation 3.3.

$$f_{\text{max}_{\text{res}}} \leq \sqrt{\frac{3}{2}} \cdot \frac{f_{\text{samp}_{\text{min}}}}{\pi 2^N} \cdot \frac{2 f_{\text{clk}}}{f_{\text{clk}} + f_{\text{samp}_{\text{min}}}} \quad (3.2)$$

$$\Rightarrow \boxed{\text{decouple: } f_{\text{samp}_{\text{min}}} \text{ to } f_{\text{conv}}} \Rightarrow$$

$$\boxed{f_{\text{max}_{\text{res}}} \leq \sqrt{\frac{3}{2}} \cdot \frac{f_{\text{conv}}}{\pi 2^N} \cdot \frac{2 f_{\text{clk}}}{f_{\text{clk}} + f_{\text{samp}_{\text{min}}}}} \quad (3.3)$$

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## Validation of the Bandwidth Expansion Algorithm

The validation process of the bandwidth expansion algorithm is performed based on equation 2.57 for the SNR of non-uniformly sampled signals. Therefore, the signal-to-noise ratio course of the conventional Tracking ADC and the proposed tracking scheme is calculated based on comparable system parameters. In this terms, the feedback delay  $\tau_d$ , defined as  $f_{\text{samp}_{\text{min}}}$  is assumed for 10 MHz and the resolution  $N = 8$  bit. Related to the constraints of the conventional Tracking ADC algorithm the conversion rate equals the step generation rate, thus that  $f_{\text{conv}} = f_{\text{clk}}$ . Furthermore, the conversion rate is assumed for an optimum, which implies, that it equals to the feedback delay  $f_{\text{samp}_{\text{min}}} = f_{\text{conv}} = 10$  MHz. In order to illustrate the bandwidth extension property, the reference generation rate of the proposed tracking scheme is assumed to be 5 times higher, thus that  $f_{\text{clk}} = 50$  MHz. The resulting conversion rate of the proposed algorithm needs to be considered separately, since it is based on the algorithmic properties. On the one hand it is restricted to the dead time of the physical ADC properties, thus that  $f_{\text{samp}_{\text{min}}} = 10$  MHz needs to be assumed as upper limit. On the other hand, the algorithm defines how the conversion rate can be derived based on the algorithmic parameters and the minimum sample rate. Referred to figure 3.7a, the evolving triangular sample scheme defines that after the detection of the comparator ( $\text{CMP}_{\text{out}}$ ) the inversion of the counting direction is initiated. Due to the faster step generation rate compared to the sampling rate ( $f_{\text{clk}} > f_{\text{samp}_{\text{min}}}$ ) the reference signal level is deviated from the analog input signal by a number of steps. In order to initiate a new conversion cycle and thus the initialization of a new sampling time ( $f_{\text{samp}_{\text{min}}}$ ), the reference signal is forced to return to a level opposite orientation to the analog input. Due to the sequential counting process the return to the opposite orientation to the analog input requires the same time as for the detection. The process is explained in figure 3.7a based on a constant input level, but also under the assumption of a time variant signal the relative dependency of the slopes reveals the same behavior. Due to the fact, that the return to the input signal requires as long as the detection, the conversion rate is composed by the sampling delay and by a number of reference steps, thus that  $T_{\text{conv}} = \tau_d + nT_{\text{clk}}$  results for the conversion time. Indeed, it can be derived, that the process of additional steps ( $nT_{\text{clk}}$ ) requires the sampling time ( $f_{\text{samp}_{\text{min}}}$ ) again, because it is the constraint for the detection of the signal by the feedback delay. Thus, the average conversion time of the proposed tracking scheme requires twice as long the sampling time and results in a conversion rate of  $f_{\text{conv}} = 5$  MHz, which is half of the conventional Tracking ADC conversion rate.

Based on the described parametrization, the absolute limitation of both tracking approaches can be determined by equation 3.1. The prediction by the equation reveals a maximum bandwidth for the conventional ADC of  $f_{\text{bwconv}} = 29.29$  kHz and for the proposed tracking scheme of  $f_{\text{bwprop}} = 146.45$  kHz, which corresponds to a 5 times extension by the linear dependency. Based on equation 3.3 the limit for the maximum resolution of 8 bit is determined. Thus, it reveals in  $f_{\text{resconv}} = 15.22$  kHz for the conventional design and in  $f_{\text{resprop}} = 12.69$  kHz for the Bandwidth-Extended-Algorithm (BEA) tracking scheme. The signal-to-noise ratio course of both designs, which is calculated by equation 2.57 is illustrated in figure 3.6 and demonstrates the validity of the assumptions.

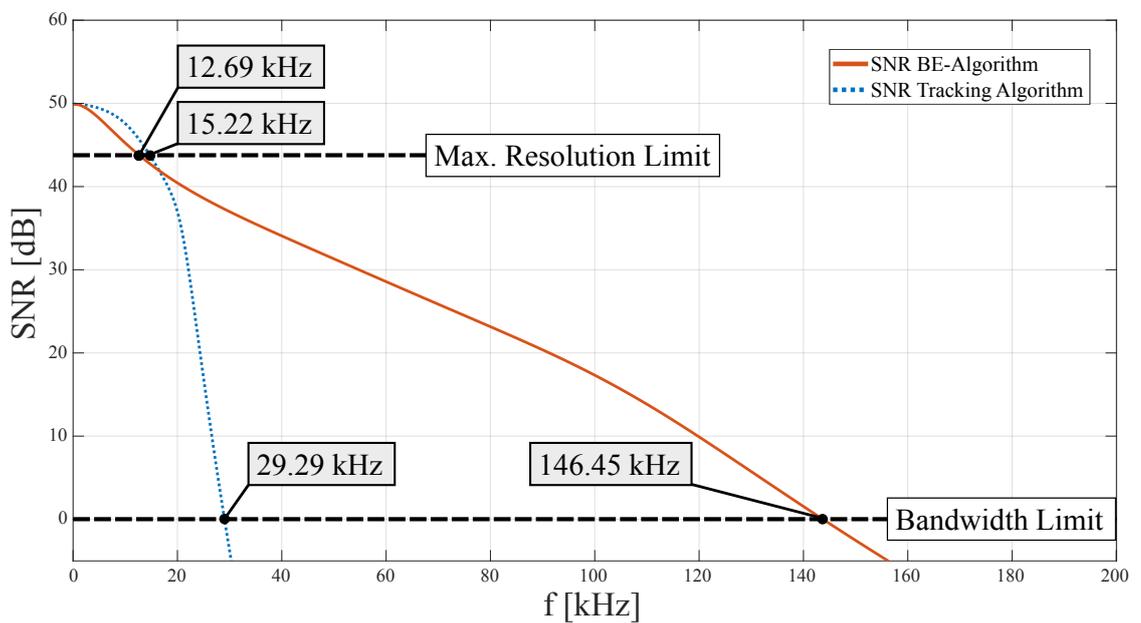


Figure 3.6: Comparison of the signal-to-noise ratio course for the Conventional Tracking scheme algorithm based ADC and for the BEA tracking scheme based ADC. The reference step generation rate (i.e. the digital clock  $f_{\text{clk}}$ ) is 5 times higher for the proposed approach. Therefore, the bandwidth limit is 5 times higher compared to the conventional approach.

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### 3.1.2 Algorithmic Enhancement of the Effective Resolution

Based on the proposed algorithmic approach it can be demonstrated, that the bandwidth limitation can be extended by the application of a clock frequency which is faster than the system feedback delay allows. Furthermore, it could be derived, that the effective resolution within the extended bandwidth also increases. Figure 3.4(b) has illustrated the exemplary assumption and based on the SNR course in figure 3.6 the concept is validated. The effective resolution, which is derived from the signal-to-noise ratio, is spread over the bandwidth. This fact enables the applicability of the proposed tracking scheme for a large part of the extended bandwidth. However, the evaluations regarding the bandwidth limitation for the maximum resolution show a rapid drop of the signal-to-noise ratio, which is even below the limitation of the conventional Tracking ADC. Investigations revealed, that this effect depends on the proposed sampling algorithm. Thereby the maximum possible conversion rate ( $f_{\text{conv}}$ ) is reduced due to the sequential counting process, where the return to the opposite orientation to the analog input requires the same time as for the detection. This effect halves the possible conversion rate which is at least the reciprocal of the sampling time ( $f_{\text{samp}}$ ) defined by the dead time. In consideration of the SNR equation (2.57), a transfer towards maximum possible conversion rate, thus that  $f_{\text{conv}} = f_{\text{samp}}$ , promises a higher effective resolution, since the sampling noise portion is reduced by an increasing sampling frequency. Based on this fact, it is rational to increase the sampling rate and thus the conversion rate to the system limit.

In order to improve the conversion rate, the algorithm needs to be redesigned. Based on the evaluation of the algorithmic behavior the return to the opposite orientation of the analog signal by the reference signal is necessary to initialize a new conversion step. However, the sequential counting process generates intermediate values, that are not contributing to the conversion result. These intermediate values determine the deviation of the reference signal from the analog signal related to the triangular staircase function. However, by further processing of the converted results in terms of generating the mean value of the staircase extrema, the intermediate values are not of interest. Therefore, the time to return to the opposite orientation is wasted. In conclusion, instead of sequential step generation, it would be advantageous to return to the opposite direction immediately after the level crossing detection by the comparator. Thus, the next conversion cycle can be initialized.

The detection of the level crossing is detected by the comparator. Thereby, the processing is restricted to the sampling time  $f_{\text{samp}}$ . In order to return the reference signal back to the opposite direction of the input signal the intermediate counting steps can be skipped. In

this terms, the algorithm has the task to initiate a jump of the reference, which is triggered by the comparator switching moment. The knowledge of the sensible number of steps that must be skipped is of great importance in order to achieve the optimum sampling time. Since previous steps are known from the conversion, it seems sensible to use these steps as a jump reference at first glance. Though, the continuous time property of the ADC ensures, that the deviation between the analog input and the jump reference is not negligible. The time needed for tracking the input signal by the reference introduces further errors defined as additional noise. Related to this fact, the prediction of the jump reference should be closer to the analog input. Based on the generation of the arithmetic mean values between consecutive conversion samples for the general conversion result, also the jump reference can be determined. Hereby, the mean value is determined by the extrema of the staircase function which are defined by the comparator switching moments. In order to jump to the mean value, an initialization point, which is closer to the analog input, is applied to the reference signal. Due to the binary representation the mean value can either be the exact value, or the deviation by one least significant bit. The evolving tracking scheme is illustrated in figure 3.7(b). The triangular sampling scheme is transferred to a sampling scheme with jumps after each respective comparator transition in order to optimize the conversion time ( $T_{conv}$ ). The reference signal is not forced to return to a level of the opposite orientation to the analog input by sequential counting, but jumps immediately to the opposite orientation.

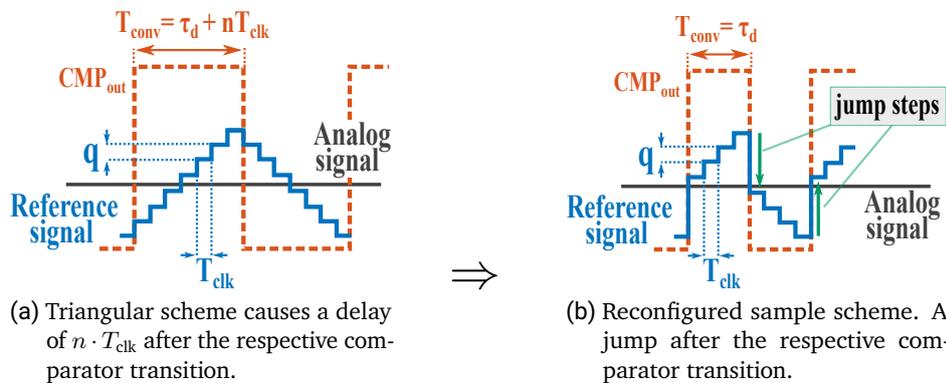


Figure 3.7: Transfer of the triangular sampling scheme (a) to a sampling scheme with jumps after each respective comparator transition (b) in order to optimize the conversion time ( $T_{conv}$ ). The reference signal is not forced to return to a level of the opposite orientation to the analog input by sequential counting, but jumps immediately to the opposite orientation.

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The reconfiguration of the proposed tracking algorithm reduces the previous conversion time by half, which leads to fact, that the conversion rate corresponds to maximum possible sampling ability prescribed by the feedback delay. However, the absolute bandwidth ( $f_{\max_{\text{bw}}}$ ) remains unaffected, since it is defined by the clock rate ( $f_{\text{clk}}$ ). But the influence of the conversion rate and the relating the feedback delay to the effective resolution becomes obvious. This can be clarified by the determination of the signal-to-noise ratio course, which is calculated by equation 2.57 for the SNR of non-uniformly sampled signals. The parametrization is again assumed to a resolution of  $N = 8$  bit and a clock rate of  $f_{\text{clk}} = 50$  MHz. The conversion rate corresponds to the sampling rate and is defined for  $f_{\text{conv}} = f_{\text{samp}_{\text{min}}} = 10$  MHz. Figure 3.8 compares the results of the triangular tracking scheme with the proposed tracking scheme with jumps. As predicted, the absolute bandwidth remains unaffected by the reconfiguration with jump with  $f_{\max_{\text{bw}}} = 146.45$  kHz. But the influence of a faster conversion rate is apparent. The frequency related to the 8-bit resolution limit is doubled with  $f_{\max_{\text{res}}} = 25.38$  kHz, which can be also determined by equation 3.3. The effective resolutions is increased by approximately 1-bit over a wide frequency range due to doubling the conversion rate. This effect can be explained by the SNR equation which predicts the dependency between the sample resolution ( $N$ ) and the conversion rate ( $f_{\text{conv}}$ ) as a ratio of  $2^N / f_{\text{conv}}$ . In general it can be summarized, that the higher the conversion rate and thus the number of successful samples, the higher the effective resolution.

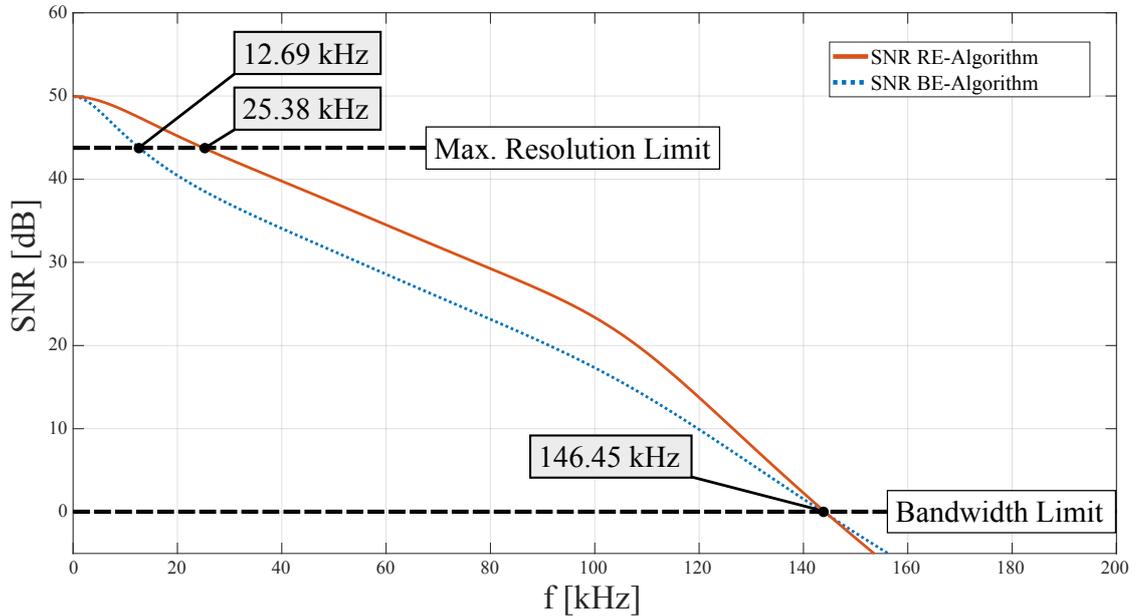


Figure 3.8: Comparison of the SNR course for the Bandwidth-Extended-Algorithm tracking scheme based ADC and for the Resolution-Enhancement-Algorithm (REA) tracking scheme based ADC. The jumps enable an immediate conversion related to the minimum feedback delay of the ADC. This improves the effective resolution.

### Evaluation and Comparison to Uniformly Sampled ADCs

The application of the proposed tracking scheme has demonstrated an extension for the absolute bandwidth compared to the conventional Tracking ADC approach. At the same time it reveals an enhancement of the effective resolution related to the bandwidth. Furthermore, the dependency between the effective resolution and the number of conversion steps could be derived. The application of jumps has improved the algorithm, thus that the conversion rate is related to the system restrictions based on feedback delay. As a result, the effective resolution could be further improved. The comparison to the conventional tracking demonstrated the advantages of the proposed tracking scheme. Both algorithms consider a non-uniform sampling behavior. Certainly, in order to evaluate a wide range of ADC schemes, the proposed algorithm should be compared to uniformly sampled ADC schemes. One of the most famous of them is the Successive Approximation Register (SAR) ADC [3].

The SAR algorithm is a classical representation of uniformly sampled ADC scheme. It approximates the analog input by the comparison with the reference, which is constituted as a binary search algorithm. Therefore, each current reference step always represents half of the predecessor step. The comparator determines the state of the current step in orientation to the analog signal. Once, each comparison step is approximated the conversion cycle is finished and a new conversion cycle can be initiated. Due to the demand that the SAR logic needs to compare each approximation step, the conversion rate is a multiple of the minimum sampling rate ( $f_{\text{samp}_{\text{min}}}$ ). The multiple is based on the resolution of the ADC and one acquisition cycle in addition, with  $f_{\text{conv}} = f_{\text{samp}_{\text{min}}}/N + 1$ . The acquisition cycle is necessary for the sample and hold device, since the SAR ADC can not be applied as a continuous time ADC. This is related to the fact, that the conversion is restricted due to the demand of a variety of comparisons until the analog signal is converted.

In order to compare the non-uniform sampling behavior of the proposed tracking algorithm with the uniform sampling behavior of the SAR algorithm, the system restrictions must be complied. Therefore, the conversion rate of the SAR is related to the resolution and the minimum possible sampling rate of  $f_{\text{samp}_{\text{min}}} = 10$  MHz. Again, the resolution of both systems is for  $N = 8$  bit. Thus, the conversion rate of the SAR ADC is defined by  $f_{\text{conv}} = f_{\text{samp}_{\text{min}}}/(N + 1) = 1.1$  MHz. In order to compare each reference step the step generation rate needs to be synchronous to the sampling rate, thus that  $f_{\text{clk}} = f_{\text{samp}_{\text{min}}} = 10$  MHz. As derived, the conversion rate of the tracking scheme algorithm is reduced to the minimum sampling rate, thus that  $f_{\text{conv}} = f_{\text{samp}_{\text{min}}} = 10$  MHz. The advantage compared to the uniform algorithms is depicted by the additional degree of freedom for the step generation rate of the is assumed for  $f_{\text{clk}} = 50$  MHz for the proposed ADC. Figure 3.9 illustrates the comparison between the extended tracking algorithm and the SAR algorithm. In addition, the conventional tracking scheme with  $f_{\text{clk}} = f_{\text{samp}_{\text{min}}}$  is shown in order to demonstrate the abilities of the proposed tracking scheme. The signal-to-noise ratio course over the desired bandwidth of each implementation is decisive about the relationship between bandwidth and effective resolution. In order to evaluate the SNR behavior, the non-uniformly sampled schemes are calculated by equation 2.57 and the uniformly sampled scheme of the SAR logic is calculated by equation 2.25.

Figure 3.9 compares the SAR algorithm with both tracking algorithms. The uniformly sampled SAR algorithm exhibits a wide bandwidth which is limited by the Nyquist theorem the half of the conversion rate. However, besides the wide bandwidth compared to the tracking approaches the SNR course reveals a rapid drop. In turn, the effective resolution can not be provided over the entire Nyquist frequency. This is an effect, which relates to the uniform sampling and can be estimated by the ratio between the input signal period and

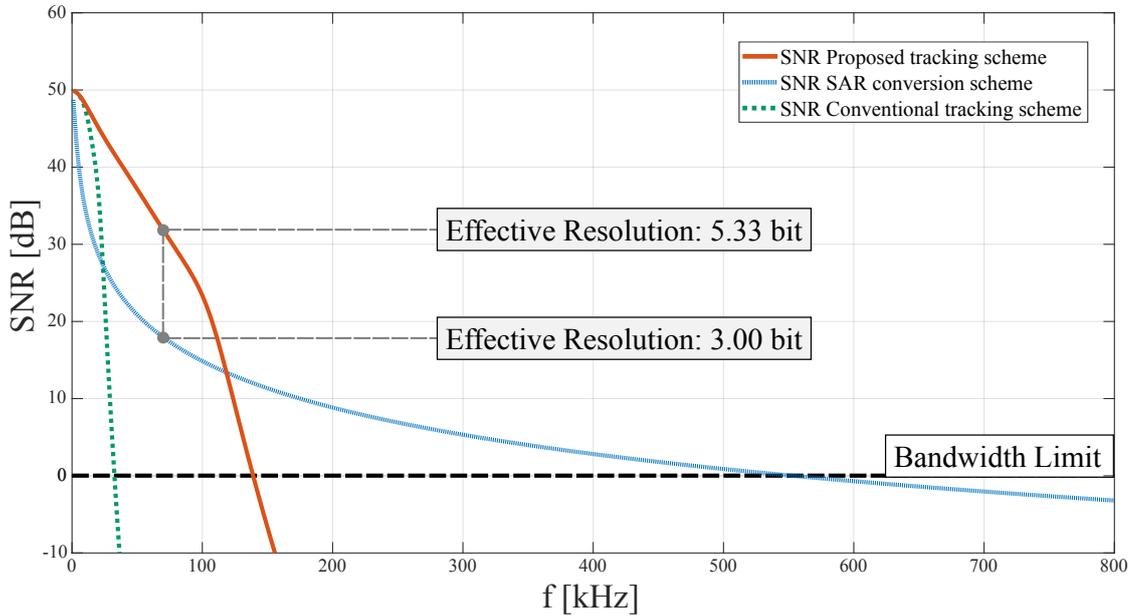


Figure 3.9: Comparison between the application of a uniform sampling scheme by the SAR algorithm and non-uniform sampling scheme by the proposed tracking algorithm (REA). The ability of a fast conversion rate enables significantly higher effective resolution for the proposed approach compared to the SAR logic. However, the SAR logic has a higher absolute bandwidth.

the conversion time ( $T_{\text{sig}}/T_{\text{conv}}$ ). Thus, the ratio defines the number of possible samples. As described the number of samples or successful conversions is decisive about the effective resolution. Therefore, it defines the provided information per time step (i.e. information density). The higher the information density, the more accurate a signal can be described. Referred to uniform sampling, each time step has an equidistant spacing, which implies that the information for representing a signal needs to be encoded by the quantized magnitude information. On the other hand, non-uniform sampling has the ability to encode the information of a signal by the quantized magnitude as well as by the quantized time. This factor can be demonstrated by the comparison between the uniform sampling of the SAR ADC and the non-uniform sampling of a tracking scheme. Hereby, the algorithms are characterized by the same system parameters. By the application of a tracking scheme, the delta between consecutive conversion steps enables a conversion within a single sampling step. The conversion, in turn, provides information about the passed time and

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the passed magnitude and is encoded by the difference between consecutive conversion steps. Already the conventional Tracking ADC exhibits an effective resolution, which is higher than the effective resolution of SAR ADC, since the SNR course drops slower related to the maximum of the SNR. However, the region for providing a higher resolution only covers a small area of the bandwidth. This is related to the bandwidth limiting property of the conventional Tracking ADC. The closer the input signal frequency to the respective bandwidth limitation, the rapid the SNR of the Tracking ADC drops. This leads to the fact, that the conventional Tracking ADC is impracticable for most of the applications.

In order to overcome this limitation, the proposed tracking scheme defines an algorithm, which extends the bandwidth limitation drastically. Compared to the SAR ADC the maximum bandwidth is still significantly lower, but the representable information density is significantly higher within the bandwidth of the proposed tracking scheme. Nevertheless, in consideration to equation 2.57 it can also be shown, that a further increase in the reference step generation rate (i.e. clock rate) implies an extension for the bandwidth. On the other hand, although the SAR ADC has a wide bandwidth, but is limited to the possible number of information. For a wide range within the bandwidth of the proposed tracking scheme a significantly higher information density results. The inferior information density of the SAR ADC demonstrates the strength of the novel ADC scheme. The comparison of the effective resolution for both designs can be applied to an example. It is assumed, that the SAR ADC provides an effective resolution of 3.00 bit bit in order to represent the analog signal. If one considers the same input signal frequency on the other hand, the proposed tracking approach has an effective resolution of 5.33 bit. Therefore, the analysis shows, that the novel approach exhibits an approximately 5 times higher accuracy than the SAR ADC within a wide frequency range. To demonstrate the advantage over the SAR ADC even more clearly, the bandwidth of the novel tracking scheme can be extended towards the SAR ADC bandwidth limitation by the application of a higher clock frequency and provides a higher effective resolution at the same time.

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### 3.1.3 Equation-based Analysis for Algorithmic Improvement

The analysis of the bandwidth limitation and the effective resolution of the general purpose ADC has revealed, that the marginal alteration of the basic tracking scheme results in significant improvements in order to convert a higher information density. So far, by the application of a higher clock frequency, the absolute bandwidth and the resolution could be improved compared to the conventional Tracking ADC. The comparison to the uniformly sampled SAR ADC it could be demonstrated, that the relative performance (i.e. parameters related to the applicability) is superior. So, the approaches open a perspective for a dynamic ADC arrangement, which can be designed for a wide area of applications. Still, these applications need to be defined. The effects of parametrization based on the degrees of freedom can be estimated by the proposed equation for non-uniformly sampled ADC. Hereby, the general equation (Eqn. 2.57) can be traced back to the uniform sampling method. Therefore, the set of equations defines a tool for the design of rational algorithms for the general purpose ADC.

In order to determine rational algorithms, the general equation for the SNR (Eqn. 2.57) provides information about the parametrization of the algorithm. In order to derive an improved algorithm, the equation is considered again and broken down related to the meaning of individual parameters. Based on the expression for the noise, introduced by sampling in equation 2.54, the relationship between resolution, conversion rate, and step generation rate is analyzed.

The proportionality condition applied for the derivation of the SNR equation assumes that a reference step is proportional to a quantization step. Thus, the temporal influence of the sampling noise could be transferred to quantization noise based on the "Bernstein"-relation. The integral limits for the power density derivation assumes a mean value free interval between  $-2^{N-2} T_{\text{ref}}$  and  $2^{N-2} T_{\text{ref}}$  (Eqn. 2.43). This assumption corresponds to half of the maximum amplitude of the input signal, whereby the amplitude can be expressed by the resolution parameter  $N$  and the least-significant bit magnitude ( $A = q 2^N$ ). Referred to this consideration, it was assumed that the resolution parameters are the same for both the magnitude resolution and the time resolution. But the fact, that their origins are based on different physical significations enables the separation of these parameters related to an magnitude resolution ( $N_{\text{amp}}$ ) and temporal resolution reference ( $N_{\text{ref}}$ ). Therefore, it makes sense to separate these parameters in the SNR equation as well. In the further course, relationships are established that define the conditions under which a separation can be meaningfully applied to the algorithm.

In order to examine the interactions of the individual parameters, the sampling noise expression in equation 2.54 is considered. The equation, in turn, provides information about the composition between the conversion time (assumed as:  $T_{\text{conv}} = T_{\text{samp}_{\text{min}}}$ ) and the reference step generation time (assumed as:  $T_{\text{clk}} = T_{\text{ref}}$ ). In order to clarify the effects of the parametrization of the individual resolution proportions, the sampling noise equation is decomposed in a portion of conversion noise ( $\mathcal{N}_{\text{conv}}$ ) and a portion of reference noise ( $\mathcal{N}_{\text{ref}}$ ). The decomposition is revealed by equation 3.4 and 3.5.

**Conversion noise:**

$$\mathcal{N}_{\text{conv}} = \frac{A^2}{24} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 = \frac{q^2}{3} 2^{2N-3} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{conv}}} \right)^2 \quad (3.4)$$

**Reference noise:**

$$\text{limit} = 4 (\text{N}_{\text{amp}} - 1) - 2 (f_{\text{clk}}/f_{\text{conv}} + 1)$$

$$\mathcal{N}_{\text{ref}} = \left[ 1 + 2^6 \cdot \sum_{k=4}^{\text{limit}} (-1)^k \frac{(\pi 2^{N-2} k \cdot f_{\text{sig}}/f_{\text{clk}})^k}{(k+1)!} \right] \quad (3.5)$$

First, the expression 3.4 for the conversion noise portion ( $\mathcal{N}_{\text{conv}}$ ) is considered. It describes the dependency between the input signal and the conversion rate ( $f_{\text{conv}}$ ). The input signal is characterized by the input frequency ( $f_{\text{sig}}$ ) and the signal amplitude (A). By the rearrangement for the amplitude expression with  $A = q 2^N$ , the resolution related dependency is revealed. Therefore, the conversion noise portion ( $\mathcal{N}_{\text{conv}}$ ) is constituted by the ratio between the number of resolution steps ( $2^N$ ) and the conversion rate ( $f_{\text{conv}}$ ). The ratio is referred to the input signal frequency ( $f_{\text{sig}}$ ). Related to uniform conversion intervals, this definition can be referred to the uniform sampling assumption in chapter 2. Therefore, this relationship defines the number of possible conversion steps within the input signal period. In conclusion a statement for the relationships of the conversion noise expression results:

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**Statement:**

The relationship between the magnitude resolution and the conversion rate within the input signal period defines the noise portion based on conversion.

Based on the relationship between the conversion rate and the amplitude magnitude the statement can be continued. Thus, the higher the conversion rate for a fixed resolution, the less conversion noise is introduced by the system. Since the conversion rate ( $f_{conv}$ ) is the composition between algorithmic switching moments and the total feedback delay ( $\tau_d$ ), the maximum conversion rate is available in the event that only the feedback delay effects, defines as minimum sampling time ( $T_{s\text{amp},\text{min}}$ ). In this case, the conversion noise is at the available minimum. The maximum of the frequency related effective resolution is obtainable as demonstrated in section 3.1.2 by the reduction of the conversion time. In addition, a further dependency is revealed. If the amplitude of the input signal is not constituted by the reference resolution (i.e. less than  $2^N$ ), the conversion noise portion increases. Related to an algorithmic implementation this is the case if reference steps are skipped. Generally, this implies if the full-scale amplitude can not be represented due to algorithmic properties. Therefore, the algorithmic related expression for the resolution is referred to the amplitude as  $N_{\text{amp}}$ . The amplitude resolution, in turn, is related to the total number of skipped steps  $M_{\text{skip}_a}$  and linked via a log 2-depiction. Equation 3.6 summarizes the assumptions for the algorithmic definition of the conversion noise.

**Conversion noise:**

The relationship between the magnitude resolution ( $N_{\text{amp}}$ ) and the conversion rate ( $f_{conv}$ ) within the input signal period ( $T_{\text{sig}}=f_{\text{sig}}^{-1}$ ) defines the noise portion based on conversion ( $\mathcal{N}_{conv}$ ).

$$\text{Amplitude resolution: } N_{\text{amp}} = \log_2 [2^N \pm M_{\text{skip}_a}]$$

$$\mathcal{N}_{conv} = \frac{q^2}{3} 2^{2N-3} \pi^2 \left( \frac{f_{\text{sig}}}{f_{\text{samp}}} \right)^2 \Leftrightarrow \boxed{\mathcal{N}_{conv} = \frac{q^2}{24} f_{\text{sig}}^2 \pi^2 \left( \frac{2^{N_{\text{amp}}}}{f_{\text{conv}}} \right)^2} \quad (3.6)$$

---

Next, the reference noise expression ( $\mathcal{N}_{ref}$ ) in equation 3.5 is considered. In general, it describes the dependency between the input signal period ( $T_{sig}$ ) and the reference step generation time defined by a multiple of the clock period ( $T_s = k T_{clk}$ ). As a result, the sum (derived from the Taylor series expansion) adds up by proportional noise. It is based on the respective number of temporal reference steps ( $k T_{clk}$ ) within the signal period. In conjunction with equation 3.4, the application of the "Bernstein Theorem" enables the transfer between the temporal noise to a corresponding quantization noise. The relation in equation 3.5 provides the proportionately noise component, which is introduced by the constitution of the reference signal. Therefore, the noise component is constituted by the ratio between the number of resolution steps ( $2^N$ ) and the scaled step generation rate ( $k f_{clk}$ ). Since the constitution of the reference signal is based on the temporal relationship between the input signal period and the scaled step generation time, the algorithmic related expression for the resolution is referred to as the temporal reference portion as  $N_{ref}$ . This relationship defines the number of possible scaled reference steps within the input signal period. In conclusion, also in this case a statement results for the relationships of the reference noise expression:

**Statement:**

The relationship between the reference resolution and a scaled step generation rate within the input signal period defines the individual noise components with respect to a step. The sum of the individual components defines the total portion of the reference noise.

Based on the ratio between  $N_{ref}$  and  $f_{clk}$  the constitution of the reference signal is characterized. Hereby, the ratio reveals that the relation between the resolution and the step generation rate can be considered as interaction. This assumption was already verified by the approach for the algorithmic bandwidth expansion in section 3.1.1, where the step generation rate was increased in order to extend the bandwidth. On the opposite site, the separate consideration of the step resolution ( $N_{ref}$ ) enables the characterization of the bandwidth as an additional degree of freedom. Applied to a practical design of an algorithm, the reference step height, described as a multiple of basic resolution steps, is decisive about the slope of the reference signal, which implies the input signal bandwidth. The step height, in turn, can be considered as jump, which is constituted as a scaling factor by the number of steps defined as  $M_{jump_t}$ . In fact, the decomposition of the reference noise power by the Taylor series expansion even enables the ability to decompose the jump step number related to the individual elements of the series expansion. This implies the application of jump steps for individual reference signal steps. Therefore, the step

resolution is characterized as a vectorial parameter which is related to the series element by  $\vec{N}_{ref}(k)$ . In addition, the jump scaling factor can also be related to the series element by  $\vec{M}_{jump_r}(k)$ .

Besides the definition of individual scaled time steps the Taylor series expansion is characterized by the number of elements, which describe a proportionally noise. In turn, the number of possible noise elements is characterized by the number of representable conversion steps. Already in the expression for the conversion noise (Eqn. 3.6) it was deduced that the number of possible conversions is described by the relationship between the input signal amplitude and the conversion time. In this contemplation, the magnitude resolution ( $N_{amp}$ ) has defined the upper limit due to the "Bernstein" transformation. In this terms, the upper limit is defined by the resolution parameter  $N_{amp}$ . Equation 3.6 summarizes the assumptions for the algorithmic definition of the reference noise.

### Reference noise:

The relationship between the temporal reference resolution ( $N_{ref}$ ) and a scaled step generation rate ( $k \cdot f_{clk}$ ) within the input signal period ( $T_{sig} = f_{sig}^{-1}$ ) defines the individual noise components with respect to a step. The sum of the individual components defines the total portion of the reference noise ( $\mathcal{N}_{ref}$ ).

$$\text{Temporal reference resolution: } \vec{N}_{ref}(k) = N \pm \log 2 \left[ \vec{M}_{jump_r}(k) \right]$$

$$limit = 4 (N_{amp} - 1) - 2 (f_{clk}/f_{conv} + 1)$$

$$\mathcal{N}_{ref} = \left[ 1 + 2^6 \cdot \sum_{k=4}^{limit} (-1)^k \frac{(\pi 2^{N-2} k \cdot f_{sig}/f_{clk})^k}{(k+1)!} \right]$$

$$\Leftrightarrow \mathcal{N}_{ref} = \left[ 1 + 2^6 \cdot \sum_{k=4}^{limit} (-1)^k \frac{\left( (\pi/4) \cdot f_{sig} \cdot \left( k 2^{\vec{N}_{ref}(k)} / f_{clk} \right) \right)^k}{(k+1)!} \right] \quad (3.7)$$

---

Based on the renewed consideration of the signal-to-noise expression for non-uniformly sampled signals (Eqn. 2.57), the proportionally sampling noise components were broken down. Thus, the behavior of each individual noise can be considered separately by the conversion noise ( $\mathcal{N}_{conv}$ ) and the reference noise ( $\mathcal{N}_{ref}$ ). Both noise portions are derived by the "Bernstein Theorem", which transfers the sampling noise to quantization noise. The conversion noise is based on the relationship between the amplitude resolution ( $N_{amp}$ ) and the conversion rate ( $f_{conv}$ ) within the input signal period ( $T_{sig} = f_{sig}^{-1}$ ). On the other hand, the reference noise is constituted by the relationship between the temporal reference resolution ( $N_{ref}$ ) and a scaled step generation rate ( $k f_{clk}$ ) within the input signal period ( $T_{sig} = f_{sig}^{-1}$ ) and defines the individual noise components with respect to a step. The sum of the individual components defines the total portion of the reference noise ( $\mathcal{N}_{ref}$ ). Thus, the consideration of the individual noise sources, enables the decomposition of the general parameter for the resolution. This has the background, that the amplitude resolution ( $N_{amp}$ ) is related to the physical parameter of the input signal amplitude ( $A$ ), whereas the temporal reference resolution ( $N_{ref}$ ) is related to the physical parameter of the reference step generation. Thereby, the amplitude resolution can be considered as a global parameter, since it is related to the input signal. It influences not only the sampling noise, but also the quantization noise. Therefore, the resolution is defined as global amplitude resolution. The temporal resolution, in turn, is exclusively related to the generation of reference steps. Therefore, it is denoted by the local temporal resolution in order to establish a reference point for differentiation. Furthermore, the renewed consideration of the resolution can be directly represented as individual steps by the log 2-function, where  $M_{skip_a} = M_{jump_r} = 1$  denotes the initial step. Related to derived algorithms this approach enables the ability to describe the algorithm by the number of steps instead by resolution. This offers the application of algorithmic jumps during the ADC runtime, which are not necessarily scaled binary. Since it was demonstrated in section 3.1.2, that the algorithmic introduction of rational jumps manipulates the behavior of the sampling scheme, the decomposition of the resolution parameter describes an additional degree of freedom by  $N_{ref}$ . Furthermore, the application of jump steps leads to a reduction in the maximum number of resolvable steps, since possible conversion steps are skipped. The number of skipped steps needs to be considered globally and depends on the applied algorithm. As a result, the amplitude resolution is related to the temporal resolution and restricted to the general ADC resolution, but despite these dependencies it is also a certain degree of freedom. In order to predict the behavior of the signal-to-noise ratio in more detail, the new approaches of the introduced resolutions are taken into account for the general SNR equation 2.57. The jump step number definitions are included and illustrate the resulting variety of possible algorithmic implementations. Equation 3.8 summarizes the approaches as an extended version of the general SNR expression.

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**Extended General SNR for Non-uniform Sampling:**

(3.8)

$$\text{Global amplitude resolution: } N_{\text{amp}} = \log_2 [2^N \pm M_{\text{skip}_a}]$$

$$\text{Local temporal resolution: } \vec{N}_{\text{ref}}(k) = N \pm \log_2 [\vec{M}_{\text{jump}_r}(k)]$$

$$\text{limit} = 4 (N_{\text{amp}} - 1) - 2 (f_{\text{clk}}/f_{\text{conv}} + 1)$$

$$SNR = 10 \log \left[ \left( \frac{2}{3 \cdot 2^{2N_{\text{amp}}}} + \Gamma_{\text{crest}}^2 \cdot \left( \frac{\pi f_{\text{sig}}}{f_{\text{conv}}} \right)^2 \left[ \frac{1}{3} + 2^6 \cdot \sum_{k=4}^{\text{limit}} (-1)^k \frac{(k \cdot (\pi/4) \cdot 2^{\vec{N}_{\text{ref}}(k)} \cdot (f_{\text{sig}}/f_{\text{clk}}))^k}{(k+1)!} \right] \right)^{-1} \right]$$

**Degrees of freedom:**

- Step generation rate ( $f_{\text{clk}}$ )
- Conversion rate ( $f_{\text{conv}}$ )
- Amplitude resolution ( $N_{\text{amp}}$ )
- Temporal resolution ( $\vec{N}_{\text{time}}(k)$ )

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## Algorithmic Approaches Derived from the Extended SNR Expression

The analysis of the general SNR equation (Eqn. 2.57) has revealed, that the resolution parameter can be decomposed to a portion of amplitude resolution ( $N_{\text{amp}}$ ) and temporal resolution ( $N_{\text{time}}$ ). The decomposition of these parameters reveals further degrees of freedom. These are practical in order to describe sampling algorithms for the general purpose ADC. Until now, sampling schemes for ADCs are principally considered as a static sampling behavior, where the sampling ability is predefined. Based on the investigation of two theoretical sampling approaches a possibility for dynamic sampling algorithms shall be illustrated related to the tracking scheme approach.

Based on the degree of freedom for the temporal resolution ( $N_{\text{ref}}$ ) the property of a reference step width adjustment shall be explained. Related to the absolute bandwidth limitation defined by equation 2.8 turns out, that it is restricted by the number of resolution steps ( $N$ ). However, this implies that the step size is the decisive parameter. If the resolution is decreased, the absolute size of a reference step is increased and therefore, the bandwidth is higher. This fact is related to the ability to track the input signal slope. Thus, an adjustment of the temporal resolution parameter ( $N_{\text{ref}}$ ) seems reasonable. From the dynamical point of view of the general purpose ADC this implies that the DAC still has the ability to provide a full scale resolution (e.g. 8 bit), but the algorithmic provision of the reference step size is decreased (e.g. 7 bit). Therefore, the tracking algorithm increases the step size with every step generation period by  $T_{\text{clk}}$  (e.g. count by 2 instead of 1). The resulting sampling scheme for the tracking algorithm including jumps is illustrated in figure 3.10. It transfers the already proposed tracking scheme including jumps from a 1 reference step generation scheme to a 2 reference step generation scheme.

Referred to equation 2.11, the application of a higher step size (e.g. by 2) extends the absolute bandwidth limitation in relation to the scaling of the step size (e.g.  $2 \rightarrow$  twice the basic bandwidth). Thus, the temporal resolution parameter needs to be decreased related to the step scaling parameter to  $\tilde{N}_{\text{ref}}(k) = N - \log_2[\tilde{M}_{\text{jump}}(k)]$ . Thereby it is assumed, that each step within the series expansion is adjusted by the same magnitude, thus that the vectorial description is neglected. Besides the improved bandwidth related to a higher step size, it needs to be considered, that the ability to resolute the full-scale resolution of the DAC is not available. This is the fact due to skipping of intermediate steps. As derived for the extended SNR equation (Eqn. 3.8), the degree of freedom that describes this behavior is defined by the amplitude resolution ( $N_{\text{amp}}$ ), whereby the total number of skipped steps can be related by  $M_{\text{skip}_a}$ . Even increasing the step size only to twice the basic size means that only half of all possible steps can be resolved.

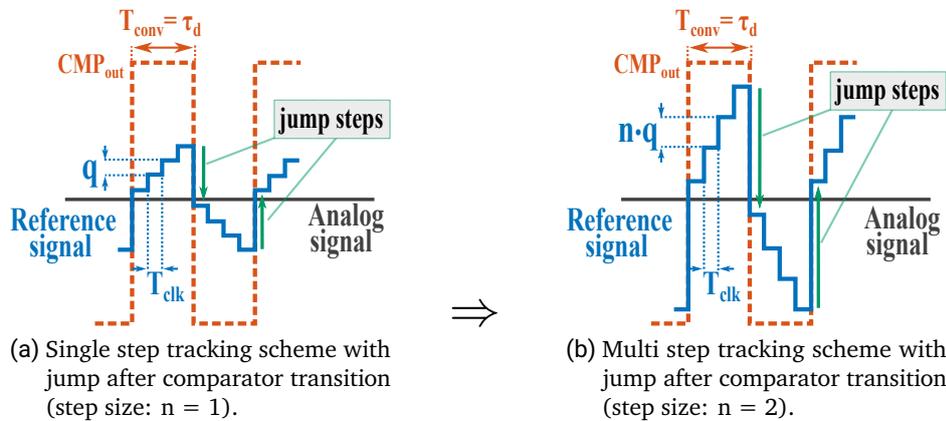
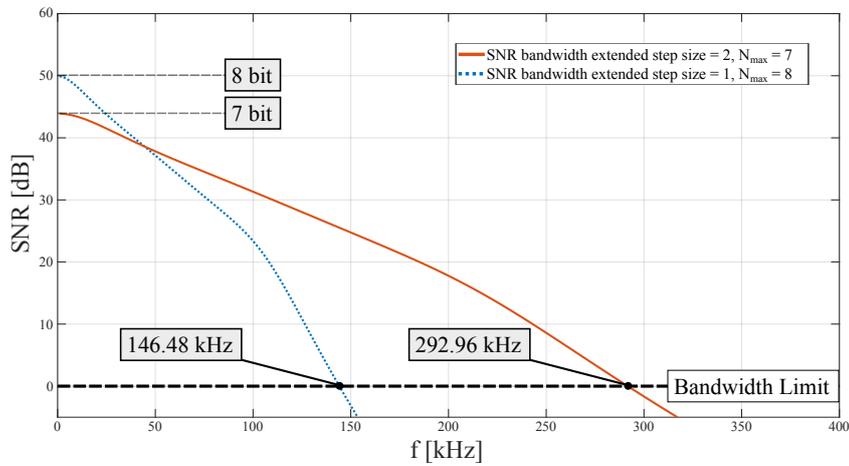


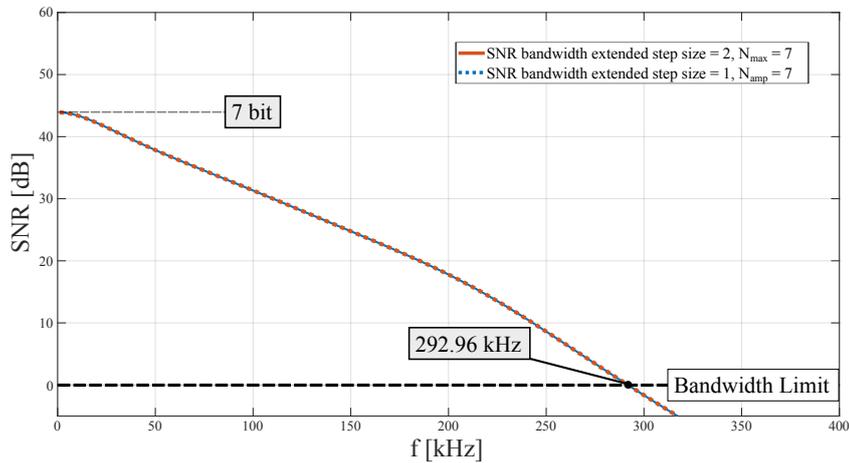
Figure 3.10: Transfer of the single step tracking scheme with jumps (a) to the multi step tracking scheme with jumps (b) in order to extend the bandwidth. The jump steps are applied after the comparator transition. The step width of the multi step approach equals 2 times the step width of the single step approach.

Figure 3.11(a) illustrates the resulting signal-to-noise ratio course and is compared to the initial tracking ADC approach. Both algorithms apply the jump to the mean value of consecutive conversion steps. The assumed parameters are characterized by a conversion rate of  $f_{conv} = 10$  MHz, the step generation rate of  $f_{clk} = 50$  MHz and a physical resolution (DAC) of 8 bit. The step size of the newly proposed scheme is adjusted by  $M_{jump_r} = 2$  (the already derived tracking algorithm has still a step size of 1). Due to the application of a higher step size the global resolution (characterized by  $N_{amp}$ ) is decreased by the number of skipped steps, thus that  $M_{skip_a} = 128$ . For the global resolution this implies a reduction of 1 bit compared to the single step approach, where no steps are skipped.

In comparison of the single step and the multi step scheme (step size = 2), the bandwidth can be extended by a factor of 2 due to increasing the step size. However, by a higher step size, the global resolution (characterized by  $N_{amp}$ ) is reduced. Obviously, the application of a higher step size implies, that the SNR behavior is transferred to a lower resolution representation. Referred to the investigation in 3.11(a), the SNR course is transferred from a resolution property of 8 bit to the property of 7 bit. In this terms the maximum available effective resolution is also transferred from 8 bit to 7 bit, but the absolute bandwidth is doubled at the same time.



(a) Comparison between single step approach and multi step approach (step size = 2) illustrating a bandwidth extension by a factor of 2.



(b) Comparison between single step approach (global resolution  $N = 7$  bit) and multi step approach (step size = 2) illustrating the same SNR course.

Figure 3.11: Comparison of the SNR course for bandwidth extended approaches including jumps. The transfer of the single step approach (step size = 1) to the multi step approach (step size = 2) illustrates a bandwidth extension by a factor of 2. Due to a higher step width the effective resolution is limited to half of the maximum resolution (i.e. 8 bit  $\rightarrow$  7 bit). The comparison to the single step approach for a global resolution of  $N = 7$  bit illustrates the same SNR course.

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Based on the described connection, it can be concluded, that the effective resolution to bandwidth dependency can be adjusted dynamically and independently from the hardware constitution except for the upper resolution limit (e.g. DAC resolution). Figure 3.11(b) illustrates the expected result. The 8 bit approach is transferred to a 7 bit approach under the restriction of the respective advantages and disadvantages.

This mind experiment shall demonstrate the ability of a dynamical algorithm. The advantage of digitally adjustments of the sampling algorithm by the step size enables the property to scale the effective bandwidth/resolution ratio linearly by the number of basic steps. Furthermore, it provides a possibility to dynamically react to the sequence of the algorithm. Thus, it would be imaginable to track the slope of the input signal by the comparison of consecutive conversion steps. An increasing slope determines a higher input frequency, thus that the step size needs to be adjusted. Thereby, in consideration to the bandwidth/resolution ratio, so that the desired effective resolution is not subject to change.

So far it could be demonstrated, that a dynamic behavior of the tracking scheme can be applied to the general purpose ADC without adjusting the hardware abilities. This property enables to dynamically decide for the character of the bandwidth and of the resolution of the ADC by algorithmic step size adjustment. But a drawback of this approach considers, that an increasing step size implies the decrease of the absolute effective resolution. Of course, the dynamic adjustment could compensate this drawback, since the maximum effective resolution is always related to the frequency dependent maximum resolution limitation as defined in equation 2.10. But even under the assumption of a dynamical bandwidth adjustment based on a slope detection, the physical limitation of the resolution (specified by the DAC) can not be resolved in combination with an extension of the bandwidth. This is related to the fact, that the relation between resolution and bandwidth is relative. Thus, a modification of the step size always implies a proportional variation of the maximum resolvable amplitude. It is indicated by the amplitude resolution ( $N_{amp}$ ), which is conjuncted with the reference resolution ( $N_{ref}$ ).

In order to overcome the restriction by  $N_{amp}$  the separate consideration as degrees of freedom for  $N_{amp}$ , and  $N_{ref}$  was derived. The derivation has revealed, that the conjunction between these parameters is not absolute, but predefined by the sampling algorithm. That suggests, that the sampling algorithm can be modified in order to provide the maximum resolution on the one hand, and also provide the bandwidth extension on the other hand. Referred to equation 2.11, the absolute bandwidth limitation is defined by the relationship between the reference step resolution ( $N_{ref}$ ) and the reference step generation rate ( $f_{clk}$ ). The bandwidth for the maximum resolution (Eqn. 2.10), in turn, is constituted by the relationship between the amplitude resolution ( $N_{amp}$ ) and the conversion rate ( $f_{conv}$ ).

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Since, the previous sampling scheme modifications already considered the influence of the conversion rate and the influence of the step generation rate, a further algorithmic modification should be based on the consideration of the resolution parameter  $N_{\text{amp}}$  and  $N_{\text{ref}}$ . Therefore, in order to increase the absolute bandwidth, the step width was increased, which enabled the tracking of a higher slope. The ability to track a higher slope depends on the absolute reference signal magnitude (represented as reference slope) within a conversion cycle ( $T_{\text{conv}}$ ). So far, the absolute magnitude was based on the number of scaled reference steps within a conversion cycle. Since the individual reference steps are scaled by increasing, the accuracy by detecting the intersection of the reference signal and the analog input signal is reduced. This effect is expressed by the number of skipped steps ( $M_{\text{skip}_a}$ ). By step size scaling the relative skipping is related to each individual step. Hereby, the number of skipped steps increases with the total number of reference steps. Therefore, the maximum resolution can not be resolved.

The extension of the absolute bandwidth is achieved by the modification of the relationship between reference resolution ( $N_{\text{ref}}$ ) and step generation rate ( $f_{\text{clk}}$ ). In order to provide a corresponding bandwidth extension, the reference signal magnitude within a conversion step needs to establish the same magnitude for a modified version of the sampling scheme. Based on the fact, that the step size of the reference resolution ( $N_{\text{ref}}$ ) was the determining parameter for the effective resolution limitation, the step size needs to be scaled down to the basic step again. But the condition for the bandwidth extension, which is related to the reference magnitude, must still be met. Since the detection of a level crossing by the comparator is restricted to the feedback delay ( $\tau_d \rightarrow f_{\text{samp,min}}$ ), the system experiences a dead time between the possible switching moments of the comparator. In general, this restriction leads to a low-pass behavior of the ADC. Thus, the reference signal can behave in any constitution without being detected during the comparator switching moments. Referred to the requirement of providing the same reference signal magnitude and the condition, that the reference step resolution is constituted by the physical resolution of the DAC (e.g. 8 bit), the dead time allows the algorithm to apply jumps to the reference signal. Sensibly from the algorithmic point of view, the jump should be applied at the moment of the comparator detection. Indeed, the moment is already occupied by the jump return to a level of the opposite orientation to the analog input. Therefore, the jump is extended by additional steps, so that the reference signal jumps to the opposite direction with a number of steps in addition. The evolving tracking scheme is illustrated in figure 3.12(b). It is transferred from the multi-step tracking scheme regarding the magnitude, but conditioned by the basic step resolution. The transfer is clarified in figure 3.12.

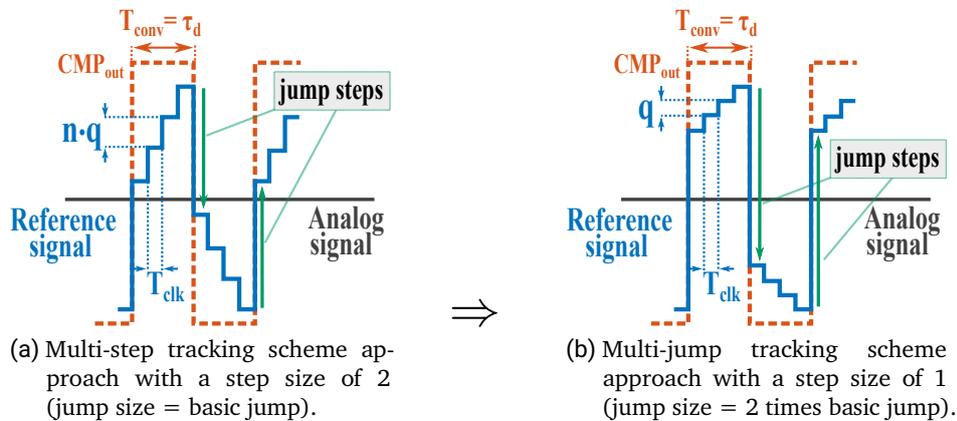


Figure 3.12: Transfer of the multi step tracking scheme (a) to the multi jump tracking scheme (b) in order to extend the absolute effective resolution. The jump steps are applied after the comparator transition. The number of jump steps for the multi jump approach equals 2 times the jump size of the multi step approach. Thus, the absolute magnitude within a conversion step equals.

The transfer in figure 3.12 illustrates, that the requirement of the reference signal magnitude is still be met, but the resolution of the individual reference steps are constituted by the maximum resolution (e.g. 8 bit). The sequential counting process related to the maximum resolution is initialized after the application of the jump step. Since the reference signal continues to propagate relative to the input signal, the temporal switching moments of the comparator are still based on this relation. The propagation of the reference signal in relation to the comparator transition takes place in a similar way to the behavior shown in figure 3.5. However, the detection of the respective reference step arises related to the maximum resolution. Indeed, an offset is introduced to the conversion result due to the application of jumps. But by the formation of the mean value between consecutive conversion steps, the general reference point is established at the level of the analog input signal. Thus, the resulting offset by the jump is eliminated. Furthermore, due to the establishment of the general reference point towards the input signal level, it can be concluded, that the maximum resolution can be resolved within the respective conversion step. This implies, that in general the global resolution is not restricted to the size of the jump within the conversion step. However, outside of the conversion step the general limitations needs to be considered. These limitations are related to the maximum

and minimum of the input signal. Based on the application of jumps, the reference signal needs to be located relatively orientated below or above to the input signal. This implies, that twice the number of the jump magnitude needs to be subtracted from the theoretical maximum of the input signal. Again, this demand can be considered by the definition of  $N_{\text{amp}}$ . Compared to the previous approach based on the extended step size, the number of skipped steps is twice the number of a single jump instead of a multiple of the basic step size by scaling. Exemplary, this means for a jump of 2 additional steps  $M_{\text{skip}_a} = 4$  instead of  $M_{\text{skip}_a} = 128$ . In conclusion, the number of skipped steps can be reduced drastically, which enables the algorithmic application of an extended bandwidth and the quasi maximum resolution at the same time. Figure 3.13 compares the signal-to-noise ratio course for both bandwidth extended approaches including jumps for a reference step size of 1. The transfer of the single step approach (jump size = basic jump) to the multi jump approach (jump size = 2 times basic jump) illustrates a bandwidth extension by a factor of 2. The maximum resolution limit of 8 bit can be achieved due to the relative dependency of the reference step to the analog input signal. The assumed parameters are again characterized by a conversion rate of  $f_{\text{conv}} = 10$  MHz, the step generation rate of  $f_{\text{clk}} = 50$  MHz and a physical resolution (DAC) of 8 bit. The amplitude resolution is reduced by to  $M_{\text{skip}_a} = 4$  to  $N_{\text{amp}} = 7.97$  bit.

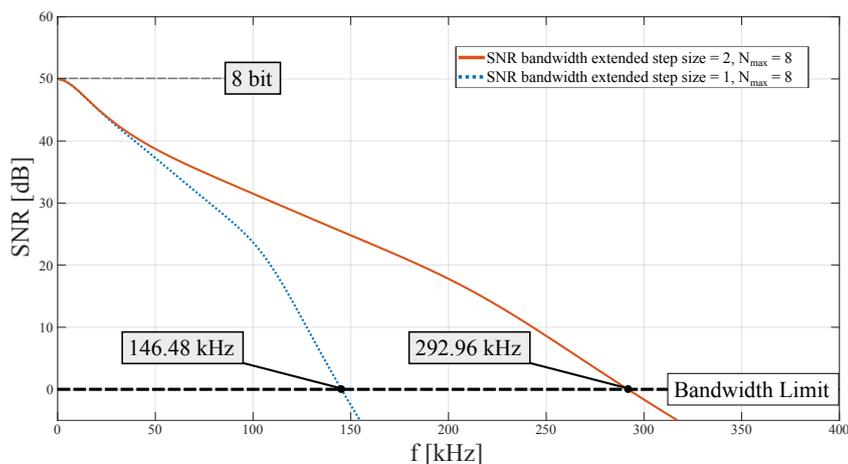


Figure 3.13: Bandwidth extension by a factor of 2 and a quasi maximum resolution of 8 bit due to the transfer of the single step approach (jump size = basic jump) to the multi jump approach (jump size = 2 times basic jump).

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## Evaluation of the Equation-based Analysis

The equation based analysis has decomposed the resolution parameter ( $N$ ) into the global amplitude resolution ( $N_{\text{amp}}$ ) and the local reference resolution ( $N_{\text{ref}}$ ). The fact, that their origins are based on different physical significations enables the separation of these parameters. The amplitude resolution describes the resolvable amplitude based on the algorithmic sampling scheme as global parameter. It considers the skipping of possible resolution steps by jumps or scaled reference steps. These steps needs to be considered by their respective number of occurrence within the entire input signal amplitude by  $M_{\text{skip}_a}$ . Thereby, the sampling behavior of the algorithmic implementation is decisive about the number of steps. The temporal reference resolution ( $N_{\text{ref}}$ ), in turn, defines the characterization of the bandwidth by the reference step size. In this connection the absolute bandwidth property is constituted by the relationship between the reference step resolution ( $N_{\text{ref}}$ ) and the reference generation rate ( $f_{\text{clk}}$ ). In this conjunction, the step resolution is related to the scaling factor based on the ratio between the input signal period and the step generation time. In this terms, it is defined as the temporal reference resolution.

In order to examine the interactions of the individual noise sources, also the general sampling noise expression (Eqn. 2.54) was decomposed to a portion of conversion noise 3.6 and a portion of reference noise 3.7. The noise portion which is based on conversion ( $\mathcal{N}_{\text{conv}}$ ) is defined by the relationship between the amplitude resolution ( $N_{\text{amp}}$ ) and the conversion rate ( $f_{\text{conv}}$ ) within the input signal period ( $T_{\text{sig}} = f_{\text{sig}}^{-1}$ ). However, the reference noise ( $\mathcal{N}_{\text{ref}}$ ) defines the sum of individual noise components related to the series expansion. Thereby, the relationship between the temporal reference resolution ( $N_{\text{ref}}$ ) and a scaled step generation rate ( $k f_{\text{clk}}$ ) within the input signal period ( $T_{\text{sig}} = f_{\text{sig}}^{-1}$ ) describes the individual noise components with respect to a step. A subdivision of the reference resolution into respective resolution parameter can be related to individual Taylor series elements. Therefore, the reference resolution is defined as a vectorial parameter ( $\vec{N}_{\text{ref}}$ ) where the step size is considered by ( $\vec{M}_{\text{ref}}$ ).

Based on these decomposed sampling noise expressions, the general expression for non-uniform sampling was evolved to an extended representation, where the additional degrees of freedom based on reference resolution ( $\vec{N}_{\text{ref}}$ ) and amplitude resolution ( $N_{\text{amp}}$ ) can be considered. In conjunction with the already defined degrees of freedom for the conversion rate ( $f_{\text{conv}}$ ) and the reference step generation rate ( $f_{\text{clk}}$ ), a set of parameter for the design of an algorithm is derived. Based on the new degrees of freedom for the resolution two possible algorithmic extensions were derived. The first algorithm considers the application

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of a higher reference step size. The derived sampling scheme is illustrated in figure 3.10(b). As a result, it was demonstrated, that the relationship between effective resolution and bandwidth can be adjusted. It is imaginable, that the algorithm of the general purpose ADC can be modified on demand. This enables a dynamic sampling algorithm, which can be adjusted due to the scaling of reference steps. A modification of the bandwidth or the effective resolution is possible. However, a drawback of the reference step scaling is depicted by the reduced amplitude resolution while skipping possible reference steps. In order to overcome this drawback, an extension of the algorithm is proposed, which is also related to the considerations of the step size adjustment. This approach introduces jumps at the moment of the comparator transition as illustrated in figure 3.12(b). These jumps can be referred to as the already introduced mean value jumps as an addition. Compared to the step scaling approach, the corresponding reference magnitude is provided in order to generate the same bandwidth extension. However, right after the jump, the sequential counting process related to the maximum resolution is initialized and is able to provide the entire physical resolution of the general purpose ADC (DAC). The made assumptions of this section were verified by equation analysis and demonstrated the ability of the extended SNR equation 3.8 to predict the algorithmic behavior or to derive algorithms from the expression.

In conclusion, the equation based analysis revealed 4 general degrees of freedom for the design of algorithms:

- Conversion rate ( $f_{\text{conv}}$ )
- Reference step generation rate ( $f_{\text{clk}}$ )
- Amplitude resolution ( $N_{\text{amp}}$ )
- Temporal reference resolution ( $\vec{N}_{\text{ref}}$ )

Furthermore, the possibility to derive algorithms from this base or to predict the behavior of a proposed sampling scheme was demonstrated due to theoretical application examples. In this way, the SNR expression reveals a variety of possible sampling algorithms.

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## 3.2 Summary on Algorithmic Tracking Schemes

Nowadays, a variety of individual ADC schemes concerning specific areas of application exist [11, 13, 20]. The characteristic of each ADC scheme decides the applicability to a specific area. In principle, these characteristics specify the physical properties of the ADC related to resolution and input signal frequency. Each variant related to the state-of-the-art offers advantages and disadvantages. Thereby, the topology of the ADC describes its characteristics and thus the applicability for a specific purpose. Many of these topologies behave statically, implying the fixed effective resolution and bandwidth parameter by predefinition. Based on the variety of application areas and the fact that many physical signal properties alternate, a dynamic ADC would be desirable. The desired ADC property relates to adjusting its essential resolution and bandwidth parameters concerning alternating application demands in these terms. This chapter proposes a novel ADC topology, which offers a dynamic property due to a general analog component constitution and an algorithmic interface. The proposed ADC is defined as general-purpose ADC (Fig. 3.2) and enables the ability to adjust the conjunction between effective resolution and input signal bandwidth by the reconfiguration of the sampling algorithm [85, 87].

The proposed ADC methodology describes a general-purpose algorithmic ADC. In these terms, the hardware effort is reduced to the main basic properties of digital-to-analog conversion and compare, classified by a DAC and a comparator. The primary characteristics of the ADC can be dynamically configured by a sampling algorithm, which is implemented on an ALU. This approach offers the ability to configure the algorithm related to the demand of the application area. Based on a variety of possible algorithmic implementations, this chapter concentrates on the design of algorithms. Therefore, possible sampling algorithms were derived from the theoretical approach in chapter 2, which provides a set of mathematical expressions for the description of the conjunction between the effective resolution and the bandwidth. Referred to the equation (Eqn. 2.57) for the signal-to-noise ratio of non-uniformly sampled signals, the conjunction between these parameters can be predicted. Since uniform sampling is a subset of the non-uniform sampling, this expression provides a general description of sampling methods. It is applicable as a design tool for possible algorithms. Within the equation, the resolution, the conversion rate, and the clock rate are considered degrees of freedom for the design. Derived from the stated relationship of these parameters, the dependency of the conversion rate is evaluated. A set of tracking schemes is proposed to provide a variety of dynamic conversion methods. Based on a detailed analysis of expression 2.57 additional degrees of freedom for the characterization of the reference signal revealed. Derived from the extended version of the general SNR equation 3.8, further possibilities for the design of algorithms are demon-

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strated. Thus, a design method for the general implementation of algorithms is provided for the application of the general-purpose ADC. An analysis of possible implementation methods, especially for non-uniform sampling schemes and a uniform sampling scheme, is performed to evaluate the assumed approaches.

Furthermore, the physical constitution of the proposed ADC was examined, and characteristics related to the feedback system delay were discovered. Thereby, these characteristics describe the physical limitations of the analog hardware configuration and revealed non-linearities regarding the system delay. Besides the influence of the digital-to-analog converter, it turned out that the comparator constitutes the main portion of a non-linear feedback delay. The proposal of new compensation methods, which provide the ability to compensate non-linearities in the timing of the feedback configuration, may overcome this situation.

Based on the sampling scheme of a conventional Tracking ADC, a novel tracking approach was proposed related to the separation of the reference step generation rate from the conversion rate of the ADC (Fig. 3.3). Referred to the general SNR expression, this approach was derived from the separate consideration of these parameters. Compared to the conventional Tracking ADC, the bandwidth limitation was algorithmically extended under the assumption of the same physical system constraints. Furthermore, the relationship between the conversion rate and the effective resolution could be revealed. Algorithmic modifications were applied that can extend the effective resolution towards the physical limitation (Fig. 3.7). Based on the proposed algorithmic implementation for bandwidth expansion and resolution optimization, the evaluation process of the design compares to a SAR algorithm to examine strengths and weaknesses related to uniform sampling schemes (Fig. 3.9). Due to the uniform constitution of SAR algorithms, the absolute bandwidth limits to half of the conversion rate concerning Nyquist. However, the signal-to-noise ratio course over the bandwidth shows a rapid drop after passing the maximum resolution bandwidth. Since the SNR is representative of the effective resolution, it also experiences a rapid drop. It is a general fact that refers to uniform sampling because the number of possible conversion steps is reduced linearly with the temporal decrease of the input signal period. Thereby, the reduction of conversion steps determines the increase of the noise portion.

Compared to the proposed tracking algorithm, the non-uniform sampling scheme reveals its strength. Under consideration of the SNR course, the novel scheme provides a higher effective resolution within a comparable bandwidth. However, the absolute bandwidth is lower compared to uniform sampling. Nevertheless, a modification of the algorithm is applicable. Related to the SNR course, the higher bandwidth limit of uni-

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form sampling cannot provide a high information density (i.e. effective resolution). A modification of the proposed sampling algorithm promised a definite improvement of the conjunction between bandwidth and resolution compared to the SAR algorithm. This approach was validated in the further course of this chapter by the extension of the mathematical description for the general SNR equation and the derived algorithmic modifications.

In order to apply further modifications to the algorithmic tracking scheme, the general SNR equation was considered in more detail. The influence of the individual noise sources was examined. The general sampling noise expression was decomposed to a portion of conversion noise and a portion of reference noise in these terms. On the one hand, the conversion noise source results from a conversion step based on the relationship between the resolution of the input amplitude and the conversion rate within the input signal period. On the other hand, the reference noise source results from the generation of a reference step. It is based on the relationship between the resolution of the reference step and the step generation rate within the input signal period. Since the conversion rate and the reference step generation rate already define a degree of freedom, the amplitude resolution and the reference resolution were determined to be additional degrees of freedom for the algorithmic design.

Derived from the extended version of the general SNR expression, which considers additional degrees of freedom, enabled algorithmic modifications of the proposed tracking scheme based on applying step scaling and jumps. The prediction by the extended SNR equation demonstrates the ability to expand the bandwidth limitation under the reduction of the maximum available resolution (Fig. 3.11) by an upscaling of the step size (Fig. 3.10). In general, the procedure corresponds to the down-scaling of the resolution. Therefore, this approach enables the algorithm's ability to alternate between the bandwidth limit and the effective resolution by the adjustment of the step size. Based on the application of step scaling, the alternation of the step size can be adjusted directly and connects to a binary number. Thus the adjustment for an intermediate magnitude of the resolution is enabled. It would also be imaginable that the algorithm tracks the slope of the input signal by the comparison of consecutive conversion steps and adjusts the relationship between bandwidth and resolution dynamically by step size adjustments related to the slope.

An approach for extending the bandwidth limitation and provide the physical resolution limit simultaneously was derived as further modifications from the extended SNR equation. Thereby, the analysis of the expression revealed that the bandwidth limitation is related to the individual reference signal level within a respective conversion step. The effective resolution, in turn, is related to the reference step size. Thus, the conversion

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step can be considered a global parameter, and the reference step can be considered a local parameter. A modification of the tracking algorithm refers to this contemplation by applying jump steps after a respective comparator transition. In this procedure, the sequential process for a change of the reference step initializes after the jump (Fig. 3.12). The size of the jump defines the bandwidth extension ability, and the step size defines the effective resolution ability of the algorithm. In this way, the renewed modified version of the tracking scheme algorithm expands the bandwidth and provides the maximum physical resolution (Fig. 3.13).

In conclusion, this chapter introduces the **Algorithmic Tracking Scheme ADC** and demonstrates the application of respective sampling algorithms. It offers a methodology to derive sampling algorithms from the set of equations described in chapter 2. In addition, these equations can be applied to predict the bandwidth and the resolution properties of a designed sampling algorithm. Thereby, four degrees of freedom for the characterization of ADCs were determined: The conversion rate, the clock rate, the amplitude resolution, and the reference step resolution. In these terms, general design methods are proposed to develop a variety of new sampling algorithms. The freedom to describe the ADC behavior algorithmically can benefit from a dynamic and flexible design. It opens up a field of novel technologies based on digital assistance.



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## 4 Analog Hardware System Characteristics

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The proposed ADC topology constitutes by the ALU providing the algorithmic implementation, and the hardware components based on the DAC and the comparator providing the task for reference signal conversion and comparison. Thereby, the DAC and the comparator are representative of the minimum required hardware configuration of a general-purpose ADC. Chapter 3 derives that the system feedback delay ( $\tau_d$ ) is decisive for the conversion rate ( $f_{\text{conv}}$ ). The maximum conversion rate, in turn, can be achieved by constraining the conversion rate to the sampling rate ( $f_{\text{samp}}$ ), defined as the reciprocal of the system delay ( $f_{\text{samp}} = \tau_d^{-1}$ ). Based on equation 2.57, which is representative for the SNR of non-uniform sampled signals, the dependency between the conversion rate and the effective resolution was illustrated in section 3.1.2. The detailed consideration of this dependency revealed that the faster the conversion rate, the higher is the effective resolution. Indeed, this fact is valid if one considers that the number of conversion samples within the input signal period ( $T_{\text{sig}}$ ) is decisive about the information density. Due to the direct relationship, this aspect can be transferred to the sampling rate ( $f_{\text{samp}}$ ), which corresponds to the system delay. Therefore, the shorter the system delay ( $\tau_d$ ), the higher the effective resolution.

Indeed, further characteristics of the analog constitution like non-linearity effects of the digital-to-analog conversion or mismatch of comparator parameter affect the effective resolution. In these terms, the digital-to-analog converter (DAC) demand is based on the accuracy of the least significant bit LSB of the ADC system. Thus, the Integral-Non-Linearity and the Differential-Non-Linearity needs to correspond to the system requirements of the ADC in order to provide a linear conversion. Besides the demand for the linearity of the DAC, the accuracy demand for the comparator is relaxed. Therefore, the main characteristics of the comparator, required for the proposed analog-to-digital conversion, are related to the gain (A) and the propagation delay ( $\tau_{\text{cmp}_d}$ ). An analysis regarding the conjunction between gain and propagation delay for the comparator derives interdependencies in this chapter. In general, a derivation that an altered relationship between the analog reference signal and the analog input signal results in alternating the propagation delay ( $\tau_{\text{cmp}_d}$ ). The related physical effect is defined as dispersion and describes the shift of the comparator propagation delay due to overdrive or underdrive the analog input

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signal by the reference signal. Since an analog-to-digital conversion by a comparator requires the overdrive/underdrive of the reference signal relative to the analog input signal, the dispersion effect is a decisive parameter for the definition of the comparator propagation delay [41]. Primarily, this effect determines the conversion rate abilities of the proposed tracking scheme since overdrive/underdrive is a crucial parameter in order to provide jumps and scaled reference steps as described in section 3.1.3. The accuracy of those algorithms depends on the configuration of the comparator. In this context, the comparator reference refers to the algorithmic clock rate ( $f_{ref}$ ) for a step generation. This aspect is contrary to common ADC approaches that require equalization of the comparator clock reference to the conversion rate ( $f_{conv}$ ) [3]. Since the comparator switching moments, which act as a digital reference for the proposed algorithm, determine the conversion rate, the dispersion effect significantly influences the ADC linearity. Thus, it is decisive about the effective resolution.

Based on the dispersion effect, the comparator introduces non-linearity to the proposed ADC system. Therefore, the ADC requires a compensation method [42] to equalize for the non-linearity effect and thus eliminate deviations caused by the comparator. This method can either be applied internally in terms of basic analog configuration or by global system properties related to algorithmic implementation or system block constitution. Concerning the analogous internal constitution, the dispersion effect can be reduced or even eliminated. However, in contemplation to further parasitic influences, systematic restrictions must be expectable. In particular, this applies to temperature influences or process variations. Thus, to compensate the dispersion effect by internal analog adjustments is contrary to the general applicability of the proposed ADC. The possibility to compensate the dispersion effect by global algorithmic implementation or system block constitution, in turn, offers a process to accept the appearance of non-linearities on the one hand and compensate them on the other hand. In general, this approach should provide the ability to extend the compensation method towards other non-linearity effects (i.e., temperature or process variations) that are physically related to the propagation delay or derivable from the propagation delay.

In the course of this chapter, the general influence parameter for the system feedback delay ( $\tau_d$ ) is investigated. The theoretical feedback delay is deduced as a composition between the comparator ( $\tau_{cmp_d}$ ) and the DAC propagation delay ( $\tau_{dac_d}$ ) and derives the origin of these delays. Based on these investigations, general compensation methods related to algorithmic implementations and system block constitution are proposed. These methods enable the ability to compensate non-linearity effects related to the dispersion and physical variations.

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## 4.1 Propagation Delay of the Feedback Configuration

To characterize the internal system delay the physical constitution of the feedback configuration is analyzed and the general influence parameters are determined. Related to figure 2.1 the total system delay ( $\tau_d$ ) is caused in the feedback configuration. Thereby,  $\tau_d$  is defined by the sum of the propagation delay, which is caused by the respective hardware component. Therefore, it is based on the propagation delay of the tracking module representative for the ALU ( $\tau_2 = \tau_{\text{clk}}$ ), the propagation delay of the DAC ( $\tau_3 = \tau_{\text{dac}_d}$ ) and the propagation delay of the comparator ( $\tau_1 = \tau_{\text{cmp}_d}$ ).

The propagation delay of the ALU results from the digital generation of the reference signal by the clock frequency ( $f_{\text{clk}}$ ). While the digital representation of an updated reference signal is in phase to the digital clock, the response of the comparator is delayed within the physical feedback system by the signal propagation. Due to the respective delay of the system, the detection signal loses the exact relation to the digital clock phase. Therefore, the detection signal, which corresponds to the comparator switching moment, is synchronized by the digital algorithm. In order to determine the switching moment as accurate as possible, the detection signal is therefore synchronized to the ALU operations by the clock frequency. Thus, the maximum propagation delay of the ALU is described by the maximum possible deviation due to synchronization. So, the worst case assumption implies for  $\tau_1 = \tau_{\text{clk}}$ . Thereby, the physical propagation delay of the digital elements, representing the ALU, is assumed to be negligible in relation to the clock period.

The propagation delay of the digital-to-analog converter (DAC) results from the physical topology of the component. In this terms a variety of DAC topologies are imaginable. However, with regard to the design of a Algorithmic Tracking Scheme ADC the DAC topology should be as simple as possible. This has the background, that a general purpose system demands for a high flexibility and a wide dynamic range. This point of view suggests, that the general digital-to-analog conversion system is reduced to the basic properties of a scaling network, which is directly connected to the comparator input. In consideration, that the digital inputs of the scaling network are sufficiently buffered, this configuration represents the minimum complexity. As a side note, similar to the ALU the buffer propagation delay is assumed to be negligible.

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Based on the proposed complexity reduction the scaling network in conjunction with the comparator input interface is responsible for the occurrence of the physical propagation delay. The comparator interface, in turn, is assumed to behave in a capacitive manner, as it would be valid for a CMOS implementation of the comparator differential input stage. In this terms, the decisive element for the delay analysis is reduced to the scaling network topology. Thereby, it would be possible to implement a current scaling topology, a charge scaling topology or a voltage scaling topology. Each individual implementation has respective propagation delay properties, which are considered in more detail regarding the applicability for the Algorithmic Tracking Scheme ADC.

The current scaling is excluded, since it requires either that also the comparator and the input signal is processed by a current or the voltage dependency of these needs to be transferred to a current. This demand implies a higher complexity of the analog hardware configuration and is contrary to the general applicability of the proposed ADC. The remaining possibilities for a charge scaling network (i.e. based on capacitors) or a voltage scaling network (i.e. based on resistors) are subject to the same conditions regarding the propagation delay. In general, the delay approximation of both designs is based on the consideration of a resistive and a capacitive element, thus that the propagation delay can be determined by  $\tau_{\text{dac}_d} = R \cdot C$ . However, the respective reference point is different. While the capacitive element of the capacitive scaling network is obvious, the resistive component is composed of the parasitics of the buffer and the interface to the comparator. On the other hand, the resistive element of the resistive scaling network is obvious. The capacitive element is also constituted by parasitics but the main influence is depicted by the input capacitance of the comparator.

In order to decide for a best suited topology, the technical point of view regarding applicability is considered in more detail. While the capacitive network provides a high accuracy, the individual capacitors needs to be large (e.g. several pF), but the resistive portion is comparably low (e.g. several  $\Omega$ ) related to parasitics. With respect to provide a variety of reference levels referred to the ADC resolution, the total capacitance of the scaling network alternates constantly. Since the capacitive portion is great compared to the resistive portion, the charge and discharge process also alternates in a high order. The alternating propagation delay is a direct consequence from this contemplation. The voltage scaling approach by a resistive network on the other hand provides technically speaking a lower accuracy than the charge scaling approach. However, the voltage scaling offers a nearly constant capacitance, which is based on the comparator input. Similar to the charge scaling topology, the total resistance of the resistive network alternates with the digital input. However, since the capacitance of the comparator input is low (e.g.

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several fF) and the resistive value is high (e.g. several k $\Omega$ ) a rapid charge and discharge option of the scaling network is available. Related to this fact, the voltage scaling option provides the ability to perform over a wide range and fast switching properties. Therefore, it is the preferable scaling topology for the Algorithmic Tracking Scheme ADC. The low capacitance of the comparator input allows for the consideration of rapid charge and discharge, which implies, that the propagation delay of the DAC based on this topology can be assumed as constant in relation to the clock frequency and is approximated by the maximum resistive configuration  $\tau_{\text{dac}_d} = R_{\text{max}} \cdot C_{\text{cmp}}$ .

The comparator forms the third influencing factor that causes a propagation delay ( $\tau_{\text{cmp}_d}$ ). In general, the comparator can be considered as an amplifier in open loop configuration. Therefore, the characterization of influencing factors of the propagation delay is related to the common amplifier configuration based on a differential input stage and an output driver. As common for integrated circuits, the process variations determine the mismatch characteristics of the differential input stage, whereby the physical mismatch by processing leads to mismatch for the propagation delay related to the input signal level. The same effect can be described for temperature or power supply variations. Besides the process variations, the influence of temperature or power supply variations offers a higher level of control, but can not be completely excluded from the design. Thereby, a lower supply voltage or else a higher temperature implies a slower propagation delay.

The capacitive load, in turn, is a key factor for propagation delay and needs to be considered for the system design. Besides the available output current, it is the determining factor for the switching properties of the comparator. The physical term is defined as slew rate, which is the general limiting factor of the propagation delay. Referred to the Algorithmic Tracking Scheme ADC, the comparator output drives the digital input interface of the ALU. Related to the technical side of view, the digital interface can be assumed as a CMOS circuit, where the parasitic input capacitance is of major interest. In general, it can be accepted of small size, but may not be neglected for high speed circuits. An additional parameter that influences the propagation delay is depicted for the configuration of the differential stage. Since the output needs to be tapped at one of the differential branches, the capacitive load is unequal in comparison between the branches. This leads to the fact, that the differential stage is unbalanced and the propagation delay relationship between rising and falling edges is skewed. Since the algorithmic approach considers the level crossing detection for both comparator edges, even the quantized relationship between consecutive conversion samples is imbalanced related to the input signal. The generation of the mean value for consecutive samples equalizes this imbalance on the one hand, but introduces a constant offset to the digital output on the other hand.

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Also the influence of the Input-Common-Mode-Rejection (ICMR) is of major interest, especially for a rail-to-rail design. The closer the input signal level to the rails, the slower the comparator reacts. This fact is technically related to the source and sink of the differential input stage which are based on transistors (e.g. MOSFET). The ICMR is defined by the common-mode voltage range where all MOSFETs remain in the saturation region. For the case this cannot be guaranteed, the gain and thus the slew rate are adversely affected. A slower propagation delay results for the case that the input signal is located closer to the comparator rail level. Referred to the algorithmic conversion, this effect can be considered as fact that lowers the conversion rate close to the rails.

An important factor that influences the propagation delay of the comparator is the amount of overdrive or underdrive of the analog input signal by the reference signal. The related physical effect is defined as dispersion [41, 43] and describes the variation in the propagation delay that results from overdrive/underdrive a reference level. In this case, the effect of the variation in the propagation delay is related to both the amount and the time (Slew Rate) of the overdrive/underdrive. The dispersion contributes an important factor to the level crossing approach, since it is based on the exact intersection of the signals to be compared. Since the level crossing by overdrive/underdrive is a key aspect for the design of the proposed tracking schemes, especially in contemplation with jumps or step scaling, the influence to the propagation delay by this factor is significant. The dispersion results in a non-linear distortion of the converted output signal from the ADC. In addition, the conversion rate, which is decisive about the effective resolution and thus the accuracy within the bandwidth, is subject to the variations of the propagation delay.

The analysis of the propagation delay, which is subject to the feedback configuration of Algorithmic Tracking Scheme ADC, revealed the respective delay portions of the individual hardware components. Thereby, the investigations regarding propagation delay, which is based on the hardware constitution results in a practical design for the ALU and the DAC under the assumption of a constant or negligible propagation delay. But besides, the delay assumptions for the ALU and the DAC the investigations revealed, that the comparator is subject to a propagation delay variation (i.e. dispersion). It causes the ADC for a non-linear distortion in time, which is the reason for a restriction of the effective resolution. Therefore, based on this analysis there is a demand for a detailed investigation of the propagation delay in the scope of the Algorithmic Tracking Scheme ADC in order to compensate the dispersion factor.

### 4.1.1 Comparator Propagation Delay Characteristics

The propagation delay characteristic has a major influence to level-crossing ADCs [44] and therefore to the respective algorithmic implementations of the proposed ADC. Besides the slew rate, which acts as limitation the for propagation delay, especially the dispersion effect is decisive for the linearity of the ADC and the design of an algorithm. It is subject to the distortion of a converted sample, which implies that propagation delay variations are contemplated as additional noise. The noise portion by dispersion, in turn, can be referred to the conversion time of the algorithm. In this terms, also a mathematical prediction under the influence of dispersion noise can be determined by the general SNR equation (Eqn. 2.57). Thereby, the assumed conversion rate ( $f_{conv}$ ) results from the reciprocal of the statistical mean for the propagation delay including the dispersion. An alternative is depicted by the approximation for the worst case scenario. hereby, the maximum arising noise portion in relationship between the delays of the physical comparator parametrization (Slew rate) and the dispersion needs to be established. A general contemplation of the rms noise is illustrated in figure 4.1 by the transition region of the comparator where jitter and phase noise is caused by the uncertainty of the transition caused by delay variations. The increasing input voltage difference of  $v_p - v_n$  causes the output of the comparator ( $v_o$ ) for a low ( $V_{OL}$ ) to high voltage level ( $V_{OH}$ ) transition.

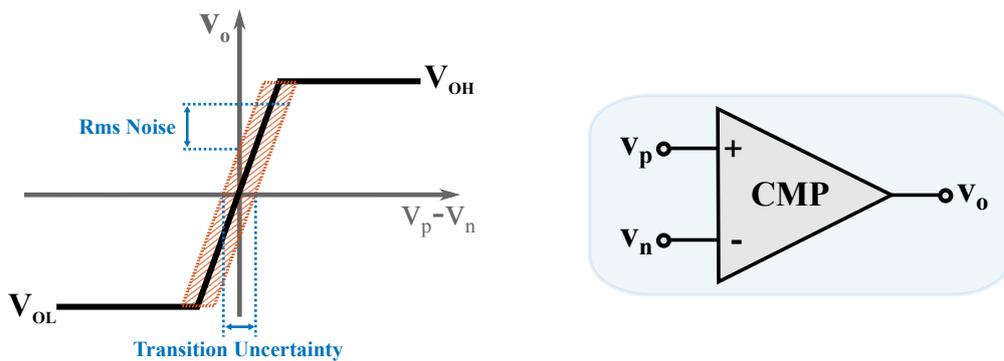


Figure 4.1: Transition region of the comparator that introduces noise due to uncertainty. Parametrization of the comparator, which is subject to the input voltage difference of  $v_p - v_n$  for a low ( $V_{OL}$ ) to high ( $V_{OH}$ ) transition of the output voltage level [45].

The comparator characteristic of the propagation delay is a decisive factor in limiting the linearity and conversion rate. For this reason, the most important parameters of the propagation delay (Slew rate and dispersion) are described in this section based on reference [45]. With regard to the design of the Algorithmic Tracking Scheme ADC these parameters are considered in order to compensate emerging nonlinearity. The term propagation delay can generally be referred to as the time required for a response of the comparator with respect to generate an output based on the input signal. Therefore, the temporal effects of the conjunction between the output signal and the time varying input signal needs to be considered. In contemplation to a low to high transition of the input ( $V_{IL} \rightarrow V_{IH}$ ) the output experiences the same low to high transition ( $V_{OL} \rightarrow V_{OH}$ ) for an non-inverting configuration, but with respect to the propagation delay ( $t_{pr}$ ). Thereby, the reference point for a transition is defined for the 50 % level of the respective signals by convention. Certainly, the propagation delay ( $t_{pf}$ ) emerges also for the high to low transition. But due to the physical implementation of the differential input stage the delay of the rising edge ( $t_{pr}$ ) is in many cases unbalanced to the delay of the falling edge ( $t_{pf}$ ). Therefore, the mean value of both delays defines the average propagation delay ( $t_p$ ) of the alternating transitions. The described behavior for the general estimation of the propagation delay is illustrated in figure 4.2.

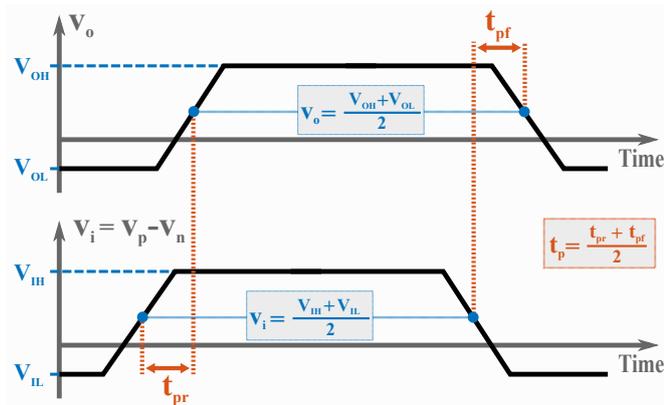


Figure 4.2: Propagation delay ( $t_p$ ) for an input to output transition. Parameter:  $V_{IH}$ : smallest input voltage at output voltage  $V_{OH}$ ,  $V_{IL}$ : largest input voltage at output voltage  $V_{OL}$ . The total propagation delay is based on the mean value of the delays for the rising ( $t_{pr}$ ) and falling ( $t_{pf}$ ) signal edge. The reference point is defined for the 50 % level of the respective signals by convention.

In contemplation to the temporal conjunction between the output transition and the input transition it can be determined, that a response of the comparator is based on a voltage transition within a certain amount of time. Thus, the characteristics can be described as voltage per time, which implies a slope. This slope, defines the ability to charge or discharge an output load within a time. Therefore, the characteristic can be transferred to a slew rate which describes the large signal behavior of the comparator. The slew rate, in turn, represents the general limitation of the propagation delay ( $t_{p\text{limit}}$ ). The relationship can either be described by the physical property to charge/discharge a capacitive load by  $SR = I/C$  or by equation 4.1 which defines the transferred voltage per time.

The small signal behavior in conjunction with the large signal behavior defines the dynamic characteristic of the comparator. It is the speed limitation (conversion rate) of ADCs. Since the large signal property is determined by the slew rate, the small signal behavior depends on the frequency response of the comparator. In consideration of a linear frequency response based on a single pole, the differential voltage gain can be expressed by equation 4.2, where  $A_v(0)$  and  $\omega_c$  is the -3 dB frequency of the single (dominant) comparator pole. It is assumed, that a minimum change of voltage at the input of the comparator is equal to the resolution, thus, that the input voltage represents a single step for an output voltage difference divided by the DC gain. In order to derive a relation between the comparator parameter and the time response, the Laplace expression of the differential voltage gain is inverse transformed under the consideration of a single step response ( $1/s \rightarrow V_{in}(t)$ ). The resulting equation depicts a first order exponential time response for the output transition. By rearranging the expression the propagation delay ( $t_p$ ) is derived based on equation 4.3. As a result, the input voltage difference ( $V_{in} = V_p - V_n$ ) is contrasted to the physical comparator parametrization by the DC gain ( $A_v(0)$ ), the output level ( $V_{OH} - V_{OL}$ ) and the cutoff frequency ( $t_c^{-1}$ ). Thereby it reveals, that the more overdrive/underdrive is applied to the input ( $\uparrow V_{in}$ ) the less the propagation delay ( $\downarrow t_p$ ). Applied to the algorithm of the Algorithmic Tracking Scheme ADC, this result implies, that the greater the deviation of the reference signal from the analog input signal, the higher the conversion rate.

**Statement:**

The greater the deviation of the reference signal from the input signal, the shorter the propagation delay and the higher is the conversion rate.

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**Propagation delay limitation by Slew Rate (SR):**

$$\boxed{t_{p\text{limit}} = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{SR}} \quad (4.1)$$

**Propagation delay by dispersion:**

Parameter:  $A_v(0)$  = DC voltage gain  
 $\omega_c$  = -3 dB cutoff frequency

Differential voltage gain and step response:

$$A_v(s) \cdot \frac{1}{s} = \frac{A_v(0)}{s} \cdot \frac{1}{\frac{s}{\omega_c} + 1} \quad \bullet \text{---} \circ \quad v_o(t) = A_v(0) \left[ 1 - e^{-(t_d/t_c)} \right] \cdot v_{in}(t) \quad (4.2)$$

Single step transition:

$$\frac{V_{OH} - V_{OL}}{2} = A_v(0) \left[ 1 - e^{-(t_d/t_c)} \right] \cdot V_{in}$$

Propagation delay:

$$\boxed{t_p = t_c \cdot \ln \left[ \left( 1 - \frac{V_{OH} - V_{OL}}{2 A_v(0) V_{in}} \right)^{-1} \right]} \quad (4.3)$$

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## Evaluation of the Propagation Delay Associated with Tracking Scheme ADCs

Besides the signal propagation of the remaining components in the feedback configuration, the propagation delay of the comparator is the main influencing factor related to misalignments of the ADC. While, the DAC and the ALU cause a quasi constant delay, the delay of the comparator depends on the relationship between the reference signal of the ADC and the analog input signal. Therefore, the the propagation delay associated with the Algorithmic Tracking Scheme ADC is investigated in more detail. Two equations were derived, that describe the propagation delay of the comparator. The first equation (Eqn. 4.1) defines the general propagation delay ( $t_{p\text{limit}}$ ) based on the slew rate. It is representative for the large signal properties of the comparator and describes the absolute delay limitation. The second equation (Eqn. 4.3) defines the delay ( $t_p$ ) dependency related to the applied input signal. It is representative for the small signal properties of the comparator and describes the influence to the delay based on a varying input signal magnitude. Thereby, it was determined, that the higher the deviation between the input voltages ( $V_p$ ,  $V_n$ ), the shorter the propagation delay ( $t_p$ ). Based on these facts, the propagation delay behavior is representative for the deviation between the reference signal and the analog input signal of the ADC. Since the equations transfer the overdrive/underdrive magnitude to a corresponding delay variation, they are able to describe the imbalance of the conversion regarding non-linearity. The overdrive/underdrive behavior of a comparator is known as dispersion. The relation to the dispersion of the Algorithmic Tracking Scheme ADC considers two perspectives.

The first perspective relates the dispersion to the global properties of the ADC. Therefore, the delay dispersion considers the average deviation of the reference signal from the input signal and is decisive about the conversion rate. The second perspective considered the local dispersion of the comparator which relates a single conversion step to a delay variation. Thereby, the relative dependency between the reference signal and the varying input signal introduces an additional delay variation, which is considered as noise. Related to the first perspective, the basic concept of a tracking scheme requires the overdrive/underdrive in order to detect the analog input signal. The magnitude of the dispersion defines the maximum conversion rate as the reciprocal of the propagation delay. In practical terms, the more overdrive/underdrive related to the input signal is applied by the reference signal, the higher the conversion rate. Thereby, a higher deviation is achieved by increasing the step size or by the application of jumps. The upper limit for the conversion rate is set by the slew rate of the comparator, which is based on the physical implementation of the differential input stage and the capacitive load to be driven by the comparator within the system. Figure 4.3(b) illustrates an example of the propagation

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delay characteristic for the comparator which is transferred to the conversion rate ( $f_{\text{conv}}$ ). The exemplary depiction contrasts the number of overdrive/underdrive steps to a global conversion rate by the application of equation 4.3. Thereby, the ratio between the output voltage difference ( $V_{\text{OH}} - V_{\text{OL}}$ ) and the DC gain ( $A_v(0)$ ) is normalized to the resolution of a single reference step. Furthermore, the -3 dB cutoff frequency ( $\omega_c$ ) is assumed in a manner, so that the comparator provides a conversion rate of  $f_{\text{conv}} = 10$  MHz for the application of a single reference step. Based on the fact, that the conversion rate is the reciprocal of the propagation delay, the relationship between the number of overdrive steps and the conversion rate offers a quasi linear course. However due to the logarithmic definition, the relationship is not to be regarded as proportional. As defined by assumption, the conversion rate is referred to 10 MHz for an overdrive of a single reference step. But with respect to an overdrive of 4 reference steps, the conversion rate results in more than 50 MHz. Exemplary, this relationship determines also the absolute delay limitation caused by the slew rate.

The second perspective considers the relative dependency between the reference signal and a temporal varying input signal within a single conversion step. Since the input signal changes over time and the reference signal is accordingly formed relative to it, the size of the overdrive is also relatively related to the input signal. This aspect, in turn, leads to an unbalanced propagation delay compared to several conversion steps between each other. The imbalance is always to be viewed as also relative to previous conversion steps, as these are also subject to the respective dispersion effect. The start initialization of a conversion step is processed by the comparator which implies, that the dispersion effect is already included for updated reference steps. Indeed, viewed globally, due to the relative propagation of the reference signal it adapts back to the analog signal. However, since every delay between the comparator switching moments leads to a corruption of the respective conversion step in time, the conversion step is also corrupted within its reference step number. Based on a corrupted reference step number, the conversion result is also corrupted, thus that the effective resolution decreases. In general, this imbalance introduces noise to the system, which is based on the uncertainty of the comparator transition.

To illustrate the corruption of a conversion step, which is affected by dispersion, figure 4.3 contrasts the number of overdrive/underdrive reference steps to the propagation delay ( $t_d$ ). It is normalized to the reference step generation time ( $T_{\text{ref}}$ ). Since the propagation delay is related to the required conversion time, the normalization to the step generation time clarifies the number of reference steps which would actually be generated during this time. Indeed, this perspective is considered for a snapshot of a single reference

step, since the sequential propagating in time for the step generation implies the increase in magnitude by the number of steps. This in turn reduces the actual propagation time, thus that each individual reference step magnitude needs to be considered separately relative to the analog input. Therefore, a deviation from the input signal by a reference step magnitude of 1 results in a delay of 5 times the reference generation time. Thus, the algorithm is forced to generate another step, which reduces the initial propagation delay. This process continues until the relationship is balanced. Referred to a linear course of the relationship between overdrive and propagation delay, this process would average. But the relationship is based on the logarithmic function, thus the process leads to non-linearities. Only if the conversion can be performed within a single reference step in time, this error is compensated for a static input signal as shown for a step size of 4 which corresponds to slew rate limit. Since the input signal can be considered as static in the rarest case, a permanent error arises relative to the input signal.

In conclusion, the associations of the propagation delay with the Algorithmic Tracking Scheme ADC reveals, that the dispersion effect has a major impact on the noise performance of the ADC. Two perspectives were considered. On the one hand the global dispersion effect which affects the conversion rate and on the other hand the local dispersion effect which leads to non-linearities of a converted sample. Since dispersion is a physical property of each comparator, the design of an ADC needs to be constituted either for a clocked comparator design related to its worst case parameter, or compensation methods needs to be applied.

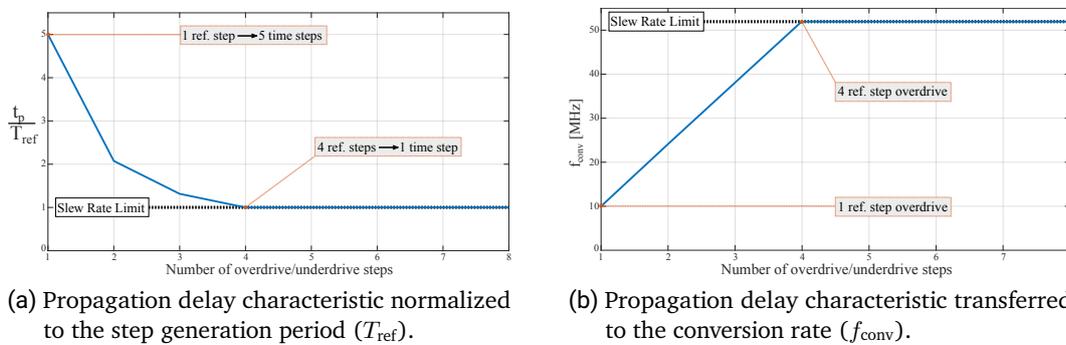


Figure 4.3: Propagation delay characteristic for an overdrive by a number of reference steps normalized to the step generation period ( $T_{ref}$ ) in (a) and referred to the conversion rate ( $f_{conv}$ ) in (b). The more overdrive in terms of reference steps, the more the delay decreases. Absolute delay limitation by the slew rate.

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## 4.2 Compensation of Non-linearity Effects

Every analog-to-digital conversion is influenced by noise which leads to conversion errors in the digital output stream [46]. Thereby, errors in the digital output stream are constituted by the relationship of quantized magnitude information within a quantized time. Referred to the tracking algorithm of the proposed ADC, the errors in magnitude are proportional to emerging errors in time as derived for the expression of the signal-to-noise ratio (Eqn. 2.57). Therefore, an error in time is transferred to an error in magnitude. In this terms it can be concluded, that any inaccuracy in magnitude which occurs during the conversion process has its origin in an inaccuracy in time. Based on the investigation for the propagation delay of the ADC feedback configuration this fact becomes particularly clear for the comparator. The dispersion effect, that occurs for every comparator, introduces non-linearities to the ADC system. Based on the propagation delay, its relationship to the applied reference voltage relative to analog signal could be unequivocally demonstrated. Thus the dispersion effect represents a source of noise, which can be determined by equations (Eqn. 4.3). Another noise source is represented by physical properties and can not exactly be determined, except for snapshots under the consideration of a static system. These noise sources are related to temperature, power supply instabilities or process variation. Due to the unpredictability of the occurrence within the system these parameters needs to be stochastically approximated. Also in this case, it can be assumed that stochastic noise is represented as non-linearity in the magnitude-time relationship. Therefore, it is distinguished between noise that causes deterministic non-linearity as for the dispersion effect and noise that causes stochastic non-linearity as for temperature. Both types of error affect the magnitude-time relationship of the ADC.

The magnitude-time relationship is represented due to the constitution of the reference signal which generates a proportional dependency between time and number of reference steps. In the simplest case a triangular staircase function results for the proposed tracking scheme as depicted in figure 3.3(b). Based on the proportionality ratios between conversion time and number of reference steps, every reference signal constitution can be traced back to a triangular staircase which is described by its slope. This implies, that a conversion which is represented by the binary step size also represents the time (propagation delay) needed for the conversion. Each conversion error, in turn, is conjunct with the conversion as an addition or subtraction of reference steps. This fact can be explained in consideration of a static case. Thereby, the analog input is assumed as static by the application of a DC signal. If the reference signal formation is assumed to be triangular it is expected, that the conversion time and thus the number of reference steps is based on equal magnitudes for overdrive and underdrive in relationship between the

reference signal and the analog signal. This behavior describes the ideal case and is illustrated in figure 4.4(a). As examined in the previous section (Sec. 4.1) the dispersion effect can even be related to a disparity between overdrive and underdrive in relationship between the reference signal and the analog signal. Thus, the number of reference steps for overdrive is unequal to the number of reference steps for underdrive. In relation to the converted output signal, this implies a constant offset of a static signal, which is expressed by mean value averaging. For a time variant input signal, in turn, each conversion step would be conjunct with this offset which globally leads to an offset formed as slope in relation to the analog input. In general, it can be considered as non-linearity. Figure 4.4(b) compares the reference signal formation under the influence of nonlinearity to the ideal case. The mean value of the reference signal extrema is shifted due to the dispersion effect which adds an offset to the output stream of the ADC.

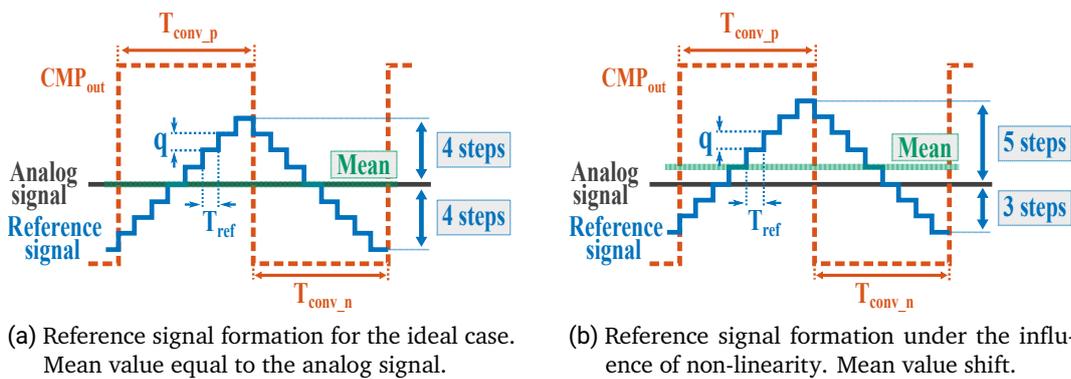


Figure 4.4: Comparison between the reference signal formation for the ideal case (a) and under the influence of nonlinearity (a) for a static analog input (DC signal). The dispersion effect of the comparator is assumed for a disparity between overdrive and underdrive in relationship between reference signal and analog signal. The mean value of the reference signal extrema is shifted due to the dispersion effect.

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The example in figure 4.4 signifies the displacement between overdrive and underdrive of the analog signal by the reference signal. It reveals, that the comparator has a mismatch between the rising and the falling edge. Thus the dispersion effect has an influence on the switching moments of the comparator which leads to a distortion of the converted binary stream. The distortion by dispersion results in an offset which is related to the static DC input signal. Separately considered, it can be deduced, that each conversion step introduces an offset to the output stream which is constituted relative to the analog signal. If the signal is time variant, the offset is subject to a time shift in addition. In general, the time-magnitude relationship is distorted compared to the ideal case where the comparator would be a constant device. The introduction of further non-linearity (i.e. stochastic non-linearity) generates further distortion to the time-magnitude relationship. However, in contemplation to a separate conversion step, the dispersion effect causes offsets relative to the input signal. Therefore, the main task of a compensation application requires the recognition of the respective offset in order to equalize the misplacement between the input signal and the digital output stream. Based on the time-magnitude relationship there are various options related to offset cancellation by the algorithmic approach or by analog extension. The basic principle utilizes the time-magnitude relationship, thus that either the conversion time or the magnitude is manipulated under the assumption of a known offset. The most obvious method would detect the worst case parameter of the comparator regarding offset and extends the conversion time towards this limit. Indeed, this approach implies, that the dispersion effect is skipped, by the application of a constant conversion clock. However, since the level crossing approach requires the exact intersection of the input signal and the reference signal, the accuracy of the algorithm is deteriorating. Therefore, it would be advantageous to detect the respective offset and apply foreground or background compensation. In this terms, foreground compensation adjusts the sample algorithm and background compensation adjusts the output stream.

In scope of compensation, two methods are proposed. The first method concentrates on the detection of the offset as described by figure 4.4. Therefore, constant input signals (i.e. DC signals) are applied to the ADC. Under the assumption, that the corresponding output stream to the respective input signal is known, the offsets can be determined and processed by an algorithm. This approach requires a training in advance of the actual conversion and provides the ability to globally detect non-linearity by means of deterministic (i.e. dispersion noise) and stochastic influences (e.g. temperature). Referred to alternating system properties over time, the training must be repeated. The more accurate the offsets can be located, the more accurate the compensation method. In order to maintain any degree of freedom in the algorithmic implementation, background compensation is proposed. Thereby, the conversion is processed including the non-linearity.

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The second approach is concerned to the conversion. The analog-to-digital conversion is also processed under the influence of non-linearity, but no training is required. Thus the conversion step occurs distorted for the single conversion. Due to the time-magnitude relationship each individual distortion can be considered as a mismatch in magnitude within a time period. This also applies to stochastic non-linearity, which modifies the dispersion property. Thereby it is assumed, that the probability of alternations for stochastic effects is almost negligible between consecutive conversion cycles. Separately, the deterministic non-linearity based on dispersion is related to the comparator properties and can be assumed as a constant variation within the comparator limits. Referred to this hypothesis, consecutive conversion steps are subject to the same conditions under the constraint of an unchanged analog input signal. This implies, that under these conditions exactly equal conversion results can be expected for an immediate repetition of the conversion. Furthermore, if the repetition is processed by the opposite noise constraining the non-linearity is canceled. Therefore, the second approach proposes a method to cancel the non-linearity by an inverse conversion based on a consecutive conversion step. As a result, the knowledge of the respective offsets is no longer necessary and the conversion process is self adaptive to non-linearity.

#### **4.2.1 Method 1: Non-linearity Tracking and Correction**

As investigated in section 4.1 the propagation delay of the comparator is considered to be inconstant. The relationship between alternating propagation delay and the input voltage difference is known as dispersion effect. It describes the ability of the comparator that for a higher input voltage difference the propagation delay is reduced. This reduction was derived by equation 4.3, which represents a logarithmic function. Therefore, it signifies a non-linear dependency between the overdrive/underdrive of input signals. For the general purpose ADC the overdrive/underdrive of the analog signal by the reference signal is the basic behavior. It is established by the algorithmic tracking scheme. However, the amount of overdrive/underdrive depends on the relative course of the reference signal to the analog signal. In general, it can be deduced, that the greater the deviation of the reference signal from the input signal, the shorter the propagation delay. For a continuous tracking, this implies that deterministic non-linearity is added to the conversion process. As illustrated in figure 4.4 the additional non-linearity effect, which is introduced by dispersion, causes an offset to the general conversion. Thereby, the dispersion effect was illustrated for a single conversion step under the assumption that the overdrive induces another delay than the underdrive. Or from the opposite side, the amount of overdrive/underdrive

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differs for the same propagation delay. Thereby, the constant offset is caused for the application of a constant input signal. By the application of a time variant input signal, a conjunction of the offsets related to each respective conversion step, causes a slope. Thus, the converted signal is distorted by non-linearity as well in the magnitude as in the time. In order to apply a correction scheme, a compensation method needs to provide information about the offset for individual conversion steps. Based on the exemplified method for the illustration of unbalanced comparator delays, the determination of the offset deviation related to each resolution step of the ADC is apparent. Therefore, the compensation in this section is related to the measurement of the individual offsets for a set of input voltages. In the further course these offsets are applied to the converted output stream as a correction in the scope of background compensation. Thus, this method is described as a tracking and correction method.

In addition, two further aspects are representative for the non-linearity of the comparator. The slew rate (SR) limitation which determines the absolute limitation of the propagation delay on the one hand. On the other hand the common mode input range (ICMR) limitation. It indicates, that the closer the input signal and thus also the reference signal is located to the comparator rail the slower the comparator response, which implies an increased propagation delay. Each of these parameter contributes to the overall deterministic noise, which can be predicted by the comparator characterization. Nonlinearity based on internal mismatch or external PVT variations affect the overdrive dispersion of the comparator in addition and can be considered by compensation methods as stochastic non-linearity, but not predicted. These additional noise sources can also be measured by the application of the proposed tracking method. Thereby, the total delay of the analog feedback system (i.e. comparator and DAC) determines the total deviation including the noise portion.

The proposed tracking scheme allows the measurement of the analog system based on the DAC and comparator combination and relates the linearity deviations to a correction factor. Based on the triangular sampling scheme, the correction factors are related between time and absolute voltage and can be expressed by an offset. The measurement principle relates boundary conditions to the ADC system, so that the input signal needs to be constant for the respective conversion step. Therefore, a symmetric oscillation of the triangular staircase function is expected with respect to the analog input (i.e. vertically mirrored). Each noise portion added to the propagation delay due to the time-magnitude relationship forces the triangular staircase function to be asymmetric. Thus, the mean value, which is generated from the extrema of the triangular function, deviates from the analog signal origin. In contemplation, that the corresponding digital representation of

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the analog signal is known by the measurement system as a reference, the deviation can be determined as signed difference. In order to relate the deviation to the background compensation, the offset value is stored in combination with the digital reference and applied whenever a comparable condition is met. A comparable condition is met for the case, that the converted output value corresponds to the previous measurement reference. Thus, the deviation can be interpreted as an offset to be adjusted. This process is repeated for a set of constant input voltages.

With respect to the application of a general purpose ADC, the requirements for the algorithmic implementation presuppose, that the tracking signal for the measurement is symmetrical on the one hand. On the other hand, the demand for the time-magnitude relation presupposes, that the measurement considers the algorithm to be applied. E.g. if jumps are applied to the algorithm, the conversion time is reduced due to a higher step size (section 3.1.1), which implies that the dispersion effect appears different as for the triangular scheme. However, under certain boundary conditions a similar behavior can be obtain as illustrated in figure 4.5. Thereby, the boundary conditions are assumed for the same analog input signal and the same total step size. The transfer from the triangular signal to the tracking scheme which includes mean value jumps (as described in section 3.1.1) is depicted by figure 4.5(a) to figure 4.5(b). Under ideal conditions (i.e. no non-linearity effects) the generated mean value of both signals is located at the input signal magnitude. Under the assumption of a dispersion effect which contributes to a higher overdrive magnitude than an underdrive magnitude, the generated mean value is located as a deviation to the input signal as shown in figure 4.5(c). Based on the initial boundary condition the shift is of the same magnitude as for the triangular signal (figure 4.4(b)). However, this behavior is achieved under the consideration to apply comparable boundary conditions. Indeed, the application of jumps to the mean value reveals another effect. The jump to the calculated mean value is exactly of the magnitude of the offset. Therefore, the adjustment of the jump size by the derived offset value reveals another possibility. Thus, the algorithm is able to apply the correction to the tracking scheme, which is defined as foreground compensation. The resulting effect shifts the conversion time ( $T_{\text{conv}_p} \neq T_{\text{conv}_n}$ ) which is illustrated in figure 4.4(d). Certainly, the total conversion time based on the sum  $T_{\text{conv}_p}$  and  $T_{\text{conv}_n}$  is unaffected for this type of algorithm, but the influence to the conversion time for a variety of algorithmic implementations can be demonstrated.

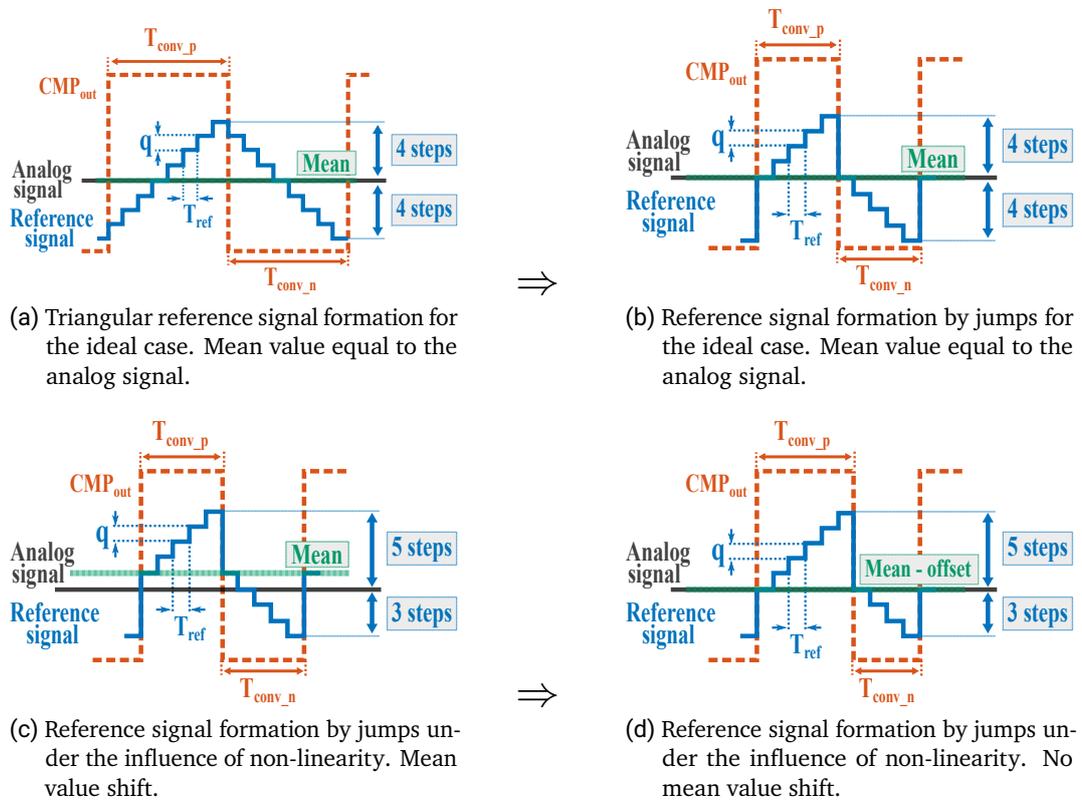


Figure 4.5: Comparison between the reference signal formations under the application of jumps to the mean value of consecutive conversion steps. The ideal case (a) is compared to the case of an applied dispersion effect (b). The mean value of the reference signal extrema is shifted due to the dispersion effect. Reference signal jump adjustment by offset consideration (c). The adjusted jumps of the reference signal cancels the offset, but introduces conversion rate uncertainty (d).

In order to apply the tracking and correction operation the proposed ADC system (Fig. 3.2) is extended in terms of digital implementation and additional analog hardware blocks. Thereby, from the hardware perspective the main processing of the tracking algorithm is farther located on the ALU, but the algorithmic implementation is extended by the measurement operation. Therefore, the abstract level of additional functional blocks describes the constitution of a correction FSM, a correction register and an output

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correction module. The Finite-State-Machine (FSM) represents the basic functionality and has the task of process and control the tracking and correction sequence. Thereby, the main sequence for measurement operations is based on a data exchange process between the FSM and the system. However, the processing is not subject to a real time behavior. Related to the current state of the correction sequence, the application of correction values is processed whenever a condition comparable to the condition of the measurement sequence is met. Therefore, a memory functionality needs to be established which is represented by the correction register. The correction register, in turn is the main interface between the ADC system and the tracking and correction system, thus that it stores respective data information as well as status information. The data exchange is controlled by the FSM which orders the register proceeding to transmit or receive information. Thereby, the communication between the algorithmic sampling scheme and the FSM is passed by the correction register in order to apply jumps to the algorithm, or to receive status informations like signal detection by the comparator. A further communication is established to an output correction unit, which processes the converted signal of the basic ADC by the application of correction schemes. Therefore, the register provides the combination of the converted binary stream and the matching correction values. So far, the correction scheme is based on the adjustment for the offset shift, but extended algorithmic approaches are imaginable.

### **Functional Implementation of Non-linearity Tracking and Correction**

Referred to the measurement requirement the system needs to provide constant analog reference voltages to be measured. Therefore, the proposed design is extended in terms of analog functionality by a bandgap reference and an analog multiplexer. The bandgap reference provides a set of constant analog voltages declared as pilot signals. The sequence of the pilot signals is defined by the FSM, therefore, bandgap block is digitally controllable. To verify an accurate analog pilot signal for the system, the demand on the design of the bandgap reference is referred to permissible deviations within the physical constitution of process parameters. Thus the deviation from the constant level should not exceed the accuracy of the ADC system (i.e. DAC resolution). A tolerable voltage mismatch of the pilot signal is limited to be less than 1 LSB of ADC resolution within the desired operating range. Based on the decision, if the input signal or the pilot signal should be processed, the analog multiplexer block is controlled by the FSM. To exclude parasitic or process related mismatch, the requirement for the multiplexer relates to the physical properties. The same mismatch for the analog signal and the pilot signal must be established concerning the capacitive load and resistance. Thus, the measurement of the pilot signal can represent the same offset deviation introduced by the analog multiplexer for the input signal.

Figure 4.6 illustrates the resulting functional block diagram of the proposed ADC which is extended by the tracking and correction system. Analog signals are depicted in blue and digital signals are depicted in black. The ALU represents farther the central processing unit. The combination of the comparator and the DAC is extended by the bandgap reference and the multiplexer in order to provide further analog functionality.

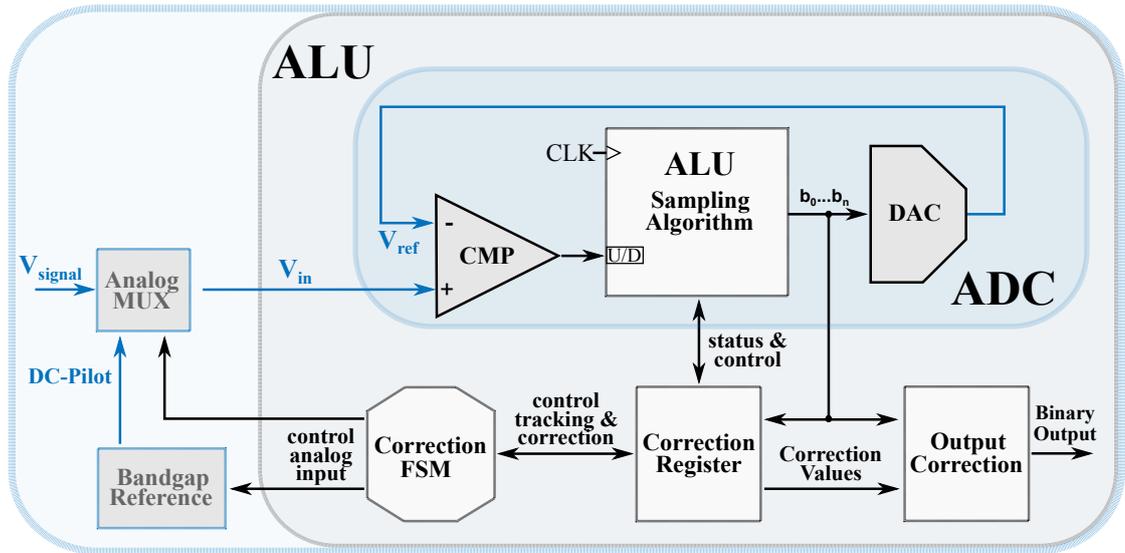


Figure 4.6: Block diagram of the proposed ADC configuration. The ADC is constituted by the basic approach of the analog comparator DAC combination and the part of the ALU for the algorithmic implementation. The algorithmic implementation is extended in terms of the measurement operation by tracking and correction. Additional operation blocks: Finite state machine, correction register and output correction. Additional analog blocks: Bandgap reference and analog multiplexer.

The functional sequence of the measurement (tracking) and the correction is depicted in figure 4.7 as a simplified version for a single analog reference step (pilot signal) and a subsequent input signal conversion and correction. The sequence starts with the application of the analog DC reference to the ADC system and the corresponding digital DC representation to the FSM algorithm. Thereby, the conversion of the analog DC reference enables the determination of the offset due to the known digital representation of the

applied reference. This process allows to measure the shift value of the symmetrical tracking scheme and supervises an offset to the corresponding positive (overdrive) and negative (underdrive) edge of the comparator. The determined offsets are stored in the correction register in combination with the converted result (correction reference). In consideration, that a single pilot signal is processed for the offset measurement, the actual conversion can be triggered. Initially, the converted output is conjuncted with the offset, but if the condition is met, that the output is close or equal to the stored correction reference, the converted output is adjusted by the corresponding offset. In contemplation to provide a high accuracy of the measurement system, a multiple of offsets and correction references needs to be determined. Therefore, a training is applied in advance of the actual conversion. For this purpose, individual analog reference signals are applied to the measuring system in a sequence, which is operated by the FSM. In order to describe a quasi dynamic sequence, the pilot signal is formed as a staircase function. In subsequent steps the respective correction results are determined and stored by the measurement system. If the sequential training process is completed, the conversion including correction is initialized.

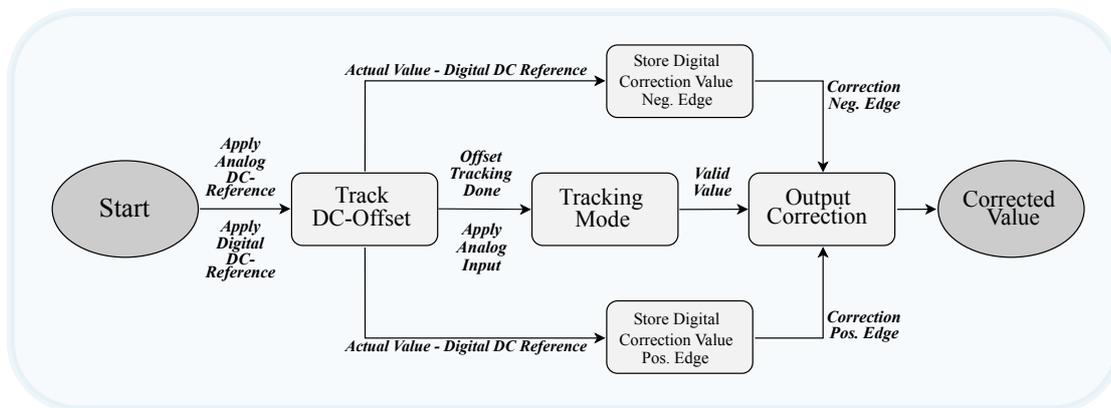


Figure 4.7: Functional sequence of the correction FSM illustrating the measurement method for a single reference step (pilot signal) and subsequent correction of the digital conversion.

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Figure 4.8 illustrates an exemplary measurement scheme for the tracking and correction unit. The pilot signal is generated as a staircase function by the FSM in order to describe a quasi dynamic sequence. Therefore, the FSM orders to the bandgap reference and the analog multiplexer to apply the first pilot signal. The tracking scheme of a triangular staircase function is applied and the first value is converted. If the comparator detects an overdrive transition and an subsequent underdrive transition, the first measurement results are generated ( $Max_p$ ,  $Min_n$ ). Thus, the mean can be determined by the extrema of the triangular function (i.e  $Max_p + Min_n/2$ ). Since the digital representation for the analog pilot signal is known to the FSM, the difference between the digital pilot and the mean value results in a signed offset. Based on the fact, that the calculation of the mean value as binary representation is averaged for an odd summation, the offset between the pilot signal and the maximum/minimum is determined as well ( $Offset_p$  and  $Offset_n$ ). In addition, this approach enables the application of jumps to the actual input signal by the respective switching moment of the comparator as described in figure 4.5d. In order to apply the correction by the offset adjustment, the results are stored in the correction register in combination with the corresponding measurement results. In the further course, the second detection (underdrive detection) of the comparator initializes an updated measurement sequence by the FSM status control to the bandgap. Thus, the measurement sequence starts again by an updated version of the pilot level. Referred to the staircase scheme, the pilot signal is increased by the basic steps size. This process is repeated for the entire set of pilot level of the bandgap reference. Indeed, the accuracy of the proposed tracking and correction scheme depends on the number of the measurement results and thus the number of pilot level provided by the bandgap reference. However, due to physical limitation of the possible number for pilot level, an algorithmic interpolation or extrapolation based on the combination of offset results and measured levels is also conceivable.

### **Evaluation of the Non-linearity Tracking and Correction Method**

The proposed tracking and correction method offers the possibility to measure the ADC system regarding non-linearity. Thereby, the nonlinearity is generalized for the combination of the analog configuration based on comparator, DAC and analog multiplexer. As investigated in section 4.1 especially the dispersion effect of the comparator causes a deterministic non-linearity effect, which is decisive for the conversion process. Besides the dispersion effect, the proposed method also considers non-linearity which is introduced to the system by stochastic processes (e.g. temperature). Therefore, the measurement of constant pilot signals enables the detection of a summed deviation, which is declared as an

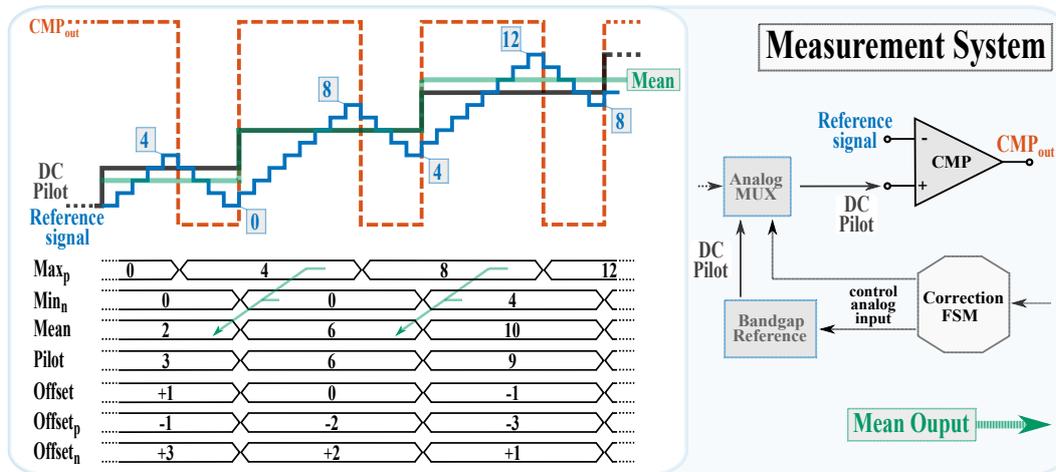


Figure 4.8: Exemplary measurement scheme. The pilot signal is generated as a staircase function by the FSM. For illustration purpose, the mean is shifted to the occurrence of the pilot signal. The offset is determined by the difference between mean and pilot. Offset<sub>p</sub> and Offset<sub>n</sub> is the difference to the pilot signal for the respective triangular maximum and minimum.

offset. In this terms the offset represents the correction magnitude which is applied to the converted output stream as background compensation or directly to the sampling scheme as foreground compensation. The measurement method proposes a set of constant pilot level, that are generated by a bandgap reference in order to satisfy the requirement of an unaffected calibration. Furthermore, the accuracy of the bandgap reference needs to correspond to the ADC resolution provided by the DAC. Related to the fact of accuracy, the number of calibration level (pilot level) is decisive about the correction ability. The higher the number of reference level, the more accurate deviations can be determined and thus corrected. Therefore, the proposed compensation method demonstrates an approach to determine especially the dispersion effect of the comparator, but requires a high number of constant voltage reference level. Indeed, there is a high analog implementation effort for a full ADC resolution set of calibration level (i.e. the bandgap provides each respective voltage level). However, the digital interpolation/extrapolation offers an additional possibility to increase the accuracy despite a small number of measurement results. Additionally, the higher the number of correction values, the higher the requirement on storage capacity. Another aspect is considered by the measurement method which is applied as a training sequence in advance of the conversion. Therefore, the higher the calibration step number,

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the longer the duration of the training. Since, the variation of stochastic non-linearity influences the analog property, the training process needs to be repeated from time to time. E.g. if the temperature of the ADC rises, or the supply voltage drops, it is an indication to repeat the training process and update the correction values. In conclusion, the proposed approach of non-linearity compensation by a measurement method allows to detect the non-linearity, but additional system effort of analog accuracy and storage capacity reveals to be high. Furthermore, the measurement process needs to be repeated under the influence of stochastic effects. Therefore, the system is suited for a controlled environment or if an accurate measurement of the dispersion effect is intended.

#### **4.2.2 Method 2: Non-linearity Compensation by Inverse Conversion**

As investigated in section 4.1 the conversion method based on the proposed tracking scheme is subject to distortions of the digital output stream. The distortions are related to diverse noise sources which are subdivided in groups of deterministic noise and stochastic noise. The deterministic noise portion is based on the dispersion effect and the limitations of a comparator (ICMR, Slew rate). The deterministic characteristic is defined as propagation delay variation which is expressed by the derived equation set (Eqn. 4.1, 4.3) in section 4.1. The dispersion effect causes the comparator for delay variations based on the amount of overdrive/underdrive the analog input by the reference signal. Referred to equation 4.3 the propagation delay variation can be determined. Thereby, the uncertainty of the comparator transition for various delay is predictable for a respective conversion step. If the overdrive/underdrive property is expected to be constant, the additional noise by dispersion can be considered globally. But as derived in chapter 3, the amount of overdrive/underdrive and thus the dispersion effect depends on the generated reference signal which propagates relatively to the analog input as common for a tracking scheme. Thus, the deterministic noise portion always depends on the applied algorithm. Therefore in case of a mathematical description of the noise, equation 4.3 is representative for a corresponding delay variation of a single conversion step. In order to describe the variation for the entire signal, the knowledge of each intersection property between the input signal and the reference signal is required. In this case, the statistical mean of the resulting propagation delays can be applied to the general signal-to-noise-ratio equation (Eqn: 2.57). Besides the fact, that the deterministic noise can be predicted in a certain way, the stochastic noise (e.g. temperature variations) can be estimated in the best case, since the exact description is related to a variety of conjunct physical degrees of freedom. However, the influence on the propagation delay based on stochastic variations was examined. As derived, the tracking scheme applied to the comparator relates the magnitude information

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to a time information in a proportional relationship (chapter 2). Therefore, any distortion on the converted signal magnitude can be traced back to a distortion in time. The distortion in time is represented by the variation of the propagation delay. Furthermore, 4.3 describes the same relationship for the propagation delay of the comparator. Thus, a distortion of the analog reference signal step (generated by the DAC) is translated to a distortion in time. Based on these considerations, a general statement reveals, that any introduced noise to the system causes a variation in the propagation delay regardless if the noise is deterministic or stochastic. The proportionality condition between time and magnitude of the tracking scheme transfers the distortion in time to a distortion in magnitude. This assumption is also referred to the measurement scheme in the previous section (section 4.2.1), where the delay variation of the entire system was transferred to an magnitude distortion (offset) in order to apply a correction scheme to the converted output signal.

**Statement:**

Any introduced noise to the system causes a variation in the propagation delay regardless if the noise is deterministic or stochastic. The proportionality condition between time and magnitude of the tracking scheme transfers the distortion in time to a distortion in magnitude.

The second method for non-linearity compensation is subject to the proportionality condition of the time-magnitude relationship. Thereby, it is assumed, that any distortion in magnitude is represented by a distortion in time within the conversion process. In general, the influence of deterministic and stochastic noise causes a variation of the propagation delay within the feedback configuration of the ADC which is translated to an magnitude variation by the tracking scheme. This, therefore, allows the conclusion that the feedback delay parameter is the only remaining variable within the system that is affected by noise. The initial dispersion effect in combination with the component delay of the feedback configuration can be considered as superimposed with the delay variation based on stochastic noise. In simplified terms, any stochastic variation of the propagation delay is signified by a variation of the dispersion effect.

The proposed method for a non-linearity compensation by an inverse conversion applies the approach of the alternating dispersion effect to the conversion scheme. The dispersion effect describes the displacement in the propagation delay in relation to the

overdrive or underdrive of the analog input by the reference signal as a conversion offset relative to the input signal. This relationship was derived for the assumption, that the global overdrive magnitude is different to the global underdrive magnitude for a constant input signal as depicted in figure 4.4. Furthermore, as derived for the tracking and correction approach based on measurements (section 4.2.1) the offset can be related separately for the overdrive as well as for the underdrive. In relation to the fact that the same magnitude must occur for the overdrive and the underdrive if the same boundary conditions are met, it is irrelevant whether the analog signal or the reference signal represents the physical inertial system. This implies application related, that an interchange of the input signal and the reference signal related to the comparator input terminals induces the same overdrive/underdrive magnitude. Thus, the absolute deviation between the input signal and the reference signal in terms of offset is unaffected. But if the inertial system is farther defined for the input signal, the sign of the offset (figure 4.8) changes. Thus, the magnitude for the overdrive corresponds to the previous (no terminal interchange) magnitude of the underdrive and vice versa. Therefore, overdrive becomes underdrive and underdrive becomes overdrive (overdrive  $\rightarrow$  underdrive, underdrive  $\rightarrow$  overdrive). The principle is exemplary illustrated for a conversion step related to a constant input signal in figure 4.9. The regular comparator terminal configuration (Fig. 4.9(a)) has an overdrive of 5 steps and an underdrive of 3 steps referred to the input signal. The resulting offset is determined by the difference between the mean and the analog signal for a signed magnitude of offset =  $-1$  step. The inverse comparator terminal configuration (Fig. 4.9(b)), in turn, interchanges the overdrive to 3 steps and the underdrive to 5 steps which turns the relation of the mean and the input by offset =  $+1$  step.

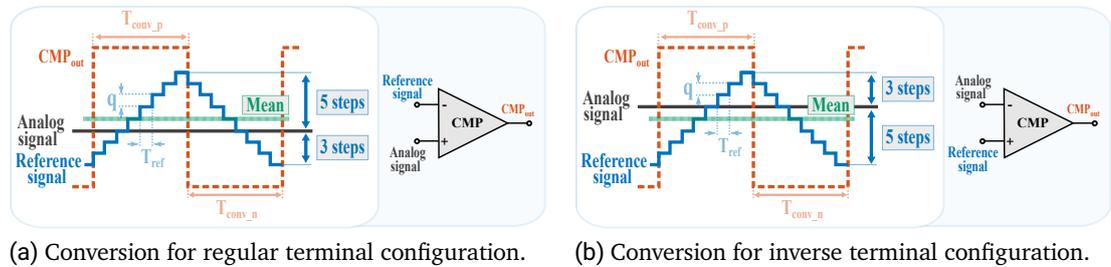


Figure 4.9: Comparison between regular terminal configuration (a) and inverse terminal configuration (b) illustrates the conversion behavior for an interchange of the input signal and the reference signal related to the comparator input. Result: overdrive  $\rightarrow$  underdrive and underdrive  $\rightarrow$  overdrive.

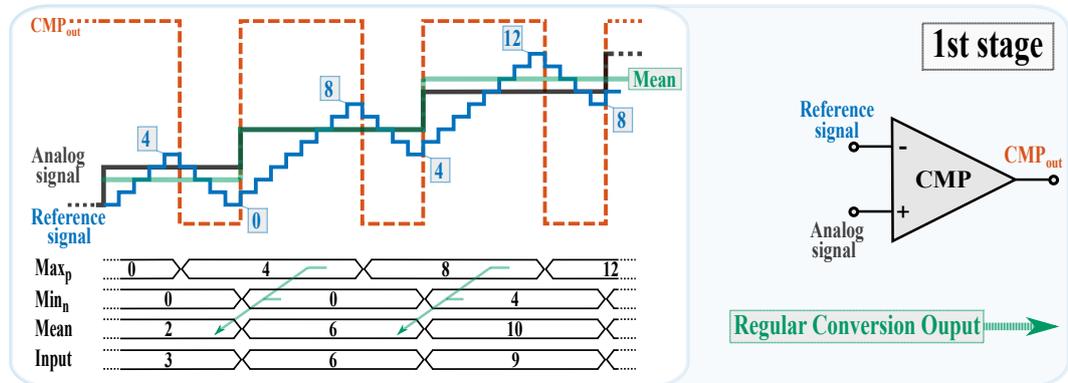
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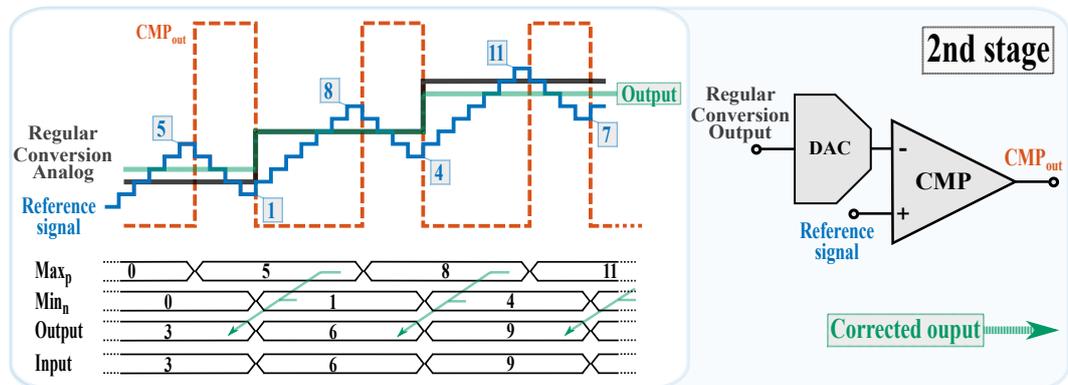
Physically, this behavior can be explained by the fact that swapping the terminals turns a non-inverting comparator into an inverting comparator. This also implies, that the delay introduced by overdrive is swapped to the delay introduced by underdrive. Since the output level of the comparator is also swapped due to the inverting behavior, the tracking algorithm requires the configuration as mirrored version of the regular scheme. E.g. if the regular scheme increases the reference signal for a high level of the comparator, the inverse scheme requires to decrease the reference level and vice versa.

In comparison between the regular comparator configuration and the inverse comparator configuration, the resulting reference signal scheme develops in the opposite direction. Thus, that for the generated mean of the sampling scheme extrema also results the opposite orientation in relation to the input signal. Therefore, the offset can be considered as opposite signed. As a result, the mean of the regular configuration mean and the inverse configuration mean corresponds exactly to the input signal magnitude. Thereby, the offset and thus the influence of the dispersion effect can be compensated. As derived in section 4.2.1 the modification of the tracking scheme by jumps reveals an equal offset generation (figure: 4.5c) as compared to the triangular sampling scheme. Therefore, the approach for offset compensation by an inverse conversion is transferable to modified sampling schemes.

The approach for a regular conversion and an additional inverse conversion offers the possibility to compensate the dispersion effect. Thereby, the dispersion effect is considered as variable parameter, that is influenced by the overdrive/underdrive magnitude as well as by stochastic variations. Based on the equalizing effect between the regular and the inverse conversion, a theoretical compensation scheme can be derived. It is proposed, that the regular conversion is processed in advance to the inverse conversion as illustrated in figure 4.9a. Thus the conversion step occurs distorted for the single conversion. By the detection of a conversion step, the mean value of the tracking scheme extrema can be generated. Related to a continuous time conversion, the sequential mean generation is always based on the maximum and the minimum of the tracking scheme (except for the initialization). In an subsequent step, the generated mean value is passed to the inverse conversion system. Thereby, the digital mean is converted to the corresponding analog representation as a quantized and distorted input for the inverse conversion system. By the application of the inverse conversion the generated distorted input is sampled by the same tracking scheme in a mirrored constitution. Since it must be noted, that the inverse conversion is affected by the same non-linearity as the regular conversion, the distortions are compensated by the negative signed non-linearity effect. It is enabled by the interchange of the overdrive dispersion effect with the underdrive dispersion effect. As a result, the output stream is free of non-linearity distortions. Figure 4.10 illustrates an exemplary conversion scheme of the proposed method.



(a) Conversion for regular terminal configuration.



(b) Conversion for inverse terminal configuration.

Figure 4.10: Sampling process and result generation of the proposed compensation method. A two-stage conversion establishes by a regular conversion cycle in (a) followed by an inverse conversion cycle in (b). The non-linearity affection of the regular conversion stage compensates concerning an equivalent parameterization and topology design by a subsequent inverse conversion.

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Referred to the measurement scheme in the previous section (section: 4.2.1) the analog input signal is assumed as a staircase function which increases the input by equidistant steps. The first stage converts in the regular scheme by the application of a triangular reference signal. Thus, the regular converted output, which is generated by the mean, is conjunct with the non-linearity effect. It results, that the mean value of the triangle extrema is deviated from the analog origin. In a subsequent step the regular converted digital output is transformed to the corresponding analog representation by a DAC and is considered as input signal. In the second stage the comparator terminals are interchanged and the conversion algorithm by the triangular scheme is applied to the reference signal in the opposite constitution. The inversion of the dispersion effect regarding overdrive and underdrive is processed by the conversion. Thereby, the non-linearity effect, which was introduced for the regular conversion in the first stage, is canceled. Based on the inverse conversion, the corrected output stream is free of non-linearity.

The proposed approach can also be explained by the mathematical expression of the dispersion effect due to propagation delay variations (Eqn. 4.3) as derived in section 4.1. Thereby, the mathematical expression can be considered for a step within the staircase function similar to the exemplary illustration in figure 4.10. Thus, in contemplation of a single conversion step equation 4.3 is rearranged with regard to the input voltage difference between the analog input signal and the reference signal. Related to the detection of a single conversion step the resulting output is expected as the actual reference signal magnitude ( $V_{\text{out}_{1\text{st}}} = V_{\text{ref}}$ ). E.g. with reference to figure 4.10(a) the first conversion output signifies a magnitude of 4 steps. Based on the overdrive effect the reference level deviates by 1 step from the analog input magnitude of 3 steps. Thus, the result of the reference signal corresponds to the respective input of the comparator at the intersection moment which is determined by the propagation delay ( $V_{\text{sig}}(t_{p_{1\text{st}}})$ ). This results in the following relationship for the expression of the converted output voltage ( $V_{\text{out}_{1\text{st}}}$ ) as given in equation 4.4. Thereby, the number of overdrive steps is assigned to a respective propagation delay ( $t_p \leftrightarrow \Delta V_{\text{in}}$ ) which is assumed as constant for the corresponding reference step magnitude. In addition, it is a valid assumption that the parametrization of both comparators regarding output level ( $V_{\text{max}}$ ), DC gain ( $A_v(0)$ ) and cutoff frequency ( $t_c$ ) is constant.

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**Parametrization:**

Input signal difference:	$\Delta V_{in1st} = (V_{sig} - V_{ref}) = (V_{sig} - V_{out1st})$
Comparator output level:	$V_{max} = (V_{OH} - V_{OL}) \rightarrow \text{constant}$
Comparator DC gain:	$A_V(0) = A_{V1st}(0) = A_{V2nd}(0) \rightarrow \text{constant}$
Comparator cutoff frequency (-3 dB):	$t_c = t_{c1st} = t_{c2nd} \rightarrow \text{constant}$
Delay assigned to No. of ref. steps:	$t_{p1st} \leftrightarrow \Delta V_{in1st} \rightarrow \text{constant}$

**Output level 1st conversion stage (regular):**

$$V_{out1st} = V_{sig}(t_{p1st}) - \frac{V_{max}}{2 A_V(0) \left[ 1 - e^{-(t_{p1st}/t_c)} \right]} \quad (4.4)$$

**Interchanged terminal assignment:**

$$\boxed{\Delta V_{in2nd} = (V_{ref} - V_{out1st}) = (V_{out2nd} - V_{out1st})}$$

$$\text{Delay assigned to No. of ref. steps: } t_{p2nd} = t_{p1st} \leftrightarrow \Delta V_{in2nd} \rightarrow \text{constant} \quad (4.5)$$

**Output level 2nd conversion stage (inverse):**

$$V_{out2nd} = V_{sig}(t_{p1st}) - \frac{V_{max}}{2 A_V(0) \left[ 1 - e^{-(t_{p1st}/t_c)} \right]} + \frac{V_{max}}{2 A_V(0) \left[ 1 - e^{-(t_{p1st}/t_c)} \right]} \quad (4.6)$$

$$\Rightarrow \boxed{V_{out2nd} \hat{=} V_{sig}(t_{p1st})} \quad (4.7)$$

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The process of the second stage is again represented by the relationship between the converted output voltage ( $V_{out_{2nd}}$ ) and the propagation delay of the comparator ( $t_{p_{2nd}}$ ). Due to the interchange of the input terminals for the second stage, the comparator behavior is translated to inversion. This implies that the previous overdrive delay is equal to the underdrive delay of the second stage ( $t_{p_{2nd}} = t_{p_{1st}}$  Eqn: 4.5). In a subsequent step the converted output voltage of the first stage ( $V_{out_{1st}}$ ) is applied to the opposite input terminal of the second stage comparator. Therefore, the reference signal is also applied to opposite terminal in reference to the first stage. Based on the terminal interchange, the difference between the reference voltage and the previous converted output is applied to the input of the second comparator. Again, the related reference voltage detection of the second stage determines the output magnitude for a single conversion step. By rearranging the expression for the propagation delay and the application of the terminal interchanging, the relationship for the converted output ( $V_{out_{2nd}}$ ) is established. As depicted in equation 4.6, the output level depends on the propagation delay relation of the first stage and on the propagation delay relation of second stage. Furthermore, the sampled input voltage ( $V_{sig}(t_{p_{1st}})$ ) is part of the relation in equation 4.4. Since due to the terminal interchange both delays and even the parametrization must be equal, the relationship to the propagation delay ( $t_p$ ) is canceled and the input voltage which is sampled at the intersection moment remains ( $V_{sig}(t_{p_{1st}})$ ). Therefore, it can be demonstrated, that the output of the inverse conversion corresponds to the input voltage at the the propagation delay sample moment (intersection). The corresponding relation is expressed in equation 4.7. As a result the non-linearity is compensated.

With respect to equation 4.6 the compensation ability of the proposed approach was derived for the contemplation of a single step. Therefore, the application of the inverse conversion demonstrates, that the influence of the propagation delay variations, which were introduced by a regular conversion, can be canceled. Since the combination of both conversion schemes reveals that the dependency of the magnitude displacement under the influence of the propagation delay must be of the same magnitude for both conversion schemes, the analog input representation remains. Related to the application of a level-crossing approach, the analog input is represented at the intersection moment between the input and the reference signal which is located at the conversion time. However, the demonstration of this effect is referred to the assumption of a single step and the requirement for the equality of the analog parametrization. Since equation 4.6 illustrates the compensation ability for a single step, it can be defined as local relationship. In order to illustrate the compensation approach for a multiple number of conversion steps, a global definition can be applied for demonstration. Therefore, it is assumed, that the

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delay variation is constant for each respective conversion step. To achieve the goal of comparability a propagation delay which is not subject to the dispersion effect is considered (e.g.  $T_{\text{conv}} = 100\text{ns}$ ). Due to the dispersion effect it is assumed, that the regular conversion (first stage Fig: 4.10(a)) is subject to a delay extension (e.g.  $T_{\text{conv}} + 33\text{ns}$ ). Due to forcing the comparator for an inverting configuration by the terminal interchange, the inverse conversion is related to the opposite delay effect. Thus, it is assumed, that the inverse conversion (second stage Fig: 4.10(b)) is subject to a delay reduction (e.g.  $T_{\text{conv}} - 33\text{ns}$ ). Indeed, for a global consideration, this approach must always be valid since a tracking scheme requires the overdrive intersection and the underdrive intersection. Thereby, the conjunction between an overdrive intersection and an underdrive intersection (rising/falling edge) determines the average propagation delay as derived in section 4.1.1. Referred to the constitution of a differential input stage (as common for comparator), the effect of increasing delay for an overdrive intersection always leads to the proportional decrease of the underdrive intersection and vice versa. Therefore, the physical properties of a differential stage can be considered as a balance. Based on the separate evaluation of a single step, which is related to overdrive and underdrive detection, the interchange of both cancels the single variation and results in an average. Therefore, the global definition can be assumed for an extension by an addition of the delay variation and an reduction by a subtraction of the same delay variation.

In order to investigate the compensation method by inverse conversion the global delay variation is applied to the general signal-to-noise ratio expression (Eqn: 2.57). In section 3.1.3 the influence of propagation delay variations were referenced to the conversion rate. Therefore, the global delay variations are representative for variations of the conversion rate ( $f_{\text{conv}}$ ). The courses of the signal-to-noise-ratios under the application of delay variations to the general SNR equation are illustrated in figure 4.11. They are described as positive effect (i.e. delay extension) and negative effect (i.e. delay reduction). If no delay variation effect is applied, the general expression reveals the derived SNR course of the jump-to-the-mean tracking algorithm (Fig: 3.8) and is parametrized in the same manner. Thus, the parameter are applied for a step generation rate of  $f_{\text{clk}} = 50\text{ MHz}$ , a resolution of  $N = 8$  and an initial conversion rate (no delay variation) of  $f_{\text{conv}} = 10\text{ MHz} = (100\text{ ns})^{-1}$ .

The resulting signal-to-noise ratio courses are investigated in the following. As expected, the absolute bandwidth limitation is unaffected by the assumption of a global delay variation. But a shorter propagation delay ( $T_{\text{conv}}$ ), which implies a higher conversion rate ( $f_{\text{conv}}$ ) reveals a higher effective resolution (SNR). On the opposite site, the reduction of the propagation delay also reduces the effective resolution. These results are representative for a global delay variation of the regular (first) conversion stage. Thus, in order

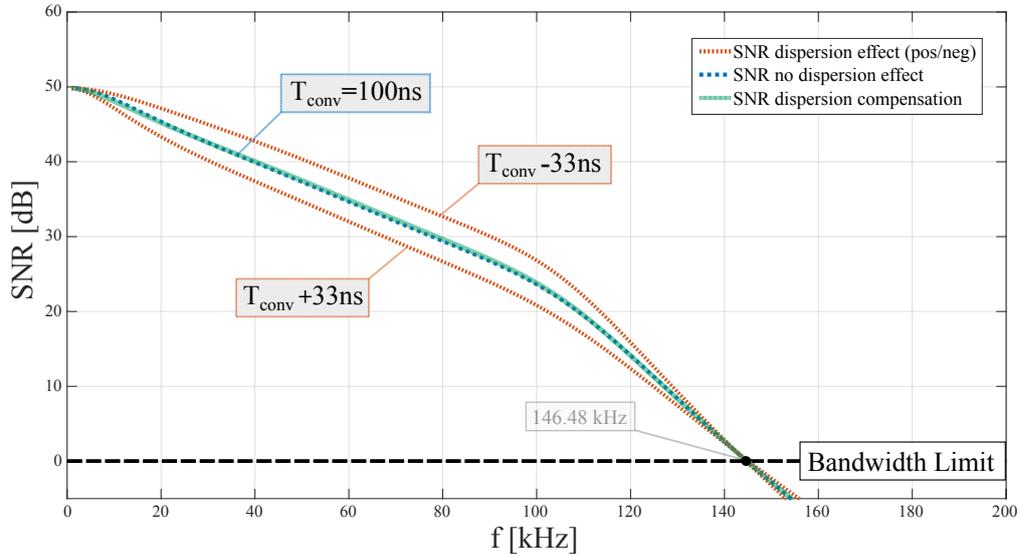


Figure 4.11: Compensation of the dispersion effect calculated by the general signal-to-noise-ratio equation (Eqn: 2.57). Adjustment of the conversion rate ( $f_{conv}$ ) regarding global delay variations by  $T_{conv} \pm 33$  ns. The mean of both SNR courses signifies the compensation ability by the matching to the SNR course without dispersion effect. Conversion time  $T_{conv} = 100$  ns  $\rightarrow f_{conv} = 10$  MHz.

to apply the inverse conversion (second stage) the opposite delay variation is processed. Therefore, the average of both functions, which is defined as the mean value, results in the signal-to-noise ratio course of the initial function with no delay variations. Thus, this approach represents the behavior of the compensation method based on a regular and a subsequent inverse conversion for a global delay variation. Based on the propagation delay relationship applied in equation 4.6 for the local step behavior and the propagation delay relationship for a global behavior in equation 2.57 it can be concluded, that the proposed method is applicable for the non-linearity compensation.

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## Functional Implementation of Non-linearity Compensation by Inverse Conversion

The theoretical assumption for an cancellation of the dispersion effect by the application of an inverse conversion presupposes the equality of environmental parameters for a practical implementation. In this terms the dispersion effect and the corresponding delay variations by stochastic noise demand for the same physical configuration of the analog implementation. Therefore, it is proposed that the same assembly regarding the analog configuration is applied for the regular conversion as well as for the inverse conversion. This mainly concerns the comparator, which is subject to the same dispersion effect. This also applies for the requirements of the stochastic variations, which influence is related to the global system. However, the tolerance is relaxed by the assumption that stochastic effects like temperature or supply variations are subject to a gradually process. Therefore, the inverse conversion can be applied time shifted, but close to the regular conversion. Thereby it is assumed, that the probability of alternations for stochastic effects is almost negligible between consecutive conversion cycles. Thus, both analog assemblies correspond to equal stochastic variations.

Based on the conversion and the compensation process, the respective assemblies are constituted by the basic ADC implementation in figure 3.2. Both are based on a comparator, a DAC and the sampling algorithm which is implemented on the ALU. Compared to the regular conversion module (first stage), the inverse conversion module (second stage) requires the interchange of the comparator input terminals regarding the reference signal and the input signal. Due to the terminal interchange the comparator operation is forced to an inverting behavior compared to the regular module. This implies, that the sampling algorithm is also processed by the interchanged parametrization (e.g. count up  $\rightarrow$  count down). This approach enables the inverse operation in comparison to the regularly parametrized algorithm, thus that the compensation is enabled. The interface between the regular conversion module and the inverse conversion module is constituted as an serial sequence. Thus, the inverse conversion is always processed as a subsequent step referred to the regular conversion. As a side note, a parallel conversion process is also applicable with reference to the theoretical approach. But compared to the methodical derivation in this section, the conversion provides alternating delays referred to overdrive and underdrive which depends on the dynamic relationship between the analog input signal and the reference signal. As derived in section 4.1.1, the reference signal develops relative to the input signal, which implies, that the overdrive/underdrive magnitude is relative related to the analog signal. As a result, also the propagation delay is relative to the analog signal. Thus, the establishing of a connection between the parallel configuration requires an exact timing. Based on the alternating delays, time distortions

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arise in case of averaging by the mean value. In contrast, the serial interfacing enables a controllable process due the completion of the regular conversion, which also includes the knowledge of the timing. If the regular conversion cycle is completed, which is signified by the comparator intersection detection, the inverse conversion is initialized. This approach enables a sequential processing of the conversion cycle, which validates, that an time interleaving of consecutive conversion steps is improbably. The algorithmic control is established by the Process-Control-Unit (PCU) which is implemented on the ALU and acts as the general interface between the regular and the inverse module. Therefore, it exchanges status control information between the respective sampling algorithm and the system. Besides the status control, the PCU provides a transceiver operation for receiving the distorted output of the regular conversion cycle which is forwarded to the inverse conversion module. In order to process an analog comparison, the forwarding of the digital stream is subject to prior digital-to-analog conversion. Therefore, the hardware assembly is extended by an additional DAC. Also in this case, the PCU controls the application of input signals, thus that the influence of additional propagation delay is controlled. Based on the general control process the additional system delay does not affect the phase alignment, but delays the general ADC output. In order to provide a synchronized output for the transmission to external systems, the compensated output stream of the inverse conversion module is prepared by the process control unit. The resulting functional block diagram of the proposed general ADC module with non-linearity compensation method is illustrated in figure 4.12. Thereby, analog voltages like the input signal voltage ( $V_{in}$ ) both reference signal voltages ( $V_{ref}$ ) are signified by a blue color. The digital signals like the status and control information or the digital output streams of the modules are black colored. Each individual algorithm is implemented on the ALU which describes the central processing unit.

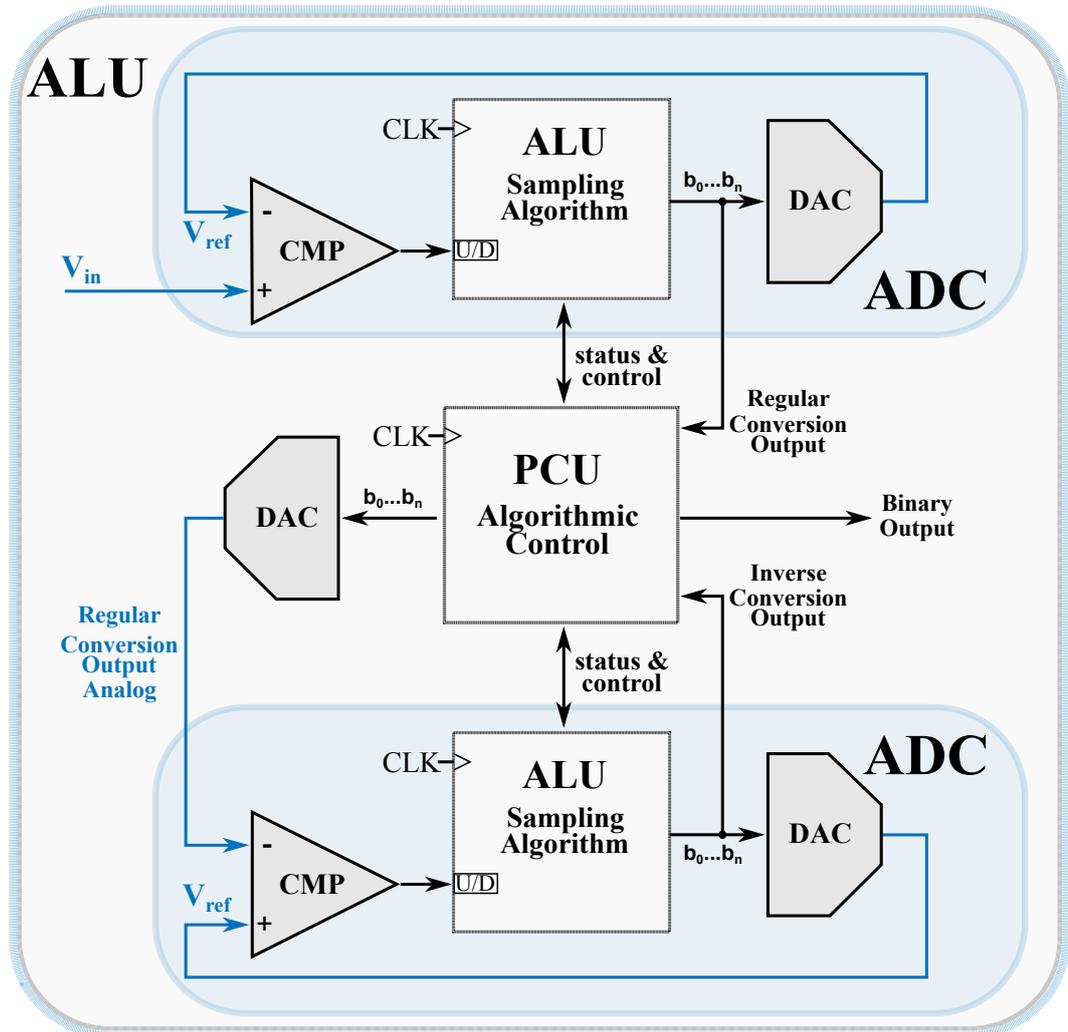


Figure 4.12: Block diagram of the proposed ADC configuration for a compensation method by inverse conversion. The basic ADC is constituted by the analog comparator DAC combination and the part of the ALU for the algorithmic implementation. It is applied for a regular conversion and a subsequent inverse conversion. The algorithmic implementation is extended in terms of a process control unit (PCU) for the regulation of the sequential compensation. Additional blocks: Process control unit, DAC and an additional ADC.

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The proposed approach for a non-linearity compensation by an inverse conversion demonstrates the theoretical applicability. Thereby the statement was derived, that any introduced noise to the system causes a variation in the propagation delay regardless if the noise is deterministic or stochastic. Furthermore, the proportionality condition between time and magnitude of the tracking scheme transfers the distortion in time to a distortion in magnitude. Based on this statement, the stochastic noise portion is transferred to a variation in the dispersion effect. In order to compensate this effect, the resulting functional block diagram in figure 4.12 illustrates a physical implementation which is based on the inverse compensation method. A second conversion stage was introduced which must be subject to the same physical parametrization in order to be subject to identical delay variations. If the variations are contemplated for a global influence, the proposed implementation meets these requirements. But if the implementation is subject to local variations like local process parameter, supply drops in the power tree or even heat spots, the influence of stochastic noise can lead to a mismatch between the regular conversion stage and the inverse conversion stage. This requirement applies in particular to the comparator which processes any affected dispersion effect. Therefore, an extended approach for a functional implementation is proposed which is based on an analog component reduction. Thus, the required functionality is transferred to digital operations.

The extended approach reduces any possibility of a mismatch between the comparators. Thereby, the claim for equality of process parametrization is extended in terms of the application of the inverse conversion process to the same comparator instead to an additional device. In this terms a sample interleaving which is controlled by the process control unit (PCU) is proposed. The inverse conversion is still considered as a subsequent process to the regular conversion, thus that the regular and the inverse stage is alternately applied to the same comparator. Thereby, the variations of stochastic effects like temperature or supply variations are subject to a gradually process. This approach implies for local or global variations. Due to the application of a single comparator, the manufacturing process-related variations for the comparator are compensated by the inverse conversion method.

Even by the transfer of the proposed method to a single comparator approach, the inverse method requires the terminal interchange of the comparator. Thus, either the combination of a reference signal and the input signal, or the combination of the regular conversion output and the corresponding reference signal can be applied to the comparator. Since one terminal is always interfaced by a DAC, the PCU processes the digital switching between the regular reference voltage and the output of the regular stage. The analog extension re-

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quires the additional DAC, which output must alternate relative to the analog input voltage. Thereby, an additional analog multiplexer is required. This device is also controlled by the PCU, which regulates the signal application. The extended functional block diagram of the proposed general ADC module with non-linearity compensation method is illustrated in figure 4.13. Again, analog voltages are signified by a blue color and digital signals are black colored. The ADC algorithm as well as the process control is implemented on the ALU.

The process control unit (PCU) is even more important in this approach and enables the digital implementation of the algorithmic ADC behavior as well as the compensation behavior. This opens up further possibilities for compensation. It is imaginable, that the remaining analog components represented by the DACs or the analog multiplexer introduce further mismatch or noise based on non-linearity. In this case an algorithmic extension is imaginable which provides a self measurement related to the non-linearity measurement method described in section 4.2.1. In this way, the constitution of the DACs that are interfaced to each comparator terminal enables the self measurement and the elimination of the dispersion effect at the same time. However, an approach implemented in this way requires training sequences.

### **Evaluation of the Non-linearity Compensation by Inverse Conversion Method**

The compensation method proposed in this section is based on the property, that a conversion process is subject to dispersion effects. Furthermore, these effects are influenced by stochastic non-linearity. Therefore, the dispersion effect, which is defined as deterministic non-linearity alternates with stochastic effects. Due to a time-magnitude relation of the tracking scheme the dispersion effect is considered to be deterministic and can be predicted by equation 4.4. Therefore, each respective variation in the propagation delay causes a variation in the overdrive/underdrive magnitude of the reference signal. Since the propagation delay variations can be determined, for a single conversion, the compensation approach considers, that the same variation occurs if the conversion is repeated under the same system constraints. Therefore, a conversion which is inverse to the previous (regular) cancels the dispersion effect regardless if the noise is deterministic or stochastic. This statement was verified by the derivation of equation 4.7 under the consideration of a single conversion step, which is defined as local delay variation. Furthermore, an example of a global propagation delay variation which considers a constant deviation for a sequence of conversion steps was verified by the general SNR expression (Fig: 4.11). It was demonstrated, that even the global variations can be compensated by the proposed method.

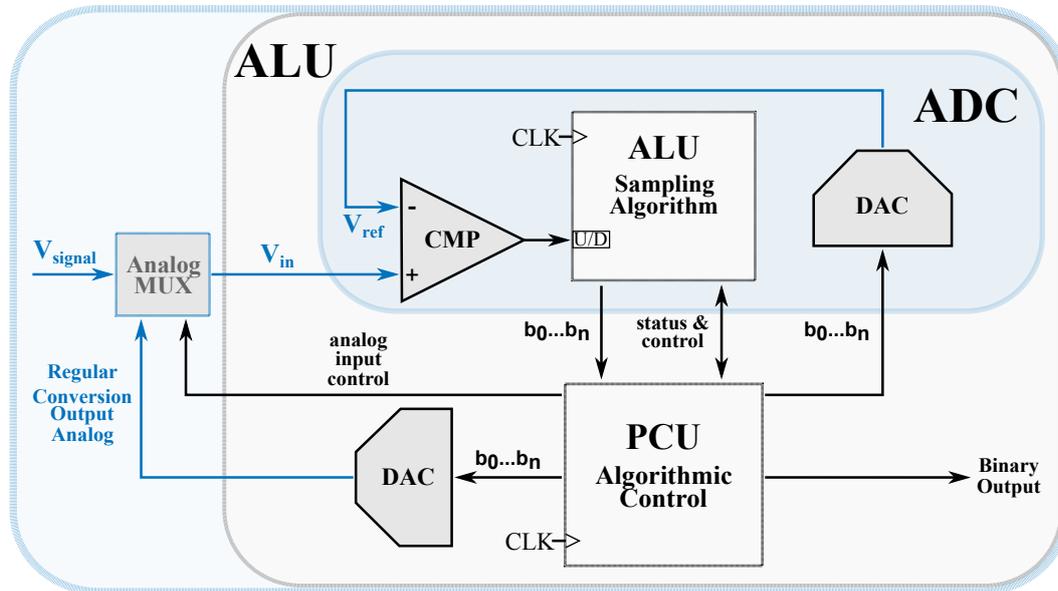


Figure 4.13: Block diagram of the proposed ADC configuration for a compensation method by inverse conversion with functional extension. The basic ADC is constituted by the analog comparator DAC combination and the part of the ALU for the algorithmic implementation. The regular conversion method as well as the compensation method by inverse conversion is applied by alternations. The process is controlled by the process control unit (PCU). Additional analog blocks: DAC and analog multiplexer.

Based on the verified theoretical compensation approach, a functional block diagram for the physical implementation was derived (Fig: 4.12). It is based on two identical configurations for the analog-to-digital conversion as illustrated in figure 3.2. But the interchange of the comparator terminals between the reference signal and the analog signal enables the compensation ability as described in section 4.2.2. Furthermore, the dependency between global and local process parameter were described, which demand for an extended version of the proposed block diagram related to possible mismatch effects between both comparators. Therefore, the functional block diagram was extended regarding functionality by the alternating application of the regular conversion and the inverse conversion at a single comparator. The resulting block diagram is illustrated in figure 4.13 and offers the ability to dynamically configure the sampling algorithm and

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the compensation algorithm at the same time. Furthermore, due to the interconnection of the comparator terminals to a respective DAC, additional functionality like self calibration is applicable.

Referred to the mathematical verification by equation 4.7 for a local dispersion effect and by equation 2.57 for a global dispersion effect, the compensation by an inverse conversion signifies potential. Compared to the compensation method by tracking and correction in section 4.2.1 the initial training sequence can be dispensed and the compensation processes can be applied immediately. Especially, the self adaption to stochastic variations and the related dispersion effect turns out to be beneficial. Furthermore, a permanent storage of correction values is not necessary in contemplation to the actual compensation process. Indeed, in order to provide a higher degree of self calibration, the measurement method can be applied in addition, which enables the compensation of mismatch or non-linearity in the remaining analog components based on the DACs and the multiplexer.

### 4.3 Summary on Non-linearity Compensation Methods

The proposed ADC is constituted by the hardware configuration as illustrated in figure 3.2. Besides the sampling algorithm, the feedback configuration of the DAC and the comparator are decisive about the conversion ability regarding effective resolution. This dependency was derived in chapter 3 based on the general signal-to-noise ratio expression 2.57. As a result, it could be determined that the shorter the system delay ( $\tau_d$ ), the higher the effective resolution. The analysis of the analog system configuration revealed that the non-linearity based on mismatch, process variations, or external influences (e.g. temperature) could be traced back to a variation in the propagation delay. The transfer between magnitude mismatch and time mismatch was derived in section 4.1 and signified a non-linearity effect of the comparator. Due to the structure of a differential stage, the magnitude of overdrive/underdrive causes propagation delay variations of the comparator as expressed in equation 4.3. Based on the analysis of the equation the statement, that the greater the deviation of the reference signal from the input signal, the shorter the propagation delay reveals. In general, this property of a comparator defines as the dispersion effect.

Furthermore, the intersection detection of the proposed ADC sampling scheme requires an overdrive or underdrive of the analog input signal by the reference signal. Concerning the fact that the reference signal develops proportionally in step time and step size, the non-linearity of the comparator thus transfers to the conversion output via the reference signal moments. In these terms, the propagation delay behavior represents the devi-

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ation between the reference signal and the analog input signal of the ADC. However, related to the ADC constitution, the dispersion effect is not constant but depends on the overdrive/underdrive magnitude relative to the analog signal. Therefore, the relationship between the signals determines the main influencing factor for delay variations. The relationship between these signals, in turn, is related to the fact that the reference signal develops relative to the analog input signal as described in chapter 3 for the proposed tracking scheme. The evaluation of the propagation delay, which is associated with the proposed algorithmic ADC tracking scheme, is illustrated in figure 4.3. Thereby, the conjunction between the dispersion effect and the conversion rate is established and reveals the behavior between overdrive/underdrive by the reference signal step size. The higher the step size, the faster the conversion rate. However, the absolute limit determines by the slew rate of the comparator.

In general, the propagation delay variation by the dispersion effect results in a non-linearity of the conversion, which is described as noise. Indeed, every analog-to-digital conversion is influenced by noise, leading to conversion errors in the digital output stream. The noise sources can be subject to various processes related to the ADC characteristics. Referred to the proposed set of tracking algorithms, the errors in magnitude are proportional to emerging errors in time. Based on this fact and the comparator dispersion property, which also transferrers the overdrive/underdrive in magnitude to the propagation delay, the variation can be determined. Therefore, the non-linearity caused by the dispersion defines as deterministic noise. In addition, also the influence of physical properties like temperature, power supply instabilities, or process variation represents additional noise sources. However, the unpredictability of the noise occurrence presupposes the stochastic approximation of these parameters. Thus, the noise portion defines as stochastic noise. Since the stochastic noise affects the magnitude-time relationship of the ADC in addition, the dispersion effect can be considered as superimposed with the delay caused by stochastic variations. In conclusion, any noise portion introduced to the system can be traced back to a delay variation, which can be expressed as a variation in magnitude (e.g. reference step number). Thereby, two perspectives can be considered: On the one hand, the global dispersion property affects the conversion rate, and on the other hand, the local dispersion effect leads to non-linearities of a converted sample. The effect is illustrated in figure 4.4. It demonstrates the dispersion effect of the comparator, which assumes a disparity between overdrive and underdrive in the relationship between the reference signal and analog signal. Thus, the mean value of the reference signal extrema displaces due to the dispersion effect.

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Two methods were proposed to provide a conversion, which is free of non-linearity. These methods can compensate for the dispersion effect and the superimposed delay variation by stochastic noise. The first method (section: 4.2.1) applies a training sequence to the ADC, which detects the deviations in the converted magnitude by a measurement approach. Thereby, a constant input signal whose digital value is known to the system is converted by the ADC system. Based on the application of constant input levels, the deviation parameter between the input and the converted output representations defines a set of corresponding correction parameters. In these terms, the actual conversion is processed, including the non-linearity, and the output stream is corrected based on a background compensation. Indeed, alternating system properties over time causes that the system needs to repeat the training sequence. The tracking of non-linearity correction parameters defines a measurement method. However, the complete set of correction parameters implies a storage capacity to the system. Since it generally applies that the more accurate the offset detection, the more accurate the compensation method. Thus, the tracking and storage capacity of the system defines an essential aspect of the design. In conclusion, the proposed approach of a non-linearity compensation by a measurement method allows detecting of the non-linearity. However, additional system effort of analog accuracy and storage capacity reveals to be high. Furthermore, the influence of stochastic effects requires the repetition of the measurement process. As a result, the system is suitable for a controlled environment or accurate measurements of the dispersion effect.

The second approach has its origin in the actual conversion process. The conversion result superimposes the non-linearity introduced by dispersion for the regular conversion. Thereby, it is assumed that the same non-linearity effect must arise for a repeated conversion under the same system configuration. If the system parameter configuration is in the opposite (inverse) direction, the polarity of the dispersion affects the conversion in a contrary way. Based on this fact, a regular conversion followed by a subsequent inverse conversion can be processed. Due to the contrary polarity, the influence of the dispersion effect compensates. From the perspective of an implementation approach, the terminal interchange of the comparator and the simultaneous inverse algorithmic adjustment applies the inverse behavior.

The approach was verified by the propagation delay equation for the comparator and describes the influence on dispersion for a single-step conversion. In these terms, the influence description enables the consideration of local deviations by dispersion effect. The summation of each dispersion that affects consecutive conversion steps under the assumption of a constant variation enables considering total deviations. In these terms, the general signal-to-noise ratio equation (Eqn. 2.57) determines the influence of propagation delay variations on the effective resolution of the ADC. In section 3.1.2 the influence

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of propagation delay variations was examined and revealed the dependency between effective resolution and conversion rate. The conversion rate, in turn, is restricted by the propagation delay. Thus, variations of the conversion rate enabled the investigation of the global variations. As expected, the result for the total bandwidth is unaffected, but the effective resolution reduces for an increasing delay and vice versa. The compensation property was verified based on the mean of the SNR for an increased delay and a reduced delay by the same absolute deviation. In these terms, the resulting mean value exhibits the same SNR course as for the case, that no delay variations are applied. The verification of the proposed method by the local and the global delay variations allows the conclusion that this compensation scheme is also valid for superimposed delay variations.

In comparison to the proposed measurement method in section 4.2.1, a self-adaption process is applied by the proposed method for non-linearity compensation by an inverse conversion. Since the inverse conversion is subject to the same properties as the regular conversion, the cancellation of the dispersion effect and the superimposed stochastic variations is processed. In this case, the system requires no knowledge about the actual deviation for the entire set of reference levels. Thus, a permanent storage ability is not necessary. However, the compensation method can be extended to the measurement process, enabling the detection of mismatch or non-linearity properties of the remaining analog components.

In conclusion, the propagation delay analysis in this chapter revealed that the significant influence of non-linearity could be traced back to the comparator properties. The dispersion effect determines the conversion abilities of the proposed ADC, and stochastic delay variations superimpose to the dispersion effect. Therefore, two methods are proposed in order to compensate for the non-linearity. The first method is defined as the tracking and correction method Tracking-and-Correction-Compensation (T&C). It describes the possibility of measuring the non-linearity effects based on delay variations and addressing them as correction parameters. These parameters are applied in a subsequent step to correct the digital output stream. In this procedure, the actual conversion processes under the influence of non-linearity. The second approach, described as inverse conversion Inverse-Conversion-Compensation (IC), also processes the conversion affected by non-linearity by a pre-conversion (regular conversion). In a subsequent conversion process, the same boundary conditions apply as the regular procedure, but the interchange of the comparator terminals enables the inverse behavior. The second (inverse) conversion is subject to the same delay variations as the regular conversion. As a result, the non-linearity compensates. In these terms, both compensation methods provide the ability of non-linearity adaption to the conversion, which can be applied to the proposed ADC design [86] as described in section 4.2.1 and 4.2.2.



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## 5 FPGA based ADC System Design

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Programmable Digital-Signal-Processing (DSP) has been quite instrumental in the last two decades [47]. This context leads to digital signal processing with Field Programmable Gate Arrays (FPGA). Analog-to-Digital-Converters (ADC) are the most basic interface between the real-world analog signals and any DSP application. The main challenge in designing DSP with FPGAs is the interfacing of analog signals to the FPGA as they commonly do not have built-in ADCs. Although several vendors offer ADC interface boards for FPGAs, they are expensive and have fixed specifications such as achievable bandwidth and resolution. Suppose an ADC must cover multiple use cases, or there is no initial specification for the requirements, an ADC selection that covers all possible use cases or possible requirements is often over-dimensioned. In most cases, the design and development of an ADC covering multiple use cases requires a high effort. In order to accelerate the design process, a fully programmable ADC, which covers a minimal amount of hardware, is beneficial [88].

There are already some approaches to implementing an ADC concept with a minimal number of external analog components [48]. The basic principle applies the LVDS transceiver as an analog comparator. It compares the analog input signal, which needs to be converted, to a second signal which acts as a reference. An external Digital-to-Analog-Converter (DAC) generates the analog reference signal. Thus, the configuration is constituted in a feedback system between the FPGA and the DAC. The constitution enables the comparator to generate a 1-bit digital stream related to the input signal. The majority of approaches [48, 49, 50] apply the DAC behavior by generating the analog reference signal due to a low-pass configuration based on a resistor and a capacitor. The most minimalistic approach is proposed by [49] and is constituted by a single resistor and the parasitic capacitance of the LVDS transceiver. In this way, the low-pass configuration integrates a digital square wave reference signal to a triangular representation. The time for crossing the input signal level by the triangular reference is related to the input signal itself. It is encoded in the 1-bit digital stream of the comparator output as Pulse-Width-Modulation (PWM). Furthermore, the width of the pulses is converted by a Time-to-Digital-Converter (TDC) based on a carry-chain.

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Since the implementation of the proposed designs in [49, 50, 51] are timing critical, the linearity of the ADC transfer function and the robustness against process variations are of major interest. As investigated in chapter 4, the dispersion effect of the comparator has a significant impact on the propagation delay. This effect degrades the linearity of the ADC transfer function by delay variations. In addition, the interaction of the external resistor with the parasitic capacitance of the LVDS receiver needs to be designed carefully to establish integration of the rectangular reference towards a triangular shape. The interaction of the resistor-capacitor combination, in turn, acts as a bandwidth limiting factor for the reference signal by the low-pass behavior. Therefore, the external resistor needs to adjust to the reference clock frequency and the parasitic capacitor. Thereby, process-dependent variations, especially for temperature, degrade the matching. Another aspect concerns the TDC implementation, which requires adaptation of the delay elements in the carry-chain. Which in turn is crucial for the linearity of the TDC transfer function [52]. The deviations based on unadjusted delay elements are not constant and differences between different FPGAs and process variations. [49, 52] proposes a calibration method to adjust to the delay deviations.

In order to avoid linearity degradations, a hardware system approach is proposed, which is independent of the TDC and the external hardware configuration. Therefore, a scaling network converts the digital reference signal into an analog representation instead of an RC-low-pass configuration. This approach enables a high degree of reconfigurability and establishes the independence of the conversion algorithm. This approach enables the applicability of a general-purpose ADC. Due to the independence of the hardware configuration from the sampling algorithm, a wide range of ADC architectures is conceivable, which can be programmed regarding the desired application area. In the context of this chapter, the application-specific algorithms proposed in chapter 3 are implemented on the FPGA. In order to verify the applicability, the proposed tracking scheme algorithms are compared to basic ADC implementations. Thus, a Counter ADC topology, a SAR ADC topology, and a Tracking ADC topology are implemented. In addition, the enhanced tracking scheme introduced in section 3.1.1 and the modification of the tracking scheme by jumps, which was introduced in section 3.1.2, are implemented. The measurement results demonstrate the applicability of the proposed equation set for the signal-to-noise ratio prediction derived in chapter 2. Furthermore, the implementation parameter for the ADC topologies are examined by measurements regarding the linearity performance of the LVDS driver applied as an analog comparator. In the scope of the evaluations, the conversion rate ( $f_{\text{conv}}$ ) and the step generation rate ( $f_{\text{clk}}$ ) for the respective ADC topology is defined in order to provide a linear conversion. Based on these constraints, the ADC topologies are investigated regarding dynamic and static performance. The

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dynamic performance is evaluated in the scope of the signal-to-noise ratio course within the respective bandwidth. The static performance is evaluated regarding DNL and INL.

In the further course of this chapter, the advantages of digital signal processing (DSP) are used to implement additional functionality. Thus, filtering and signal interpolation is applied to the converted output stream of the proposed non-uniformly sampled signals. The approach considers the non-uniformity of the conversion stream. As described in chapter 2, the information of any signal is distributed in magnitude and in time. The non-uniform sampling scheme retains the information about the time compared to uniformly sampled signals. So far, the information was converted regarding the magnitude information, which is formed by the relative dependency between the analog input signal and the reference signal. However, the conversion scheme still contains information about the signal within the time, constituted by the non-uniform behavior. In order to increase the effective resolution of the converted signal, the time information can be converted to magnitude in addition. As described in chapter 2, the transformation prescription can be mathematically defined by the "Bernstein Theorem", which translates the time information into magnitude information. In this way, an application needs to provide the same property. Therefore, the time information is quantized with relation to the respective magnitude information. The quantization in time of the converted stream is applicable by the step generation rate ( $f_{ref}$ ), which translates a proportional ratio between time and magnitude of the reference signal. Due to this fact, the interpolation of the converted output stream by a Comb-Integrator-Comb structure as depicted in [53] is possible, which converts between time and binary representation of an input vector. Therefore, the CIC structure is applied to the non-uniform tracking scheme. In order to demonstrate the interpolation ability, the SNR course and the DNL and INL are evaluated.

In summary, this chapter demonstrates a general-purpose ADC topology based on various sampling schemes and verifies the derived equation set of chapter 2. In addition, the digital signal processing ability of the FPGA is applied to improve the digital output stream of the ADC, which is based on the conversion of the time information into magnitude information of the non-uniform sampled signal.

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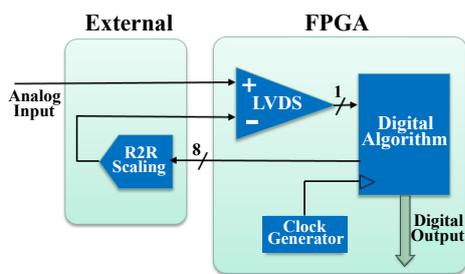
## 5.1 System Architecture

The ability of reconfiguration depends on the composition of the reference signal formation and the corresponding conversion into a multi-bit digital representation of the 1-bit digital stream of the comparator output. Since the conversion scheme of the cited methods is fixed by the application of a RC generated reference signal and the time-to-digital conversion, the ability of reconfiguration is restricted to this method. Therefore, the proposed approach in this chapter is designed for a hardware independence of the reference signal generation scheme. Whereby, this ability is achieved by replacing the external resistor by an external resistive R2R scaling network available as integrated circuit. Thus, the formation of the reference signal depends on the binary input reference, which is generated by the FPGA. A capacitance, and especially the hard to control parasitic capacitance of the LVDS receiver used as comparator, has no meaning. If the R2R network is matched, the R2R scaling ability is independent of the exact resistive value. In this way, even the feedback path is independent of process variations like temperature. Furthermore, the replacement by an R2R scaling network enables the system to generate a reference signal controlled by the algorithm that is implemented on the FPGA. Thereby, this approach provides another degree of freedom regarding reconfigurability. Also the application of a TDC is not absolutely necessary and a more robust design with fixed timing properties can be applied. Based on this application the ADC behavior depends exclusively on the implemented algorithm. The architecture of the proposed system is depicted in figure 5.1(a). The basic FPGA configuration is constituted by a LVDS receiver acting as comparator, a clock source for a constant timing reference and the desired digital conversion algorithm. The ability of programming a synchronous AD conversion scheme enables the independence of timing constraints besides the clock constraints and thus can be applied to any FPGA.

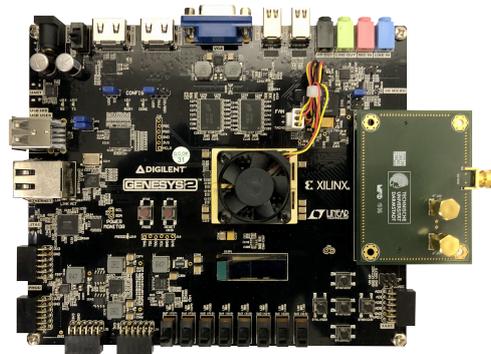
The experimental setup for the proposed system architecture is illustrated in figure 5.1(b). It is constituted by the FPGA and the R2R ASIC. Thereby, the R2R ASIC is connected via a FMC port of the FPGA which is established as standard configuration for every state-of-the-art FPGA. The R2R scaling network is located at an external PCB and constitutes the interface with the FPGA specific IOs of the FMC. Furthermore, it passes the analog input signal and the analog reference signal of the R2R output to a dedicated LVDS Driver for the purpose of a comparator. The implementation to evaluate the design is applied to a Genesys 2 development board [54] which is equipped with a Kintex 7 FPGA (Commercial -2 speed grade) [55].

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In order to demonstrate the applicability of the general purpose ADC, the concept is implemented as a multi topology system that includes the specific ADC topologies. Based on the desired test setup or area of application, the accompanying conversion scheme can be selected by external hard- or soft-switches. Therefore, the dynamic property and the reconfigurability of the proposed system can be exploited. In addition, the application allows the choice of digital signal processing techniques.



(a) Reconfigurable ADC system architecture.



(b) Reconfigurable ADC experimental setup.

Figure 5.1: System architecture (a) and experimental setup (b) of the proposed reconfigurable ADC design based on a FPGA and an external R2R scaling network. The basic FPGA configuration is constituted by a LVDS receiver acting as comparator, a clock source for a constant timing reference and the desired digital conversion algorithm.

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### 5.1.1 FPGA IO-Driver Analysis for Application as Analog Comparator

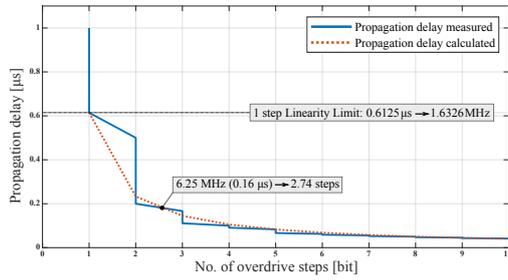
As evaluated in section 4.1, the feedback delay signifies an important factor of the ADC implementation. Besides the stochastic non-linearity of external sources, the deterministic non-linearity introduced by the dispersion effect determines the ability of the ADC topology to convert an analog input signal. The delay variation introduced by the dispersion effect affects the conversion rate ( $f_{\text{conv}}$ ) which is decisive about effective resolution of the ADC. Especially, uniformly sampled ADCs like the SAR topology demand for a constant propagation delay. This is related to the fact, that a single conversion cycle requires a multiple of comparator detections. Whereby, the number of detections depends on the desired resolution of the SAR ADC. In case that the individual detection cycles varies due to propagation delay, the SAR logic is not able to detect the correct transition. Thus, the investigation for the feedback delay between the FPGA and the external configuration is an elementary design requirement in order to define the parametrization regarding conversion rate ( $f_{\text{conv}}$ ) for the ADCs.

In order to investigate the deterministic non-linearity based on the dispersion effect, a measurement approach was proposed in section 4.2.1. Again, for the FPGA implementation a measurement process which is related to the tracking of the dispersion effect is implemented as a rudimentary model. But since the uniformly sampled SAR ADC requires a constant propagation delay, the LVDS driver of the FPGA is measured in terms of discover a constant delay configuration. Therefore, the measurement of the feedback configuration is established by the Counter ADC. This approach provides the ability to track the overdrive/underdrive level related to a constant input signal (DC) in terms of resolution steps. In order to establish the relationship between the number of overdrive/underdrive steps and the propagation delay, the reference step generation rate ( $f_{\text{clk}}$ ) of the Counter ADC is iterated. Thus, the dispersion effect can be determined by the difference between the Counter ADC conversion output and the digital representation of the corresponding DC input signal. Related to the fact, that the counter ADC offers a proportionality between the number of reference steps and the step generation rate, the propagation delay can be translated based on the number of overdrive/underdrive steps. The resulting linearity characteristic of the feedback configuration in figure 5.2(b) was measured for a set of reference step generation rates ( $f_{\text{clk}} = 1 \text{ MHz} \rightarrow 25 \text{ MHz}$ ). Thereby, the full-scale input level, which is expressed by the binary representation is tracked and corresponding overdrive/underdrive steps are addressed. The transfer characteristic illustrates the input common mode range (ICMR) of the comparator which is related to the dispersion effect. In order to determine an applicable propagation delay, the dynamic behavior of the ICMR needs to be constant for the full-scale input range

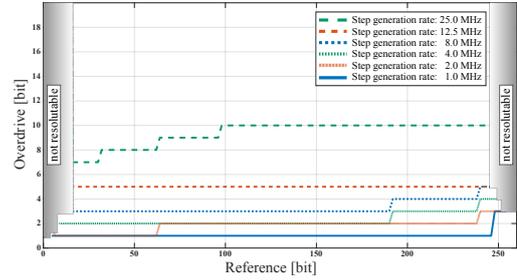
of the ADC. Related to the measurements in figure 5.2(b) this aspect is revealed for a conversion rate limit of  $f_{\text{conv}} = 12.5 \text{ MHz}$ . Due to the uncertainty of the reference step quantization, a deviation of  $\pm 1$  step is subject to the measurement error. Related to the overdrive/underdrive effect, the absolute maximum/minimum is not resolvable by the reference scheme, since a certain amount of overdrive/underdrive is required for a step detection.

As constraint for the uniformly sampled SAR ADC any amount of overdrive/underdrive affects the conversion scheme for a failure detection. Thus two implementation possibilities remain. On the one hand, a permanent step adjustment on the algorithmic side is imaginable under the effect of constant dispersion. On the other hand, the dispersion effect needs to be eliminated by the reduction of the step generation rate towards the single step related propagation delay. Referred to figure 5.2(b) this consideration reveals a step generation rate of  $f_{\text{clk}} = 1 \text{ MHz}$ , which implies a single propagation delay of  $t_p = 1 \mu\text{s}$ . Based on the propagation delay restriction, a detection cycle of the feedback configuration requires twice the propagation delay, since the underdrive is equal to the overdrive. Therefore, the detection of a single reference step requires  $2 \mu\text{s}$ . Related to the Tracking ADC implementation this evaluation corresponds to the absolute conversion rate, thus that  $f_{\text{convTRACK}} = 500 \text{ kHz}$ . As described, the SAR implementation requires a multiple of detection cycle, which is related to the resolution of 8 bit. Thus the conversion rate results in  $f_{\text{convSAR}} = 500 \text{ kHz}/9 \approx 55.6 \text{ kHz}$ . Even the conversion rate for the Counter ADC can be approximated as an average of a multiple of detection cycle. If an equal distribution is assumed, the average number of time steps is related to the half of the resolvable steps. Thus, the average conversion rate for an 8 bit Counter ADC results in  $f_{\text{convCOUNT}} = 500 \text{ kHz}/128 \approx 3.9 \text{ kHz}$ .

Based on the measurement results the dispersion effect of the comparator in combination with the additional delay of the feedback configuration can be approximated. Due to the proportionality condition of the linear reference signal of the Counter ADC the number of overdrive/underdrive steps corresponds to the number of delay steps. Conversely, it can be assumed, that the absolute overdrive/underdrive size in number of reference steps corresponds to a single reference step in time as applied in figure 4.3(a). Therefore, the approximated propagation delay for the feedback configuration results from the measured step number as illustrated in figure 5.2(a). The result of the plot reveals the assumed propagation delay behavior of section 4.1.1. The greater the deviation of the reference signal from the input signal, the shorter the propagation delay and the higher is the conversion rate.



(a) Propagation delay characteristic of the feedback configuration (measured, calculated).



(b) Linearity characteristic of the feedback configuration for a set of generation rates.

Figure 5.2: Propagation delay characteristic (a) and linearity analysis (b) for the feedback configuration between FPGA and resistive voltage scaling network. The linearity in (b) was analyzed for a set of reference step generation rates ( $f_{\text{clk}}$ ). The higher the step generation rate the more the linearity degrades. The linearity characteristic depicts the basis for the propagation delay analysis. The measurement results are verified by the mathematical model of expression 4.3. The 1 step overdrive limitation is signified by a propagation delay of  $t_p = 0.6215 \mu s$ .

This statement was claimed referred to the derivation of the propagation delay of a comparator. Based on the predictive behavior of a mathematical expression, the examined propagation delay approximation can be verified. With this regard further assumptions needs to be defined in order to derive the propagation delay of the feedback configuration by equation 4.3. Therefore, known parameter are determined in advance. Thus, the comparator output level is related to  $V_{\text{max}} = 1.8 V$ , which implies a single reference step magnitude of  $\approx 7.05 \text{ mV}$  for an 8 bit system. In addition, another assumption is confirmed by the measurements. So the results in figure 5.2(b) verify, that the LVDS driver of the FPGA is able to amplify an input difference of a single reference step magnitude. This confirmation implies that the driver which is applied as comparator provides an amplification of a single step until the limit of the cutoff frequency ( $\omega_c$ ) as derived for the equation. In this terms reciprocal of the cutoff frequency is defined as cutoff delay ( $t_c$ ). At the cutoff delay limitation, the propagation delay is equal to the cutoff delay ( $t_p = T\&C$ ) under the constraint of a single reference step magnitude ( $V_{\text{in}}$ ). Referred to these considerations equation 4.3 can be rearranged to expression 5.1 and a minimum required DC gain ( $A_v(0)$ ) can be calculated to  $\approx 46 \text{ dB}$ . The estimation of the DC gain, in turn, can be used to determine the cutoff frequency ( $\omega_c$ ) by rearranging equation 4.3

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again. Thus, in order to minimize the error which is introduced by the measurement inaccuracy related to the step quantization, the relation for the minimum propagation delay (i.e.  $t_p = f_{\text{clk}}^{-1} = 25 \text{ MHz}$ ) depicts the most accurate representation. In application of expression 5.2, the approximated cutoff frequency for the feedback configuration results in 1.632 MHz, which corresponds to a delay of  $t_p = 0.612 \mu\text{s}$ . Based on the fact, that the cutoff frequency depicts a physical limitation, the approximation can be applied to 4.3 as a constant. Therefore, the resulting course of the propagation delay is calculated in relationship to the number of overdrive/underdrive steps as absolute value. Indeed, the approximation of the propagation delay course reveals the measurement results illustrated in figure 5.2(a). Although, the result is not exact, it can be demonstrated, that an estimation of the propagation delay is possible by the measurement of the number of overdrive/underdrive steps. Thus, even the approximation provides a guideline for the design of an ADC where the LVDS driver of the FPGA is used as analog comparator. Indeed, the calculated cutoff frequency defines the maximum possible step generation rate ( $f_{\text{clk}}$ ) to represent an accuracy of a single reference step which is related to the ADC resolution and thus a design limit for the SAR ADC topology. Nevertheless, due to the implementation purpose on the FPGA an exact clock generation represented as division of the clock tree reference is more applicable. Therefore, the applied clock frequency for the step generation is related to  $f_{\text{clk}} = 1 \text{ MHz}$  as examined in figure 5.2(b). But the approximation of the dispersion effect applies as guideline for the design of the modified tracking schemes are presented in chapter 3.

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### DC gain assumption based on measurement results:

Assumption:  $t_p = t_c$  for a single reference step  $V_{in} = 7.05 \text{ mV}$

$$A_v(0) = \frac{V_{\max}}{2 V_{in} \cdot [1 - e^{-t_p/t_c}]} = \frac{V_{\max}}{2 V_{in} \cdot [1 - e^{-1}]} \approx 201.7 \rightarrow \approx 46 \text{ dB} \quad (5.1)$$

### Delay limitation based on cutoff frequency:

Assumption: constant cutoff frequency ( $\omega_c$ ) for any delay  $t_d = f_{\text{clk}}^{-1}$

$$\omega_c = f_{\text{clk}} \cdot \ln \left[ \left( 1 - \frac{V_{\max}}{2 A_v(0) V_{in}} \right)^{-1} \right] \approx 1.632 \text{ MHz} \Leftrightarrow t_c = 0.612 \mu\text{s} \quad (5.2)$$

## 5.2 Measurement Results of the Reconfigurable Implementation

Common ADC topologies were implemented on the reconfigurable hardware constitution presented in figure 5.1 in order to demonstrate the proof of concept. Therefore, a Digital Ramp ADC (Counter ADC), a SAR ADC and a Tracking ADC were evaluated. Each topology has specific characteristics that are decisive about the area of application [56]. A hardware limitation is set by the 8 bit scaling network. The Digital Ramp ADC generates a ramp by counting up and thus converts the signal by the level crossing of the input signal. The major drawback of this kind of ADC is depicted by the constitution of the conversion rate ( $f_{\text{conv}}$ ), since the ramp generation requires a reset to the initial value for every new conversion cycle. This leads to the fact, that the conversion time depends on the duration of the level crossing which introduces an additional delay to the actual propagation delay of the feedback configuration. The additional delay is relatively constituted to the analog input signal which implies a non-uniform sampled signal. The Tracking ADC enhances this behavior due to the renouncing of the reset by tracking the input signal. Ideally, it provides a valid conversion for every iteration and is considered as the fastest conversion scheme beside Flash-ADCs. Also the respective conversion cycle of the Tracking ADC is

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relatively constituted to the analog input signal by the sampling scheme as described in chapter 3. Thus the Tracking ADC also generates a non-uniform conversion. Both of the mentioned ADC topologies are counter based schemes, which generates ramps. The slope of these ramps is decisive about the absolute input bandwidth as derived in section 2.1.1. Thereby, they are bandwidth limited and can not be considered as Nyquist rate ADCs as for uniformly sampled conversion schemes [3]. A common Nyquist rate ADC is given by the SAR topology. In comparison to the introduced ADC schemes the absolute bandwidth, which is described by the Nyquist rate, is much higher, but the conversion rate is way slower than the conversion rate of the Tracking ADC. But as demonstrated in section 3.1.2 the higher conversion rate of the tracking scheme provides a higher effective resolution for a wide range of the absolute bandwidth of the Tracking ADC compared to SAR ADC.

Compared to the SAR implementation, the Tracking ADC implementation shows its major disadvantage regarding bandwidth limitation but offers its major advantage regarding conversion speed and effective resolution within its respective bandwidth. The reconfigurable ADC design allows the possibility to adjust the sampling scheme of the Tracking ADC by programming. This also means that it allows to generate a reference signal, which is not related to a classical approach. Rather, it can be described as an algorithmic approach. Chapter 3 proposes sampling methods for the expansion of the bandwidth and the improvement of the effective resolution by algorithmic modifications. In consideration of the tracking scheme, it turns out, that increasing the reference step generation rate applied by the clock frequency ( $f_{\text{clk}}$ ) and maintaining the conversion rate ( $f_{\text{conv}}$ ) of the feedback configuration is a simple solution. The resulting sample scheme is still tracking, but instead of generating a signal that oscillates by one bit within a comparator sample, it generates a triangular reference based on several bit within a conversion cycle (Fig. 3.3). In this terms, the tracking algorithm is extended by a synchronization system between the comparator sample and the faster reference. The improvement ability of the proposed design is illustrated in figure 3.6 by the comparison between the conventional tracking scheme and the proposed approach. In addition, an algorithmic enhancement scheme for the effective resolution is proposed in section 3.1.2. Since the effective resolution is directly related to the conversion rate as predicted by the general SNR equation (Eqn. 2.57), the reduction of the average propagation delay within the feedback loop increases the conversion rate ( $f_{\text{conv}}$ ) and improves the signal-to-noise ratio. So, the effective resolution is improved as well. Due to the fact, that the resulting triangular sampling scheme requires the return to the opposite direction of the analog input signal the conversion delay is twice the possible delay. Therefore, the modified approach proposes a jump to the mean of consecutive conversion cycles in order to reduce the additional delay introduced by the triangular sampling scheme. Thus, the delay reduction improves the effective

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resolution as well as the bandwidth limitation. The approaches proposed in chapter 3 were predicted by the application of the extended mathematical model of the general SNR equation for non-uniform sampling (Eqn. 3.8).

The verification for the predicted behavior of algorithmic modifications is based on implementing the algorithmic configurations on the reconfigurable ADC topology. In these terms, the implementation represents a functional FPGA prototype for algorithm analysis. The investigation of the implemented designs considers the dynamic ADC behavior based on the signal-to-noise ratio course within the absolute bandwidth. Additionally, the static ADC behavior analysis regarding the differential non-linearity (DNL) and integral non-linearity (INL) of the measurement results is performed. Thus, the proposed algorithmic approaches can be examined for real-world processing and evaluated regarding the applicability. A comparison between modified tracking schemes and common ADC architectures based on Counter ADC, SAR ADC, and Tracking ADC provides a basis for the validation process.

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### 5.2.1 Evaluation of Common ADC Architectures

The common ADC architectures based on Digital Ramp ADC (Counter ADC), SAR ADC and Tracking ADC are implemented on the FPGA of the experimental setup as illustrated in figure 5.1(b). In order to demonstrate the applicability of a general purpose ADC, the algorithmic behavior of the FPGA is configured by programming. The concept implements as a multi topology system that includes the respective ADC topology. Based on the desired test setup, the associated conversion scheme can be selected by external soft switches. The analog input signal is provided by an external signal generator which is constituted in terms of accuracy corresponding to the ADC, thus that the analog input signal has a resolution above the 8 bit resolution of the ADC. The global reference clock is generated on the Genesys 2 development board where the FPGA is located. The step generation rate for the ADC architectures is derived from this clock.

Based on the propagation delay analysis for the LVDS driver which is used as comparator as explained in section 5.1.1, the step generation rate for the ADC architectures was discovered. Since each of the basic topologies is constraint to detect the least-significant-bit of the ADC configuration, the corresponding propagation delay for a linear conversion is evaluated to  $1 \mu s$  as illustrated in figure 5.2(b). Based on the fact, that the overdrive and the underdrive magnitude is equal for this configuration, a validation of a conversion cycle is established within a delay of  $2 \mu s$ . Therefore, it corresponds to a conversion rate of  $f_{\text{conv}} = 500 \text{ kHz}$  for a single conversion cycle. Under the contemplation of a step generation rate of  $f_{\text{clk}} = 1 \text{ MHz}$  for each ADC architecture the topology related average conversion rate results. Therefore, the Tracking ADC implementation provides an average conversion rate for every comparator detection, thus that  $f_{\text{convTRACK}} = 500 \text{ kHz}$ . The conversion rate of the SAR ADC implementation is based on the aspect of a multiple number of comparator detections related to the ADC resolution. In consideration of the 8 bit representation by the R2R voltage scaling network, the conversion rate results from 8 comparisons and an additional validation step. Thus the conversion rate of  $f_{\text{convSAR}} = 500 \text{ kHz}/9 \approx 55.6 \text{ kHz}$  results. Based on the non-uniform sampling behavior of the Counter ADC implementation, the average conversion rate is approximated by the occurrence of the respective intersections. Due to the proportionality condition between the number of magnitude steps and the number of time steps of the counter generated ramp, the average number of reference steps corresponds to the mean of the conversion time. In assumption of the ideal case, each step number occurs once, thus that an equal distribution results in the procedure. Statistically, the arithmetic mean value based on the sum of each individual cycle is representative. Thus, a 8 bit Counter ADC implementation reveals an average conversion rate of  $f_{\text{convCOUNT}} = 500 \text{ kHz}/128 \approx 3.9 \text{ kHz}$ .

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Based on the definition of the resolution ( $N$ ), the reference step generation rate ( $f_{\text{clk}}$ ) and the respective conversion rates ( $f_{\text{conv}}$ ), the absolute bandwidth ( $f_{\text{max}_{\text{bw}}}$ ) of each topology can be determined. In contemplation of the SAR ADC, the absolute bandwidth limitation is restricted to the Nyquist criterion, which claims that the largest bandwidth that can be sampled without aliasing is constraint to the half of the conversion rate. Since the specified conversion rate for the SAR implementation is approximated to 55.6 kHz, the absolute bandwidth results in  $f_{\text{sar}_{\text{bw}}} \approx 27.8$  kHz.

The Counter ADC and the Tracking ADC implementation are characterized by a non-uniform sampling behavior. Nevertheless, as derived in chapter 2 the conversion ability is restricted to the maximum possible slope of the reference signal. Based on this consideration, the absolute bandwidth limitation was derived for equation 2.11. Due to the validation property of the Tracking ADC an additional conversion step is foreseen, thus that the slope generation corresponds to the conversion rate. Based on equation 2.11, the absolute bandwidth for the Tracking ADC results in  $f_{\text{track}_{\text{bw}}} \approx 1.46$  kHz.

In comparison to the Tracking ADC the bandwidth of the Counter ADC is also limited by the reference signal slope, but no validation cycle is necessary. Therefore, the slope of the reference signal is constituted by the step generation rate ( $f_{\text{clk}} = 1$  MHz). Applying equation 2.11, thus results in an absolute bandwidth limitation for the Counter ADC of  $f_{\text{count}_{\text{bw}}} \approx 2.93$  kHz.

Table 5.1 summarizes the parametrization of the applied ADC architectures. In addition, the derived conversion rates and bandwidth limitations are depicted in order to compare the ADC implementations. Thus, the SAR ADC provides the highest absolute bandwidth, but the Tracking ADC provides the highest conversion rate which is one representative character for the effective resolution. The Counter ADC provides the lowest conversion rate, but doubles the bandwidth limitation of the Tracking ADC by the renouncing of the validation step.

Related to the configuration parameters depicted in table 5.1, the common ADC architectures are evaluated. Therefore, the analog input signal frequency is iterated in order to illustrate the entire bandwidth property of the respective ADC. So, the converted digital output streams of the ADCs are investigated referred to the spectrum by a MATLAB analysis comparable to the evaluation of the simulation model described in section 2.1.4. Thus, the fast-Fourier transform is representative for the signal-to-noise ratio which is the basic character for the determination of the effective resolution. Related to the evaluation of the individual conversion outputs by an frequency sweep of the input, the signal-to-noise ratio course is determined. As a side note, the signal-to-noise-and-distortion (SINAD) ratio was examined in addition, but reveals comparable results. Thus, it can be concluded, that the

Table 5.1: Parametrization summary of common ADC Architectures

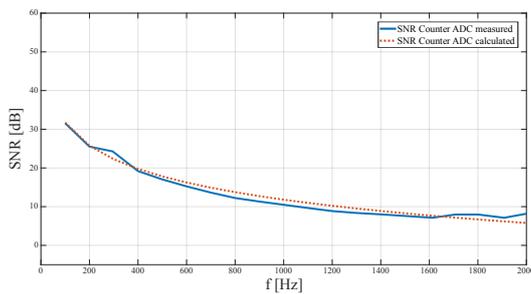
ADC Architecture	ADC resolution (N)	Reference step generation rate ( $f_{\text{ref}}$ )	Conversion rate ( $f_{\text{conv}}$ )	Bandwidth limitation ( $f_{\text{max}_{\text{bw}}}$ )
SAR ADC	8	0.5 MHz	$\approx 55.6$ kHz	$\approx 27.8$ kHz
Counter ADC	8	0.5 MHz	$\approx 3.9$ kHz	$\approx 2.93$ kHz
Tracking ADC	8	0.5 MHz	$\approx 500$ kHz	$\approx 1.46$ kHz

influence of signal distortions is low. However, in order to provide a basis for the equation comparison, the SNR is more meaningful. Thereby, the signal-to-noise ratio defines the dynamic property of the respective ADC. Related to the static performance, a linearity analysis was instrumented. The sine wave representation of the input signal enables the determination of the differential non-linearity (DNL) and the integral non-linearity (INL) by the histogram method described in citation [57].

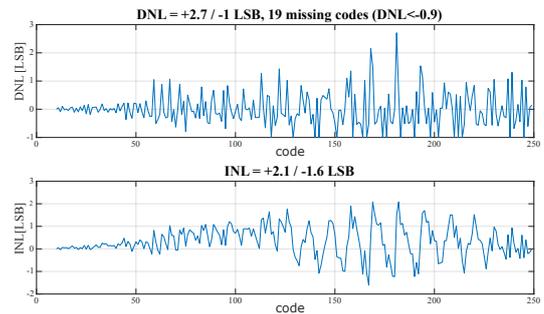
In order to validate the set of mathematical models derived in chapter 2 for the determination of the signal-to-noise ratio, the measured ADC results can be compared with the predicted results by the equations. Therefore, the corresponding SNR courses were calculated based on the ADC parametrization depicted in table 5.1. In consideration of the respective mathematical model, the sampling behavior of the implemented ADCs defines the selection. Thus, the model for the calculation of the uniformly sampled signals by equation 2.23 is representative for the SAR ADC. It was derived by the hypothesis, that if at least two intersections between the input signal slope and the reference signal slope exists, it will be in the interval  $[0, T_{\text{sig}}]$ . If it is not existing the effective resolution is less than "1-bit" and the input signal frequency is not within the ADC bandwidth. In course of the evaluation, the hypothesis was approved by the MATLAB simulation model. The signal-to-noise ratio course of the conventional Tracking ADC, in turn, is considered for a non-uniformly sampled signal, where the individual noise portions by varying level-crossing moments needs to be taken into account. Therefore, expression 2.39 was derived which claims the hypothesis, that if there is an intersection between the input signal and the reference signal at a sample time ( $T_{\text{samp}}$ ) and under the constraint, that the step generation time  $T_{\text{ref}} = T_{\text{samp}}$ , the intersection can be located at the input signal moment of the sampling time. The total noise is based on the sum of the noise portions for a

variety of sampling times. Thereby, this expression defines a simplification of the general SNR expression by the consideration of a conversion rate which is equal to the reference step validation of a tracking scheme. Also, the hypothesis was validated by the MATLAB simulation model and can be transferred to a validation related to the measurement system.

In comparison to the Tracking ADC, also the Counter ADC exhibits a non-uniform sampling behavior. But due to the fact, that there is a level crossing intersection related to the hypothesis of an existing slope within the interval  $[0, T_{\text{sig}}]$  equation 2.23 is representative. Although, the expression determines the uniform sampling, the result is comparable, because there is a single intersection moment for the counter scheme as for the SAR scheme, where both are reseted. Indeed, the Counter ADC exhibits varying conversion times, but the average conversion time for equally distributed samples is representative. Thus, compared to the Tracking ADC, the Counter ADC scheme does not detect interdependent reference signals related to the switching moments of the comparator detection. Rather, it generates always the same reference ramp for each repetitive conversion step, but the conversion result varies with the analog input signal. Therefore, the conversion scheme is similar to uniform sampling schemes which does not change the reference signal relative to the analog signal.



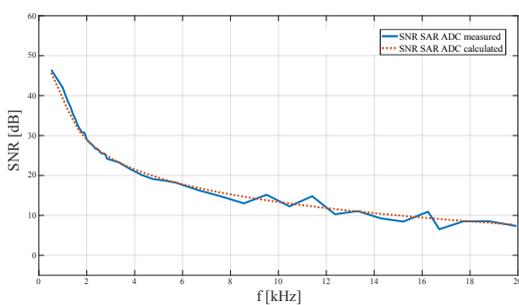
(a) Mathematical model verified by the SNR course of the Counter ADC.



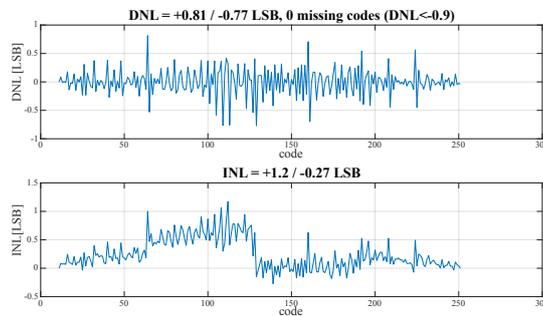
(b) DNL and INL measurement of the Counter ADC.

Figure 5.3: Counter ADC performance measurement. Dynamic performance (SNR) measurement results in (a) verified by equation 2.25. Measurement results of the static performance (DNL, INL). Parameter: resolution ( $N = 8$  bit), step generation rate ( $f_{\text{clk}} = 1$  MHz) and conversion rate ( $f_{\text{conv}} = f_{\text{clk}}/2^{N-2} = 500$  kHz/128  $\approx 3.9$  kHz).

The measurement result for the SNR course of the Counter ADC is illustrated in figure 5.3(a). It demonstrates that the assumption of a uniformly sampled signal is confirmed, since the measurement results and the calculated results agree. Besides the agreement, the measured result as well as the calculated result illustrate the strong dependence of the conversion rate which determines the number of successful samples. Due to the reset aspect of the Counter ADC, the effective resolution is reduced by approximately 2 bit within the considered input frequency range compared to the possible ADC resolution of 8 bit. This effect is confirmed by the DNL and INL analysis of the counter ADC in figure 5.3(b). A large number of conversion steps is missing which affects the linearity of the counter ADC system.



(a) Mathematical model verified by the SNR course of the SAR ADC.



(b) DNL and INL measurement of the SAR ADC.

Figure 5.4: SAR ADC performance measurement. Dynamic performance (SNR) measurement results in (a) verified by equation 2.25. Measurement results of the static performance (DNL, INL). Parameter: resolution ( $N = 8$  bit), step generation rate ( $f_{\text{clk}} = 1$  MHz) and conversion rate ( $f_{\text{conv}} = f_{\text{clk}} / (N + 1) = 500 \text{ kHz} / 9 \approx 55.6 \text{ kHz}$ ).

The signal-to-noise ratio course of the SAR ADC was also calculated by the uniform sampling equation. The measurement results verify the mathematical model as depicted in figure 5.4(a). But in this case the higher conversion rate (Tab: 5.1) exhibits the higher effective resolution compared to the Counter ADC. As specified for a uniformly sampled ADC, the absolute bandwidth is defined by the half of the conversion rate which is demonstrated by the wide input range compared to the Counter ADC. Also the static performance of the SAR ADC reveals, that the conversion exhibits no missing codes as illustrated in figure 5.4(b). Thus, the differential non-linearity (DNL) depicts a deviation below 1 LSB for the

restricted range of the 8 bit representation. Indeed, due to the intersection property of the physical sample scheme the full-scale scope can not be detected, as described in section 5.1.1. The integral non-linearity (INL) exhibits a maximum deviation of 1.2 LSB, which is related to the fact, that an implementation of the SAR topology requires a Sample&Hold device. However, the general purpose ADC setup proposed in figure 5.1 is not equipped with a Sample&hold unit.

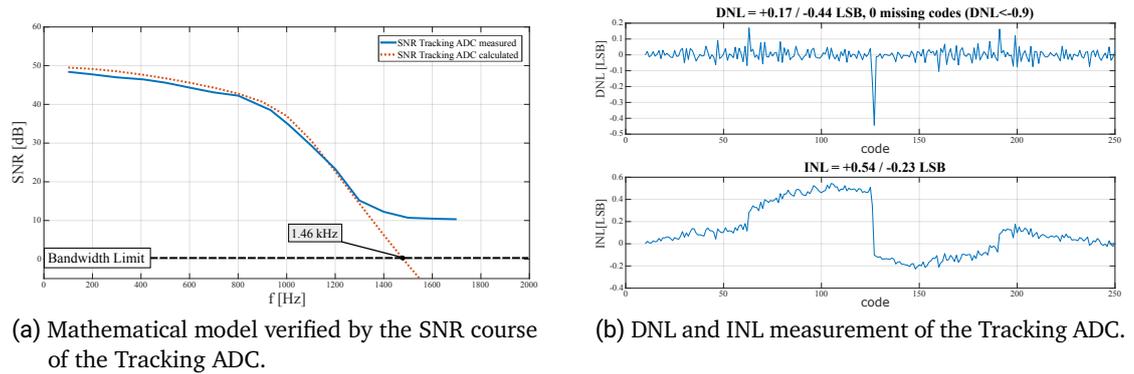


Figure 5.5: Tracking ADC performance measurement. Dynamic performance (SNR) measurement results in (a) verified by equation 2.39. Measurement results of the static performance (DNL, INL). Parameter: resolution ( $N = 8$  bit), step generation rate ( $f_{clk} = 1$  MHz) and conversion rate ( $f_{conv} = f_{clk}/2 = 500$  kHz).

The measured signal-to-noise ratio course of the Tracking ADC implementation is illustrated in figure 5.5(a). Thereby, the mathematical model is verified by the measurement results. The parametrization for the implementation of the experimental setup as well as the parametrization for the mathematical model is based on the determined characterization in table 5.1. In comparison to the application of the uniform sampled SNR model for the SAR ADC and the Counter ADC, the mathematical SNR course derivation for the Tracking ADC is considered by equation 2.39. Due to the fact, that a tracking scheme is based on the resolution related step combinations, the conversion scheme is non-uniform. Referred to the aspect, that the conversion rate corresponds to step generation rate (including the validation step), the general SNR expression is applied by its simplified version which was derived in section 2.3.1. In comparison of the mathematical model and the experimental design, the results exhibit a high degree of agreement.

Based on the Tracking ADC ability to detect an signal intersection for every reference step in the ideal case and the fact, that the reference signal develops relative to the analog input signal, a Sample&Hold unit can be renounced. Therefore, the tracking scheme does not experience a postponement to the analog signal as for the SAR ADC which requires a multiple of conversion cycle for a constant input level. This advantage is illustrated by the linearity analysis of the Tracking ADC. Thereby, the deviations for the DNL and the INL are less than 1 LSB which demonstrates a high linearity.

Figure 5.6 compares the experimental measurement results of the common ADC implementations. As derived in section 3.1.2, the SAR ADC has a wide bandwidth compared to the Tracking ADC, but the Tracking ADC has a higher effective resolution within the respective bandwidth. Related to the mathematical verification the Counter ADC and the SAR ADC exhibit a comparable SNR behavior. The resulting SNR courses of the respective ADC topologies are comparable with the calculated SNR behavior predicted in figure 3.9.

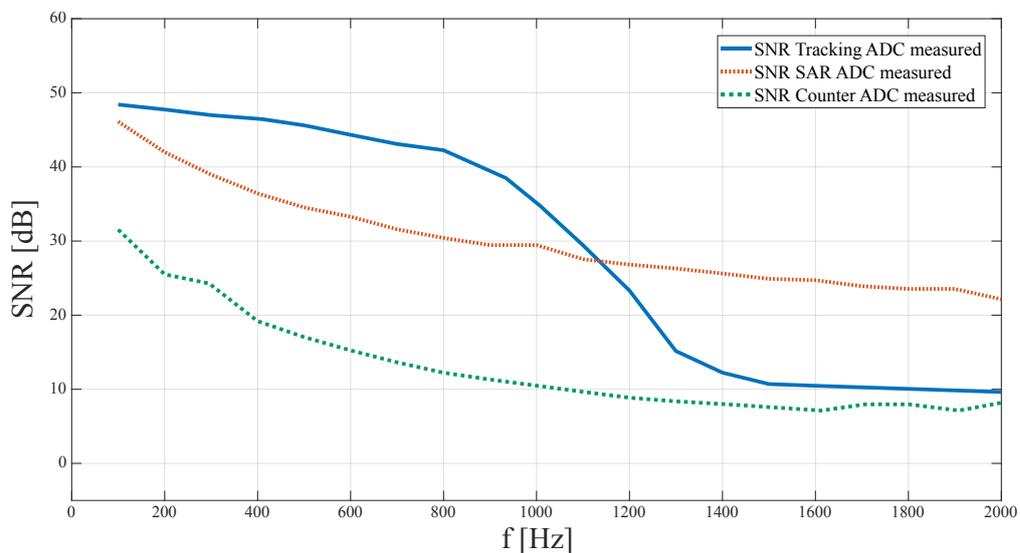


Figure 5.6: Comparison of the measured signal-to-noise ratio courses of the implemented basic ADC topologies (Counter ADC, SAR ADC, Tracking ADC). As derived in section 3.1.2, the SAR ADC has a wide bandwidth compared to the Tracking ADC, but the Tracking ADC has a higher effective resolution within the respective bandwidth. Besides, the Counter ADC has the least effective resolution due to the return to zero state, which causes missing conversion steps.

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## 5.2.2 Evaluation of Algorithmic Enhanced ADC Architectures

The reconfigurable ADC design allows the possibility to adjust the sampling scheme of the Tracking ADC by programming. This also means that it allows to generate a reference signal, which is not related to a classical approach. Rather, it can be described as an algorithmic approach. The evaluation of the algorithmic enhanced ADC architectures proposed in chapter 3 are implemented on the FPGA within the experimental setup as illustrated in figure 5.1(b). As postulated in section 3.1.1 and section 3.1.2 the modifications of the tracking scheme should be able to enhance the conversion property of the ADC. Thereby, the postulated enhancement ability concerns to the bandwidth expansion of the conventional tracking scheme and the enhancement of the effective resolution within the bandwidth expansion. The hypothesis, to enhance the ADC properties was derived by the extended general signal-to-noise ratio equation (Eqn: 3.8). It separates the consideration of the conversion noise property from the reference noise property in order to derive additional degrees of freedom for the algorithmic design. Thus, the design parameter based on the step generation rate ( $f_{clk}$ ), the conversion rate ( $f_{conv}$ ), the amplitude resolution ( $N_{amp}$ ) and the temporal resolution of the reference ( $\vec{N}_{ref}(k)$ ) reveal as degrees of freedom. In this terms, general design methods are proposed in chapter 3 to develop a variety of new sampling algorithms. In the scope of the experimental design for the general purpose ADC, the bandwidth extension BEA and the effective resolution enhancement algorithm REA are implemented and evaluated. In the following, the implementation of the BE-Algorithm defines the ASGA ADC referred to an acceleration of the reference step compared to the conventional Tracking ADC approach. In the same sense, the RE-Algorithm defines the Jump-Accelerated-Step-Generation-Algorithm (RE-Algorithm) (JASGA) ADC referred to the induction of jumps. In order to validate the postulated equation set, the calculated results verify the measurement results in terms of the signal-to-noise ratio course. In addition, the linearity of the proposed tracking schemes is evaluated based on DNL and INL.

As previously discussed, the bandwidth limitation is restricted by the maximum slope of the reference signal. Thus, the slope of the reference signal was increased by accelerating the reference clock frequency. In this terms, the conversion rate develops as a combination of the feedback delay and the algorithmic delay which is introduced by the return to the opposite orientation of the analog signal (section 3.1.2). The resulting tracking scheme generates a triangular staircase function, which develops within the conversion cycle. Thus the detection of a conversion step is based on the magnitude of multiple reference steps instead of a single step for the conventional tracking scheme. This implies that the relative reference signal slope is increased, which improves the detection capability for higher input signal slopes and thus expands the bandwidth.

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As investigated in section 5.1, the average conversion time is related to the dispersion effect of the feedback configuration. This implies, that the overdrive/underdrive of the input signal by the staircase function causes a shorter feedback delay. This dependency consequences, that the average conversion rate is accelerated. In order to approximate the reduction of the feedback delay, figure 5.2(a) is informative about the corresponding propagation delay in relation to the number of overdrive/underdrive steps. The relation was established based on the applied step generation rate for a Counter ADC, thus the expected number of overdrive/underdrive steps can be derived by the duration of the increased step generation rate. Related to the FPGA investigation of the LVDS driver, the transfer to the functionality of an analog comparator reveals a linear characteristic for a clock frequency of  $f_{\text{clk}} = 12.5 \text{ MHz}$ . The transfer to the ADC design implies a step generation rate of  $f_{\text{ref}} = 6.25 \text{ MHz}$ . Referred to figure 5.2(a) the step generation rate corresponds to the dispersion step number of  $N_{\text{disp}} \approx 2.75$  by a duration of  $t_d = f_{\text{ref}}^{-1} = 0.16 \mu\text{s}$ . Indeed, the exact value can also be determined by the propagation delay equation and the assumptions made in section 5.1.1. As there is the proportionality relation of the triangular function, the conversion time can be expressed by the reciprocal of the step generation rate multiplied by the number of steps. Due to the fact, that the triangular reference signal develops relative to the analog input signal, the number of overdrive/underdrive steps varies with the input signal as illustrated in the previous chapter 3 for the triangular reference scheme by figure 3.4. On the other hand, the measured overdrive/underdrive steps are related to a constant input level. Thus, it is expectable, that the magnitude of steps varies with the relationship between the triangular reference signal and the analog input signal. Therefore, the previous defined dispersion effect needs to be normalized to the development of the reference signal.

Referred to the fact, that the input signal is sinusoidal and the reference signal develops triangular, the normalization between these signals is related to the RMS value of the respective signal. The relationship of the RMS values for the composition between the input signal and the reference signal was already derived in section 2.1.2 and defined as crest ratio by the factor of  $\Gamma_{\text{crest}} = \sqrt{3/2}$ . Thereby, the RMS value of  $\text{RMS}_{\text{sin}} = \sqrt{2}$  is representative for the sinusoidal input signal and the RMS value of  $\text{RMS}_{\text{tri}} = \sqrt{3}$  is representative for the triangular reference signal. The RMS value for the measured DC signal, in turn, is defined by  $\text{RMS}_{\text{DC}} = 1$ . Thus, the normalization between the measured constant input and the developing reference signal reveals in the ratio between the crest ratio and the RMS value for the DC signal, thus that  $\text{RMS}_{\text{DC}}/\Gamma_{\text{crest}} = \sqrt{2/3}$  results. Since the measured number of constant overdrive/underdrive steps ( $N_{\text{disp}}$ ) represents the  $\text{RMS}_{\text{DC}}$  value, the normalization results in the division of the steps by the crest ratio to

$N_{\text{disp}}/\Gamma_{\text{crest}}$ . Thus, based on the statistically determined step normalization, the statistical conversion rate ( $f_{\text{conv}_{\text{tri}}}$ ) under the influence of the dispersion effect is defined by equation 5.3. Thereby, the effect is considered for the level crossing in both orientations relative to the analog input signal. This implies, that the number of normalization steps must be considered for the overdrive as well as for the underdrive. Since the measurements validated an equality for both deviations the number of steps is considered twice.

**Dispersion effect normalization by the crest ratio:**

$$f_{\text{conv}_{\text{tri}}} = \Gamma_{\text{crest}} \cdot \frac{f_{\text{ref}}}{2 N_{\text{disp}}} \Leftrightarrow \sqrt{\frac{3}{2}} \cdot \frac{6.25 \text{ MHz}}{2 \cdot 2.75} \approx 1.39 \text{ MHz} \quad (5.3)$$

The second algorithmic approach which is implemented on the experimental setup concerns the enhancement of the effective resolution for the bandwidth extended approach. The method to enhance the effective resolution within the bandwidth was proposed in section 3.1.2. The effect of returning to the opposite direction by the triangular reference signal is considered. It is developed within a conversion cycle by the acceleration of the reference step generation rate. Due to the return, the duration for the level crossing is extended which in turn extends the conversion time. As derived, the effective resolution depends on the conversion rate which is the reciprocal of the conversion time. Thus, the higher the conversion rate, the higher the effective resolution. Therefore, the effect of extending the conversion duration can be avoided by the skipping of the reference steps that are required for the level crossing to the opposite direction. This approach causes the conversion time to reduce due to the jump to the mean value of consecutive samples. Thereby, consecutive samples are constituted by the developing maximum and minimum of the reference signal (section 3.1.2). Indeed, the method of jumping reduces the conversion time by the algorithmic modification on the one hand, but on the other hand a jump of several steps implies that the dispersion effect reduces the conversion time by the physical properties in addition. Therefore, the approximation of the affected conversion rate also needs to be considered for this method.

The procedure for the conversion rate approximation concerns similar to the previous derivation by the crest ratio. However, the developing reference signal addresses another dependency due to the modified sampling scheme which is illustrated in figure 3.7(b).

Based on the introduction of jumps related to the specific comparator detection, the developing of the reference signal depends on the jump and the subsequent triangular property. In comparison, the triangular reference scheme depends on the triangular property which develops in relationship to the analog input signal during the returning to the opposite direction. In consideration of a continuous time input signal, this implies, that the time for the level crossing depends on the triangular reference signal as well as on the input signal (sinusoidal). Therefore, the time for the return state defines the dependency to the input signal. Contrary, the reference signal, which is constituted by jumps, renounces the return state due to skipping. In a broader sense, this implies that the dependency to the analog input signal is skipped by the jumps. However, the dispersion effect for the triangular reference scheme remains. Thus, the normalization by the crest ratio demands for an additional modification.

As described, the crest ratio is defined by the ratio of the RMS value for the sinusoidal signal and the RMS value for the triangular signal. Since the dependency to the input signal is skipped by jumps, the normalization by the RMS ratio is modified in relation to the jump instead of the sinusoidal signal. The jump, in turn, can be considered as a square wave application. Thus, the RMS value of the jump results in  $\text{RMS}_{\text{JUMP}} = 1$ . Based on the composition between the jump and the triangular signal, the modified crest ratio results in  $\Gamma_{\text{crest}_{\text{mod}}} = \sqrt{3/1}$ . Again, the transfer between the measured DC level for the examination of the dispersion effect (figure 5.2(a)) describes the adjustment factor. It results in the normalization ratio of  $\text{RMS}_{\text{DC}}/\Gamma_{\text{crest}_{\text{mod}}} = \sqrt{1/3}$  for the adjustment of the measured overdrive/underdrive steps ( $N_{\text{disp}}$ ). In contemplation to the afore examined step number ( $N_{\text{disp}} = 2.75$ ) for the step generation rate of  $f_{\text{ref}} = 6.25$  MHz equation 5.4 reveals the corresponding conversion rate result ( $f_{\text{conv}_{\text{jump}}} \approx 1.97$  MHz).

**Dispersion effect normalization by the modified crest ratio:**

$$f_{\text{conv}_{\text{jump}}} = \Gamma_{\text{crest}_{\text{mod}}} \cdot \frac{f_{\text{ref}}}{2 N_{\text{disp}}} \Leftrightarrow \sqrt{3} \cdot \frac{6.25 \text{ MHz}}{2 \cdot 2.75} \approx 1.97 \text{ MHz} \quad (5.4)$$

Table 5.2 summarizes the parametrization for the algorithmic ADC architectures based on the resolution, the step generation rate ( $f_{\text{ref}}$ ) and the resulting conversion rate ( $f_{\text{conv}}$ ) which is affected by the dispersion effect. The parameterization is applied to the imple-

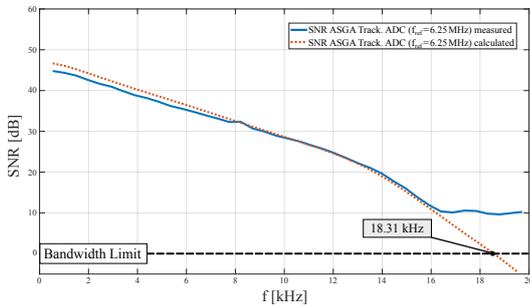
mented algorithms of the experimental setup in figure 5.1. Therefore, the measurement results are generated by a clock frequency of  $f_{\text{clk}} = 12.5$  MHz which implies the step generation of  $f_{\text{ref}} = 6.25$  MHz. The resolution is again restricted to 8 bit by the R2R scaling network. In the further course, the determined conversion rate is applied to the extended general SNR expression (Eqn: 3.8) in order to calculate the SNR behavior of the proposed algorithm. Thus, the measurement results of the physical implementation verify the mathematical model.

Table 5.2: Parametrization summary of algorithmic ADC Architectures

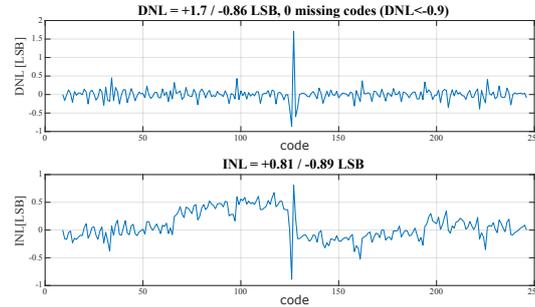
ADC Architecture	ADC resolution (N)	Reference step generation rate ( $f_{\text{ref}}$ )	Conversion rate ( $f_{\text{conv}}$ )	Bandwidth limitation ( $f_{\text{max}_{\text{bw}}}$ )
Bandwidth extension ADC	8	6.25 MHz	$\approx 1.39$ MHz	$\approx 18.31$ kHz
Resolution enhanced ADC	8	6.25 MHz	$\approx 1.97$ MHz	$\approx 18.31$ kHz

The measurement results for the SNR course of the bandwidth extension method (ASGA ADC) is illustrated in figure 5.7(a). It demonstrates a high degree of correspondence between the mathematical SNR model and the measured SNR results. Thereby, the dispersion effect is considered due to the application of the derived conversion rate. This confirms the postulated assumptions related to the ability of the bandwidth extension property by accelerating the step generation rate. Related to the fact, that the exact intersection moment with the absolute bandwidth limitation can not be determined by a spectral analysis (section 2.1.4), the verified mathematical model is applied in order to determine the bandwidth limitation. Thus, the absolute bandwidth limitation results in  $f_{\text{max}_{\text{bw}}} \approx 18.31$  kHz. Compared to the conventional Tracking ADC approach in figure 5.5(a) the result corresponds to the multiplication factor of the step generation rate.

The static performance based on DNL and INL still indicates high linearity by an average deviation of below one LSB. Except for the switching moment of the Most-Significant-Bit (MSB), as illustrated in figure 5.7(b). Since each code sequence can be processed, incorrect detection of the reference signal causes non-linearity. In general, the MSB of a scaling network is the most critical sequential step since the charge/discharge process of the capacitive load (i.e., parasitic load) attains the maximum. This effect is observable for the common ADC architectures. However, in comparison to the conventional Tracking ADC, the accelerated step generation rate amplifies that error.



(a) Mathematical model verified by the SNR course of the Tracking ADC with increased step generation rate (ASGA Tracking ADC).



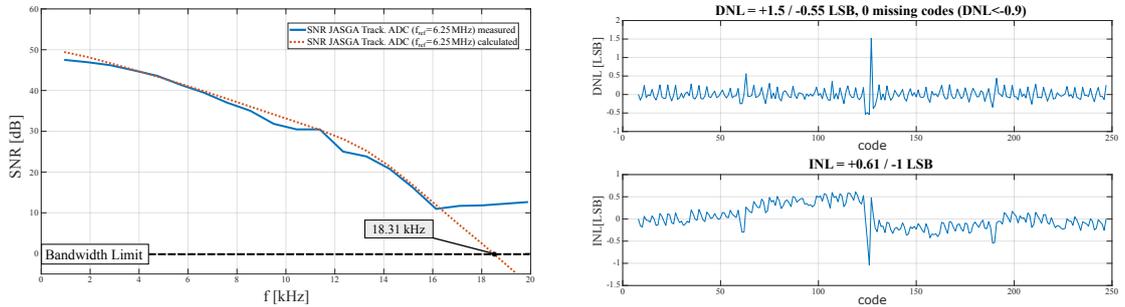
(b) DNL and INL measurement of the Tracking ADC with increased step generation rate (ASGA Tracking ADC).

Figure 5.7: Tracking ADC with increased step generation rate and jumps performance measurement. Dynamic performance (SNR) measurement results in (a) verify equation 2.39. Measurement results of the static performance (DNL, INL) in (b). Parameter: resolution ( $N = 8$  bit), step generation rate ( $f_{\text{ref}} = 6.25$  MHz) and dispersion affected conversion rate as described in section 3.1.2 ( $f_{\text{conv}} = \sqrt{3/2} f_{\text{ref}} / (2 N_{\text{disp}}) \approx 1.39$  MHz).

The application of jumps to the sampling scheme which is based on an accelerated step generation rate additionally demonstrates the applicability of the general signal-to-noise ratio expression (Eqn: 3.8). The mathematically postulated enhancement of the effective resolution under maintaining the extended bandwidth is verified by the measurement result of the SNR course as illustrated in figure 5.8(a). Also in this case, the mathematical model considers the conversion rate acceleration by the dispersion effect. Related to the static performance, the linearity deviations for the differential non-linearity and the integral non-linearity are comparable to the triangular approach.

Figure 5.9 compares the measurement results of the algorithmic enhanced tracking schemes with the previously examined SAR implementation. Based on the acceleration of the step generation rate, the input frequency range of a higher effective resolution can be explicitly extended compared to the conventional Tracking ADC. Thus, the frequency range of a higher resolution covers almost the entire bandwidth of the SAR ADC. This aspect applies to the bandwidth extension method (ASGA Tracking ADC) as well as especially for the resolution enhanced method (JASGA Tracking ADC).

The implementation of the Counter ADC also allows for an acceleration of the step generation rate (Counter Plus ADC), which improves the effective resolution due to a faster



(a) Mathematical model verified by the SNR course of the Tracking ADC with increased step generation rate and jumps (JASGA Tracking ADC).

(b) DNL and INL measurement of the Tracking ADC with increased step generation rate and jumps (JASGA Tracking ADC).

Figure 5.8: Tracking ADC with increased step generation rate and jumps performance measurement. Dynamic performance (SNR) measurement results in (a) verify equation 2.39. Measurement results of the static performance (DNL, INL) in (b). Parameter: resolution ( $N = 8$  bit), step generation rate ( $f_{ref} = 6.25$  MHz) and dispersion affected conversion rate as described in section 3.1.2 ( $f_{conv} = \sqrt{3} f_{ref} / (2 N_{disp}) \approx 1.97$  MHz).

detection. In comparison to the SAR implementation a corresponding SNR course reveals. This aspect demonstrates, that the assumed mathematical model for uniform sampling establishes an interdependence in relation to the reference signal detection as predicted in section 5.2.1 for the mathematical derivation of the Counter ADC. Especially, due to the acceleration of the reference step generation the influence of the dispersion effect is obvious, since the average conversion rate increases.

In conclusion, the measurement results confirm the mathematically postulated results of the algorithmic enhanced modeling. Thus, the extended general signal-to-noise ratio expression (Eqn: 3.8) is verified. Furthermore, the influence of the dispersion effect within the feedback configuration of the proposed experimental setup (Fig: 5.1) can be determined under the consideration of the measured deviation from a constant input signal. However, the measured deviation needs to be transferred to the sampling algorithm as derived for the modified conversion rate (Eqn: 5.3, 5.4). Based on these considerations, the calculated SNR courses correspond to the measurement results. The verification additionally confirms the assumption of the proposed dispersion measurement method (tracking and correction) in section 4.2.1. Thereby, it was postulated, that the dispersion

effect has to be measured by the applied sampling scheme in order to track the exact deviation of overdrive/underdrive steps under the influence of dispersion. Furthermore, the similarity between the SNR course of the Counter ADC for an accelerated step generation rate (accelerated Counter ADC) and the common SAR topology confirms the correspondence of the SNR equation for uniform sampling. In summary, the acceleration of the reference step generation beyond the feedback delay limitation is applicable to any ADC architecture, that allows a continuous time input signal. In case that a multiple of detections is necessary for a single level, the acceleration of the reference step generation is not applicable due to the deviations related of the dispersion effect. This aspect concerns to the SAR ADC architecture which is limited by the constance of the feedback delay.

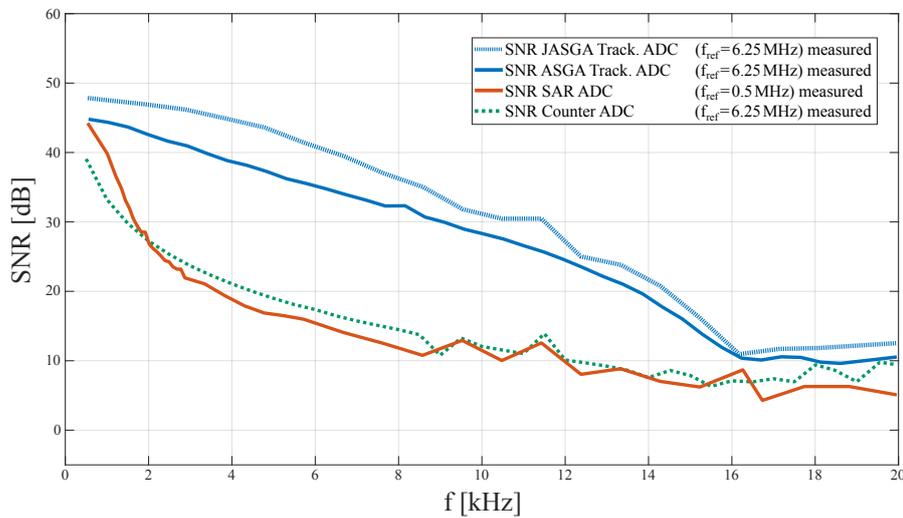


Figure 5.9: Comparison of the measured SNR courses of the advanced ADC topologies (Counter ADC, ASGA Tracking ADC, JASGA Tracking ADC) to the SAR ADC implementation. As derived in section 3.1, the bandwidth and the effective resolution of the Tracking ADC can be advanced by algorithmic rearranging and a higher step generation rate ( $f_{ref}$ ). The acceleration of the reference step generation is applicable to any ADC architecture that allows a continuous time input signal (demonstrated by accelerated Counter ADC).

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### 5.2.3 Cascaded Integrator Comb Structure for Post Processing

Digital post processing represents an important key feature for analog to digital conversion [58]. Further data processing provides the property of minimizing conversion errors by effective interpolation methods or to filter unwanted signal portions. The moving average filter is one of the most common approaches to provide digital post processing for FPGAs. The moving average filter can be implemented as a direct form FIR type. A simple structure is realized by the application of a series of delay elements, a summing unit and a divider element in the FPGA. In order to provide a high accuracy by division, floating point arithmetic needs to be applied, but increases the complexity of the system. Another possibility for implementing the moving average behavior is based on a recursive form by using a decimation filter. The Cascaded-Integrator-Comb (CIC) filter is a commonly used decimation filter. It consists of an integrator section and a comb section [53]. Exclusively addition and subtraction operations are required, which provide an efficient structure for the application of a reconfigurable DSP system on a FPGA. In general, CIC filter implement a sampling rate decrease which is defined as decimation or a sampling rate increase which is defined as interpolation. Thus, it is applied in modern signal processing systems where a sample rate conversion is necessary. Especially, in the area of oversampled analog-to-digital conversion like  $\Delta\Sigma$ -ADCs, the CIC structure is implemented as a decimator which decreases the sample rate. Therefore, the Performance of decimation for  $\Delta\Sigma$ -ADCs functions as down-sample and clock rate reduction on the one hand and the remove of the entire out-of-band signals and noise. As a result, the down sampling provides a higher effective resolution by filtering the higher frequency order quantization noise as cited in [59, 60].

The ability of down and up sampling of the CIC provides an important feature for digital signal processing, which especially applies to oversampling ADCs. But contrary to the functionality of decimation, the interpolation functionality is applied to the proposed conversion scheme of accelerating the step generation rate within the application of the general purpose ADC design. As derived, the tracking schemes reveal a non-uniform sampling behavior which is based on the varying conversion time due to the intersection moment of the reference signal and the analog input signal. So far the relationship was established to the magnitude information, but the conversion time also provides information about the signal in the way thus that the magnitude information is generated during the conversion time. In order to address the information of the conversion time to a synchronous digital processing system, the up-sampling ability of the CIC structure can be applied. Therefore, the information in time is generated by the conversion due to level crossing by the reference signal which is in turn generated by the constant reference step

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generation rate (section: 3.1.1). Due to the proportionality condition between reference step generation time and step magnitude, the converted output value is representative for the time as well as the magnitude. This implies, that the difference in step magnitude between consecutive conversion cycle equals the required time for the detection of the conversion. Consequently, the conversion time is known based on the step generation rate. Therefore, the number of steps which is generated by the triangular reference signal represents the information in time. In consideration of the up-sampling ability of the CIC structure a number of additional resolution steps can be put in between of consecutive conversion cycles. Furthermore, the linear interpolation property of the CIC structure scales the number of additional steps proportional. Due to the relativity between the analog input signal and the reference signal, the phase information of the converted input signal remains for the CIC output signal, but the information in time is translated to an additional information in magnitude. Since the original ADC output stream was sampled by the accelerated reference step generation rate, the clock rate of the CIC structure needs to correspond at least the reference generation rate. Thus, the up-sampled output signal results in an ADC conversion rate which is corresponding to or derived from the reference generation rate. Additionally, the time information is interpolated to magnitude information which implies a higher effective resolution.

The CIC structure is implemented in a single stage constitution as depicted in figure 5.10(a). The CIC interpolator schematic is based on a common comb section which subtracts delayed input samples and a common integrator section which adds up the generated difference [53]. In order to interpolate, the input samples needs to be delayed due to the reference step generation time by the number of additional resolution steps. E.g. in consideration of a single occurrence of consecutive conversion steps, the delay corresponds to the difference between these conversion steps. Since the additional information needs to be packed in between of the conversion steps the total delayed function is based on the sum of the initial resolution steps and the additional delay steps. Thereby, the added number of delay steps is constituted by the ratio between the conversion time and the reference step generation time. Related to the combination between the magnitude resolution and the time resolution the number of additional interpolated steps results in  $N_{\text{int}} = \log_2 (f_{\text{ref}}/f_{\text{conv}})$ . Therefore, the number of delay elements is constituted by  $N_{\text{delay}} = 2^{(N+N_{\text{int}})}$  or rearranged in  $N_{\text{delay}} = 2^N \cdot (f_{\text{ref}}/f_{\text{conv}})$ . This is related to the fact, that the transformation of the time information constitutes additional resolution information.

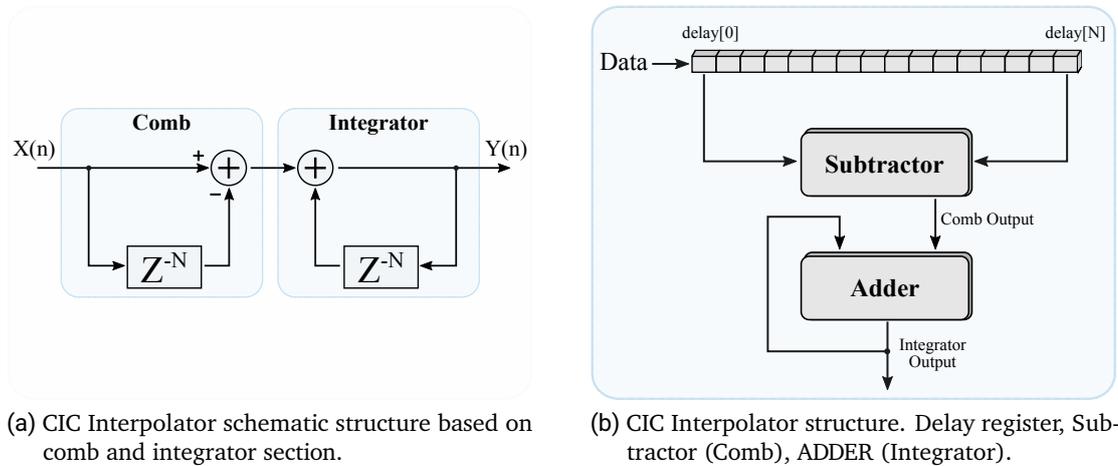


Figure 5.10: Cascaded-Integrator-Comb Interpolator structure as implemented on the FPGA. The conversion rate ( $f_{conv}$ ) based output stream of the ADC with accelerated reference generation rate ( $f_{ref} = f_{clk}/2$ ) is up-sampled by the clock frequency and interpolated by the difference between consecutive conversion steps. Thereby, the non-uniform information in time is converted to uniform information in magnitude.

Figure 5.10(b) illustrates the structure of the CIC interpolator as implemented on the FPGA within the experimental setup. The output data stream of the (ASGA Tracking ADC) is provided as the input of the interpolator which is read into a shift register by the clock frequency of  $f_{ref}$ . Thereby, the shift register constitutes the delay element of the interpolator, thus that the length of the register is determined by the number of delay stages. The interpolation process is initialized by the subtraction of the current input from the delayed data of the last stage. In the further course, the difference which is defined as comb output is accumulated with the previous comb output by an adder. Thus, the integrator output is constituted by the up-sampling of the reference step generation rate which describes the newly developed ADC conversion rate for an higher resolution result. In this terms, the time information is translated into magnitude information. The previously non-uniform constituted conversion stream is therefore translated into a uniform conversion stream with higher resolution. Since the magnitude information as well as the time information is transferred to absolute magnitude information (i.e. the time information of the presently uniform conversion scheme describes no additional information), the statement reveals: The magnitude result can be defined as information density. However, the information

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density describes the number of conversion steps within a time. This implies, that if the number of input conversion steps within a time reduces (i.e. the input information density is reduced), also the magnitude information reduces.

**Statement:**

If the non-uniform conversion time information of the ADC output is translated to additional magnitude information by interpolation, the magnitude resolution of the CIC interpolator output describes the total information density of the ADC conversion result applied as CIC input.

In order to evaluate the postulated ability of the CIC structure, the interpolator was implemented on the general purpose ADC experimental setup illustrated in figure 5.1. The base ADC algorithm to be evaluated is constituted by the bandwidth extension method based on the developing triangular reference scheme due to accelerated step generation (section: 3.1.1). In scope of the implementation, the reference step generation rate was applied for  $f_{\text{ref}} = 6.25$  MHz which is generated by a clock frequency of  $f_{\text{clk}} = 12.5$  MHz. Thereby, the derived system constraints for the CIC interpolator clock frequency ( $f_{\text{clk}}$ ) states, that the non-uniform conversion time needs to be up-scaled by the reference step generation time in order to maintain the phase relationship between conversion time and conversion step magnitude. This implies, that the subdivision of the conversion time needs to be constituted by a divisor related the step generation time. Indeed, the divisor can also be constituted by a higher clock frequency which is however derived from the step generation rate. The requirement that must be complied only relates to the exact conversion time ( $f_{\text{conv}}$ ). Thereby, a higher interpolator clock rate ( $f_{\text{clk}}$ ) implies a more accurate translation of the conversion time information to magnitude information. In order to verify this statement, the clock frequency for the CIC interpolator is applied by the global clock rate of the ADC with  $f_{\text{clk}} = 12.5$  MHz. Based on this aspect, the number of delay elements for the register structure is defined by the ratio of the applied clock rate and the average ADC conversion rate in addition to the actual ADC resolution. Therefore, the required number of delay elements results in equation 5.5. With reference to [53] the result of the number of delay elements is related to the expected resolution. thus, based on the result of required delay elements ( $N_{\text{delay}} \approx 2302$ ), the interpolated resolution results in  $N_{\text{int}} \approx 11.17$  bit.

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### Required number of delay elements for CIC interpolation:

System parameter:

ADC resolution:  $N = 8$  bit

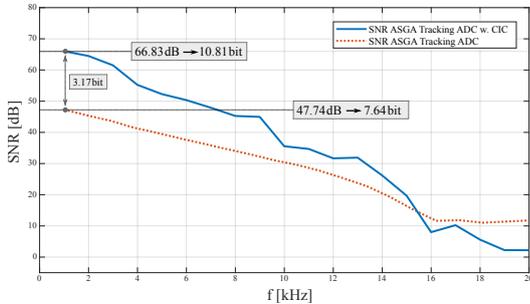
ADC average conversion rate:  $f_{\text{conv}} = 1.39$  MHz

CIC clock rate:  $f_{\text{clk}} = 12.5$  MHz

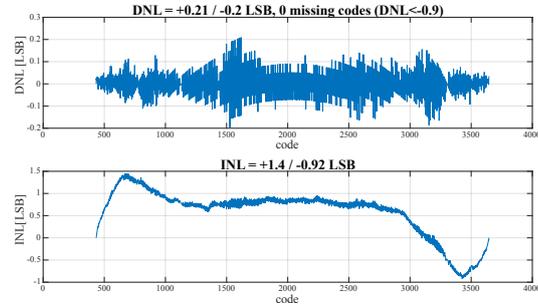
$$N_{\text{delay}} = 2^N \cdot \frac{f_{\text{clk}}}{f_{\text{conv}}} \approx 2302 \quad \Rightarrow \quad \approx 11.17 \text{ bit} \quad (5.5)$$

Related to the application of the ASGA Tracking ADC (accelerated reference step generation) in combination with the proposed CIC interpolator the postulated property can be verified by measurements. Therefore, figure 5.11(a) illustrates the signal-to-noise ratio course of the ADC without CIC interpolation in comparison to the ADC with interpolation stage in addition. Thus, it is demonstrated that the application of the interpolation stage enhances the signal-to-noise ratio over the entire bandwidth, which implies that also the effective resolution is enhanced. In comparison of the SNR course maximum for the ADC application without interpolator (47.74 dB  $\rightarrow$  7.64 bit) and the ADC application with interpolator (66.83 dB  $\rightarrow$  10.81 bit), the effective resolution enhancement corresponds exactly to the predicted additional steps by  $N_{\text{int}} = \log_2(f_{\text{clk}}/f_{\text{conv}}) \approx 3.17$  bit.

The static performance is based on the differential non-linearity (DNL) and the integral non-linearity (INL) of the ADC-interpolator combination and is depicted in figure 5.11(b). A comparison to the ADC without interpolation (Fig: 5.7(b)) reveals, that the DNL is explicitly enhanced. this aspect concerns to the interpolation ability of the CIC stage which compensates for the single occurrence of the afore investigated deviation by averaging. But in comparison of the integral non-linearity the result illustrates the limitation of averaging based on the non-linearity introduced in the conversion time. Since the interpolation transfers the non-uniform conversion time to magnitude information, also the non-linearity in time is transferred. This implies, that the INL cannot be improved and remains related to the corresponding deviation of the interpolator input. However, the deviation is transferred to a higher resolution order, which illustrates the possibility to reduce the deviation effect by binary cropping.



(a) Measured SNR enhancement of the CIC interpolated output stream under the application of the ASGA Tracking ADC.



(b) DNL and INL measurement of the CIC interpolated output stream under the application of the ASGA Tracking ADC.

Figure 5.11: Measurement results of the ASGA Tracking ADC in combination with the CIC interpolator based on the SNR course in (a) and the static performance (DNL, INL) in (b). The conversion rate is transformed to the CIC clock rate ( $f_{\text{clk}}$ ) and the non-uniform conversion time is transformed to additional magnitude information.

In general, the measurement results illustrate the ability of the CIC interpolator structure to convert the time information in additional magnitude information. Therefore, the measurement results verify the applicability of the postulated interpolation stage to improve the conversion rate towards an up-sampled uniform representation on the one hand. On the other hand, it enhances the effective resolution by the transformation of the time information. As a result, the CIC output stream is representative in terms of magnitude for the total information density of the CIC input stream. Thus, the results related to the measurement setup reveal an enhancement of the ASGA Tracking ADC performance by a uniform conversion rate of  $f_{\text{conv}} = 12.5 \text{ MHz}$  and an effective resolution of  $N_{\text{eff}} = 10.81 \text{ bit}$ .

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### 5.3 Summary on the FPGA-based ADC System Design

In today's electrical systems, signal processing is becoming increasingly important to record or process information about the environment. Signal processing is the generic term for digital and analog signal processing. Nowadays, almost every electrical system processes environmental information digitally. In general, digital signal processors are used for this purpose. FPGAs are fundamental components in modern systems based on the concepts of programmability, reconfigurability, and parallel data processing. Contrary, analog-to-digital converters are the most basic interface in terms of analog signal processing. They provide the interface between the natural world and the DSP system. However, an off-the-shelf combination of FPGAs and ADCs is relatively rare or static in most cases. Since the real world changes dynamically, there is a demand for ADCs, which provide high performance on the one hand and reconfigurability regarding the application area on the other hand. Therefore, this chapter introduced the hardware implementation of a general-purpose ADC with dynamic software implementation ability for various sampling algorithms.

The programming property of the FPGA provides the ability of reconfiguration. Applying a wide range of algorithmic implementations, the FPGA processes most of the ADC functionality. Due to this fact, a hardware reduction to a minimum requirement implements a reconfiguration property for various application possibilities. The minimum hardware requirement, in turn, is based on a comparator, a digital-to-analog-conversion unit, and the processing unit as depicted in figure 3.2. In these terms, the FPGA acts as a programmable and reconfigurable processing unit on the one hand. On the other hand, the reuse of a digital LVDS receiver of the FPGA IO bank serves as an analog comparator. This approach implies that the remaining hardware component constitutes an external R2R scaling network that acts as a digital-to-analog-conversion unit in the feedback configuration of the ADC. This architecture allows a high degree of reconfigurability, whereby the programmed constitution of the generated reference signal, which compares to the analog signal, determines the ADC performance. Figure 5.1 illustrates the proposed architecture and the experimental setup. It is based on a Genesys 2 development board equipped with a Kintex 7 FPGA and an R2R scaling network available as ASIC. In this constitution, various digital conversion algorithms were implemented on the FPGA.

In the system configuration, the FPGA IO-driver represents the analog comparator which constitutes the ADC feedback system combined with the R2R scaling network. The evaluation of the feedback system performance was representative of the applicability as an ADC. As derived in chapter 4, the feedback delay is the most significant characteristic for

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the ADC conversion rate. Thereby, further investigations turned out that the conversion rate is the major influencing factor about the effective resolution of the ADC. The linearity of the IO-driver interface, reused as an analog comparator, is decisive for the feedback delay. Therefore, investigations based on the proposed non-linearity measurement procedure in chapter 4 revealed the dispersion effect for the comparator and the entire feedback configuration. Figure 5.2 depicts the measurement results for the linearity and the propagation delay characteristic. The analysis is informative about the applicability of common ADC implementations since they require a constant propagation delay. The limitation for the dispersion effect was examined regarding the reference step generation rate, which corresponds to an overdrive/underdrive of a single resolution step. Thereby, analysis resulted in an absolute limit for the propagation delay of  $t_p = 0.6125 \mu s$  which corresponds to a maximum ADC step generation rate of  $f_{ref} = 1/t_p \approx 1.63 \text{ MHz}$  for the single level intersection. Based on the propagation delay expression of a comparator (Eqn. 4.3), the delay function of the ADC feedback configuration could be calculated and verified the measurement results. Thus, the scattered measurement results interpolated to a propagation delay function that is informative about the dispersion effect for applying the algorithmic enhanced tracking schemes proposed in chapter 3.

The examined feedback delay characteristic revealed the properties for an initial ADC parametrization. Common ADC topology implementations on the FPGA of the experimental hardware setup (figure 5.2(b)) demonstrated the ability of reconfiguration. A multi-topology system design includes respective ADC schemes based on a Digital Ramp ADC (Counter ADC), a SAR ADC, and a Tracking ADC implementation. A selection of the associated conversion scheme can apply by programmable soft switches based on the desired setup. As derived for the delay analysis, the common ADC architectures require a constant feedback delay. Thus, the step generation rate for a single intersection may not exceed 1.63 MHz. The step generation rate was selected to 1 MHz to maintain a constant delay behavior for the common ADC architectures. Based on the reference step generation rate, the corresponding conversion rate and the bandwidth limitation were determined for the individual ADC topology (Tab. 5.1). The measurement results were evaluated regarding the dynamic performance and the static performance of the ADCs. Measurement results for the SNR courses verified the mathematical models of the respective SNR expression by comparing the equation-based results. In conclusion, the set of expressions derived in chapter 2 for the prediction of the SNR and the bandwidth limitation offer validity. Furthermore, the proposed hardware approach can be reconfigured by programming and offers a flexible design for a general-purpose ADC application. In addition, the comparison between the measurement results of the SNR courses validated the assumptions and postulations in chapter 3 for the general ADC design.

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The measurement results of the common ADC designs in section 5.2.1 validate the implementation approach. Therefore, the proposed algorithms for the bandwidth extension defined as ASGA Tracking ADC and the algorithm for the enhancement of the effective resolution defined as JASGA Tracking ADC were implemented and evaluated (section 5.2.2). The evaluation method concerns the same procedure as for the common ADC topologies. However, the accelerated reference step generation rate emerges propagation delay variations due to the dispersion effect. As derived, the variations due to the dispersion effect affect the conversion rate. Therefore, the propagation delay evaluation was examined by the interpolated propagation delay function in figure 4.3. Since the reference step generation rate was accelerated to 6.25 MHz, the propagation delay is represented by  $0.16 \mu\text{s}$  which corresponds to a number of overdrive/underdrive steps of  $N_{\text{disp}} \approx 2.75$ . Related to the fact that the dynamic number of overdrive/underdrive steps of the reference signal is relative to the analog input signal, the results of the dispersion effect needs to be transferred to the property of the developing reference signal (section 5.2.2). Due to the measurement process, a linear dependency for the propagation delay was established for a constant input signal by the Counter ADC (section 5.1.1). Since the reference signal develops as a triangular signal relative to the analog input signal, the translation factor of the dispersion step number for the bandwidth extended approach reveals the crest ratio derived in chapter 2. Thereby, the crest ratio defines the reference signal development based on the ratio between the RMS value of the sine wave and the RMS value of a triangular wave. Especially the RMS value of the sine wave is representative for the sequential return of the reference signal to the opposite direction of the analog input signal in a subsequent step of the conversion cycle detection. The procedure is necessary for the tracking scheme described in chapter 3. In the second approach, the return state skipped due to the application of jumps. In these terms, the reference signal develops as the relation of a square wave and a subsequent process of a triangular function. Thus, the translation factor of the dispersion number is defined by  $\sqrt{3}/1$ . Based on the translation of the constant number of overdrive/underdrive steps to the reference scheme, the resulting average conversion rate determines by the ratio of the reference step generation rate and the number of adjusted dispersion steps. The behavior is depicted for the respective method by equation 5.3 and equation 5.4. The resulting parametrization based on resolution, step generation rate and conversion rate is depicted in table 5.2.

Related to the resolution restriction of  $N = 8$  bit by the R2R scaling network and the applied reference step generation rate of  $f_{\text{step}} = 6.25 \text{ MHz}$  the FPGA implementation of both tracking scheme algorithms were evaluated. The same evaluation procedure for the common ADC architectures was applied to investigate the dynamic performance

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and the static performance. Thereby, the measurement result of the SNR course for the bandwidth extension algorithm reveals the expected behavior of the bandwidth extension by accelerating the reference step generation rate. Furthermore, the measurement results confirm the prediction ability of the extended general SNR equation (Eqn. 2.39) as illustrated in figure 5.7(a). The static performance is also linear as compared to the common tracking ADC approach. Except for the transition of the most significant bit, which defines the most critical digital-to-analog translation. The peak of the differential non-linearity (DNL) and integral non-linearity (INL) is caused by the accelerated reference step generation rate which concerns to both algorithms as also illustrated in figure 5.8(b). The investigation of the effective resolution enhancement algorithm is based on the SNR course and reveals the expected behavior in addition (Fig: 5.8(a)). Furthermore, it also confirms the predictive ability of equation 2.39 and implies that the effective resolution increases by the postulated increase of the conversion rate. In comparison, the dispersion effect increases the average conversion time due to the acceleration of the reference rate to  $f_{\text{conv}_{\text{tri}}} = 1.39$  MHz. The additional application of jumps increases the conversion rate to  $f_{\text{conv}_{\text{tri}}} = 1.97$  MHz. This aspect confirms the postulation of the algorithmic approach in section 3.1.2 as well as the predictive ability of the general SNR equation. In conclusion, both proposed algorithmic approaches are verified by measurements. Figure 5.9 compares the measurement results of both algorithmic implementations with the measurement results of the SAR implementation to clarify the enhancement by algorithmic approaches. Compared to the conventional Tracking ADC, it reveals that the input frequency range of a higher effective resolution can be explicitly extended by the acceleration of the step generation rate. As a result, the frequency range covers almost the entire bandwidth of the SAR ADC but with a higher effective resolution.

Digital post-processing is a key feature to enhance the converted signal properties regarding linearity and effective resolution. Since the proposed tracking schemes perform level-crossing, an irregular (non-uniform) conversion behavior in time is caused (chapter 2). The development of the reference signal for those schemes is relative to the analog input signal. Therefore, detecting the intersection moment describes exactly the required number of reference steps within the conversion time. So far, exclusively, the number of reference steps was addressed to the ADC output stream in the scope of magnitude information. However, the required time for a conversion cycle describes the analog input signal's information and defines it as information in time. Related to the data processing ability of digital systems, the information in time can not be processed without further effort by synchronous systems. In order to transfer the entire information of the converted ADC output signal, the information in time was converted to information in amplitude. Thereby, a cascaded-integrator-comb (CIC) structure was used as interpolator as described

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in [53]. Contrary, the CIC decimator is a common approach for the sake of down-sampling the oversampled signal of  $\Delta\Sigma$ -ADCs as described in [59, 60]. However, the converse ability of a CIC structure was applied to translate the time information of a non-uniform conversion cycle. Thereby, the up-sampling ability enables the translation of the time information due to interpolation. A key aspect concerns the generated conversion time as a linear representation between the reference step generation rate and the number of reference steps within the triangular conversion. Due to the proportionality condition, the interpolation method enables to insertion of additional steps in between consecutive conversion results. Under the constraint that the interpolation rate refers to as the accelerated reference step generation rate, the sum of the additional number of resolution steps in between consecutive conversion cycles corresponds precisely to the conversion time. Based on this fact, the phase information remains for the interpolated signal. However, it is up-sampled to the reference step generation rate, which now corresponds to a synchronous conversion rate of a higher magnitude. Related to the interpolation, the individual magnitude of additional steps depends on the difference of consecutive samples multiplied by the number of occurrences. In these terms, the information in time translates to information in magnitude. The resulting magnitude information constitutes by the sum of the initial magnitude information and the translated time information. As a result, the output of the interpolator stage defines the information density of the converted ADC output stream. Therefore, a statement results: If the non-uniform conversion time information of the ADC output is translated to additional magnitude information by interpolation, the magnitude resolution of the CIC interpolator output describes the total information density of the ADC conversion result applied as CIC input. However, information density implies that the number of conversion cycles is decisive about the resulting magnitude information. Thus, the magnitude of the interpolator output decreases with the reduction of conversion cycles (i.e. if the input signal frequency increases).

Figure 5.11 illustrates the performance enhancement of the ASGA Tracking ADC which triangular conversion scheme is developed by an acceleration of the reference step generation rate. The course of the SNR demonstrates the ability of signal enhancement in terms of effective resolution, thus that the maximum improvement revels in 3.17 bit of effective resolution. Likewise, the conversion rate transfers to the higher order of twice the reference step generation rate ( $f_{\text{clk}} = 12.5 \text{ MHz}$ ). The signal-to-noise ratio describes the dynamic property of the converted signal. Additionally, the static property based on DNL and INL depicts the enhancement. Thus, the differential non-linearity improved, but the relative integral non-linearity deviation remains. The results are comparable to the initial results of the ASGA Tracking ADC. This behavior is related to the fact that the INL refers to the linearity in time translated to information in magnitude.

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In summary, this chapter introduces the experimental setup and measurement results of a general-purpose ADC, which demonstrates the reconfigurability by common ADC architecture implementations (section 5.2.1). The parametrization of the common ADC architectures was determined by the hardware configuration of the R2R scaling network (8 bit) and the analysis of the analog comparator properties of the FPGA LVDS driver. The measurement results of the common ADC architectures confirmed the prediction ability of the derived equation set for the bandwidth and the signal-to-noise ratio in chapter 2. Furthermore, the bandwidth extension algorithm and the effective resolution enhancement algorithm were implemented on the experimental setup to demonstrate the postulated enhancement properties of chapter 3. The measurement results confirmed the enhancement ability of the proposed algorithms on the one hand. On the other hand, they also confirmed the ability of the extended general SNR equation (Eqn. 3.8) to predict the postulated enhancement properties. In addition, a method for the translation of the non-uniform conversion time information to magnitude information demonstrates that the entire information density of the converted ADC output stream can be processed. Thereby, the effective resolution, as well as the conversion rate, is improved. The ability to transfer between time information to magnitude information was provided by applying a CIC interpolator stage described in [53]. The dynamic (SNR) measurement results and the static (DNL, INL) performance confirm the applicability of an interpolator stage to the non-uniform conversion scheme. Furthermore, it reveals the property of a translation to a uniform conversion rate based on a higher frequency than the initial rate.

The measurement results of the algorithmic enhanced ADC architecture by the reference step acceleration and the application of the interpolator summarizes in table 5.3. Additionally, it compares both designs with an FPGA ADC implementation based on an external RC network and a programmable clock phase TDC as described in [50]. Furthermore, a XADC design, which is frequently built-in for high-performance FPGAs, is listed. The comparison between the individual ADC architectures is based on the dynamic and the static performance. As a result, the Clock Phase TDC implementation has a low resolution but a high conversion rate. The XADC, in turn, has a high resolution but a low conversion rate. Therefore, to describe a fair comparison, the information density of the respective design is examined by the number of effective resolution steps, which is multiplied by the conversion rate. The direct comparison can be noticed that the proposed ADC architecture without interpolation provides the lowest information density based on the configuration. However, the effective resolution is higher than the Clock Phase TDC approach, which implies that the performance decrease relates to the conversion rate of the current configuration. As examined in this chapter, the modification of the conversion algorithm enhances the conversion rate. However, the ability to accelerate the reference

step generation rate towards a higher order is also applicable due to the reconfigurable design. As derived, the time information of the conversion output can be translated to amplitude information by the CIC interpolator, which increases the conversion rate at the same time. Thus, the resolvable information density of the converted signal is way higher than the information density of the Clock Phase TDC and the XADC implementation. In comparing the static performance regarding DNL and INL, the algorithmic approach has better linearity than the XADC (except the single peak). Thus, the proposed ADC methods with CIC interpolator demonstrate advantages regarding conversion rate, linearity, and resolution over existing ADC designs implemented on FPGAs. The small number of external components based on an R2R scaling network, available as ASIC, enables a high degree of reconfigurability. The R2R approach shows much higher robustness against process variations compared to existing designs based on RC networks. The calibration of the external network is not necessary. Therefore, the proposed design is independent of the FPGA platform. Furthermore, no restrictions based on design implementations for delay elements of a TDC are present since the design is fully clock-capable. This approach simplifies the porting of the implemented design to other platforms. The high degree of reconfigurability enables application area-specific ADC applications by providing a fully controllable reference signal generation due to programming.

Table 5.3: Comparison Algorithmic Tracking Scheme ADC (with and without CIC), a clock phase TDC architecture and a FPGA built in XADC.

	<b>This Work</b>	<b>This Work</b>	NSSCR'07 [50]	FPGA built in
Architecture	<b>Algorithmic</b>	<b>Algorithmic Interpolation</b>	Clock phase TDC	XADC
Resolution (bit)	<b>8</b>	<b>12</b>	6	12
Conversion Rate (MS/s)	<b>1.39</b>	<b>12.5</b>	22.5	1
SNR (dB)	<b>47.74</b>	<b>66.83</b>	n.a.	62
ENOB (bit)	<b>7.64</b>	<b>10.81</b>	n.a.	10
Info. density <sup>1</sup> (G Info/s)	<b>277.26</b>	<b>22441.11</b>	1440	1024
DNL (LSB)	<b>[1.7,-0.68]</b>	<b>[+0.21,-0.20]</b>	n.a.	[-1,1]
INL (LSB)	<b>[+0.81,-0.89]</b>	<b>[+1.4,-0.92]</b>	n.a.	[-2,2]

<sup>1</sup> [56] Information density =  $2^{\text{ENOB}}$  · Conversion rate

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## 6 Mixed Signal ASIC Design

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The trend of continuous scaling for integrated technologies has improved switching frequency and energy efficiency for digital circuits. This aspect integrates more and more functionality on ASICs like digital-signal-processing (DSP) or digital interfaces to peripheral systems like FPGAs or processors. Based on the aspect of digital performance ability for emerging integrated technologies as the TSMC/Samsung 7 nm process or the TSMC/Apple 5 nm process [61], especially the demand for analog precision can be decisive for the applicability of mixed-signal systems. Digital implementations benefit from novel technologies in terms of switching frequency and power consumption, but precise analog implementations are becoming increasingly difficult to integrate due to physical limitations. It is related to the fact that the physical precision requirement for a digital signal reconstruction is low compared to the analog accuracy requirement. Thus, analog systems cannot benefit from the entire scope of technology scaling (except with much effort). Thus, a valid approach for applying an analog system behavior reveals the reduction of complexity by replacing analog functionality with digital functionality on the one hand. On the other hand, the remaining analog functionality needs to be calibrated, or deviations need to be compensated to obtain a precise analog behavior. However, the interfacing of real-world analog signals is a system that requires analog precision. This aspect counteracts the digital benefits of small area and power consumption [62]. Thus, there is a demand for almost digital ADCs that handle nonlinearities caused by scaled technologies and simultaneously benefit from the integration process. As introduced in [63], attempts utilize improved abilities and can apply extended digital techniques like time interleaving. Other approaches boost the performance by techniques, such as noise-shaping due to oversampling for SAR ADCs [64].

This work demonstrates a method to reduce the hardware complexity of Analog-to-digital-converter by the support of digital operations. A further advantage that relates to digital operations is represented by a high degree of configurability. The state-of-the-art for the implementation of analog to digital conversion is often related to a static and predefined environmental parametrization based on the input signal bandwidth, the sampling rate, and the resolution. The limitations of the respective ADC are often based on the applied

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sampling scheme for conversion. The advantage of digital operations allows it to enable a conversion scheme, which is adaptable to the system requirements and can be adjusted dynamically. The converter class is defined as general-purpose ADC in this work, which provides the ability to be parametrized on-demand digitally and be reconfigured on the fly. In these terms, the reconfigurability is based on the algorithmic implementation of the sampling scheme that is decisive about the bandwidth limitation, the conversion rate, and the effective resolution.

For the design of a system like the proposed ADC, initial requirements need to be explored. So, the analog hardware is reduced to a comparative device for analog signals (comparator) and a scaling network that converts the digital information about the sampling scheme representation into an analog representation compared with the analog input signal. The basic conversion operations are established by the digital sampling scheme, which processes the comparative information of the comparator to further successive instructions of the sampling scheme. Based on these considerations, the ADC's conversion rate depends on the comparator's comparative ability. The shorter the conversion time, the faster the analog-to-digital conversion. The conversion time for ADCs has two restrictive factors. On the one hand, the propagation delay of the comparator defines the maximum achievable conversion time. On the other hand, the number of comparisons needed for a single conversion multiplies the propagation delay. These considerations reveal that the applied sampling scheme is more representative than the analog restrictions of the comparator. So far, the state-of-the-art develops faster and faster comparator implementations that are designed at technology limits [65, 66]. This approach leads to specialized devices that are often restricted to a specific area regarding technology and application. The resulting disadvantages of such designs are instability or disproportionate high design processes regarding technology transfer, integration mismatch, or process variations. Therefore, the proposed approach is simplified to a robust but fast comparative device, which topology can be transferred to any technology without any effort. The same procedure is applied to the scaling network, which converts the sampling information to analog information. Indeed, the proposed approach also suffers from non-linearities in the analog components. However, the digital and, therefore, dynamic sampling scheme generation can counteract a certain extent of deviations.

As described in chapter 3, the proposed tracking scheme averages mismatches between the overdrive and the underdrive related propagation delay to an offset affected mean value. In subsequent correction steps, the offset can be eliminated under the knowledge of its magnitude and occurrence. This methodology is described in section 4.2.1 as non-linearity tracking and correction method. Thereby, analog inaccuracy is transferred to a

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digital correction process. A second method for the non-linearity compensation due to inverse conversion was proposed in section 4.2.2. The knowledge of the deviation due to analog inaccuracy is not necessary for this method, which implies a higher degree of robustness concerning environmental or process variations that affect the physical properties of the analog components. Especially, the integration process of analog designs within leading-edge short channel technologies suffers from non-linearity by mismatch or process variations. It leads to the fact that more and more design effort is applied to analog components concerning calibration methods in order to maintain or obtain high precision in the scope of reproducibility and application areas. Contrary to the implementation of calibration methods, applying the proposed methods allows the occurrence of non-linearity effects and compensates these effects by procedural methods in the digital domain.

The proposed analog-to-digital conversion method based on a tracking scheme is implemented on ASICs to benefit from the performance improvement of integrated technologies. Therefore, this chapter concentrates on implementation methods for an integrated version of the ADC. In order to compensate for the non-linearity related to the comparator dispersion effect, process variations, and mismatch, the correction and compensation methods proposed in chapter 4 are applied to the ASIC design. In these terms, a post layout linearity analysis of the ADC feedback configuration, especially for the comparator, is performed as described in section 5.1.1 for the FPGA design. In the further course, the compensation method by inverse conversion is applied to the analysis to demonstrate the system robustness regarding process variations and mismatch based on a Monte Carlo analysis. Regarding the linearity analysis, 3 ASIC prototypes were designed to implement the algorithmic approach of the tracking scheme, which is enhanced by jumps as described in section 3.1.2 and verified in section 5.2.2 by the FPGA implementation. In this terms, two ASIC designs were developed in a 65 nm technology node. The first implements the non-linearity adaption by the tracking and correction method (section: 4.2.1) and the second implements the compensation method by inverse conversion (section 4.2.2). In order to evaluate the increase in performance, the third ASIC is developed in a state-of-the-art 28 nm technology node. It implements the non-linearity adaption based on the compensation by inverse conversion method, which is investigated regarding global process variations and mismatch.

In conclusion, the ASIC designs are verified by measurement results. Thereby, the ASIC prototypes are interfaced by an FPGA that acts as receiving device to evaluate and forward the measured data. In this terms, a communication interface based on a source-series-terminated transmitter with 8B/10B protocol [67, 68] extends the ASIC implementation.

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## 6.1 Non-linearity Analysis and Compensation Method

The propagation delay within the feedback configuration based on the R2R scaling network and the comparator of the proposed ADC defines the conversion rate of the ADC system as predicted by equation 2.57. Since the propagation delay is limited by the comparator properties, in the main, the linearity behavior of the comparator decides about the average conversion rate of the ADC. The linearity represents a relation between the amount of overdrive/underdrive (required for a level-crossing detection) and the resulting propagation delay. Related to the propagation delay analysis in section 4.1 the statement is revealed, that the greater the deviation of the reference signal from the input signal, the shorter the propagation delay and the higher is the conversion rate for the ADC. In this terms, the dispersion effect of the comparator has a major impact on the noise performance of the ADC. Thereby, two perspectives revealed. On the one hand the dispersion effect affects the global conversion rate and on the other hand the dispersion effect induces a local non-linearity of a converted sample. Since dispersion is a physical property of each comparator, it is necessary to investigate the physical delay properties in relation to the ADC design. As demonstrated in section 5.1.1 for the analysis of the FPGA IO driver the dispersion effect depends on the applied conversion algorithm, which is decisive about the amount of overdrive/underdrive of the reference signal in relation to the analog input signal. Therefore, based on the applied sampling algorithm, non-linearity compensation methods can be applied to the ADC design. Section 4.2.1 and section 4.2.2 each proposes a possible compensation method of the non-linearity effect under the consideration of the applied sampling algorithm. Referred to the required ability of the ADC system to compensate the non-linearity effect methodical investigations in scope of a Monte Carlo analysis were accomplished on the basis of post layout simulations. In this terms, general process variations and mismatch as well as environmental variations like temperature or power supply are evaluated for the compensation method by inverse conversion of the 65 nm and the 28 nm technology node.

Besides, the compensation method by tracking and correction, which was applied to a 65 nm technology node is referred to the post layout measurement results. This consideration is valid, since the tracking and correction method is based on a measurement system (section: 4.2.1) of constant analog input signals (DC). Therefore, there is a demand, that the application of constant signals is stable under the influence of process variations, mismatch and temperature or power supply variations. In this terms, the constant input

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levels are established by a bandgap reference [69, 70] which ensures that the system is able to measure the deviation introduced by non-linearity effects. Therefore, a process corner analysis and a Monte Carlo analysis was performed for the bandgap reference circuit.

Besides temperature and process variations, the main influencing parameter for deviations is depicted for the core voltage supply of the 65 nm technology node (1.2 V). Thus, the supply of the reference circuit is close to the bandgap voltage of silicon, which implies a requirement for stable reference level of sub bandgap voltages. Reference [71] proposes a bandgap design which is designed in terms of this requirement in a 600 nm technology node. Therefore, the proposed bandgap design was transferred to the 65 nm process and evaluated regarding stability under the influence of process, temperature and supply variations. In order to verify an accurate reference for the ADC system, the deviation from the constant level should not exceed the voltage of 1 LSB (i.e.  $1.2\text{ V}/255 = 4.71\text{ mV}$ ). Under these constraints the analysis of the bandgap circuit results in a temperature drift of  $8.2\text{ ppm}/^{\circ}\text{C}$  (temperature range:  $0 - 125^{\circ}\text{C}$ ) for a supply of 1.2 V and  $47.7\text{ ppm}/^{\circ}\text{C}$  for  $\pm 10\%$  supply degradation, respectively. In this way, the bandgap reference is applicable for the compensation ability of the tracking and correction method and the deviant behavior of the ADC system can be derived from the comparator analysis.

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### 6.1.1 Comparator Analysis in 65nm Technology

The non-linearity of the comparator transfer function is described by the dispersion effect that affects the propagation delay. As described in section 4.1, the feedback configuration of the ADC is constituted by the composition of the scaling network and the comparator. Thereby, the influence of process variations and mismatch induce the non-linearity to the system, which in summation affects the dispersion effect and thus the propagation delay. A varying propagation delay, in turn, causes the ADC system to a faulty detection of the level-crossing intersection between the analog input signal and the reference signal. This implies, that the constitution of the comparator is a main criterion for the ADC performance. Related to the fact, that the emerging technology nodes demands additional effort in terms of precise analog performance, the reduction of the analog complexity is proposed. In application, this leads to a basic implementation of a comparative device, which constitution is reduced to the minimum required ability of a level-crossing detection. Therefore, the implementation is based on a differential input stage which is followed by a single driver stage in order to establish the load interface for further processing in the digital domain. Furthermore, the level-crossing detection of the comparator is synchronized by digital processing. In this way, the comparator is designed as a single stage based on a non-clocked configuration.

Referred to the applicability within the ADC system, the design of the comparator is based on the relating parametrization. As derived in section 5.1.1 for the analysis of the as analog comparator reused FPGA LVDS driver, the ADC resolution specifies the required DC gain ( $A_v(0)$ ). It is based on the general ability to detect an input difference of the least significant bit for input frequencies below the comparator cutoff ( $\omega_c$ ) and is defined as 1 step limitation. The analysis of the comparator is based on the 65 nm ASIC implementation of the proposed ADCs, which are equipped with a 8 bit R2R scaling network in the feedback configuration. Related to the analysis of the comparative properties of the LVDS driver in the analog domain, the minimum gain requirement of the comparator is calculated in reference to equation 5.1. Thus that the minimum required DC gain again results in  $A_v(0) \approx 46$  dB due to the fact of the same 8 bit resolution.

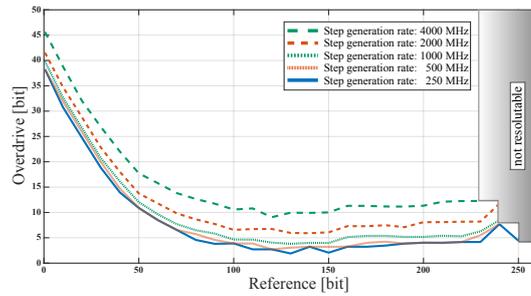
The evaluation procedure of the integrated comparator is based on the measurement approach described in section 5.1.1. Thereby, the deterministic non-linearity with respect to the dispersion effect is investigated in post layout simulations. Related to the FPGA driver analysis, the measurement configuration is based on a Counter ADC implementation which is able to detect the numerical deviation in reference steps due to overdrive/underdrive of a constant analog input level. In this way the physical implementation of the comparator

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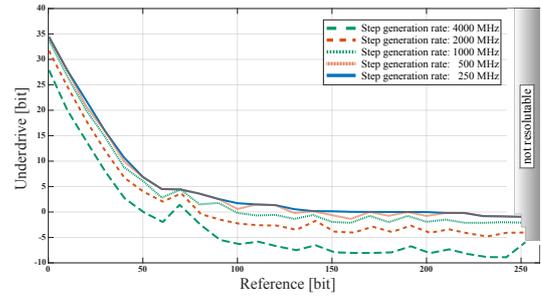
is analyzed with respect to the deviation caused by overdrive and underdrive as depicted in figure 6.1. In order to apply the results to the proposed tracking scheme with jumps the set of reference generation rates needs to be evaluated in a range for a higher reference step generation rate ( $f_{\text{ref}}$ ) than the conversion rate ( $f_{\text{conv}}$ ). This dependency was defined in chapter 3 for the algorithmic implementation of enhanced tracking scheme methods. A gain-bandwidth analysis of the implemented comparator reveals the cutoff frequency ( $\omega_c$ ) and the DC gain ( $A_v(0)$ ) of the comparator as illustrated in figure 6.2(b). Based on the gain-bandwidth analysis the cutoff frequency is simulated to  $\omega_c = 204.91$  MHz and the actual DC gain to  $A_v(0) = 47.33$  dB which is slightly higher than the calculated minimum requirement. Thus, the physical dispersion effect of the comparator was analyzed in a range from  $f_{\text{ref}} = 0.25$  GHz  $\rightarrow$  4 GHz which provides the demand of a higher step generation rate than the conversion rate. The results of the post layout linearity analysis of the comparator implemented in the 65 nm technology process illustrates the dispersion effect by the frequency dependent overdrive (Fig: 6.1(a)) and underdrive (Fig: 6.1(b)) on the one hand. On the other hand they reveal the non-linearity for the input common mode range (ICMR). Besides the slew rate limitation the input common mode range is another factor which introduces non-linearity due to the increased response time of the comparator in case the input signal level are close to the rails of the comparator (section: 4.1). Related to the analysis of the underdrive effect, the ICMR limitation implies that the level crossing intersection is above the actual input signal (Fig: 6.1(b)). In comparison to the results of the FPGA (Fig: 5.2), the implemented comparator in 65 nm is not able to provide a high linearity. This aspect qualifies the integrated design for the application and investigation of the proposed non-linearity compensation methods in section 4.2.

In order to derive a function for the propagation delay of the feedback configuration, the measurement results of the dispersion effect can be transferred as a relation between the deviation of reference steps in amplitude within a step generation period. Due to the proportionality condition which is provided by the Counter ADC measurement scheme the transfer is valid and was already derived for the analysis of the FPGA comparator. However, in comparison to the FPGA application, the analysis of the implemented comparator exhibits a significantly higher non-linearity caused by the ICMR limitation. In order to approximate the propagation delay variation based on the dispersion effect, the ICMR related non-linearity is neglected and the average of the overdrive and underdrive related results is formed as it is illustrated in figure 6.3(a). Thereby, the derived propagation delay function of the comparator results in figure 6.2(a) and is decisive about the approximated propagation delay behavior of the ADC feedback configuration. In order to verify the results of the analysis, the propagation delay function is calculated based on the post layout measurement results of the comparator that are illustrated in figure 6.2(b).

The procedure concerns to the approach which was applied for the comparator analysis of the FPGA in section 5.1.1. In this way, the methodical approach of the propagation delay equation (Eqn: 4.3) demonstrates the validity and applicability of an integrated comparator design in scope of delay approximation under the influence of dispersion.

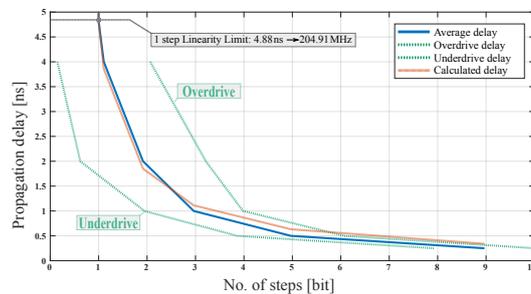


(a) Overdrive by the reference signal for a set of step generation rates.

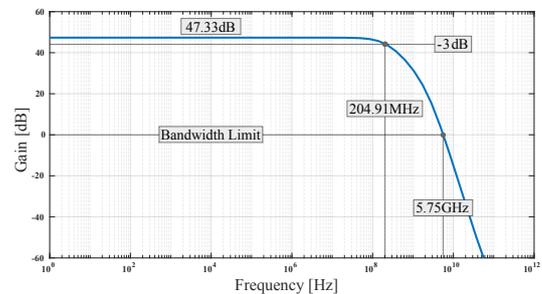


(b) Underdrive by the reference signal for a set of step generation rates.

Figure 6.1: Post layout linearity analysis of the comparator in 65 nm technology. Overdrive/underdrive of a constant analog input signal (DC) by the reference signal. Measurement method: Counter ADC with various reference step generation rate (section: 5.1.1). Imbalance between overdrive and underdrive.



(a) Average propagation delay of the feedback configuration. (post layout simulation 65 nm)



(b) Comparator gain bandwidth characteristic. (post layout simulation 65 nm)

Figure 6.2: Comparison between the calculated and simulated propagation delay of the feedback configuration in (a). Propagation delay calculation for the comparator based on post layout measurement parameters of the gain bandwidth in (b) and equation 4.3.

Related to the fact, that the dispersion effect depends on the overdrive/underdrive by level-crossing of the sampling scheme related reference signal, the application of the tracking scheme with jumps is the proposed reference for the derivation of the non-linearity interaction in the feedback configuration (section: 4.2). Therefore, the implemented sampling scheme was applied to the further analysis in addition. In order to compare the previous results of the dispersion effect, the tracking scheme algorithm was again evaluated by reference step generation rates in the range of  $f_{\text{ref}} = 0.25 \text{ GHz} \rightarrow 4 \text{ GHz}$ .

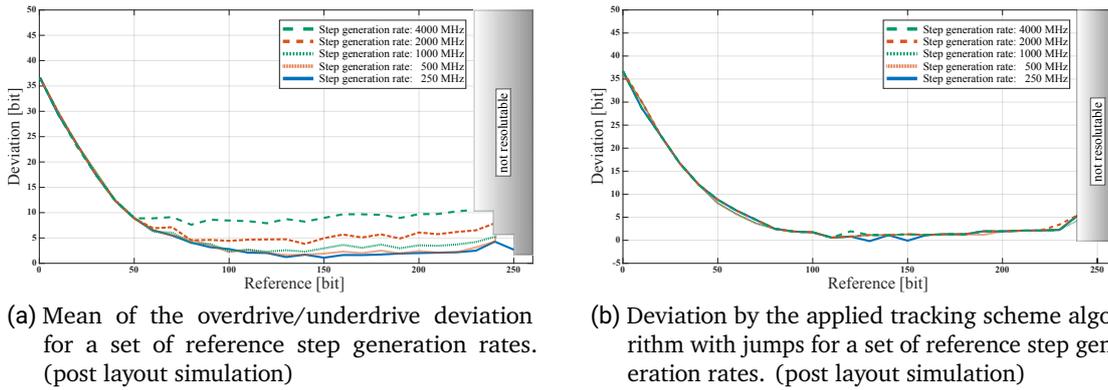


Figure 6.3: Comparison between the mean overdrive/underdrive deviation (a) and the deviation introduced by the applied tracking scheme (b). The tracking scheme averages the deviation to the comparator limitations represented by the cutoff frequency ( $\omega_c$ ). As a result the conversion rate is independent of the reference step generation rate. For a constant input signal the non-linearity effect by dispersion induces offsets (section: 4.2.1).

Figure 6.3(b) illustrates the corresponding post layout measurement results. As derived for the compensation method of tracking and correction (section: 4.2.1) the application of the tracking scheme eliminates the dispersion effect for a constant input level due to the averaging of consecutive conversion steps related to the overdrive and underdrive (Fig: 4.5). However, the averaging induces offset errors to the conversion result which needs to be corrected by one of the proposed compensation methods. In general, the averaging method equalizes the propagation delay related to the overdrive and the underdrive. Thus, the average of the afore investigated dispersion effect with respect to overdrive and underdrive is comparable to the results of the applied tracking scheme as illustrated in figure 6.3(a). In comparison of both results, it can be concluded, that the averaging method constitutes the conversion time of the ADC to the sum of the overdrive and underdrive

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propagation delay. Thus, the method induces an equalization. However, in consideration of a time varying input signal, the averaging causes offset errors to any conversion step which in turn implies that the dispersion effect is still present. In this terms, the analysis demonstrates that the offset related to constant input level can be measured and applied for correction as it is presented for the tracking and correction method in section 4.2.1. In addition, this method measures the non-linearity of the comparator transfer function which is caused by the input common mode restriction since it generates a global deviation from the respective constant input level.

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## 6.1.2 Compensation Method Analysis

The comparator analysis in scope of the 65 nm technology process revealed the non-linearity related to the dispersion effect on one hand and the non-linearity related to the input common mode range on the other hand. Compared to the LVDS driver linearity of the FPGA system design in chapter 5, the integrated comparator exhibits an explicitly higher non-linearity effect with respect to the input common mode range. I.e. close to the lower supply rail, the deviation from the actual input signal increases. This aspect also has the consequence that the propagation delay referred to the proportionality condition increases. In summary, the deviation of the regular conversion increases the closer the input signal is located to the lower rail of the comparator. Actually, the ICMR limitation even predominates the dispersion effect in this region. However, due to the fact that the comparator has a high non-linearity, it is suitable for the physical verification of the non-linearity compensation methods.

Since the ability of non-linearity measurement is already demonstrated in scope of the comparator analysis, the correction of the output stream on basis of the deviation values can be applied, as described in section 4.2.1. Thus, the method of non-linearity tracking and correction is applicable to the integrated design. However, the accuracy for the detection of deviation steps relative to a constant input level depends on the provided number of these constant levels. Contrary, the method for non-linearity compensation by inverse conversion as introduced in section 6.1.2 is independent of constant comparison levels, but applies a converse analog-to-digital conversion. Due to this fact the non-linearity which is induced by the regular conversion cycle is considered to occur by the same magnitude in case the conversion is repeated under the same system constraints. This implies furthermore, that the application of the inverse conversion function as a subsequent step to the regular conversion is able to cancel the previously superimposed non-linearity of the conversion result. Based on the proportionality condition, the deviation in reference steps is always related to the respective input level. Therefore, the inverse application eliminates the number of deviation steps and the actual input representation remains. Technically, the inverse conversion method can be applied to the regular conversion topology under the constraint of interchanging the input comparator terminals. In this terms, the result of the regular conversion represents the emerging analog input due to a digital-to-analog conversion, which is interfaced to the mirrored terminal. The remaining comparator terminal is interfaced by the reference signal, which is generated in the contrary sequence to the regular scheme, thus that the number of deviation steps arise by the same magnitude as for the regular conversion but contrary signed.

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The proposed topology for the implementation of the compensation method by inverse conversion is illustrated in figure 4.12. It is based on an analog-to-digital subsystem for the regular conversion as well as an analog-to-digital subsystem in identical construction for the subsequent inverse conversion. Both sampling algorithms are identical but are processed contrariwise for the respective sampling direction. In order to regulate the sequential compensation method with respect to the interaction between the regular and the subsequent inverse conversion, a process control unit monitors and controls the compensation procedure. The described compensation topology was implemented as integrated design in scope of a 65 nm technology node and a 28 nm technology node. The general ADC conversion functionality is based on the proposed tracking scheme with jumps which is described in section 3.1.2 and evaluated with respect to the FPGA design in section 5.2.2. In combination with the compensation method by inverse conversion the non-linearity effect of the feedback configuration should be eliminated. In this terms, the compensation ability was evaluated for a set of constant input voltages which represents the range of the respective ADC input level in a binary order. Based on post-layout simulation results the compensation ability of the dispersion effect as well as the compensation ability for the input common mode range referred non-linearity is demonstrated by a comparison to the uncompensated conversion output. In order to validate the predicted ability to compensate the non-linearity effects based on PVT variations as well as statistical mismatch variations, Monte-Carlo analyses with respect to the PVT corners were performed for the respective post-layout design. Thereby, the Monte-Carlo analysis results for the uncompensated conversion results were compared to the Monte-Carlo analysis results for the compensated conversion results. In general, the scattering of the results in relation to the deviation of conversion steps from the actual digital representation of the analog input describes the ability of compensation. Thus, the lower the scattering of the results within the Monte-Carlo analysis, the better the compensation ability.

In scope of the 65 nm process the typical case performance setup demonstrates the compensation ability of the inverse conversion method as illustrated in figure 6.4. Thereby, the deviation in reference steps was related to the respective input level which is represented as binary expression. As analyzed for the non-linearity of the comparator in the previous section (section: 6.1.1), the conversion results in non-linearity effects based on an averaged dispersion effect and the affection of the ICMR limitation. Thereby, the major non-linearity affection is caused by the restricted input common mode range. Thus, the conversion result of the uncompensated ADC reveals the non-linearity effect with respect to the applied tracking scheme with jumps, whereby the absolute deviation of the conversion increases with the proximity of the lower potential rail of the comparator. This aspect implies, that the lower the input signal and thus the reference signal, the higher

the deviations from the actual representation of the input signal. However, under the application of the compensation by inverse conversion the effect of deviation is equalized and reveals that the deviation from the actual input signal is reduced to an average of  $\pm 1$  LSB. Since the ICMR limitation dominates for this design, the compensation effect is marginal. But, especially the case for the ICMR limitation in proximity to the lower potential inputs reveals the compensation ability of the proposed design as predicted by equation 4.7.

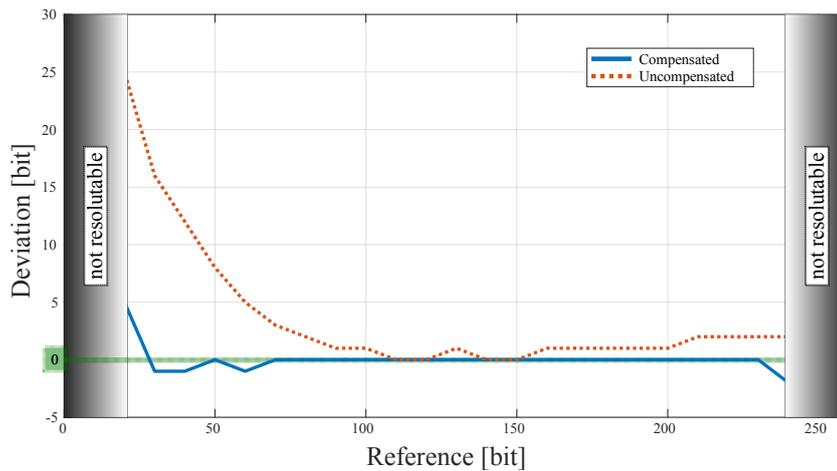


Figure 6.4: Non-linearity compensation by Inverse Conversion related to the proposed method 2 (section: 4.2.2). Verification by post layout simulations in 65 nm technology. Simulation setup based on the block diagram illustrated in figure 4.12. The analog input reference level is expressed in bit as well as the deviation to the respective level.

The validation by the investigation of the compensation method within the typical environment illustrates an impression of the compensation ability for the proposed approach. In order to verify the claim of PVT variation and statistical mismatch compensation, the analysis procedure was extended in scope of a Monte-Carlo analysis in combination with process corner variations. The statistical results of the investigation related to the uncompensated and the compensated conversion are compared by figure 6.5. In order to demonstrate the relation between deviations caused by non-linearity and the compensation method, a fixed analog input level was applied that offers an accordance of both systems in the typical case. Thereby, the corresponding input level is selected to a numerical representation of 120, thus that no deviation results in the typical case.

Figure 6.5(a) illustrates the Monte-Carlo deviations for the uncompensated case. Thereby, a broad scattering of the conversion results can be observed. In case the compensation method by inverse conversion is applied to the system, the scattering effect by deviations within the spectrum is reduced and centers the maximum of absolute deviations to zero as depicted in figure 6.5(b). As a result, the compensation method by inverse conversion compensates the majority of non-linearity deviations for the conversion result.

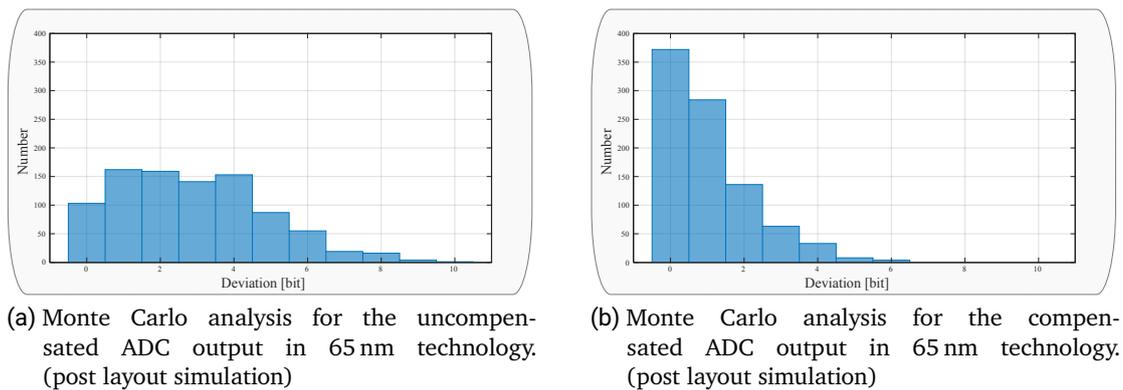


Figure 6.5: Monte Carlo analysis for the uncompensated ADC output in (a) and the compensated ADC output in (b). Simulation setup based on the block diagram illustrated in figure 4.12. Post layout simulation for 65 nm technology.

In order to investigate the compensation ability by the proposed inverse conversion method based on the design topology in figure 4.12 for general validity, the same procedure was applied to the 28 nm process node. Thereby, the system based on a regular conversion subsystem and an inverse conversion subsystem was implemented in conjunction with the process control unit. However, the global design parameter were extended in order to benefit from the advanced performance of the smaller technology node regarding switching and detection abilities especially in the digital domain. Thus, the 8 bit resolution of the 65 nm process was extended to 12 bit resolution for the 28 nm process and the reference step generation rate of 2 GHz (65 nm) was doubled to 4 GHz (28 nm). Based on the application of the inverse conversion method, the analysis of the dispersion effect was performed in combination with the input common mode related non-linearity by the direct application of the conversion algorithm based on the tracking scheme including jumps. The evaluation procedure for the 28 nm implementation is comparable to the evaluation procedure for the 65 nm implementation. Thus that the deviation of reference steps from

the absolute of respective analog input levels is analyzed by post-layout simulations for the typical case environment. In this way, the investigations were again performed for the uncompensated conversion result as well as for the compensated conversion result. Thereby, the constant analog input level as well as the deviation in reference steps is again expressed in a binary representation. The post-layout simulation results are illustrated in figure 6.6. Compared to the typical case environmental analysis for the 65 nm process the total non-linearity effect based on dispersion and IMCR limitation is significantly increased for the 28 nm process. It is caused by the faster reference step generation rate on the one hand. On the other hand, the technology transfer to a high performance computing (HPC) platform reveals physical limitations regarding the linearity of analog processes. However, the analysis revealed, that the applied compensation method by inverse conversion performs in the scope of total non-linearity compensation within a measurement tolerance of  $\pm 1$  LSB with respect to the typical case environment. Thus, a relation for the general validity within the constraint of a typical case environment is demonstrated, which implies for the necessary condition for the proof of concept.

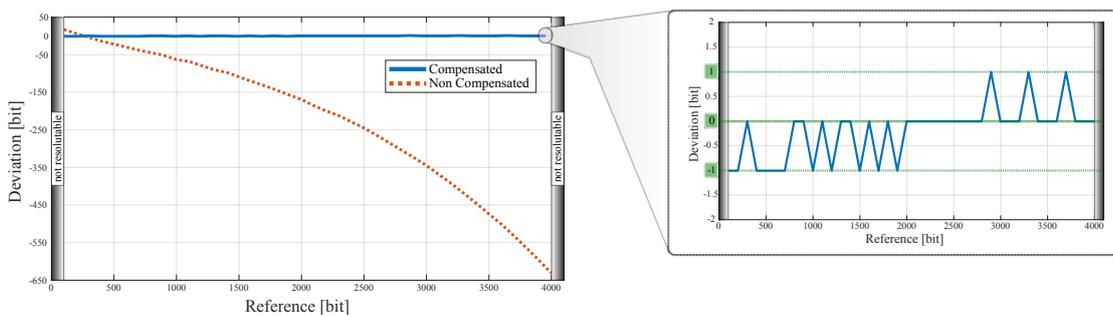
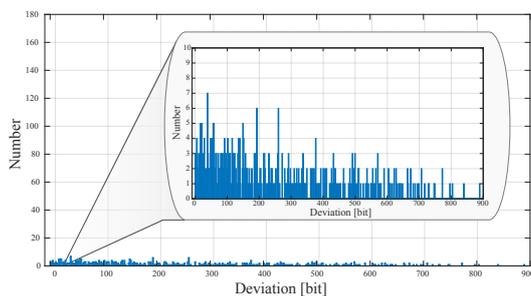


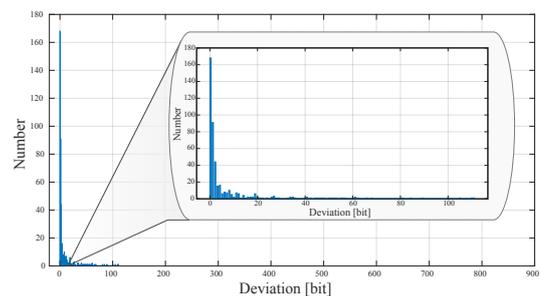
Figure 6.6: Non-linearity Compensation by Inverse Conversion related to the proposed method 2 (section: 4.2.2). Verification by post layout simulations in 28 nm technology. Simulation setup based on the block diagram illustrated in figure 4.12. The analog input reference level is expressed in bit as well as the deviation to the respective level.

In order to verify the general validity condition for the inverse conversion method in scope of a technology transfer, the compensation ability was evaluated for process, temperature and voltage variations (PVT) by a post-layout corner analysis. Thereby, the global process variations combined with a supply voltage drop of  $\pm 10\%$  and a temperature variation in range of  $-40^{\circ}C \rightarrow 125^{\circ}C$  were examined. In addition, the set of analog input levels within the total resolvable input range was performed in order to verify

the compensation methodology for a significant comparator non-linearity. Figure 6.7 compares the uncompensated results of the corner analysis with the compensated results of the corner analysis. As already derived for the 65 nm process node, the deviations of the uncompensated result are scattered across a broad spectrum, thus that the analysis of the uncompensated run reveals the need for a compensation method as illustrated in figure 6.7(a). In comparison, the depiction of the results of the post-layout process corner analysis of the compensation method in figure 6.7(b). Once again the ability to compensate by the inverse conversion method is revealed, thus that the majority of deviations are centered at zero. But compared to the 65 nm process node, the influence of PVT variations in the 28 nm node affects the accuracy of the compensation method. On the one hand the higher resolution (12 bit) and the lower power supply (0.9 V) is more sensitive to small environmental variations and on the other hand, the effect of physical mismatch induces higher losses (e.g. leakage current). Thus, a high deviation for a fast process corner combined with a slow process corner under a power supply drop of  $-10\%$  was observed. Thereby, it turned out that the drop in the supply voltage in particular causes a high level of inaccuracy. Due to this fact, a basic requirement for the ADC design in combination with the compensation method topology proposed in figure 4.12 implies, that a constant supply voltage is ensured.



(a) Process Corner analysis for the uncompensated ADC output in 28 nm technology. (post layout simulation)



(b) Process Corner analysis for the compensated ADC output in 28 nm technology. (post layout simulation)

Figure 6.7: Process Corner analysis for the uncompensated ADC output in (a) and the compensated ADC output in (b). Simulation setup based on the block diagram illustrated in figure 4.12. Post layout simulation for 28 nm technology.

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A particularity related to the increasingly scaling of technology nodes applies to the aspect, that the local process variations of integrated components is of more and more interest. Especially, the statistical mismatch variations for even local integrations causes non-linearity and inaccuracy for analog components. This aspect also implies for the proposed method of compensation by inverse conversion. Whereby an implementation of the topology method by a set of two equally designed ADC subsystems described in figure 4.12 is possible for the 65 nm node, already the analysis of the global process variations in the 28 nm node revealed a higher level of inaccuracy. This effect is increased, if the local mismatch variations are investigated in scope of a Monte-Carlo analysis. In this case, a compensation can still be established, but the deviations are significantly increased, thus that the compensation effect can not be verified for a general validity except a careful environment can be ensured. Related to that fact section 4.2 proposes the advanced version of the compensation method by inverse conversion. Due to the demand for a regular conversion cycle and a subsequent inverse conversion cycle the so far implemented topology is based on two equally designed ADC subsystems in combination with the process control unit. However, especially the implementation of two equally design topologies is prone for local mismatch and local variations. Therefore, the topology in figure 4.13 proposes the reduction of the second ADC subsystem, which eliminates the dependence of a second comparator identical in construction. Thereby, the compensation by inverse conversion is established by a second conversion cycle which is applied as inverse conversion right after the regular conversion. Thus, the regular conversion method as well as the compensation method by inverse conversion is applied by alternations. The process is controlled by an extended version of the process control unit (PCU) and the additional analog functionality is based on a further R2R scaling network and an analog multiplexer. Thereby, it needs to be ensured, that either the local process variations of the scaling network and the analog multiplexer satisfies the ADC linearity demands, or a training based on a measurement method needs to be performed as described in section 4.2.2.

So far the ADC prototypes in the 28 nm technology node were not implemented for the advanced version of the compensation method inverse conversion, because the pure functional analysis takes place under laboratory conditions. But related to the fact, that a careful environment can often just be established under laboratory conditions, the proposed method of advanced compensation was analyzed in scope of a detailed Monte-Carlo and corner analysis based on schematic simulations. Thereby, the evaluation of the proposed topology should be representative for future designs that are stabilized with respect to varying environmental conditions.

In scope of the detailed analysis, the general validity of the advance compensation topology was investigated for the typical case environment which describes the necessary condition for a verification. The schematic simulation results of the enhanced compensation design are compared to the post-layout results of the uncompensated design and reveal a comparable compensation ability as the unmodified version based on a two ADC subsystem topology. Thus, the deviations perform in the scope of total non-linearity compensation within a measurement tolerance of  $\pm 1$  LSB with respect to the typical case environment. The results for the constant input analysis are illustrated in figure 6.8 and verify the necessary compensation condition again.

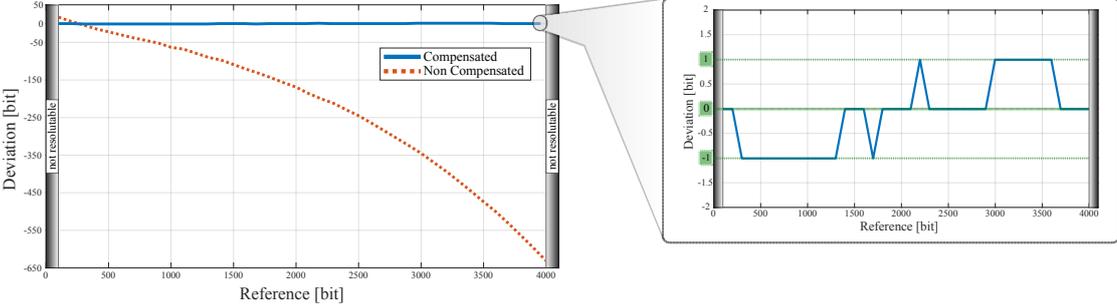
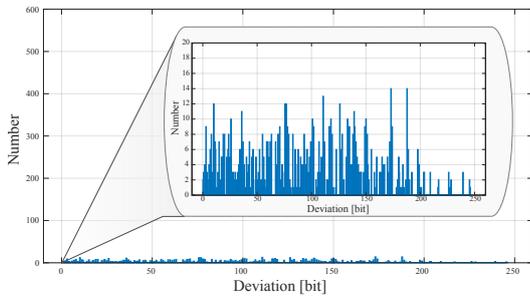


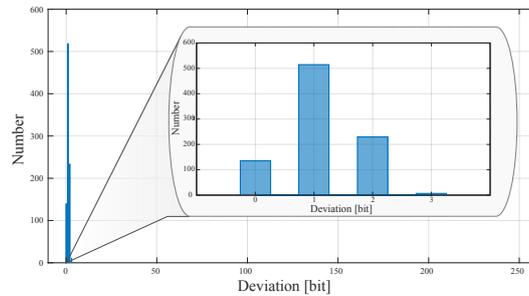
Figure 6.8: Non-linearity Compensation by Inverse Conversion related to the proposed method 2 (section: 4.2.2) based on advanced ADC compensation topology. Comparison between the uncompensated post-layout conversion result to the compensated schematic simulation result in 28 nm technology. Simulation setup based on the block diagram illustrated in figure 4.13. The analog input reference level is expressed in bit as well as the deviation to the respective level.

Based on the validity of the necessary compensation condition the detailed local process variations were examined by a Monte-Carlo analysis in scope of PVT variations. Therefore, the setup was established for a single analog input representation which corresponds to the center of the ADC input range by  $V_{in} = 450\text{mV} \rightarrow N_{in} = 2048$ . As already demonstrated for the Monte-Carlo analysis in the 65 nm process node, the distribution of the deviation from the actual input value describes the non-linearity under the influence of process related variations. In addition, the non-linearity compensation for any input level is confirmed by the typical case environmental analysis, thus that no distortion by input level variations are expected. In this way, the Monte-Carlo analysis was performed in scope of a schematic simulation for the advanced compensation method by inverse conversion

in order to provide a methodology for future designs. The results of the Monte-Carlo analysis including global and local process variations, voltage instability and temperature deviations are illustrated in figure 6.9 for the applied tracking scheme with jumps. Thereby, figure 6.9(a) depicts the distribution of the deviation for the uncompensated conversion result, where a significantly spreading of the deviation can be observed. Due to the fact, that the same environmental variations and mismatches apply for the single comparator and the variation is expected to be negligible within the period of one conversion cycle, the application of the inverse conversion method in a subsequent step for the same comparator enables the compensation of almost all non-linearity caused deviations. However, the majority of deviations is shifted to 1 LSB within a measurement tolerance of  $\pm 1$  LSB as illustrated in figure 6.9(b). Based on these results, the general validity of the advanced compensation method is confirmed and offers the opportunity for an application besides laboratory conditions.



(a) Monte Carlo analysis for the uncompensated ADC output in 28 nm technology. (schematic simulation)



(b) Monte Carlo analysis for the compensated ADC output in 28 nm technology. (schematic simulation)

Figure 6.9: Monte Carlo analysis for the uncompensated ADC output in (a) and the compensated ADC output in (b). Simulation setup based on the block diagram illustrated in figure 4.13. Schematic simulation for 28 nm technology.

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## 6.2 ASIC System Design and Experimental Setup

In chapter 5 the practicability and functionality of the proposed algorithmic tracking scheme approaches were demonstrated for a minimum set of required analog hardware. Thereby, the functionality of digital-to-analog conversion is established by a R2R scaling network and the comparative functionality was applied to a LVDS receiver of the FPGA. The actual operation of the investigated ADC sampling schemes was established in the digital domain based on FPGA operations. Thus, the proposed general purpose ADC is applicable for emerging integrated technologies. Due to the digital operations in the main, the proposed design can benefit from the performance improvement related to switching frequencies and power consumption. Especially, the fast switching frequency describes the main performance parameter in order to extend the bandwidth limitation of a tracking scheme ADC as described in chapter 3 and confirmed by FPGA implementations in chapter 5. These switching abilities also concerns to the propagation delay of the comparator. Thus, the faster the switching ability of the comparator, the higher the conversion rate. As predicted by the extended version of the general signal-to-noise ratio expression (Eqn: 3.8), the higher conversion rate results in a higher effective resolution. Related to the analysis in chapter 5, the algorithmic approach for the ADC implementation is based on the effective resolution enhancement method. Thus, the tracking scheme algorithm with jumps (section: 3.1.2 and 5.2.2) is applied to the integrated ADC design in scope of prototyping.

Related to the proposed architecture of the FPGA based ADC implementation in chapter 5 the system architecture of the ASICs is derived for a minimum set of analog hardware. Therefore, the basic analog operations are established by a R2R scaling network and a comparator which are representative for the feedback system of the ADC. With respect to the digital implementation of the tracking scheme algorithm digital blocks were generated by standard cell configurations due to synthesis and place&route operations. Thereby, this approach enables the digital configuration for a wide range of technology related integration possibilities in scope of programmability by hardware description languages. Thus, the previously described advantages of the digital FPGA design regarding configurability and generalization was transferred to the ASIC design. However, the approach of the analog feedback system based on the scaling network and the comparator implies a careful design on the one hand or a non-linearity compensation method on the other hand. Related to the fact, that the careful implementation of the feedback system is related to a linear operation which is robust against PVT variations and statistical process deviations by mismatch, the analog implementation is not able to benefit from full scope of technology scaling. Rather a robust implementation demands for high power

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consumption or a trade off with respect to the switching speed and comparator resolution. In comparison, the high linearity of the FPGA LVDS receiver is achieved by a moderate switching speed of 1 MHz and a high power consumption in addition. In order to avoid a high power consumption and simultaneously benefit from the advantage of fast switching speeds, the integrated designs suffer from non-linearity caused by physical limitations regarding dispersion affection, ICMR restriction and PVT variations. In order to avoid a high power consumption and simultaneously benefit from the advantage of fast switching speeds, the integrated designs suffer from non-linearity caused by physical limitations regarding dispersion affection, ICMR restriction and PVT variations in conjunction with mismatch. This effect increases with the shrinkage of technology nodes which implies, that the smaller the technology node, the harder to benefit from the advantages of fast switching speeds and low power consumption at the same time. Therefore, the proposed compensation methods were applied to the respective ASIC implementation which extend the functionality of the digital as well as the functionality of the analog ADC configuration. Related to the extension by compensation methods, the applicability and the functionality within an integrated ASIC design which suffers from non-linearity was investigated in previous section 6.1.2. Thereby, the validation of the compensation methods was confirmed by post-layout simulations. Therefore, the tracking and the correction method as well as the compensation by inverse conversion method was applied to a respective ASIC design in a 65 nm process node. Since the compensation ability by inverse conversion reveals a higher degree of conversion error correction for the contemplated design, the method was applied to a 28 nm technology process in addition. Thereby, the implementation was designed with respect to the topology in figure 4.12 for the tracking and correction method as well with respect to the topology in figure 4.6 for the inverse conversion method.

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## 6.2.1 ADC Implementation in 65 nm Process Node

The implementation of the respective ADC conversion and compensation methods is based on the proposed block diagrams (figures 4.6 and 4.12). Thus, the transfer of the block diagram for the tracking and correction method to a corresponding layout in a 65 nm technology node results in figure 6.10. Thereby, the analog blocks were implemented by a 8 bit R2R scaling network which is interconnected to the comparator, thus that the composition for the ADC feedback system is established. The scaling network represents the digital-to-analog operation and the comparator represents the one bit quantization operation of the feedback network. In order to provide the functionality of training sequence (section: 4.2.1) as well as the ADC functionality, the configuration was extended by an analog multiplexer (MUX) for the application of the respective input signal. Thereby, the training sequence requires the constant analog input which is provided by a bandgap reference circuit in scope of 8 equally distributed DC signals. In case the conversion functionality is enabled, the analog multiplexer turns to the analog input to be converted. The implementation of the proposed tracking scheme with jumps is derived as a standard cell placement which is developed from a register transfer level description by a synthesis and place&route tool chain. This approach concerns in general to the implementation of the entire digital operations that are proposed for the tracking and correction system, thus that the operations were described by a hardware description language (verilog) in total. Thereby, the tracking and correction functionality was applied by the digital description of the correction FSM with interpolation register block and the output correction block. Related to the proposed functionality the correction FSM is based on a finite state machine for the control of the process and a correction register which interpolates the correction results related to the constant reference of the bandgap circuit. The output correction block assigns the interpolated correction values to the uncompensated conversion result in order to establish the compensation functionality. The total square area of the layout implementation for the compensation method by tracking and correction results in  $230 \mu m \times 160 \mu m$ .

The transfer of the block diagram for the compensation method by inverse conversion is illustrated in figure 6.11. In order to provide a comparable ASIC level design between the two proposed compensation methods, the inverse conversion functionality was implemented in the same 65 nm process node. Thereby, the topology is based on comparators and R2R-scaling networks identical in construction as for the tracking and correction method. With respect to the extension in functionality, the requirement of the compensation method design by inverse conversion is established by the identical construction of two comparators. Related to the fact, that the placement of the comparators on the silicon die can be decisive about the affection on environmental stress like

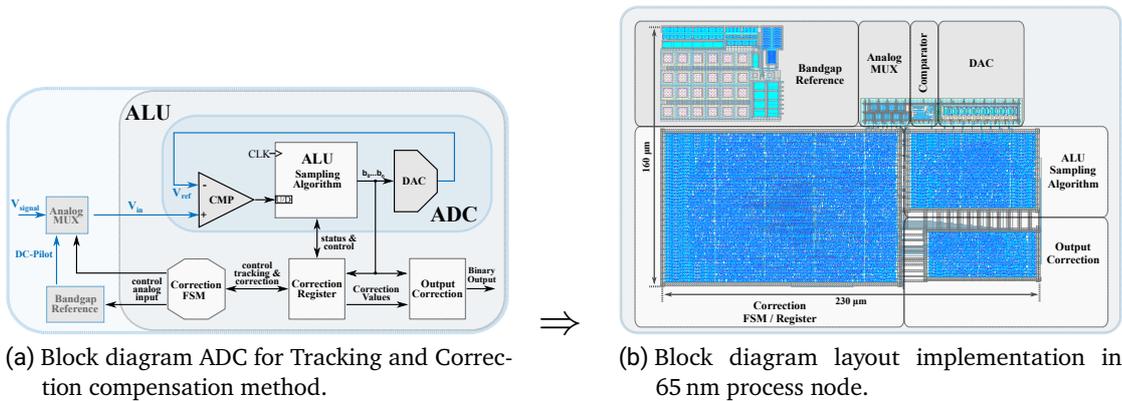


Figure 6.10: ASIC implementation in a 65 nm process node referred to the tracking and correction method as illustrated in the block diagram. Functional analog blocks: 8 bit R2R scaling network (DAC), comparator, analog multiplexer (MUX) and bandgap reference for constant analog DC levels provision (8 levels). Functional digital blocks: ALU implementation of the tracking scheme algorithm, a correction FSM with interpolation register application and output correction unit for the assignment of valid correction values to the uncompensated conversion result. Square area dimension:  $230 \mu\text{m} \times 160 \mu\text{m}$ .

PVT variations or statistical mismatch the comparators are placed as a cluster. Thus the non-linearity affection concerns both comparators in the same magnitude. In this way, an almost identical performance can be expected for both comparator implementations which property was validated by the post-layout investigation of the compensation method in previous section 6.1.2. Related to this criterion the DAC operations provided for regular conversion and for inverse conversion also demands for an adjacent placement as illustrated for the analog blocks in figure 6.11b. The actual functionality of the ADC was again derived by a register transfer level description which was translated by a synthesis and place&route tool chain into a standard cell based digital block design. Thus, the functionality of the tracking scheme implementation for regular conversion and for the tracking scheme implementation of inverse conversion was designed in conjunction with the process control unit (PCU) as a single digital block. Thereby, this approach satisfies a strict timing requirement of the interaction between the two conversion sequences that are controlled by the PCU. The total square area dimension of the compensation method by inverse conversion results in  $150 \mu\text{m} \times 130 \mu\text{m}$ .

Within the scope of the evaluation options both ADC implementations should communicate with a target platform. Therefore, additional digital operations extend the ASIC functionality in order to establish a transmission interface between the ADC implementation and the target platform. In this terms a communication based on a high speed serial transmission link was designed in order to provide a general interface to modern receiver systems. With respect to a high degree of configurability and flexibility the target is based on a FPGA platform which functionality provides the property of an integrated logic analyzer (ILA) and at the same time peripheral interfaces to state of the art processing systems. Thereby, modern systems demand for a transmission interface which is based on a serial stream with respect to a physical layer, a transaction layer and a link layer. In this terms, the layer description refers to the protocolling of a serial transmission scheme. Thereby, the ability of data throughput for a high-speed serial transmission interface is

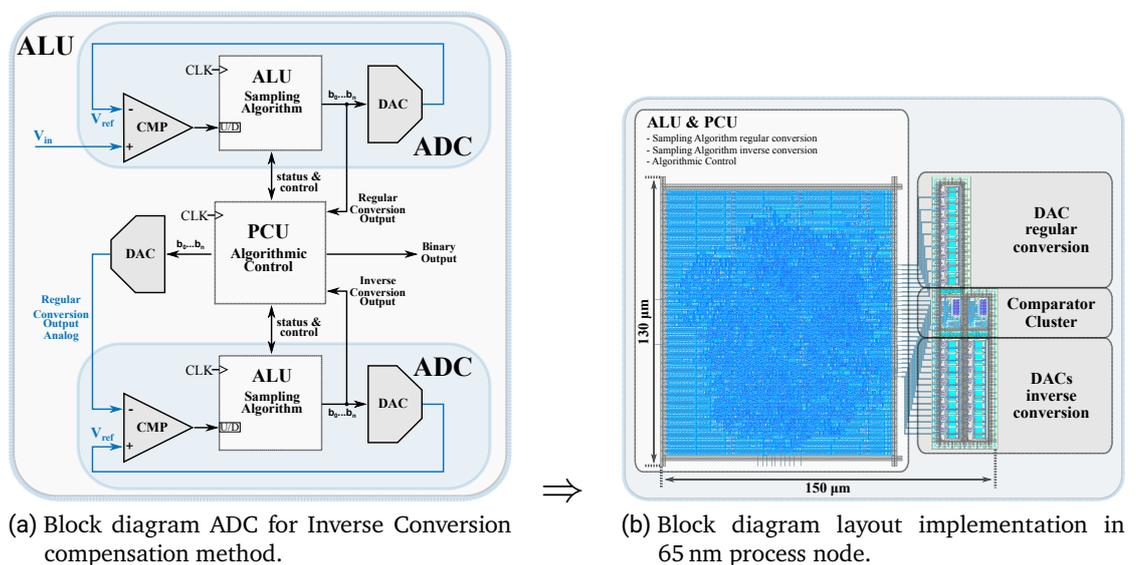


Figure 6.11: ASIC implementation in a 65 nm process node of the compensation by inverse conversion method as illustrated in the block diagram of figure 4.12. Functional analog blocks: 8 bit R2R scaling network (DAC) and a comparator (cluster) for regular conversion, two 8 bit R2R scaling networks (DAC) and a comparator (cluster) for inverse conversion. Functional digital blocks: Single block for regular and inverse tracking scheme algorithmic implementation including the process control unit (PCU). Square area dimension:  $150 \mu\text{m} \times 130 \mu\text{m}$ .

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limited by physical parameters like clock skew or DC unbalance during transmission. In order to prevent these limitations a self-synchronous timing model based on a conventional 8B/10B protocol encoding is applied. The use of this protocol enables clock-data-recovery (CDR) and DC-balance simultaneously. A digital module, providing the encoding, is part of the systems and transacts the serializer function in addition. Related to the reference frequency, the data transfer rate of the serial stream can be adjusted up to 2 Gbps. To improve the digital output signal integrity by sampling the non-uniform conversion time-steps, the ADC topologies are extended by a digital CIC-filter, which interpolates and low-passes the digital output to a desired frequency in order to be processed in further steps. Additionally, the desired frequency can be adjusted by one-hot-encoded states controlled by the FPGA. The digital standard cell extraction by synthesis and place&route results in a total square area layout dimension of  $190 \mu\text{m} \times 115 \mu\text{m}$  for the combination of the CIC structure and the digital transmission stream preparation.

To establish a communication between the ADC and the FPGA receiving module, the proposed designs are equipped with analog high-speed serial transmitting interfaces. The transmitter are based on half-rate source-series terminated (SST) designs [72, 73] and provide impedance calibration and adjustable pre-emphasis as described in [74, 75]. The transmission system is subdivided into two identical parts based on a calibration unit and a transmission unit. Additionally, a receiver module for the clock interface of the ADC was designed identical in construction. In advance to the data transmission a training is required which adjust the internal and external impedance by a search algorithm due to the selection of the right configuration by multiple pre-driver slices. For the sake of higher control degrees, a finite-state-machine (FSM) which applies a search algorithm for the configuration, is part of the FPGA implementation. The communication between FSM and transmitter calibration is based on a conventional SPI interface which transmits the evaluated slice configuration to the transmitter configuration as well as for the input clock receiver configuration with the completion of the training sequence. The respective transmission and receiving blocks are interfaced to the PADs of the ASIC. The physical signaling of the transmission and receiving is established by differential LVDS levels. The calibration system is equipped with a control FSM and interfaces an external reference resistor via an ASIC PAD in a single ended configuration. The total analog area of a single transmission block relates to  $150 \mu\text{m} \times 90 \mu\text{m}$  and total analog area of a single receiver block relates to  $130 \mu\text{m} \times 150 \mu\text{m}$ . The total analog area of the calibration block is subdivided in the digital control FSM which occupies an area of  $45 \mu\text{m} \times 50 \mu\text{m}$  and the calibration interface which occupies an area of  $100 \mu\text{m} \times 50 \mu\text{m}$ .

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Based on these configuration methods, the interface between the ADC ASIC and the FPGA target system was designed for the proposed tracking scheme ADC for the compensation method by tracking and correction as well as for the compensation method by inverse conversion. Thereby, both ADC implementations provide a resolution of  $N = 8$  bit and a maximum reference step generation rate of  $f_{\text{clk}} = 2$  GHz, which is defined by the ASIC input clock. Additionally, the maximum input clock is representative for the maximum data rate of the serial transmission interface with 2 Gbps in a Double-Data-Rate (DDR).

### 6.2.2 ADC Implementation in 28 nm Process Node

Related to the fact that emerging technology scaling promises an increase in performance with respect to the ratio between switching speeds and power consumption, the tracking scheme ADC design was implemented in a 28 nm process node. In order to compare the actual performance increase between the 65 nm technology node and the 28 nm technology node, the effective resolution enhancement tracking scheme by jumps (section: 3.1.2) was implemented in conjunction with the compensation method by inverse conversion. However, the analysis of the compensation method in section 6.1.2 revealed, that the ability of non-linearity cancellation is able to perform for a higher resolution, thus that the ADC was designed for 12 bit. In addition, the reference step generation rate was doubled to 4 GHz. Whereby, a parametrization by a more accurate resolution in conjunction with a higher reference step generation rate should demonstrate the possibilities by an application within a smaller technology node. In general, the transfer to a technology node of 28 nm in a high performance computing (HPC) technology enables a higher integration density for digital operations. Therefore, a higher degree of functionality implementation can be addressed to a single digital block that behavioral description of the register transfer level was translated to an extracted standard cell design by the synthesis and place&route tool chain. Thereby, the integration within a single digital block which includes the ADC operations as well as the serial stream preparation provides a higher degree of timing integrity due to the adjusted clock tree configuration. Related to this fact the functional block diagram of the ADC with the compensation method by inverse conversion extends the digital block diagram as depicted in figure 6.12(a). The transfer of the extended block diagram for the ADC with inverse conversion compensation method to a respective layout implementation is exemplified in figure 6.12. The layout transfer to of figure 6.12(b) demonstrates that the conjunction between the data processing system for the transmission and the ALU&PCU functionality benefits from the 28 nm technology node. However, the implemented digital block is occupied by the half of the possible integration density,

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thus a square dimension area of  $110\ \mu\text{m} \times 130\ \mu\text{m}$  results. In order to derive the same functionality of the physical layer for the serial stream by a 8B/10B protocol, the increased data width of 12 bit demands for a compression system which transfers the output vector of the ADC to an equivalent representation of 8 bit. Thereby, the compression model for the ADC output vector was derived from the tracking behavior of the ADC. Since the tracking scheme is based on a delta function between consecutive conversion cycles, the difference of the converted results is assumed as the representation of the ADC output. Thus, the information between consecutive conversion cycles is included as a portion of the total result. In this terms, the entire information of the first ADC result is transferred as the first and second compression vector which represent two consecutive 6 bit wide streams. In further proceedings the difference between successive ADC output vectors is transferred with an additional polarity state which describes a positive or negative delta. In case, the tracking scheme detects a difference which is greater than the foreseen binary stream vector, the initial start stream configuration is repeated. Thereby, an additional status information is transmitted within a 2 bit wide header of the compression stream. In this terms, the data processing for the transmission which is based on a reduced CIC stage, the 8B/10B conversion and the serializer is extended by the compression functionality and implemented in addition within the digital block. With respect to the increased reference step generation the digital implementation is clocked with 4 GHz, thus that the ALU&PCU which implements the regular and the inverse conversion is synchronous to the transmission system. Compared to the ASIC implementations in the 65 nm process, the serializer of the 28 nm ASIC is configured for a positive and negative clock edge operation. Thus that a double data rate transmission for 8 Gbps between the ASIC and the FPGA is established. In order to synchronize the FPGA high-speed receiver interface with the ASIC transmission interface digital 8B/10B module provides additional configuration interfaces which allows interrupts and clock synchronization. Therefore, the 8B/10B module in combination with the serializer was designed with respect to the FPGA receiver module.

The property of increased performance and enhanced integration density due to the technology transfer can be applied beneficial to digital operations in scope of the HPC technology on the one hand. But on the other hand analog operations demand for accuracy, which implies that a scaling in the implementation size either leads to performance reductions or is not applicable. Both assumptions concerns to the analog design, whereby the performance reduction regarding linearity of the comparator in scope of a fast switching ability was evaluated in section 6.1.2 and revealed the applicability of the compensation method by inverse conversion. Thus, the comparator cluster occupies an area of  $20\ \mu\text{m} \times 5\ \mu\text{m}$  (excluding wiring). But with respect to the analog performance and the integration ability of the R2R scaling networks, a reduction of the resistor size is not

applicable. Therefore, the focus for the scaling networks was on functionality, which also implies a symmetrical implementation and the provision of dummy resistors. Thereby, the total layout dimension of the 12 bit R2R scaling networks with additional dummy devices results in  $45 \mu\text{m} \times 300 \mu\text{m}$  for the composition of the regular conversion and the inverse conversion DAC components.

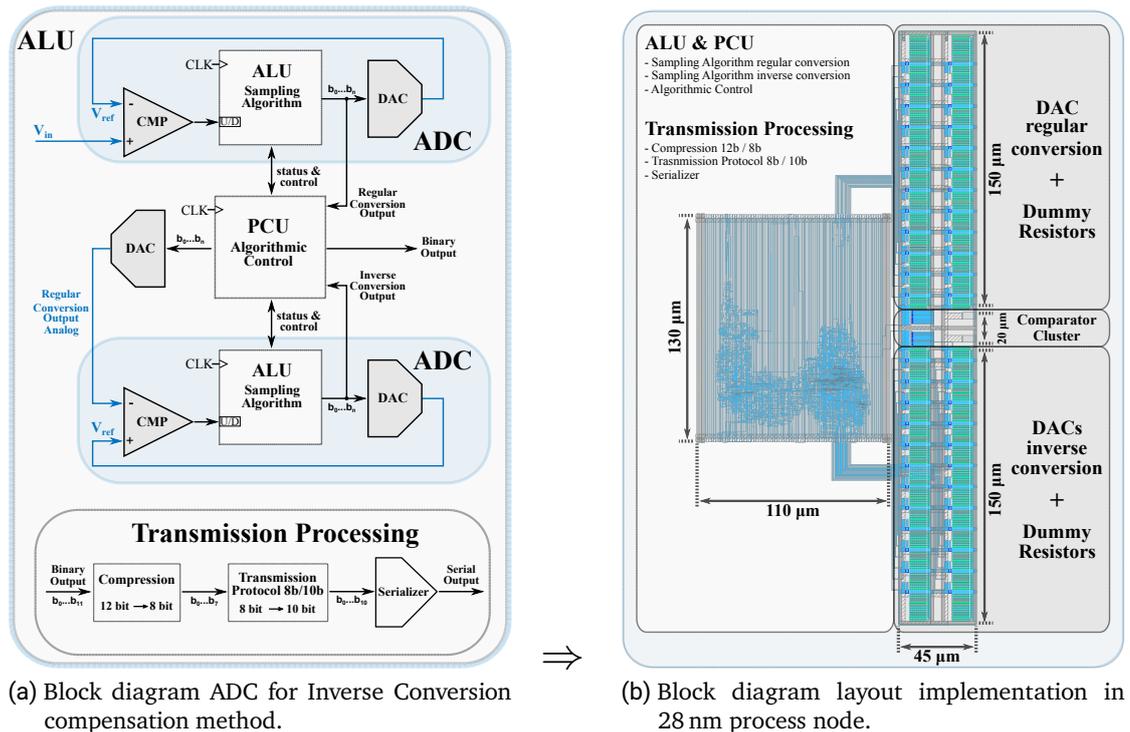


Figure 6.12: ASIC implementation of the compensation by inverse conversion method in a 28 nm process node. Functional analog blocks: 12 bit R2R scaling network (DAC including dummy resistors) and a comparator (cluster) for regular conversion, two 12 bit R2R scaling networks (DAC including dummy resistors) and a comparator (cluster) for inverse conversion. Functional digital blocks: Single block for regular and inverse tracking scheme algorithmic implementation including the process control unit (PCU) and additional data processing for output stream generation. Digital square area dimension:  $130 \mu\text{m} \times 110 \mu\text{m}$ , Analog square area dimension:  $45 \mu\text{m} \times 320 \mu\text{m}$ .

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As the ASIC implementations in 65 nm technology, the ADC in the 28 nm process node establishes a communication to a FPGA as target system. Therefore, also the 28 nm ASIC is equipped with analog high-speed transmitting and receiving interfaces based on Source-Series-Terminated (SST) transceiver design. The design procedure is comparable to the ASIC implementation in 65 nm, thus that a calibration in scope of a training sequence in advance of the actual transmission is processed. Therefore, the training sequence configures a subsystem based on a calibration interface to an external reference resistor by the selection of the required pre-driver slices in order to match the external and internal interface resistance. The configuration scheme of the search algorithm is provided by an integrated FSM on the ASIC, contrary to the 65 nm implementation where the FSM is located on the FPGA. Due to this fact, the configuration of the transmitter and the receiver is processed during the startup of the AISC. However, a SPI interface provides the possibility to reconfigure the FSM state regarding the pre-driver constitution and enables the tuning for the pre-emphasis slices. The transmission and receiving modules are interfaced to the PADS of the ASIC and provide the physical signaling by differential LVDS levels. The implementation area of the differential transmitter module with pre-driver and pre-emphasis slices occupies a square area of  $105 \mu\text{m} \times 130 \mu\text{m}$ . The area of the calibration module as well as the digital subsystem for the configuration amounts to  $50 \mu\text{m} \times 90 \mu\text{m}$ . The receiver unit is matched to a  $100 \Omega$  input resistance and waives a calibration. Therefore, the respective layout implementation occupies a reduced area of  $60 \mu\text{m} \times 20 \mu\text{m}$  which results in approximately 6.15% of the 65 nm receiver implementation.

Based on comparable configuration methods, the interface between the ADC ASIC and the FPGA target system was transferred for the proposed tracking scheme ADC with the compensation method by inverse conversion from the 65 nm process node to the 28 nm process node. Thereby, the ADC implementation provides a more accurate resolution of  $N = 12$  bit and an increased maximum reference step generation rate to  $f_{\text{clk}} = 4$  GHz related to the ASIC input clock. Additionally, the maximum transmission rate was increased due the utilization of a double edge triggered serializer, thus that a maximum transmission rate of 8 Gbps results with respect to the input clock frequency of 4 GHz.

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### 6.2.3 ASIC Prototypes and Evaluation System

Referred to the layout designs in 65 nm technology and in 28 nm technology 3 ASICs were designed. Thereby, the different compensation methods by tracking and correction (T&C) and inverse conversion (IC) were implemented in the 65 nm process node. Based on the post-layout results of the inverse conversion method in section 6.1.2 the ADC was transferred to the 28 nm process node in order to benefit from the high integration density and improved switching to power ratio of the high performance computing technology. With respect to compare the compensation method by tracking and correction with the compensation method by inverse conversion, both 65 nm implementations are based on the same analog components of the basic ADC design, thus that the influence of the ADC non-linearity in the feedback configuration can be expected in the same magnitude. The non-linearity based on the comparator dispersion effect and the input common mode range restriction was investigated in section 6.1.1 with respect to an ADC resolution of 8 bit which is provided by the R2R scaling network. The absolute limitation of the tracking scheme ADC was foreseen for a reference step generation rate which is equal to the clock rate with  $f_{\text{clk}} = 2 \text{ GHz}$ . Thus, based on the dispersion effect analysis of the comparator an overdrive/underdrive of  $N_{\text{disp}} = 5$  steps results. In conjunction with equation 5.4 the dispersion effect normalization by the crest ratio of a sinusoidal input and the applied tracking scheme with jumps is calculated to an average conversion rate of 346.4 MS/s. Since the application of an input clock of  $f_{\text{clk}} = 2 \text{ GHz}$  defines the maximum rating of the ADC, a performance drop was expected close to that limitation. As it turned out by the prototype evaluation in the later section 6.3, the recommended operating frequency should be limited to 1.6 GHz in order to maintain the ASIC performance. Therefore, the ASIC ratings regarding power consumption and conversion rate are referred to the input clock frequency of  $f_{\text{clk}} = 1.6 \text{ GHz}$ . With respect to equation 5.4 and a dispersion related deviation of  $N_{\text{disp}} = 4.5$  (figure: 6.2a) a conversion rate of  $f_{\text{conv}} \approx 308 \text{ MS/s}$  results for both ASICs within 65 nm technology implementation.

The power consumption of the ASIC implementations is derived from the basic ADC design. Thereby, the basic tracking scheme implementation with compensation by tracking and correction described by the layout in figure 6.10b is representative for a post layout power analysis. The results were evaluated as typical case analysis for a core supply voltage of 1.2V and an input clock frequency of 1.6 GHz. Thus, the average power consumption of the ADC with the compensation method by tracking and correction results in 3.65 mW. The analysis of the tracking scheme ADC with the compensation method by inverse conversion was based on the block components of the layout in figure 6.11b and was also evaluated as typical case analysis for a core supply voltage of 1.2V and an

input clock frequency of 1.6 GHz. Due to the extension of digital performance and the application of a second comparator-DAC based feedback configuration, the average power consumption of the ADC increases to 4.08 mW. Figure 6.13 illustrates the die photography and the specifications of the tracking scheme ADC with compensation by tracking and correction in the 65 nm process node. Figure 6.14 illustrates the die photography and the specifications of the tracking scheme ADC with compensation by inverse conversion method in the 65 nm process node. Furthermore, both chip photographs indicate the locations of the respective functional blocks. Thus, the peripheral interfaces for the communication with the FPGA target platform are characterized by the transmission interface (Tx), the calibration interface (Cal) and the high-speed receiver (Rx) block for the reference clock input. The pre-processing of the transmission protocol based on the physical layer, the transaction layer and the link layer is located close to the respective ADC as digital block configuration. This additionally applies for the high-speed serializer which establishes the serial link to the FPGA.

The dimension of both ASICs ( $1875 \mu\text{m} \times 900 \mu\text{m}$ ) encompasses a total silicon die area of  $1.6875 \text{ mm}^2$ . However, the actual ADC in composition with the peripheral interface arrangements occupies an area of  $0.07705 \text{ mm}^2$  for the tracking and correction method and an area of  $0.05975 \text{ mm}^2$  for the inverse conversion method. This implies, that the ADCs utilize an effective chip area of 4.57% and 3.54%, respectively.

<b>Technology:</b>	65 nm
<b>Compensation:</b>	Tracking & Correction
<b>Resolution:</b>	8 bit
<b>Avg. Conv. Rate:</b>	308 MS/s
<b>Avg. Power:</b>	3.65 mW

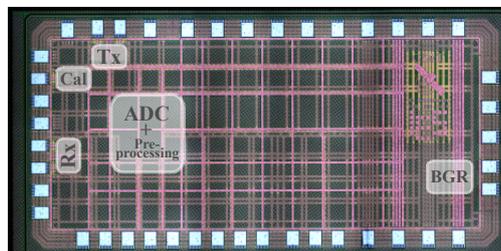


Figure 6.13: Die photography and specifications of the Tracking scheme ADC implementation with compensation method by Tracking and Correction (T&C) in 65 nm process node. Interfaces for high-speed communication with FPGA based target platform an reference clock input (Tx, Rx, Cal). Supplementary bandgap reference circuit for the provision of constant reference level for calibration sequence.

<b>Technology:</b>	65 nm
<b>Compensation:</b>	Inverse Conversion
<b>Resolution:</b>	8 bit
<b>Avg. Conv. Rate:</b>	308 MS/s
<b>Avg. Power:</b>	4.08 mW

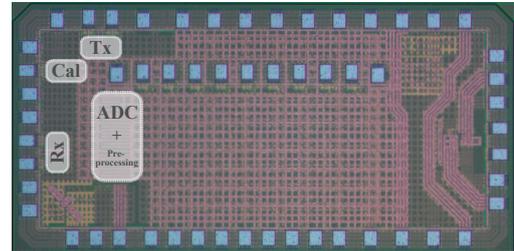


Figure 6.14: Die photography and specifications of the Tracking scheme ADC implementation with compensation method by Inverse Conversion (IC) in 65 nm process node. Interfaces for high-speed communication with FPGA based target platform an reference clock input (Tx, Rx, Cal).

The ASIC implementation of the tracking scheme ADC with compensation method by inverse conversion in the 28 nm process node is derived from the block layout in figure 6.12b. The ASIC layout draft is representative for the chip fabrication which is in progress, thus that the silicon evaluation is pending. Besides that fact, the post-layout evaluation results of the 28 nm ASIC are representative in scope of this work. Thereby, the specifications of the 65 nm ASIC with compensation by inverse conversion are extended by the transfer of the resolution towards 12 bit. Additionally, the switching speed of the high performance computing technology enables the increase of the clock frequency and therefore the increase of the reference step generation rate at the same time towards 4 GHz. In this context, the specified performance of the proposed ADC enhances in terms of an average conversion rate towards  $f_{conv} = 723 \text{ MS/s}$ . The conversion rate was extracted from a post-layout simulation of a 50 kHz sine wave input within a peak-to-peak range of  $[22 \text{ mV} \rightarrow 879 \text{ mV}]$ . Thereby, twice the average frequency of the 1 bit comparator transition output is representative for an average estimation of the conversion rate which is constituted by the high-to-low transition as well as by the low-to-high transition. The procedure in order to extract an approximate power consumption was derived from post-layout examinations of the analog components as well as the approximated results of the place&route tool for a worst case scenario. Therefore, the average power consumption of the ADC implementation related to figure 6.12b results in 7.97 mW for a core voltage

supply of 0.9 V. The total ASIC implementation which was prepared for fabrication is illustrated in conjunction with the expected specifications in figure 6.15. Besides the layout implementation of the ADC, the ASIC was also extended by the peripheral interfaces constituted of the high-speed serial transmitter (Tx), the calibration module (Cal) and the input clock receiver (Rx). Additionally, the technology requirements of a minimum amount of active components (i.e. transistors) demands for a cluster of dummy devices. In this context, the total area of the ADC in conjunction with the peripheral interfaces amounts to a total area of 0.04715 mm<sup>2</sup> (excluding dummy cluster). Since the total silicon die area of the ASIC encompasses to 0.48 mm<sup>2</sup>, the ADC implementation with communication interfaces occupies 9.82% of the available area.

<b>Technology:</b>	28 nm
<b>Compensation:</b>	Inverse Conversion
<b>Resolution:</b>	12 bit
<b>Avg. Conv. Rate:</b>	723 MS/s
<b>Avg. Power:</b>	7.97 mW

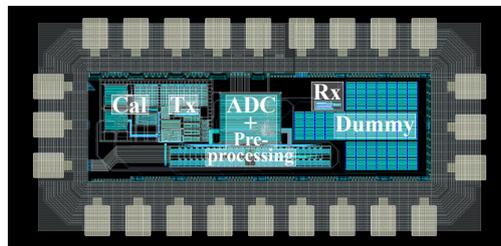


Figure 6.15: ASIC layout and specifications of the Tracking scheme ADC implementation with compensation method by Inverse Conversion (IC) in 28 nm process node. Additional interfaces for high-speed communication with FPGA based target platform by transmission interface (Tx), calibration interface (Cal) and high-speed receiver (Rx) for reference clock input. Transmission signal pre-processing located close to the ADC.

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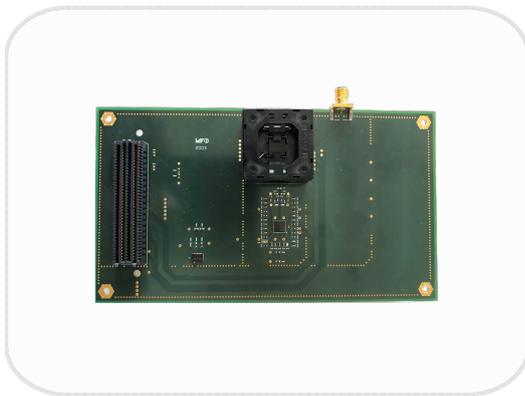
## Experimental Setup of the ASIC Evaluation System

The experimental setup for the ASIC evaluation is based on the FPGA target platform which provides a logic analyzer functionality and the interfaces to external systems within an industrial standard. A Xilinx Virtex 7 development board (VC709) [76, 77] as illustrated in figure 6.16(b) provides the basis for the FPGA sided evaluation. In order to interface the ASIC to the FPGA a printed circuit board was developed which interconnects as extension module in the FPGA Mezzanine Card (FMC) standard as illustrated in figure 6.16(a). Thus, the communication between the FPGA and the ASIC is established via the high pin count (HPC) FMC interface of the development board. Thereby, the FMC port provides a number of high-speed transceiver, whereby one of them is connected as receiver interface as the contrary side of the ASIC. The configuration for the transmitter is either implemented as finite state machine in case of the 65 nm ASICs or as communication system for the 28 nm ASIC. Thereby, the configuration of the ASICs is provided by FPGA operations which implies the forwarding of signals by SPI interfaces or soft-switches. The clock source of the ADC ASIC is established by a programmable PLL which is located in the proximity of the clock receiver port. Also the PLL is configured via a SPI interface, thus that it can be programmed by the FPGA implementation and controlled by soft-keys. Additionally, an accurate clock which is generated by a crystal oscillator ensures a stable reference for the PLL connected to the ASIC as well as the reference for the receiver PLL located on the FPGA. Thereby, the reference clock sharing ensures the signal integrity between the ASIC transmitter and the FPGA receiver side which is connected via the FMC interface. The power supply of the printed circuit board components as well as the ASIC power supply is established via the power interconnect of the FMC interface, likewise. Thereby, Low-Drop-Out (LDO) voltage regulators satisfy the component related demand for a constant supply.

The FPGA implementation of the receiver interfaces the high-speed serial output stream of the ASIC. In this terms, it defines the contrary part with respect to the transmission protocol. Therefore, a high-speed deserializer is provided by Xilinx IP which is extended by a customized 8B/10B decoding protocol in order to meet the ASIC requirements. In case of the interconnection to the 28 nm ASIC the receiving system is extended by a decompression module which implements the contrary properties of the ASIC 12B/8B compression module. In this way the conversion results of the ADCs are received and decoded. In scope of the ASICs which were fabricated in the 65 nm process node an average double data rate conversion of 308 MS/s can be achieved. Therefore, the reference frequency amounts approximately to 154 MHz. Related to this fact, the 65 nm ASICs were evaluated by an Integrated-Logic-Analyzer (ILA) core of the FPGA. In scope of the ASIC that are

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fabricated in the 28 nm process node, an average conversion rate of 723 MS/s is expected. Thus, a direct evaluation based on the ILA core is not applicable. Therefore, the received and decoded amount of data is foreseen to be forwarded to a desktop workstation via a PCIe interface of the FPGA development board. In this scope the FPGA implementation extends with the application of a Xilinx PCIe IP core which transmits the conversion result data as direct memory access to the workstation. The required Direct-Memory-Access (DMA) driver is constituted for a LINUX operating system and enables the evaluation procedure by desktop applications like MATLAB.



(a) FPGA Mezzanine Card (FMC) for target platform based ADC prototyping.



(b) ADC experimental setup based on FPGA development board interfaced by the ADC-FMC module.

Figure 6.16: Experimental setup for the evaluation of the developed prototypes. The ADC is located on a FPGA Mezzanine Card (FMC) which provides a PLL acting as clock source, a reference crystal oscillator and LDOs for a constant voltage supply. The ADC FMC board is connected to the FPGA and establishes a high-speed serial interface for data transmission. The PLL as well as the data transmitter are configured by the FPGA via SPI interface. The FPGA provides the power supply for the FMC board.

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### 6.3 ASIC Measurement Results

The ASIC prototypes which were fabricated in the 65 nm technology node were evaluated on the experimental system based on the FPGA target platform as described in section 6.2.3. Both prototypes implement the ADC conversion procedure based on the tracking scheme with jumps which is defined as (JASGA Tracking ADC). With respect to compensate the non-linearity affection of the conversion result two compensation methods were proposed and implemented in scope of the ASIC design. Therefore, one prototype is equipped with the compensation method by Tracking-and-Correction-Compensation and the other prototype is equipped with the compensation functionality by Inverse-Conversion-Compensation. In order to assess the non-linearity affected output signal of the ADC implementation one of the ASICs was equipped with the functionality to forward the direct conversion result without compensation. In this way, the compensation methods which were applied to the prototypes were evaluated in terms of a validation with respect to functionality. As an assessment criterion the signal-to-noise ratio (SNR) course of the ADC prototypes was detected in order to provide information about the dynamic performance of the ADCs. Furthermore, the affection based on non-linearity distorts the conversion result which implies that the evaluation was extended in scope of the signal-to-noise-and-distortion (SINAD) ratio. Thereby, the analysis of the SINAD course within the bandwidth of interest is informative about the compensation ability. Additionally, the evaluation of the static performance with respect to the differential and the integral non-linearity (DNL & INL) is informative about the misalignment of the binary assignment of the ADC. In order to establish a framework to assess and compare the compensation methods, the parametrization of 8 bit resolution was designed in scope of the implementation. To ensure the same environmental conditions a clock frequency (representative for the reference step generation rate) of 1.6 GHz was likewise applied to the respective ASIC prototype. Due to this parametrization an average conversion rate of 308 MSps was determined by the post-layout examination of the ADC feedback configuration in the 65 nm process as described in section 6.2.3. Thereby, the average conversion rate was traced back to the acceleration of the comparator decision due to the influence of the dispersion effect, which was derived from equation 5.4. The theoretical absolute bandwidth of the ADC was determined by equation 2.11 to  $f_{\max_{bw}} = 4.68$  MHz and defines the frequency range of interest in scope of the SNR/SINAD course analysis. The investigated input signal range of the ADC was traced back to the linearity analysis of the compensation method by inverse conversion, whereby the absence of deviations within the compensation ability determines the valid input range. Thus, the input range was constraint within a binary representation of 75 LSB  $\rightarrow$  225 LSB (351 mV  $\rightarrow$  1055 mV) with respect to the analysis in figure 6.4. Thereby, the restriction of the valid input signal range

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implies, that a maximum representable resolution of the ADC implementation reduces to  $N_{\max} = 7.23$  bit and indicates in ideal case where no conversion signal distortions are present.

Based on the defined set of ADC and input signal parameter, the ASIC prototype designs for the 65 nm process node were measured. Thereby, the results of the ADC design without compensation method serves as a basis for the evaluation of the proposed compensation methods. In order to illustrate the initial conversion ability of the uncompensated ADC tracking scheme a measurement of a sinusoidal input signal was performed and the result was compared to the actual input signal within the predefined input range. Based on equation 2.10 a limit for the full-scale resolution was determined to  $f_{\max, \text{res}} = 469$  kHz, thus that an input signal frequency of  $f_{\text{sig}} = 100$  kHz serves as reference in order to expect a full-scale conversion result. Figure 6.17 compares the actual input signal representation with the uncompensated conversion output. Thereby, signal distortions of the conversion result are signified as the deviation between the actual input signal and the uncompensated conversion signal. Related to the analysis of non-linearity effects in the feedback configuration of the ADC (section: 6.1) the distortions of the converted signal were identified for the comparator non-linearity based on ICMR restrictions and dispersion affections. In the following they are summarized as non-linearity distortions which needs to be equalized by the proposed compensation methods. In order to provide a complete impression about the conversion property, the dynamic performance based on the signal-to-noise ratio (SNR) is representative for the total binary alignment ability to the input signal and is signified by the respective effective resolution. While the analysis of the SNR provides an impression about the spatial assignment to a binary representation, the temporal assignment, which is decisive about the converted signal phase, needs to be represented by the signal-to-noise-and-distortion ratio (SINAD). In this terms, the total affection due to non-linearity distortions within a dynamic performance scope can be analyzed. Thus, the better the results of the SNR and the SINAD match, the less distortions by temporal misalignments can be processed. With respect to the static performance scope the differential and the integral non-linearity analysis provide statements about the actual deviation of the respective conversion assignments related to the respective binary representation. Thus, the higher the linearity of the static performance the less incorrect binary alignments are assigned. Based on these considerations the courses of the uncompensated SNR and SINAD within the frequency range of interest were calculated and the INL and the DNL were derived form the measured sinusoidal signal by MATLAB spectral tools as already performed for the previous investigations.

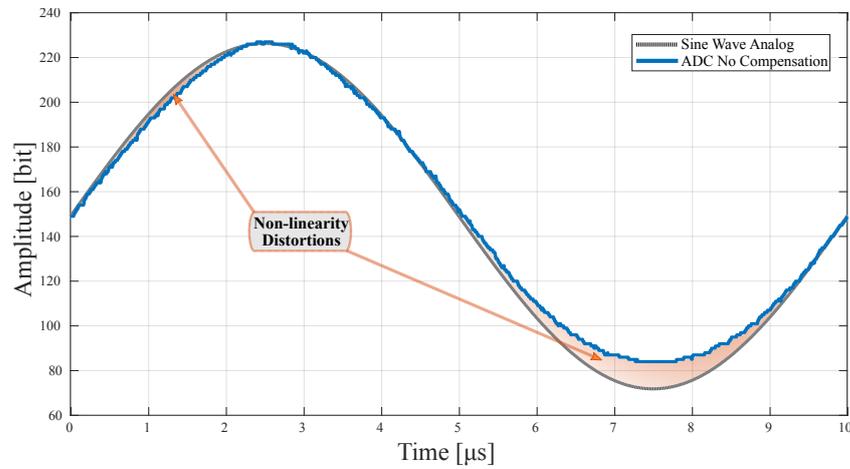
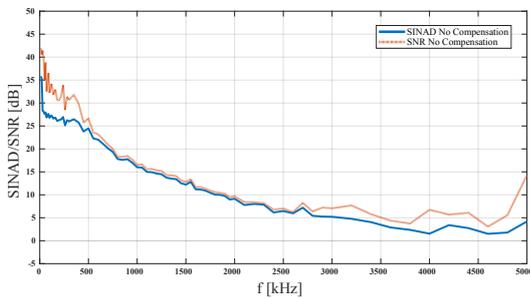
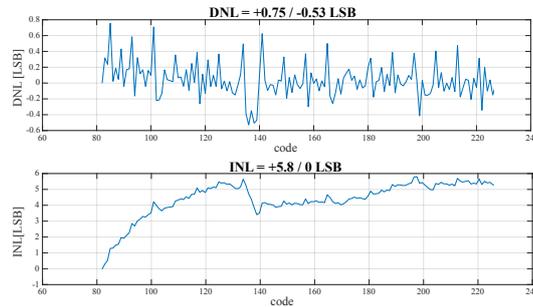


Figure 6.17: Comparison between the ideal input sine wave (100 kHz) and the measurement result of the uncompensated ADC output for the ASICs in 65 nm process node. Input signal range as binary representation of 75 LSB  $\rightarrow$  225 LSB. The conversion inaccuracy is signified by the non-linearity distortion.

Figure 6.18(a) reveals the uncompensated SNR and SINAD curves which were derived from the conversion result. Due to the influence of non-linearity effects the performance of the uncompensated ADC is reduced regarding the full-scale effective resolution. Considered separately, this implies that the effective resolution derived from the signal-to-noise ratio results in 6.68 bit (compared to full-scale: 7.23 bit). However, the reduction of the SINAD compared to the SNR signifies, that the non-linearity affection introduces temporal distortions to the conversion result which leads to a further reduction of the effective resolution by 1 bit to 5.68 bit. Thereby, the effect of distortions can be also observed for the static performance analysis which is based on the DNL and the INL investigations. In this terms, a differential non-linearity below 1 LSB satisfies the demand for a lossless conversion, but excludes additional missing codes within the valid input range of the ADC. Thus, the conversion result defines a clipped input range by approximately 10 LSB. However, the integral non-linearity reveals a deviation of 5.8 LSB which can be traced back to the non-linearity affection by the comparator. With respect to an input signal code representation below 140 LSB the distortions increase which is likewise signified by the DNL. Indeed, with respect to the investigation of a constant input signal by post-layout simulations this effect was predicted for a code representation of 100 LSB as illustrated by figure 6.4. As a result, the ADC implementation demands for compensation methods that equalize the non-linearity distortion.



(a) Comparison SINAD and SNR measurement results of the ADC with no compensation (JASGA Tracking ADC in 65 nm).



(b) ADC linearity measurement results (DNL, INL) of the uncompensated conversion result (JASGA Tracking ADC in 65 nm).

Figure 6.18: ASIC measurement results for the implemented tracking scheme algorithm with jumps (JASGA Tracking ADC) in a 65 nm process. The conversion result is uncompensated and reveals a distortion due to non-linearity effects as depicted by the SNR and SINAD measurements in (a) and the DNL and INL measurements in (b). Parameter: resolution ( $N = 8$  bit), step generation rate ( $f_{\text{ref}} = 1.6$  GHz) and dispersion ( $N_{\text{disp}} \approx 4.5$ ) affected conversion rate as described in section 5.2.2 ( $f_{\text{conv}} = \sqrt{3} f_{\text{step}} / (2 N_{\text{disp}}) \approx 308$  MHz).

Related to the ADC demand of compensation methods the tracking and correction (T&C) functionality and the inverse conversion (IC) functionality were implemented in conjunction with the ADC tracking scheme. The ASIC which is illustrated in figure 6.13 implements the tracking and correction method. Based on this application, the compensation procedure reveals an improvement of the converted output signal with respect to the range of the sinusoidal input signal. As depicted in figure 6.19 a comparison between the input signal and the converted output signal indicates that the clipping of the input range is compensated. However, the non-linearity distortions based on spatial misalignment are reduced in the main, the temporal misalignments remain and introduce phase noise to the converted output.

Compared to the results without compensation an enhancement of the signal-to-noise ratio for a broader input frequency range (200 kHz to 500 kHz) can be observed. This implies an increase of the effective resolution of  $\sim 0.66$  bit (4 dB) related to an increase of the input frequency. Therefore, the compensation method enables a higher accuracy of the ADC in case of an increasing input signal slope. This aspect also concerns to the SINAD of the compensated conversion result as depicted in figure 6.20(a).

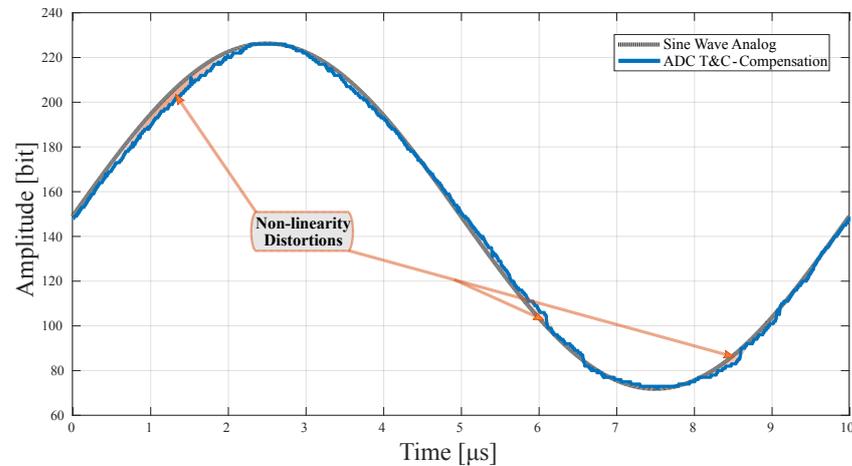
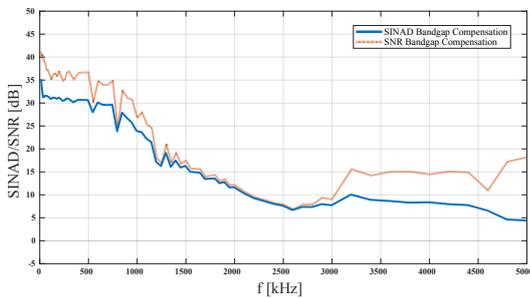
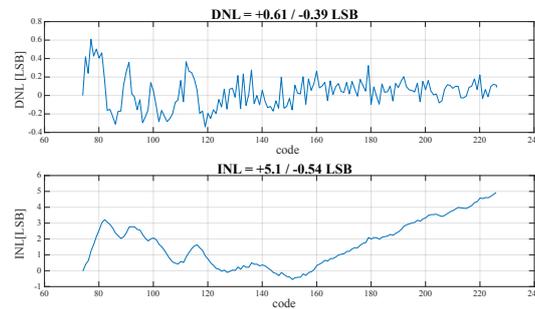


Figure 6.19: Comparison between the ideal input sine wave (100 kHz) and the compensated measurement result by tracking and correction (T&C) in 65 nm process node. Input signal range as binary representation of 75 LSB  $\rightarrow$  225 LSB. The conversion inaccuracy is signified by the non-linearity distortion.

So, the correction method reveals the property of accuracy improvement in scope of the dynamic behavior. Whereby, this property is signified by the reconstruction of the clipped input amplitude. Though, a difference of the maximum effective resolution by 1 bit remains between the SNR (6.68 bit) and the SINAD (5.68 bit). Based on this fact it can be concluded, that the temporal distortions due to non-linearity effects are not compensated. Thus the unchanged relation between the SNR and the SINAD remains as likewise illustrated by the direct comparison. The results imply, that the tracking and correction method amplifies the effective resolution compared to the uncompensated conversion result within a specific frequency range on the one hand. But on the other hand it is not able to equalize the distortions due to binary misalignment by temporal distortions in the main. This aspect is also confirmed by the result of the static performance of the ADC in conjunction with the investigated compensation method. As illustrated in figure 6.20(b) a slightly improvement of the differential non-linearity can be observed, but the main INL deviation remains at a maximum of 5.4LSB. Thus, temporal signal distortions that leads to binary misplacement are not compensated and also some spatial misalignments remain. This effect can be traced back to the less number of 8 reference level which are provided by the bandgap circuit in order to process the training sequence (section: 6.2.1).



(a) Comparison SINAD and SNR measurement results of the ADC with non-linearity compensation by tracking and correction (T&C).



(b) ADC linearity measurement results (DNL, INL) of the compensated conversion result by tracking and correction (T&C) method.

Figure 6.20: ASIC measurement results for the implemented tracking scheme algorithm with jumps in a 65 nm process. Partially compensated conversion by the tracking and correction method due to SNR and SINAD amplification in (a). Uncompensated distortions depicted by DNL and INL measurements in (b). Parameter:  $N = 8$  bit,  $f_{\text{ref}} = 1.6$  GHz,  $f_{\text{conv}} \approx 308$  MHz.

As the evaluation of the tracking and correction method reveals, the compensation ability is restricted to the property of the bandgap circuit to provide a sufficient number of reference levels. So, the higher the number of reference levels, the more accurate the reconstruction of the uncompensated conversion signal. Therefore, the application of an interpolation stage was implemented to the tracking and correction method (section: 4.2.1). So, the linear interpolation improves the signal accuracy related to the binary alignments, but is not able to compensate temporal inaccuracy. This leads to the conclusion, that the number of reference levels needs to be increased in order to improve the signal quality by a higher number of correction levels. The compensation method by inverse conversion proposes a method to assign the equivalent portion of the current correction level to a subsequent conversion step. Due to the application of the inverse conversion as a subsequent step to the regular conversion the correction level is assigned by the same magnitude as the deviation level (section: 4.2.2). This behavior was examined based on a static functionality analysis by the conversion of DC signals in scope of post layout simulations as performed in section 6.1.2. As an extension of the static functionality, the dynamic functionality considers the conversion time deviations in addition. Thus it is expected due to the linear dependency between the conversion time and the conversion result in magnitude that the application of the inverse conversion cancels the magnitude deviation as well as the time deviation. Thereby, the compensation method by inverse conversion is

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expected to be able to equalize the deviation in magnitude as well the deviation in time. Thus the main portion of non-linearity effects can be compensated for the spatial binary misalignment as well as for the temporal misalignment in the phase of the converted signal.

The signal analysis in figure 6.21 illustrates the comparison of the ideal input sine wave to the measurement results of the compensated ADC output by inverse conversion. As predicted by the evaluation of this compensation method in section 6.1.2 the equalization of the binary misalignment can be validated by measurement results. Furthermore, the temporal misalignment is compensated, thus that the conversion result is equivalent with respect to the phase progression of the input signal. However, non-linearity distortions occur for the transition moments related to the switching of the most significant bit (binary state: 128). Thereby, these transition moments signify the most critical state of the reference signal which is generated by the R2R scaling network and can be traced back to the maximum amount of load charge and discharge processes. This effect was already investigated in relation to non-linearity effects of the FPGA implementation in section 5.2.

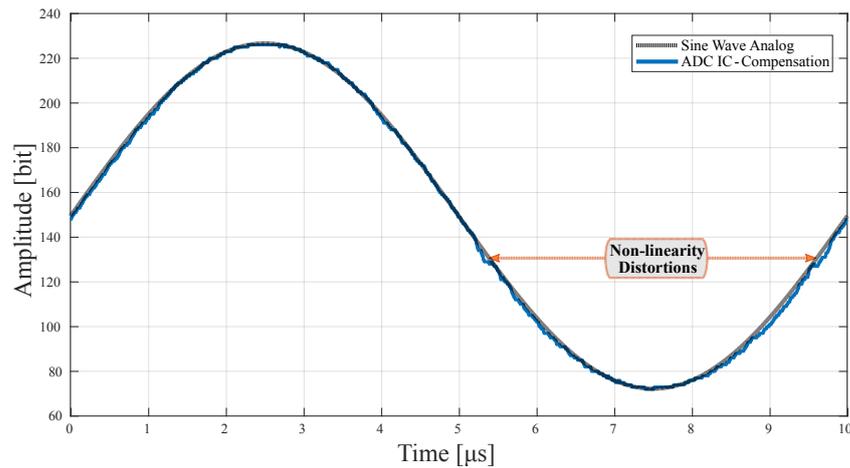
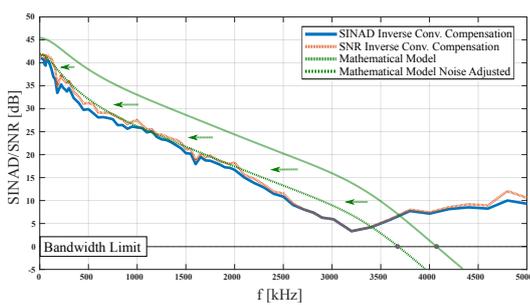
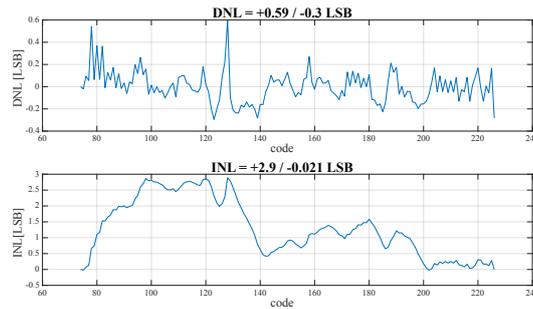


Figure 6.21: Comparison between the ideal input sine wave (100 kHz) and the measurement result of the compensated ADC output by inverse conversion (IC) for the ASICs in 65 nm process node. Input signal range as binary representation of 75 LSB  $\rightarrow$  225 LSB. The conversion inaccuracy is signified by the non-linearity distortion.

In order to validate the ability to equalize temporal misalignments under the application of the compensation method by inverse conversion the deviation between the SNR and the SINAD signifies the portion of phase noise. Indeed, as illustrated in figure 6.22(a) the proposed method provides the ability to compensated the temporal misalignments which is indicated by the proximity between the course of the signal-to-noise ratio and the course of the signal-to-noise-and-distortion ratio. Almost a complete agreement can be determined, which improves the low-frequency range in particular. Related to this aspect the static performance of the ADC is additionally improved compared to the design implemented with the tracking and correction method. Therefore, a reduction of the deviations within the DNL to below 0.5 LSB is validated, except the MSB transition for a code representation of 128. However, the greater effect can be observed for the integral non-linearity. By the application of the compensation method by inverse conversion, the deviation is reduced to a value of 2.9 LSB which corresponds to the half of the initial result. Again, this deviation can be traced back to the critical MSB transition.



(a) Comparison SINAD and SNR measurement results of the ADC with non-linearity compensation by inverse conversion (IC).



(b) ADC linearity measurement results (DNL, INL) of the compensated conversion result by inverse conversion (IC) method.

Figure 6.22: ASIC measurement results for the implemented tracking scheme algorithm with jumps in a 65 nm process. Non-linearity compensation by the inverse conversion method due to SNR and SINAD amplification and distortion equalization in (a). Improved DNL and INL measurement results in (b). Parameter: resolution ( $N_{R2R} = 8$  bit,  $N_{amp} = 7.22$  bit,  $N_{max} = 6.68$  bit), step generation rate ( $f_{ref} = 1.6$  GHz) and dispersion ( $N_{disp} \approx 4.5$ ) affected conversion rate ( $f_{conv} \approx 308$  MHz).

Since the inverse conversion method provides the ability to compensate the temporal misalignment, thus that the SNR represents approximately represents the SINAD, the measurement results can be compared to the mathematical model of the SNR. Due to the restriction of the input signal amplitude to a maximum resolution of 7.22 bit the extended mathematical model of equation 3.8 needs to be applied. In this way, the extended general SNR expression for non-uniform sampling provides the degrees of freedom to adjust the amplitude resolution ( $N_{\text{amp}}$ ) as well as the temporal resolution ( $N_{\text{ref}}$ ) in relation to the R2R scaling resolution of  $N_{\text{R2R}} = 8$  bit. Thereby, an amplitude resolution of  $N_{\text{amp}} = 7.22$  bit is represented in terms of the input signal. The temporal resolution increases by the amplitude resolution related difference ( $N_{\text{ref}} = 2 \cdot N_{\text{R2R}} - N_{\text{amp}} = 8.78$  bit). In this way a relation between the scaling network resolution and the amplitude resolution can be established. The further parameterization of the remaining degrees concerns to the reference step generation rate and the conversion rate. In this terms, the reference step generation rate of  $f_{\text{clk}} = 1.6$  GHz is represented by the input clock of the ADC. The average conversion rate of the non-uniformly sampled result was determined by the basic propagation delay of the feedback configuration in conjunction with the acceleration based on the dispersion effect. Therefore, the dispersion affected conversion rate refers to the applied reference step generation rate by a deviation of  $N_{\text{disp}} \approx 4.5$ . In this terms implies that the conversion rate results in  $f_{\text{conv}} = 308$  MHz as derived in section 6.2.3. The result of the ideal SNR course which was calculated for the frequency range of interest (limited by  $f_{\text{max, res}} = 469$  kHz) is depicted in figure 6.22(a). However, as a result the comparison between the ideal model and the measurement results reveals a deviation. This aspect implies that further noise is present within the conversion result, but the course of the SNR matches. In order to validate the exact result the maximum possible resolution of the measurement result needs to be considered as resolution limit. Related to that fact, the maximum of the measured SINAD of approximately 42 dB corresponds to the actual resolution of  $N_{\text{max}} = 6.68$  bit. Based on this aspect, the general SNR expression was reevaluated with respect to the adjusted amplitude resolution and the adjusted temporal resolution. Thus, the calculated SNR course corresponds exactly to the measurement results. However, a slight deviation between 0.5 LSB to 1 LSB can be observed for the higher input frequency investigations in the proximity of the bandwidth limitation. This effect can be traced back to measurement uncertainties due to the spectral evaluation as described in section 2.1.4.

In conclusion, the evaluation based on the comparison between the measurement result and the adjusted mathematical model demonstrates the confirmation between the theoretical approach and the practical implementation. Indeed, the adjustment of the degrees of freedom for the general SNR expression signifies the prediction ability of

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non-ideal measurement results. Furthermore, the application of the inverse conversion model compensates the non-linearity effects that introduce temporal mismatch and therefore enables the exact validation between the measurement and the theoretical approach. Additionally, non-linearity effects with respect to spatial misalignment as represented by the MSB uncertainty can be considered within the expression as an offset parameter. Therefore, the proof of concept validates the theoretical approach by a practical analysis. Or considered vice versa, the functionality of the proposed ASIC implementation in the 65 nm process node is confirmed.

With respect to the proof of concept validation in the 65 nm process node the design of the algorithmic tracking scheme ADC, which was extended by the compensation method of inverse conversion, was transferred to a 28 nm technology node. Thereby, the implementation was performed in relation to the ASIC layout in figure 6.15. Compared to the 65 nm node the parametrization of the ADC was enhanced based on the advantages of the 28 nm technology regarding switching speed and power consumption. Thus a global resolution of 12 bit within an algorithmic reference step generation rate of 4 GHz were implemented for the enhanced design. Based on post layout simulation results an average conversion rate of 723 MS/s could be established in scope of a double data rate.

In order to evaluate the proof of concept and the ability of advanced performance properties the investigation of the 28 nm implementation concerns to the dynamic and static behavior of the ADC conversion result. Likewise the evaluation process was performed as for the 65 nm technology node. However, due to the unavailability of the fabricated ASIC at the moment of the evaluation, post-layout simulations were performed in scope of the validation. Therefore, the results of the post-layout simulations provide a first impression of the expected ASIC performance. Initially, the valid input frequency range was determined based on equation 2.11 for the maximum expectable input bandwidth. Related to the basic ADC parameter with respect to a resolution of  $N_{R2R} = 12$  bit and a maximum reference step generation rate of  $f_{clk} = 4$  GHz a maximum input bandwidth of  $f_{max_{bw}} \approx 732$  MHz results by calculation. However, the bandwidth of the 28 nm ADC is lower than the bandwidth of the 65 nm ADC. Whereby, this is related to the fact, that the resolution was increased by 16 times, but the maximum reference step generation could only be increased by 2 times. This aspect concerns to physical technology limitations regarding switching speeds on the one hand. But on the other hand, this approach enables the evaluation property of higher resolutions. Therefore, conclusions based on the applicability of the proposed concept can be established in scope of physical limitations.

As for the 65 nm implementation an investigation of the sine wave conversion result was performed in advanced. Thereby, the input signal range of the ADC was derived from a 0.9 V core supply of the AISC in reference to the investigations of the static input compensation in figure 6.6. Due to the fact, that a level crossing detection is derived by the overdrive/underdrive of the input signal by the generated reference signal a valid input range of the ADC was verified for 22 mV to 879 mV which corresponds to a resolution range of 100 LSB to 4000 LSB. In order to evaluate the conversion ability of the sine wave function in scope of an accurate representation within the ADC specifications, the input frequency limit for a maximum resolution was derived from equation 2.12 and results in  $f_{\max_{\text{res}}} \approx 68.8$  kHz. With respect to provide a signal property which is in the proximity to the calculated limit a maximum resolvable input signal was evaluated for 50 kHz and thus offers a deviation specific overhead. The conversion results are compared to the ideal input representation in the depiction of figure 6.23. Globally considered, the result represents the input sine wave, but distortions become obvious in scope of a more detailed insight in the conversion result. Thereby, spatial misalignments were revealed as depicted exemplary by non-linearity distortions. Indeed, the distortions can be again traced back to inaccurate switching properties of the R2R scaling network.

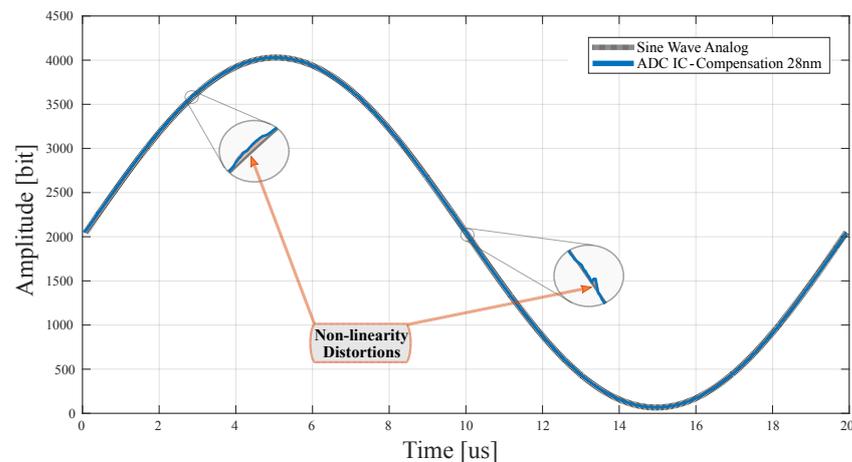


Figure 6.23: Comparison between the ideal input sine wave (50 kHz) and the post-layout simulation result of the compensated ADC output by inverse conversion in a 28 nm process node. Input signal range as binary representation of 100 LSB  $\rightarrow$  4000 LSB. The conversion inaccuracy is signified by the non-linearity distortion.

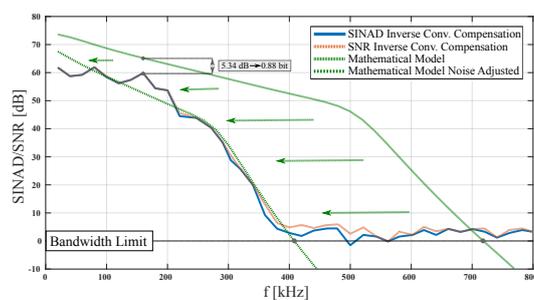
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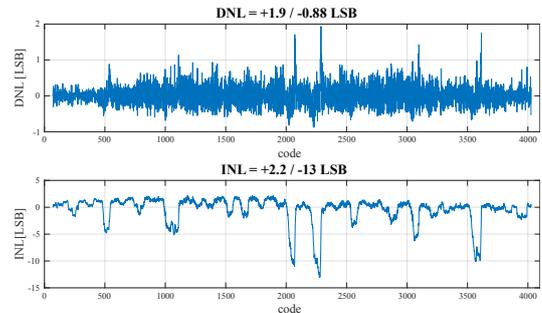
Related to the evaluation of the entire ADC bandwidth ( $f_{\max_{\text{bw}}} \approx 732$  MHz), which was derived as theoretical limit by equation 2.11, the analysis of the SNR and the SINAD were performed. As illustrated in figure 6.24(a) the previous assumption, that the non-linearity distortions refer to spatial misalignment due to the scaling network inaccuracy, is confirmed. Therefore, the application of the compensation method by inverse conversion enables the equalization of temporal misalignments. Therefore, as also confirmed for the 65 nm technology node the derived results of the SNR and the SINAD likewise agree for the 28 nm technology node implementation. Additionally, the maximum effective resolution of the compensated ADC implementation in 28 nm results in a distinct enhancement compared to the 65 nm results. Thus, due to the fact of a 16 times higher reference resolution an effective resolution of  $\approx 10.14$  bit (62 dB). This result corresponds to an absolute enhancement due to a 11 times more accurate representation in comparison to the 65 nm process (6.68 bit/42 dB).

As a result, the comparison between the 65 nm implementation and the 28 nm implementation demonstrates that the ADC performance can be enhanced due to the technology transfer. In this terms, a higher conversion rate implies the possible application of a higher resolution. Again, the verification of the improved performance ability was compared to the results of the ideal representation related to the calculated SNR course. Therefore, the calculation of the ideal results were also performed with respect the general SNR equation (Eqn. 3.8). As the comparison between the derived bandwidth of 732 MHz by calculation and the actual bandwidth limitation by simulation results ( $f_{\max_{\text{bw}}} \approx 406$  MHz), a distinct degradation of the SNR course results. Figure 6.24(a) illustrates the comparison between the simulated and the calculated results of the SNR courses, which indeed indicates the degradation. However, also the previous evaluation of the 65 nm results indicated that a parameter adjustment of the mathematical expression the validation of the ADC functionality within the scope of a non-ideal performance. Thereby, the determination of the slightest deviation between the ideal and the non-ideal results defines a reference for the parameter adjustment. But due to simulation uncertainties of the non-uniform conversion result, the slightest deviation is not assigned to the maximum resolution. Therefore, a representative deviation of 5.34 dB is revealed which corresponds to a resolution drop of 0.88 bit. Based on this examination the general SNR expression was reevaluated for an amplitude resolution equal to the maximum resolution of ( $N_{\text{amp}} = N_{\text{max}} = 11.12$  bit). As a result, the reevaluated SNR course matches the simulated SNR course. Indeed, also the drop of the calculated bandwidth limitation corresponds to the simulation results. This aspect implies, that the representable effective resolution of the ADC defines a crucial parameter in order to achieve the entire possible frequency scope. This effect was also observable for the 65 nm implementation, but the influence of a bandwidth limitation drop is more distinctive for an increasing reference resolution.

Based on the aspect of a performance reduction, especially for the relation between the bandwidth limitation and the effective resolution, the investigation of the static ADC performance also demonstrates this effect. In scope of the non-linearity examination the results of the DNL and INL were derived from a converted 50 kHz input signal (figure 6.23) by a spectral analysis. Thereby, the influence of the non-linearity which is based on distortions is signified with respect to the DNL and INL analysis in figure 6.24(b). Due to the distortions, the differential non-linearity results in a maximum of 1.9 LSB. However, the affection of the integral non-linearity is obviously higher. In this terms, a maximum deviation of 13 LSB was simulated. This implies, that the affection due to an inaccurate switching of the R2R scaling network is significant. With respect to the dynamic signal conversion respective binary reference steps are presented as spatial misalignment of the conversion result.



(a) Comparison SINAD and SNR post-layout simulation results of the ADC with non-linearity compensation by inverse conversion (IC).



(b) ADC linearity post-layout simulation results (DNL, INL) of the compensated conversion result by inverse conversion (IC) method.

Figure 6.24: Post-layout simulation results for the implemented tracking scheme algorithm with jumps in a 28 nm process. Non-linearity compensation by inverse conversion in (a) reveals a degradation compared to the ideal calculated results. In this terms the DNL and INL simulations also reveal degradations as illustrated in (b). The parameter adjustment of the general SNR expression demonstrates the predictability. Parameter: resolution ( $N_{R2R} = 12$  bit,  $N_{amp} = 11.12$  bit,  $N_{max} = 11.12$  bit), step generation rate ( $f_{ref} = 4$  GHz) and simulated conversion rate ( $f_{conv} \approx 723$  MHz).

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In conclusion, the evaluation of the 28 nm ADC design signifies the confirmation between the simulation results and the adjusted mathematical model. Furthermore, the comparison between the implementation of the 65 nm node and the 28 nm node demonstrates the possible performance improvement due to a higher switching speed and a higher resolution. However, the design implementation of a strict resolution increase results in a trade of between the effective resolution and the bandwidth. This is traced back to the reason, that the switching speed of the technology is limited by physical constraints. The compensation method by inverse conversion is applicable in scope of technology scaling, but non-linearity effects due to a scaling network inaccuracy remain. Thus, the degradation of the ideal performance results and reveals a distinct influence on the overall ADC performance regarding the bandwidth limitation and the corresponding effective resolution.

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## 6.4 Summary and Evaluation of the ASIC designs

The approach of the proposed ADC algorithm in chapter 3 was verified by the FPGA implementation in chapter 5 in the scope of a dynamic integration that describes a general-purpose ADC. Based on programmability and reconfigurability, the FPGA system design revealed a set of system configuration possibilities that can be applied to a wide range of operational areas. However, due to the flexibility of FPGAs, the performance parameter regarding switching speeds and power consumption are limited. Compared to an application-specific design, the general performance of FPGAs is often oversized concerning the actual purpose. Additionally, a drawback related to the general performance of FPGAs is based on limited switching frequencies and comparable high power consumptions. Contrary, ASICs are restricted by the programming and reconfiguration ability but provide an unmatched degree of switching speed to power consumption relation compared to FPGAs. Since the trend of continuous scaling for new technologies enables the further improvement of switching and energy efficiency, it is advisable to examine a circuit such as the proposed ADC concerning application-specific properties. Especially, the afore investigated dependency on the reference step generation rate and the conversion rate related to the ADC bandwidth and effective resolution qualifies the proposed approach for the ASIC implementation. Since the proposed ADC tracking scheme with jumps (section 3.1.2) has proven to be an efficient algorithm within the FPGA investigations, this approach was transferred to the ASIC design. However, the implementation of integrated circuits requires considering non-linearity effects. Due to this fact, the analog hardware characteristics were investigated in chapter 4. Based on the results of non-linearity affections within the feedback configuration of the general ADC topology, 2 compensation methods for non-linearity effects were proposed by the tracking & correction approach (section 4.2.1) and the inverse conversion approach (section 4.2.2). In order to evaluate the respective compensation method, 2 ASICs were designed in a 65 nm process node. Within the non-linearity analysis of the 65 nm implementation, the compensation methods were investigated. Since the compensation method by inverse conversion demonstrated a high degree for non-linearity compensation, the benefits of technology scaling were applied in the scope of an additional ASIC design in a 28 nm process node. Thus, 3 ASICs were designed and fabricated. Concerning the high degree of configuration ability and the state-of-the-art application purpose, the ASICs were evaluated with an FPGA as a target platform. In these terms, Printed-Circuit-Board (PCB) were developed as a carrier system for the ASICs. The PCBs connect to the FPGA via an FPGA Mezzanine Card (FMC) interface. The ADC communication channel with the FPGA establishes by high-speed serial interfaces that implement state-of-the-art abstraction layer configurations. The FPGA sided implementation establishes the direct data acquisition by an integrated logic

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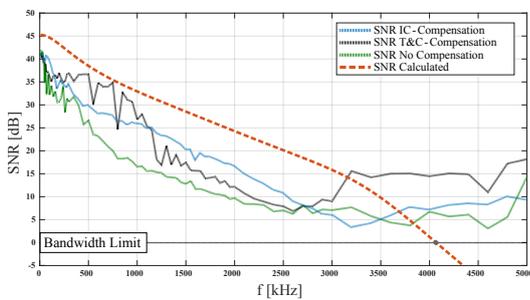
analyzer core or the forwarding via a PCIe interface that communicates with external desktop systems. The conversion results were evaluated desktop system sided by MATLAB spectral analysis tools.

Based on the experimental setup in figure 6.16 the ASICs were evaluated by measurements. In the scope of evaluating the 65 nm ASIC prototypes, the analysis for ADC properties concerned an uncompensated conversion result and the compensated conversion results. Thereby, the proposed compensation methods cover the T&C functionality as well as the IC functionality. The measurement and interpretation considered the dynamic behavior of the ADCs in the scope of the signal-to-noise ratio (SNR). The examination of the non-linearity affection for uncompensated and compensated ADC results conditioned the extension to the signal-to-noise-and-distortion ratio (SINAD) analysis. In these terms, the deviation between the SNR results and the SINAD results of the respective conversion system signifies the ability to equalize non-linearity effects. Non-linearity effects introduce a temporal misalignment of the binary assignment within the conversion. The temporal misalignment, in turn, introduces distortions of the conversion result compared to the input signal phase. Higher-order frequency portions indicate these distortions within the spectral analysis. This aspect implies that the higher the deviation between the SNR and the SINAD, the higher the proportionate distortions. Besides the temporal misalignment, the inaccuracy of the reference signal generated by the R2R scaling network induced non-linearity affections to the conversion result. Since the inaccuracy does not affect the temporal phase representation of the conversion signal, the binary assignment is only incorrect for the actual input signal magnitude. Therefore, it defines as spatial misalignment of the respective conversion step. Considering the ADC performance, the course of the SNR/SINAD is representative of the theoretical ADC bandwidth limitation. Equation 2.11 predicted a reference for the expected input signal frequency range. The validation for the SNR and the SINAD measurement results related to comparisons to the ideal results predicted by the mathematical SNR expression. In this context, the mathematical expression for the extended general SNR (Eqn. 3.8) performed the consideration of non-ideal measurement results due to the set for variable degrees of freedom. This aspect applies particularly to the representation of the amplitude resolution and the reference resolution related to the full-scale resolution of the reference signal.

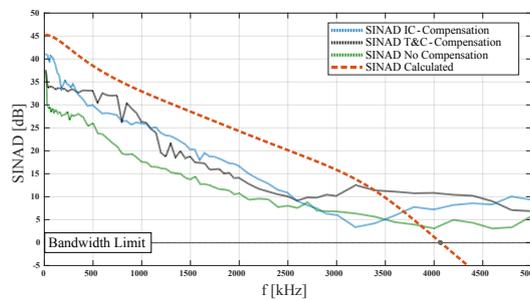
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Figure 6.25 illustrates a summary of the measured SNR courses and the measured SINAD courses for the 65 nm prototype implementations. Within the frequency range of interest, the uncompensated conversion result, as well as the compensated conversion results, are contrasted to the mathematical SNR course prediction by equation 3.8. The comparison between the individual results clarifies the non-linearity affection of the respective conversion signal. Thereby, the binary representation of the input signal magnitude processes with 7.22 bit. A deviation between the theoretical result of the effective resolution of the mathematical model (7.22 bit) and the maximum measured effective resolution of the uncompensated results (SINAD: 5.82 bit) indicates the requirement for a compensation method. In these terms, the compensation concerns the equalization of the spatial and temporal deviations within the binary alignment. The application of the T&C method assigns correction parameters to the conversion result, thus reducing the spatial misalignment. As a result, this method allows a higher effective resolution compared to the uncompensated method. However, due to a static binary correction based on a restricted number of DC levels, the ability of temporal misalignment correction is only partially performed. Considering the maximum resolution, which is unchanged (SINAD: 5.82 bit), indicates this aspect. This method allows a general improvement of the SNR and the SINAD for a specific input frequency range (200 kHz  $\rightarrow$  500 kHz). However, the improvement of the compensation ability would require increasing the number of reference levels within the training sequence of the T&C method. Due to this approach, the system complexity would also increase. Therefore, the application of the compensation method by inverse conversion was implemented and provided the ability to perform a correction for every conversion cycle independently of a reference signal requirement. As a result, the temporal misalignment was compensated totally thus that the SNR course and the SINAD course match as illustrated in figure 6.22(a). In addition, due to the equalization of the temporal misalignment, the conversion signal appears undistorted. As a result, the SINAD improved towards an effective resolution to 6.68 bit. In contrast to the mathematical prediction, the SNR/SINAD course matched the measured course except for a total offset present within the frequency range of interest. This non-linearity affection can be traced back to a mismatch of the R2R scaling network, which introduces spatial misalignments. In consideration of the DNL and INL analysis in figure 6.22(b) this aspect becomes clarified. The most critical transition of the scaling network (MSB) is affected most. An adjustment of the mathematical model concerning the spatial misalignment enabled the direct comparison between the mathematical model and the measurement results of the SNR course as illustrated in figure 6.22(a).

The conversion rate and bandwidth performance could be improved distinctly compared to the FPGA implementation, as indicated by evaluating the integrated ADC design in the 65 nm process node. As predictable by the derived set of mathematical expressions, this effect was achieved due to the applicability of a higher reference step generation rate. Thus, the ASIC designs in the 65 nm technology provide a measured reference step generation rate of 1.6 GHz, 256 times higher than the FPGA application (6.25 MHz). This factor also reflects the theoretical improvement of the bandwidth limitation. Thus, the equal effective resolution would transfer between the FPGA design and the ASIC design. However, due to non-linearity affections, the achievable bandwidth improvement by the ASICs could only be verified by a factor of 238, which implies a bandwidth  $\approx 3.8$  MHz.



(a) Comparison of the measured signal-to-noise ratio course between the compensation methods, the uncompensated result and the mathematical model.



(b) Comparison of the measured signal-to-noise and distortion ratio course between the compensation methods, the uncompensated result and the mathematical model.

Figure 6.25: Comparison between the mathematical model and the ASIC measurement results for the uncompensated result as well as for the compensated results in the 65 nm process. The implementation of the tracking scheme algorithm with jumps defines the basis for the uncompensated result as well as the compensation by the T&C and the IC method. The distortions induced by non-linearity are illustrated by the deviation of the calculated dynamic performance and the measurement results of the SNR (a) and SINAD (b). Parameter: ADC resolution ( $N = 8$  bit), amplitude resolution ( $N = 7.22$  bit), step generation rate ( $f_{\text{ref}} = 1.6$  GHz) and conversion rate ( $f_{\text{conv}} \approx 308$  MHz).

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In conclusion, the measurement results confirm the mathematical model, and the mathematical model reveals non-linearity affections of the prototype implementation. Implementing the proposed ADC conversion method by the tracking scheme with jumps was evaluated and demonstrated the applicability of the proposed conversion scheme. The requirement for compensation methods was derived, and the functionality was verified. The scope of the system evaluation validated the distinct enhancement by the application of the non-linearity compensation. Therefore, the functionality of the proposed ASIC implementation in the 65 nm process node is confirmed.

Related to the verified fact that the performance of the proposed ADC approach highly depends on the reference step generation rate (Eqn. 3.8), the assumption to transfer the design towards a faster technology process promised a further performance improvement. The technology of choice concerns a 28 nm process node, which provides a faster switching ability and a better relation to power consumption. The ADC implementation performs at 12 bit, which implies a 16 times higher resolution than the ASICs in the 65 nm process. Additionally, the reference step generation rate increased to 4 GHz by a factor of 2.5. Referred to the theoretical bandwidth limitation, the proportional increase of the resolution is less than the bandwidth of the 65 nm process but can provide a distinctly higher resolution. The requirement of compensation techniques increases relative to the resolution and the conversion rate (Eqn. 3.8). Therefore, the compensation method of inverse conversion was applied to the implementation within the 28 nm process, likewise. Based on this setup, the applicability and functionality of the compensation method were verified in advance by post-layout simulations and described in section 6.1.

Based on the description in section 6.2 also the ASIC in the 28 nm technology node was fabricated. However, at the time of evaluation, the fabrication process was not finished. Thus, the ASIC analysis was performed based on post-layout results. The simulations and evaluations were evaluated for the dynamic performance (SNR/SINAD) and the static performance (DNL/INL) of the ADC implementation. In this context, the calculation theoretical bandwidth limitation and the associated simulation were part of the evaluation process. As a result, the compensation method by inverse conversion again equalizes the temporal misalignments for the binary assignment, and the SNR and the SINAD are almost identical. Compared to the 65 nm implementation, the conversion rate was more than doubled by the faster technology to 723 MS/s (65 nm: 308 MS/s). The post-layout extracted simulation results of the SNR/SINAD course are illustrated in figure 6.24(a) and compared to the course of the calculated SNR prediction. As for the 65 nm implementation, spatial misalignments of the binary assignment degrade the ADC performance. This effect is also indicated for the 28 nm implementation by the analysis of the DNL and the INL

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in figure 6.24(b). Again, the scaling network inaccuracy causes a non-linearity affection of the reference signal leading to spatial misalignment. Thereby, the evaluation revealed that the non-linearity affection of the bandwidth increases related to the higher basic ADC resolution of 12 bit. Thus, the effective bandwidth reduces to almost 400 kHz compared to the theoretical limit of 723 kHz. However, a significantly higher effective resolution of 10.14 bit could be established compared to the 65 nm process (6.68 bit). As a result, the accuracy of the ADC improved by a factor of 11. This aspect indicates that the relation between bandwidth and resolution defines a trade-off.

In conclusion, the technology transfer towards smaller technology nodes with higher switching frequency constraints enables a performance improvement of the ADC implementation. Furthermore, the transfer indicates that the design methodology based on the proposed approach is independent of the technology. However, the technology properties set the scope for ADC parametrization. In combination with the compensation method by inverse conversion, the non-linearity affection reduces, which especially applies to temporal misalignments. A typical design requirement defines by the implementation of the reference signal scaling system. Spatial misalignments affect the ADC's ability to perform within the theoretical limitations. This effect degrades the higher the specified resolution. Based on the mathematical SNR expression verification, the applicability and the functionality of the proposed designs validated the scope of a technology transfer. As a result, the ability to parametrize the ADC based on the applied algorithm provides a flexible design methodology. However, the choice of ADC specifications defines a trade-off between the technology and the applied algorithm.

Table 6.1 summarizes the measurement/simulation results of the 3 ASIC prototypes. Each prototype implements the algorithmic tracking scheme enhanced by jumps as the JASGA Tracking ADC (section 3.1.2). The ASICs, which were fabricated in the 65 nm technology node, have a common basis in analog implementation. Therefore, the feedback configuration based on the comparator and the scaling network provides equal specifications regarding resolution, average conversion rate, and power consumption. Furthermore, the same reference step generation rate (clock rate) of 1.6 GHz applied to the prototypes. Thus, it enables a direct comparison between the compensation methods. Based on a resolution of  $N = 8$  bit and an average conversion rate of  $f_{\text{conv}} = 308$  MHz, the bandwidth limitation for both implementations was evaluated to  $f_{\text{max}_{\text{pw}}} = 3.8$  MHz. Also, the investigated input signal range of  $351 \text{ mV} \rightarrow 1055 \text{ mV}$ , corresponding to a possible amplitude resolution of 7.22 bit, applied to both ASICs. This environment enabled the evaluation regarding the compensation ability of the ADCs concerning the differences between both implementations. The influence due to distortions and the total power consumption

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defined the evaluation parameters regarding the applicability. In this terms the compensation method by Tracking-and-Correction-Compensation provides a maximum SINAD of 36.72 dB which corresponds to an effective resolution of 5.81 bit. The ADC prototype, which implements the compensation method by Inverse-Conversion-Compensation, improves the result of the SINAD due to the equalization of temporal misalignments towards 42.01 dB. Thus, the measured result corresponds to an effective resolution of 6.68 bit in the scope of the analyzed input signal range. In comparing the total power consumption, the tracking & correction method reveals a lower dissipation with 3.56 mW than the inverse conversion method with 4.08 mW. This aspect can be traced back to the increased design complexity for the implementation of the inverse conversion. Since both implementations offer advantages and disadvantages, a direct comparison of the figure of merit (FoM) was decisive. As a result, the property of a higher effective resolution reveals a distinct advantage for the IC method due to an FoM of 129.2 fJ/c.-s. compared to the result of the T&C method with an FoM of 211.2 fJ/c.-s., respectively. The technology transfer to the 28 nm process node enables a SINAD of 62.80 dB corresponding to an effective resolution of 10.14 bit. The average power consumption, in turn, results in 7.97 mW. Since the 28 nm process and the 65 nm process implement the same ADC topology and compensation method, a direct comparison based on the technology transfer was possible. Thus, the power consumption doubles by the technology transfer caused by more than double the reference step generation rate. However, the achieved effective resolution increases by a factor of 11 by the implementation within the 28 nm technology process. In summary, an FoM of 9.8 fJ/c.-s. clarifies the distinct performance increase by an improvement factor of 13 compared to the 65 nm process.

Table 6.1: Summary of the ASIC prototype performance for the ADC implementations in 65 nm technology node and in 28 nm technology node. ADC algorithm: tracking scheme enhanced by jumps (section 3.1.2).

Compensation Method		Tracking & Correction	Inverse Conversion	Inverse Conversion
Technology	(nm)	65	65	28
Resolution	(bit)	8	8	12
Conversion Rate	(MS/s)	308	308	723
Max. Bandwidth	(MHz)	3.8	3.8	0.4
SINAD	(dB)	36.72 <sup>3</sup>	42.01 <sup>3</sup>	62.80 <sup>4</sup>
ENOB	(bit)	5.81	6.68	10.14
Power	(mW)	3.65 <sup>5</sup>	4.08 <sup>6</sup>	7.97 <sup>7</sup>
Active Area	(mm <sup>2</sup> )	0.077	0.059	0.047
Walden FoM <sup>1</sup>	(fJ/c.-s.)	211.2	129.2	9.8
Info. density <sup>2</sup>	(G Info/s)	17.3	31.6	815.8

<sup>1</sup> [56] Walden FoM = Power / ( $2^{\text{ENOB}}$  · Conversion rate)      <sup>2</sup> Information density =  $2^{\text{ENOB}}$  · Conversion rate

<sup>3</sup> SINAD measured at boundary scenario defined by the resolution related frequency limit (equation 2.10)

<sup>4</sup> SINAD simulated at boundary scenario defined by the resolution related frequency limit (equation 2.10)

<sup>5</sup> Static and dynamic power dissipation for the core ADC as described in figure 6.10 measured at  $f_{\text{ref}} = 1.6$  GHz

<sup>6</sup> Static and dynamic power dissipation for the core ADC as described in figure 6.11 measured at  $f_{\text{ref}} = 1.6$  GHz

<sup>7</sup> Static and dynamic power dissipation for the core ADC as described in figure 6.12 simulated at  $f_{\text{ref}} = 4.0$  GHz (excluding transmission processing)

To categorize the ADC prototypes into the SoA, the Algorithmic-Tracking-Scheme ADC developed in the 65 nm, and the 28 nm technology node, compare to today's implementation techniques. Thereby, the SoA selection considers the technology node and a performance range comparable to that of the prototypes. In this context, SoA ADCs implement as a single channel variant and provide approximately equal basis resolutions. These ADC architectures represent tracking ADC, SAR ADCs, and Pipeline ADCs or combinations of these techniques. The evaluation of the bandwidth and the associated SINAD/SNDR covers diverse investigation approaches for SAR/Pipeline ADCs and the proposed ADC scheme. Due to this fact, the bandwidth-related limitations exclude from the rating. Therefore, the SINAD and the effective resolution refer to the low-frequency operation mode of the respective ADCs. Indeed, the SoA ADCs performance expectations are for a wide input frequency range related to the Nyquist limitation. However, as derived in the scope of the algorithmic FPGA implementations (section 5.2.1), the course of the SINAD and thus the usable bandwidth varies with the ADC parametrization. A demonstration revealed that the proposed ADC design ability surpasses the effective resolution of the

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SAR implementation within a wide input frequency range (figure 3.9) and under the same physical parametrization. Since there is no standard demand within today's publications to analyze the complete input frequency-related information density, a direct comparison is omitted. On the other hand, the ASIC design of the Algorithmic Tracking Scheme ADC represents a basic approach that can be adjusted for an area-specific parametrization as described in chapter 5. This fact includes that various possible ADC implementations are imaginable (e.g. bandwidth extension due to dynamic step width adjustment). However, for the sake of performance analysis, the basic algorithmic implementations are compared to the SoA within the scope of individual parametrization based on the Walden Figure-of-Merit [56], that defines the ratio between power consumption and information density ( $2^{\text{ENOB}} \cdot f_{\text{conv}}$ ).

Table 6.2 illustrates the comparison between the algorithmic tracking ADC prototype (inverse conversion) in the 65 nm process node, a conventional tracking ADC and common ADC architectures in 65 nm technology. As derived for the algorithmic approach, the proposed tracking method provides a higher information density than the conventional tracking ADC. Thus it performs by a six times higher conversion rate and five times higher effective resolution. Nevertheless, the conventional tracking approach characterizes by comparable low power consumption. Nevertheless, due to the physical limitation by the conventional tracking scheme, the effective resolution is distinctly lower than the resolution of the SoA. Therefore, the ADC prototype compares to SAR ADCs and a Pipeline ADC within a similar performance spectrum. The 8 bit SAR implementation provides a conversion rate of 400 MHz and an effective resolution of 7.09 bit for equal power consumption. Since the results are slightly better than the proposed approach results, this publication offers a better FOM. However, the SAR approach implements an advanced technique by a two-binary comparison. This aspect is clarified compared to the 9 bit charge injection SAR which provides a distinct higher FOM value for the same power consumption. Compared to the Pipeline ADC implementation applicable for a moderate conversion rate and a high resolution, power consumption increases. Therefore, the power to information ratio described by the Walden FOM is also higher than for the proposed approach. In these terms, it indicates that the implementation of the ATS ADC can perform within the scope of 65 nm single channel-based ADC designs.

Related to the state-of-the-art, the 65 nm technology process is outdated on the one hand. On the other hand, the performance improvement due to an improved relation of fast switching and power consumption for the 28 nm process is beneficial for integrated ADCs. Especially, the proposed architecture benefits from the performance boost regarding switching speeds. A combination between the SAR topology and Pipeline topology has

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been established by the SoA to benefit from the technology transfer. As a result, the Pipelined SAR ADC performs for high conversion rates and high resolutions simultaneously. Both specifications meet the application of the proposed design. However, due to the profoundly different conversion scheme, a distinctly higher conversion rate can be achieved by applying the proposed ATS ADC design within a comparable effective resolution. The respective implementations are compared to the prototype in table 6.3. Since it is often a trade-off between power consumption and conversion rate, the Pipelined SAR ADCs provide a similar FOM compared to the proposed approach. However, the improved information density implies a higher power dissipation, which also clarifies by the increase of the conversion rate for Pipelined SAR ADCs. The application of higher switching speeds also implies a performance decrease of the FOM. Thus, the proposed approach reveals a better power to information density ratio. A further result of the comparison applies to an increased basic resolution of the SAR topology. In these terms, the effective resolution improves on the one hand, but on the other hand, the power consumption also increases, and the conversion rate decreases. In the direct comparison, the Algorithmic-Tracking-Scheme ADC prototype provides a better figure of merit than the listed single-channel Pipelined SAR ADCs.

In conclusion, the comparison of the ADC prototypes to the state-of-the-art ADC architectures has demonstrated that the proposed approach of the Algorithmic-Tracking-Scheme ADC establishes a novel generation of ADCs which can perform within the same spectrum as current ADC generations. Furthermore, the application within high-performance technologies demonstrates the potential of the proposed system to surpass established ADC approaches. Based on a basis algorithmic implementation, the approach prospectively allows for a broad spectrum of digital enhancement.

Table 6.2: Comparison between the ATS ADC prototype in the 65 nm process node, a conventional tracking ADC, and common 65 nm ADC architectures.

	<b>This Work</b>	ISCAS' 13 [30]	ISSCC' 11 [78]	CICC' 11 [79]	ESSCIRC' 18 [80]
Architecture	<b>Algorithmic Tracking</b>	Tracking	SAR	ciSAR	Pipeline
Technology (nm)	<b>65</b>	130	65	65	65
Resolution (bit)	<b>8</b>	6	8	9	12
Conv. Rate (MS/s)	<b>308</b>	50	400	100	150
SINAD (dB)	<b>42.01<sup>3</sup></b>	27.82	44.50	47.00	67.50
ENOB (bit)	<b>6.68</b>	4.33	7.09	7.51	10.93
Power (mW)	<b>4.08<sup>4</sup></b>	2.69	4.00	4.00	48.00
Active Area (mm <sup>2</sup> )	<b>0.059</b>	0.080	0.024	0.020	0.780
Walden FoM <sup>1</sup> (fJ/c.-s.)	<b>129.2</b>	2673	73	220	190
Info. density <sup>2</sup> (G Info/s)	<b>31.6</b>	1.0	54.5	18.2	29.3

<sup>1</sup> [56] Walden FoM = Power / ( $2^{\text{ENOB}}$  · Conversion rate)      <sup>2</sup> Information density =  $2^{\text{ENOB}}$  · Conversion rate

<sup>3</sup> SINAD measured at boundary scenario defined by the resolution related frequency limit (equation 2.10)

<sup>4</sup> Static and dynamic power dissipation for the core ADC as described in figure 6.11 measured at  $f_{\text{ref}} = 1.6$  GHz

Table 6.3: Comparison between the Algorithmic Tracking Scheme ADC prototype in the 28 nm process node and common 28 nm ADC architectures.

	<b>This Work</b>	ISSCC' 17 [81]	JSSC' 19 [82]	TCSI' 21 [83]	TCSII' 19 [84]
Architecture	<b>Algorithmic Tracking</b>	Pipelined SAR	Pipelined SAR	Pipelined SAR	Pipelined SAR
Technology (nm)	<b>28</b>	28	28	28	28
Resolution (bit)	<b>12</b>	12	12	10	14
Conv. Rate (MS/s)	<b>723</b>	160	140	500	60
SINAD (dB)	<b>62.80<sup>3</sup></b>	61.10	58.00	56.60	66.9
ENOB (bit)	<b>10.14</b>	9.86	9.34	9.11	10.82
Power (mW)	<b>7.97<sup>4</sup></b>	1.90	1.10	6.00	4.26
Active Area (mm <sup>2</sup> )	<b>0.047</b>	0.097	0.202	0.015	0.368
Walden FoM <sup>1</sup> (fJ/c.-s.)	<b>9.8</b>	12.8	12.1	21.7	39.3
Info. density <sup>2</sup> (G Info/s)	<b>815.8</b>	148.7	90.7	276.3	108.5

<sup>1</sup> [56] Walden FoM = Power / ( $2^{\text{ENOB}}$  · Conversion rate)      <sup>2</sup> Information density =  $2^{\text{ENOB}}$  · Conversion rate

<sup>3</sup> SINAD simulated at boundary scenario defined by the resolution related frequency limit (equation 2.10)

<sup>4</sup> Static and dynamic power dissipation for the core ADC as described in figure 6.12 simulated at  $f_{\text{ref}} = 4.0$  GHz (excluding transmission processing)

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## 7 Conclusion

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The constant development of modern technologies enables to transfer more and more tasks of humans to machines. Key technologies such as autonomous driving or artificial intelligence have to capture and process an image of the environment as accurately as possible. There is an intermediate step in converting physical variables of the environment into corresponding analog signals by using sensors. However, analog information needs to be represented in digital units to be processed by conventional computerized systems. The corresponding key component is the analog-to-digital converter. To represent the environment as precisely as possible, the ADC must also describe the amount of information in this sense. However, the ability of ADCs to represent this accuracy is technically limited. They convert the two-dimensional message of a sensor signal consisting of magnitude and time. Although they represent the information in terms of magnitude with the greatest possible accuracy, the information in time sequences is usually insufficient. Due to an equidistant division of the time sequences, today's ADCs require several comparison cycles and fade out information during this time. Non-uniformly sampled signals represent an alternative, as these retain the relationship to a dynamic variation in the physical signal. The idea of the presented Algorithmic Tracking Scheme ADC is based on the basic concept of non-uniform conversion. A dynamic reference signal is suggested for comparison with the analog input signal. In this sense, the dynamic of the reference signal is established by the possibility of algorithmic implementation. The resulting advantages relate to programmability and reconfigurability and enable the dynamic adjustment of the sampling structure. The resulting advantages relate to programmability and reconfigurability. These aspects enable the dynamic adjustment of the sampling structure with respect to converting the information in magnitude and in time as accurately as possible. The result is the ability to represent a high information density.

The fundamental sampling structure for this type of ADC is based on the tracking scheme. This behavior enables the advantage of a fast conversion for every individual sampling cycle in the optimal case. Additionally, the non-resetting mode of tracking scheme conversion implies that consecutive conversion cycles depend on each other and form a non-uniform conversion. The relation of the conversion in magnitude to the proportional conversion

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time defines a high information density by non-uniformity. Based on the relative dependency of the consecutive conversion cycles, samples of the reference signal can represent the information density. The decisive factor here is how this reference signal is formed. For this reason, fundamental research questions have arisen:

- **What is the significance of the reference signal modification for the system?**
- **Which constitution of the reference signal influences the information density?**
- **How to realize technical approaches of the Algorithmic Tracking Scheme ADC?**

The research topic answered these fundamental questions in the scope of a mathematical derivation of information analysis models and the proposal of conversion algorithms, and the implementation of hardware solutions.

The basic approach about non-uniform sampling transfers the basic tracking scheme to a general design strategy for algorithmic implementations of the ADC reference signal. In scope of a detailed mathematical derivation an analysis concept for the information density was proposed. Thereby, the concept of information density was used as a kind of benchmark to categorize ADC properties and to evaluate various conversion algorithms. By the idea that missing information affects the information density and thus the ability of an accurate representation, the investigation of the signal-to-noise ratio (SNR) describes the deviation from the ideal signal to the converted signal. A fundamental dependency resulted from these examinations. The representation of the SNR describes a general method to predict the input frequency related information density of non-uniformly sampled signals. Furthermore, a simplified version of the general SNR equation constitutes to an expression for uniformly sampled signals. From this fact it can be deduced that the uniform sampling is a subset of non-uniform sampling. The derivation of step wise dependencies was based on logic hypotheses that were confirmed by the trace back to the initial approach of level-crossing. Additionally, a parameterizable tracking scheme algorithm was implemented in MATLAB. Thus, a verification concept of the individual mathematical derivations was established based on a behavioral simulation model. This means that in addition to the confirmation of the equation and hypotheses by tracing back to an initial approach, a simulation model-based validation method confirms the correctness. Based on these considerations, it was possible to identify individual basic parameters for the design of an algorithmic reference signal. In this sense, the underlying parameters describe the resolution, average conversion rate, and reference step generation rate. In general, these are basic parameters of ADCs and define degrees of freedom in the framework of sampling algorithms. Based on an investigation of the affection by variations of these parameters

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and the validation by the MATLAB model a theoretical approach for the reference signal constitutions were derived. Non-linearity affections which occur due to varying system delays in the feedback configuration can be considered as statistical mean or dynamic function of the conversion time. Furthermore, algorithmic properties like reference level jumps can be related to a relation between resolution and conversion cycle time. Based on these properties, the set of equations provide the ability to predict the signal-to-noise ratio for a new set of sampling algorithms. These open the way to digitally adjust the entire conversion algorithm of an ADC to an application-specific area in a dynamic manner.

The non-uniformity of the tracking-based conversion scheme required a novel definition of the ADC behavior based on information density. The sequence and the constitution of the digitally generated reference signal for the comparison to the analog input can be described by interacting with the degrees of freedom that parametrize the ADC. The derived set of equations enables the predictability of properties for algorithmic tracking scheme ADCs. Derived from these equations, a variety of possible algorithmic implementation patterns are imaginable. The approach of primarily digital implementation, therefore, offers a high degree of configuration. A novel approach derived from the sampling scheme of a conventional Tracking ADC is related to a separation of the reference step generation rate from the conversion rate of the ADC. The basic concept concerns a triangular formed reference signal that update time for step generation is faster than the internal system delay. Under the assumption of the same physical system constraints, the higher update rate provides a higher slope which implies an algorithmic extension of the bandwidth limitation compared to conventional Tracking ADCs. Furthermore, examining the relationship between the conversion rate and the effective resolution revealed that additional algorithmic modifications by jumps extend the effective resolution towards a physical limitation. As a result, the effective resolution improved. Comparing the proposed approaches to a SAR algorithm with the same parametrization examined strengths and weaknesses for uniform sampling schemes. Indeed, due to the uniform constitution of SAR algorithms, the absolute bandwidth is limited to half of the conversion rate concerning Nyquist. However, the signal-to-noise ratio over the bandwidth results in a rapid drop after passing the maximum resolution bandwidth and indicates a significant drop in information density. A general fact related to uniform sampling because the number of possible conversion steps is reduced linearly with the temporal decrease of the input signal period. The comparison demonstrates that an approach based on modified non-uniformly sampled tracking methods has distinct advantages over uniformly sampled topologies in terms of information density. In general, the set of modified non-uniformly sampled tracking methods for analog-to-digital conversion classifies the algorithmic Tracking Scheme ADC. In this context, a proposal for general design methods

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to develop a variety of new sampling algorithms. An alternating algorithm between the bandwidth limit and the effective resolution, for instance, can adjust the step size by jumps. Based on the application of step scaling, the direct alternation of the step size can enable an intermediate magnitude of the resolution. Another procedure would be imaginable by tracking the input signal slope by comparing consecutive conversion steps and a consequent adaptation to the relation between bandwidth and resolution. The freedom to describe the ADC behavior algorithmically benefits a dynamic and flexible design. The variety of possibilities opens the mind to novel technologies based on digital assistance.

The Algorithmic Tracking Scheme ADC realization as a technical approach included verifying and validating general ADC topologies. The implementation of these topologies concerns a Digital Ramp ADC, a SAR ADC, and a conventional Tracking ADC. Common to each of these ADC strategies is to digitally generate a reference signal compared with the analog input signal. Based on this requirement, these ADCs establish a feedback configuration by the algorithmic generation of the digital reference, the conversion into an analog signal, and level-crossing detection by a comparator. The comparator, in turn, provides a status for the consecutive step generation process of the digital algorithm. Based on the similarity of the ADC topologies, the difference relates to the actual conversion procedure. Thus, the methodology describes a general-purpose algorithmic ADC approach. In addition to the difference in the conversion algorithm, analog properties within the feedback configuration identified as disturbances that influence the conversion process. In this context, the feedback delay decisively decides on the conversion time and is an indicator of the conversion rate.

Due to the sequential step generation process, the delay introduced by the algorithm can be considered deterministic. However, especially non-linearity affections due to mismatch or PVT variations are statistical. The propagation delay of the feedback configuration proved to be the main character attributed to non-linearity affection for the conversion rate. Investigations revealed the comparator as a source for significant propagation delay variations concerning the dispersion effect. Furthermore, the propagation delay's general affection considers a superimposed dispersion effect by stochastic variations. The reason for the dispersion effect was examined by a topology analysis and described by a mathematical model. Any noise portion introduced to the system can be traced back to a delay variation and expressed as a describable and predictable deviation in the conversion result. For a non-linearity-free conversion, two proposed methods can compensate the dispersion effect superimposed by stochastic noise delay variation. The first method performs a training sequence to the ADC, which detects the deviations of the conversion result by a measurement approach. A constant input signal whose digital value is known to the

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system serves as a reference. The difference between a set of constant input levels and the disturbed conversion result defines corresponding correction parameters. Thus, the procedure describes a non-linearity-affected conversion with a subsequent correction of the output stream in the scope of background compensation. Indeed, alternating system properties over time causes that the system needs to repeat the training sequence. The tracking of the non-linearity represents a measurement method with an accuracy corresponding to the amount of reference level for approximating correction parameters. As a result, the compensation by measurement allows detection of disturbance, but additional system effort in analog accuracy and storage capacity is high. Therefore, the system is either suited for a controlled environment or an accurate measurement of the dispersion effect.

The second approach has its origin in the actual conversion process. The actual conversion is performed under the affection of non-linearities and declared as regular conversion. The compensation idea relates to the assumption that the displacement of the conversion result must arise for a repeated version in the same order of magnitude. However, based on an opposite polarity of the system parameters, the conversion result is affected in a contrary way. Therefore, a subsequent inverse conversion follows the regular conversion and compensates for the non-linearity disturbance. From the perspective of an implementation approach, the terminal interchange of the comparator and a simultaneous algorithmic adjustment establish the inverse behavior. The compensation ability of the proposed method was predicted by a mathematical derivation and verified by the application of the general SNR expression, which was modified to predict the regular and inverse conversion property. The first method is declared as compensation method by tracking and correction, and the second method is declared as compensation method by inverse conversion. Both methods demonstrated the required compensation ability. However, due to the independence of constant comparison levels as references, the compensation method by inverse conversion indicated a better performance compared to the compensation method by tracking and correction. Indeed, a measurement process that would enable the detection of mismatch or non-linearity properties of the remaining analog components can extend the inverse conversion method.

The actual realization implemented the Algorithmic Tracking Scheme ADC on an FPGA. The concepts of programming, reconfiguration, and parallel data processing qualify FPGAs for essential components in modern digital systems. The constitution by digital algorithms for the described and the proposed ADC schemes demand a flexible and application-specific implementation. To provide a high degree of flexibility, the analog hardware of the proposed ADC topology constitutes a minimally adequate functionality. An in-

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vestigation based on the comparison functionality of the LVDS I/O driver of the FPGA turned out to be applicable for the functionality as an analog comparator employing a highly linear transfer function. Furthermore, a detailed evaluation of the driver regarding the performance as an analog comparator application examined the dispersion effect. The analysis validated the mathematical approach to describe the dispersion effect of comparators and enables the prediction and extrapolation transfer function based on a small set of measurement results. An 8-bit R2R scaling network that converts the digital representation of the sampling algorithm into a comparable analog representation extends the hardware. This configuration implies implementing a flexible, programmable, and reconfigurable ADC topology on an FPGA with only one additional analog component. The experimental setup constitutes a Genesys 2 development board equipped with a Kintex 7 FPGA and an R2R scaling network available as ASIC.

Based on the general implementation abilities of the FPGA-based ADC configuration, the described topology defines a General Purpose ADC. The aforementioned basic ADC topologies concerning the Digital Ramp ADC, the SAR ADC, and the conventional Tracking ADC represent algorithmic approaches on the FPGA to verify the general purpose. In this contemplation, an equal parameterization of the respective ADC topology enabled the comparison of the basic designs. The measurement analysis of the SNR course confirmed the predicted behavior of the Tracking ADC to perform a higher information density than the SAR ADC within the bandwidth. The proposed Algorithmic Tracking Scheme ADC demonstrates the superiority over the simple SAR algorithm within the total SAR bandwidth. In this context, the algorithms modified the tracking scheme concerning a bandwidth extension for a faster update rate of the reference step and by the application of jumps. Also, the comparison between the measurement results of the SNR courses verifies the assumptions and postulations of the general SNR equation, which demonstrates the ability to predict algorithmic behavior mathematically. The modified tracking scheme allows for a relative temporal resolution due to a non-uniform conversion cycle generation. Due to this fact, the information density can increase partially, but the non-uniformly converted signal still contains information in time. Applying a Cascaded-Integrator-Comb interpolator (CIC) approach performs the translation of the temporal information into magnitude information. Therefore, if the non-uniform conversion time information of the ADC output is translated to additional magnitude information by interpolation, the magnitude resolution of the CIC interpolator output describes the total information density of the ADC conversion result. This aspect implies that sampling at a higher rate can represent the information in time more accurately. It follows a higher and uniformly sampled conversion rate. Mathematical relations define a framework for the design of the interpolator.

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In conclusion to the verification process based on FPGA implementation, the measurement results of both proposed algorithmic approaches confirm the postulated properties by equations. Thereby it was demonstrated that the new algorithms are superior to the SAR implementation. Compared to the conventional Tracking ADC, the acceleration of the step generation rate enables a higher effective resolution and bandwidth. The frequency range covers almost the entire bandwidth of the SAR ADC but with a higher effective resolution. The measurement results of the algorithmic enhanced ADC architecture, including reference step acceleration and jumps, reveal a maximum effective resolution of 7.64 bit, which is close to the theoretical limit of 8 bit. The representable information density results in conjunction with an average conversion rate of 1.39 MS/s in 277.26 Mbit/s. However, the functionality of the algorithmic interpolation sequence can significantly improve the resolution and conversion rate. The translation of time information into magnitude information enabled a uniformly up-sampled conversion rate result of 12.5 MS/s in conjunction with an effective resolution of 10.81 bit. Therefore, the interpolated conversion represents the total information density of 22441.11 Mbit/s which corresponds to an improvement factor of  $\approx 80$  compared to the approach without interpolation. Based on these measurement results, the class of Algorithmic Tracking Scheme ADCs demonstrates a distinctly better performance regarding information density than existing published FPGA approaches implementing ADCs.

The advantage of FPGA implementations by flexible programming and reconfiguration enables a dynamic application process. However, due to the general framework of FPGAs, the representable performance is lower compared to application-specific designs. Application-Specific Integrated Circuits (ASICs) generate the best performance related to the ratio of power consumption and switching frequencies. The analyzes of the Tracking Scheme ADC designs indicated that the switching frequency represents a key factor for converting a high information density. Thus, a transfer of the proposed ADC design enabled the investigation of the performance improvement. Therefore, the ADC process was transferred and validated on three ASIC prototypes using a 65 nm state-of-the-art technology and a high-performance-computing technology in a 28 nm process node. However, the non-linearity affection is significant for integrated circuits, as an evaluation demonstrated. So, the proposed compensation methods implement an extension to the ADC designs. The 65 nm prototypes realize both compensation methods. Since the compensation method by inverse conversion raises advantages compared to the compensation by tracking and correction, the high-performance-computing ASIC in 28 nm covers this compensation method. The technology transfer established the analyzes within a significantly better performance framework concerning switching frequencies and power consumption.

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The evaluation of the integrated ADC design in the 65 nm process node illustrated that the performance concerning the conversion rate and bandwidth could be improved distinctly compared to the FPGA implementation. As predictable by the derived set of mathematical expressions, this effect was achieved due to the applicability of a higher reference step generation rate. Thus, the ASIC designs in the 65 nm technology provide a measured reference step generation rate of 1.6 GHz, which is 256 times higher compared to the FPGA application (6.25 MHz). This factor also reflects the theoretical improvement of the bandwidth limitation by converting a similar effective resolution.

To compare the compensation methods, both ASIC prototypes in the 65 nm process have the same parametrization concerning the reference step generation rate, the resolution, and the resulting average conversion rate. Additionally, the prototypes provide uncompensated conversion results. Based on a resolution of  $N = 8$  bit and an average conversion rate of  $f_{\text{conv}} = 308$  MHz, the evaluation of the bandwidth limitation for both implementations resulted in  $f_{\text{max,bw}} = 3.8$  MHz. Furthermore, the investigated input signal range of  $351 \text{ mV} \rightarrow 1055 \text{ mV}$ , which corresponds to a possible amplitude resolution of 7.22 bit, concerned to both ASICs. Based on this setup, the affections due to distortions and the total power consumption defined the decision criterion for the applicability. Additionally to the information density analysis based on the SNR evaluation, the signal-to-noise-and-distortion ratio (SINAD) evaluation represents the distortions due to non-linearity effects. Thereby, the deviation between the SNR and the SINAD illustrates the affection due to non-linearity. It evaluates the respective method's ability to compensate. In this context, the compensation method by tracking & correction provides a maximum SINAD of 36.72 dB, which corresponds to an effective resolution of 5.81 bit. The ADC prototype, which implements the compensation method by inverse conversion, improves the result of the SINAD due to the equalization of temporal distortions. A measurement of the maximum SINAD result with 42.01 dB corresponds to an effective resolution of 6.68 bit in the scope of the analyzed input signal range. Thus the deviation from the ideal effective resolution (7.22 bit) is about half an LSB (0.54 bit). The results demonstrate that the compensation by inverse conversion is considerably more effective in the task to equalize distortions based on non-linearity. In comparing the total power consumption, the application of the tracking & correction method dissipates less power with 3.56 mW than the inverse conversion method with 4.08 mW. This aspect can be traced back to the increased design complexity for the implementation of the inverse conversion. Related to the advantages and disadvantages of both designs, the figure of merit (FoM) is representative of a direct comparison. As a result, the system with compensation by tracking & correction offers an FoM of 211.2 fJ/c.-s. compared to the

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distinctly improved result with an FoM of 129.2 fJ/c.-s. of the compensation by inverse conversion. In summary, implementing an ASIC prototype of the proposed ADC conversion method was evaluated and demonstrated the applicability in a 65 nm state-of-the-art technology. The requirement for compensation methods was derived, and the functionality was verified. The measurement results and the mathematical model mutually confirmed each other. The system evaluation validated the distinct enhancement by the application of non-linearity compensation. Therefore, the functionality of the proposed ASIC implementation in the 65 nm process node is confirmed. A comparison to state-of-the-art ADCs in the framework of integrated circuits demonstrates the performance of the Algorithmic Tracking Scheme ADC implementation. In this context, the proposed design improves the performance regarding effective resolution and conversion rate of conventional Tracking ADCs significantly. A comparison with SAR ADC and Pipeline ADC topologies in the same technology node reveals the necessity of modifying the typical SAR structure to enable performance in the same or better range.

The transfer of the ADC implementation, including the compensation method by the inverse conversion to the high-performance-computing process in 28 nm technology, improved the ADC specifications. The parametrization by a reference step generation rate (clock rate) of 4 GHz enabled an average conversion rate of 723 MS/s, which is more than doubled compared to the 65 nm implementation (65 nm: 308 MS/s). An effective resolution of 10.14 bit (SINAD: 62.80 dB) of the 12 bit system improved the accuracy of the 28 nm implementation by a factor of 11 compared to the 65 nm process (6.68 bit). The compensation method by inverse conversion suppresses the majority of non-linearity based distortions. Again, the measurement results and the mathematical model mutually confirmed each other. However, the slightest deviations affect the global performance significantly, why an enhanced method as a modification of the compensation method by inverse conversion represents a proposal for future applications. In summary, an FoM of 9.8 fJ/c.-s. clarifies the distinct performance increase by an improvement factor of 13 (65 nm: 129.2 fJ/c.-s.) due to the technology transfer.

The transfer of common ADC architectures to technology nodes providing fast switching frequencies as the 28 nm HPC became popular in recent years. The commonly established architecture relates to hybrid topologies as the Pipelined SAR ADC to simultaneously perform high conversion rates and high resolutions. The proposed ADC covers exactly this performance range. Thus, a comparison to state-of-the-art Pipelined SAR ADCs in 28 nm process nodes illustrates the performance of the Algorithmic Tracking Scheme ADC.

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A unique selling point of the Algorithmic Tracking ADC is the extremely high conversion rate compared to the Pipelined SAR ADCs. Power consumption and conversion rate is often a trade-off. Hence, the Pipeline SAR architectures have a lower power consumption than the proposed design, but the FoM is in a similar performance range. However, the Walden FoM of the proposed implementation provides the best power to information density ratio with 9.8 fJ/c.-s. compared to the listed publications (Pipelined SAR ADC: 12.1 fJ/c.-s.). Considering that the pure information density relates to both the effective resolution and the conversion rate, a key figure for evaluation is described by the information per second (Info/s) with the expression:  $2^{\text{ENOB}} \cdot \text{conversion rate}$ . Thus, the Algorithmic Tracking Scheme ADC demonstrates clear advantages by the most accurate representation of the input signal. Compared to the most accurate information density of the Pipeline SAR ADC with 276.3 G Info/s, the Algorithmic Tracking Scheme ADC establishes a three times more accurate information density with 815.8 G Info/s.

In analog-to-digital conversion, everything is about the question to accurately represent analog signals in the digital domain. The general term describes the information density. Based on non-uniform sampling, the tracking scheme approach establishes a basis to convert with high information density. The procedure to modify this basic approach by algorithmic implementations results in a variety of possible applications. This concept describes the Algorithmic Tracking Scheme ADC. The focus is on dynamic parameterization and behavioral programming. The derived set of equations paves the way to predict parameter coherences of algorithmic implementations. A flexible implementation technique based on programming enables reconfigurable FPGA designs as well as high-performing ASICs. There are no limits due to the high dynamic range. A general hardware proposal based on an FPGA with a single analog extension demonstrates the ability to implement various algorithmic designs. The Algorithmic Tracking Scheme design demonstrated advantages over common approaches and validated the mathematical approach simultaneously. Furthermore, the application of the CIC interpolator enabled the conversion of non-uniform temporal information into high resolution, and high rate uniformly sampled conversions. The transfer of the Algorithmic Tracking Scheme ADC design to SOA and HPC ASICs favored a high-end performance. Both the derived equations and the measurement results mutually confirmed each other. Thus, the proposed mathematical equations and design methodology provide a functional development tool for ADC designers in high-performance technologies. In contrast to conventional ADC designs of the same technology and performance class, the ADC proposal in the 65 nm implementation has comparable results. However, the increase in performance for HPC technologies in 28 nm is significant.

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As a result, the amount of information density by conversion is unmatched by conventional single-channel ADC designs. Thereby, the current status of the Algorithmic Tracking Scheme ADC implementation only represents a first impression of the possibilities. The application of the advanced compensation method by inverse conversion will enable further improvement. The way of application-specific algorithmic modifications demonstrates a future performance class for dynamic ADC implementations.



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