Enhancing Digital Controllability in Wideband RF Transceiver Front-Ends for FTTx Applications

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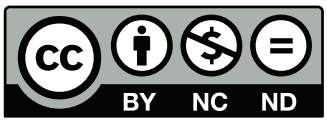

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Abstract

Enhancing the digital controllability of wideband RF transceiver front-ends helps in widening the range of operating conditions and applications in which such systems can be employed. Technology limitations and design challenges often constrain the extensive adoption of digital controllability in RF front-ends. This work focuses on three major aspects associated with the design and implementation of a digitally controllable RF transceiver front-end for enhanced digital control.

Firstly, the influence of the choice of semiconductor technology for a system-on-chip integration of digital gain control circuits are investigated. The digital control of gain is achieved by utilizing step attenuators that consist of cascaded switched attenuation stages. A design methodology is presented to evaluate the influence of the chosen technology on the performance of the three conventionally used switched attenuator topologies for desired attenuation levels, and the constraints that the technology suitable for high amplification places on the attenuator performance are examined.

Secondly, a novel approach to the integrated implementation of gain slope equalization is presented, and the suitability of the proposed approach for integration within the RF front-end is verified.

Thirdly, a sensitivity-aware implementation of a peak power detector is presented. The increased employment of digital gain control also increases the requirements on the sensitivity of the power detector employed for adaptive power and gain control. The design, implementation, and measurement results of a state-of-the-art wideband power detector with high sensitivity and large dynamic range are presented. The design is optimized to provide a large offset cancellation range, and the influence of offset cancellation circuits on the sensitivity of the power detector is studied. Moreover, design considerations for high sensitivity performance of the power detector are investigated, and the noise contributions from individual sub-circuits are evaluated.

Finally, a wideband RF transceiver front-end is realized using a commercially available SiGe BiCMOS technology to demonstrate the enhancements in the digital controllability of the system. The RF front-end has a bandwidth of 500 MHz to 2.5 GHz, an input dynamic range of 20 dB, a digital gain control range larger than 30 dB, a digital gain slope equalization range from 1.49 dB/GHz to 3.78 dB/GHz, and employs a power detector with a sensitivity of -56 dBm and dynamic range of 64 dB. The digital control in the RF front-end is implemented using an on-chip serial-parallel-interface (SPI) that is controlled by an external micro-controller. A prototype implementation of the RF front-end system is presented as part of an RFIC intended for use in optical transceiver modules for fiber-to-the-x applications.

Zusammenfassung

Die Verbesserung der digitalen Steuerbarkeit von Breitband-RF-Transceiver-Frontends trägt dazu bei, den Bereich der Betriebsbedingungen und Anwendungen, in denen solche Systeme eingesetzt werden können, zu erweitern. Technologische Einschränkungen und Designherausforderungen behindern häufig die umfassende Einführung der digitalen Steuerbarkeit in HF-Frontends. Diese Arbeit konzentriert sich auf drei Hauptaspekte im Zusammenhang mit dem Entwurf und der Implementierung eines digital steuerbaren HF-Transceiver-Frontends für eine verbesserte digitale Steuerung.

Zunächst wird der Einfluss der Wahl der Halbleitertechnologie für eine System-on-Chip-Integration digitaler Verstärkungsregelkreise untersucht. Die digitale Steuerung der Verstärkung wird durch die Verwendung von Dämpfungsglieder erreicht, die aus kaskadierten geschalteten Dämpfungsstufen bestehen. Der Einfluss der ausgewählten Technologie auf die Leistung der drei herkömmlich verwendeten Topologien mit geschalteten Dämpfern wird bewertet, um die Einschränkungen zu untersuchen, die die für hohe Verstärkung geeignete Technologie für die Leistung des Dämpfers darstellt.

Zweitens wird ein neuartiger Ansatz zur integrierten Implementierung des Gain-Slope-Equalizers vorgestellt und die Eignung des vorgeschlagenen Ansatzes für die Integration innerhalb des RF-Frontends überprüft.

Drittens wird eine sensitivitätsbewusste Implementierung eines Spitzenleistungsdetektors vorgestellt. Der verstärkte Einsatz der digitalen Verstärkungsregelung erhöht auch die Anforderungen an die Empfindlichkeit des Leistungsdetektors, der für die adaptive Leistungs- und Verstärkungsregelung eingesetzt wird. Das Design, die Implementierung und die Messergebnisse eines hochmodernen Breitband-Leistungsdetektors mit hoher Empfindlichkeit und großem Dynamikbereich werden vorgestellt. Das Design wurde optimiert, um einen großen Offset-Unterdrückungsbereich bereitzustellen, und der Einfluss von Offset-Unterdrückungsschaltungen auf die Empfindlichkeit des Leistungsdetektors wird untersucht. Darüber hinaus werden Entwurfsüberlegungen für ein Hochempfindlichkeitsverhalten des Leistungsdetektors untersucht und die Rauschbeiträge von einzelnen Teilschaltungen bewertet.

Schließlich wird ein Breitband-RF-Transceiver-Front-End unter Verwendung einer im Handel erhältlichen SiGe-BiCMOS-Technologie realisiert, um die Verbesserungen der digitalen Steuerbarkeit des Systems zu demonstrieren. Das RF-Front-End hat eine Bandbreite von 500 MHz bis 2,5 GHz, einen Eingangsdynamikbereich von 20 dB, einen digitalen Verstärkungsregelbereich von mehr als 30 dB und einen digitalen Verstärkungssteilheitsausgleichsbereich von 1.49 dB/GHz bis 3.78 dB/GHz und verwendet einen Leistungsdetektor mit einer Empfindlichkeit von -56 dBm und Dynamikbereich von 64 dB. Die digitale Steuerung im RF-Frontend erfolgt über eine On-Chip-Seriell-Parallel-Schnittstelle (SPI), die von einem externen Mikrocontroller gesteuert wird. Eine prototypische Implementierung des RF-Front-End-Systems wird als Teil eines RFIC vorgestellt, der für die Verwendung in optischen Transceivermodulen für Fiber-to-the-x-Anwendungen vorgesehen ist.

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List of Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
ADSL	Asymmetric Digital Subscriber line
AGC	Automatic Gain Control
AM-FDM	Amplitude Modulation Frequency Division Multiplexing
AON	Active Optical Network
BiCMOS	Bipolar-Complementary Metal Oxide Semiconductor
BiST	Built-in Self-Test
BJT	Bipolar Junction Transistor
CATV	Cable Television
CDN	Clock Distribution Network
CMOS	Complementary Metal Oxide Semiconductor
CSO	Composite Second Order
DC	Direct Current
DCCS	Digitally Controllable Current Source
DCGSE	Digitally Controllable Gain Slope Equalizer
DCO	Digitally Controllable Oscillator
DR	Dynamic Range
DSL	Digital Subscriber line
EDFA	Erbium-Doped Fiber Amplifier
EM	Electro-Magnetic
FTTB	Fiber-to-the-Building
FTTC	Fiber-to-the-Curb
FTTdP	Fiber-to-the-Distribution-Point
FTTH	Fiber-to-the-Home
FTTN	Fiber-to-the-Neighborhood
FTTP	Fiber-to-the-Premises
FTTx	Fiber-to-the-X
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Ge	Germanium
GHz	Gigahertz
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuit
ICI	Inter-Channel Interference
IIP3	Input 3rd Order Intercept Point
InGaP	Indium Gallium Phosphide
InP	Indium Phosphide
ISI	Inter-Signal Interference
LCE	Log-Conformity Error
LNA	Low-Noise Amplifier
MEMS	Micro-Electro-Mechanical System
MESFET	Metal-Semiconductor Field Effect Transistor
MHz	Megahertz
MIM	Metal Insulator Metal

MMIC	Millimetre-Wave Integrated Circuit
NMOS	N-channel Metal Oxide Semiconductor
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
PIN	P-Type Intrinsic N-Type
PON	Passive Optical Network
QFN	Quad Flat No-Lead
RF	Radio Frequency
RF-CMOS	Radio Frequency Silion-on-Insulator
RF-SOI	Radio Frequency Silion-on-Insulator
RFFE	Radio Frequency Front-End
RFIC	Radio Frequency Integrated Circuit
RMS	Root-Mean Square
SDLA	Successive Detection Logarithmic Amplifier
Si	Silicon
SiGe	Silicon-Germanium
SiP	System-in-Package
SoC	System-on-Chip
SOI	Silicon-on-Insulator
SPI	Serial-Parallel Interface
TWA	Traveling-Wave Amplifier
VDSL	Very High Speed Digital Subscriber line
VGA	Variable-Gain Amplifier

1 Introduction

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1.1 Overview

Optical fiber based access networks have much higher bandwidth-distance product, require lower maintenance and operation costs, and are future proof when compared to conventional access networks based on twisted-pair copper cables. Hence, optical fibers outperform cable- and copper-based networks in terms of the transmission capacity over long distances [1].

With the need for higher bandwidths to serve the increasing demands on end-user connection speeds, optical fiber based fiber-to-the-x (FTTx) technology is being widely adopted for the deployment of broadband services, such as cable television (CATV), broadcasting and satellite communications, right up to the subscriber premises [2–4]. FTTx is a generic term, and x is categorized based on where the fiber terminates. For example, x could stand for home, building, curb, node, premises, or distribution point, and the corresponding terminology of FTTH, FTTB, FTTC, FTTN, FTTP or FTTdP, respectively, can be defined.

Figure 1.1 provides a comparison of the architectures and achievable data rates of asymmetric digital subscriber line (ADSL), very high speed digital subscriber line (VDSL), and FTTx access networks. Whereas ADSL and VDSL technologies can provide data speeds up to 16 Mb/s and 50 Mb/s, respectively, optical fiber based access networks can provide up to 1 Gb/s access speeds.

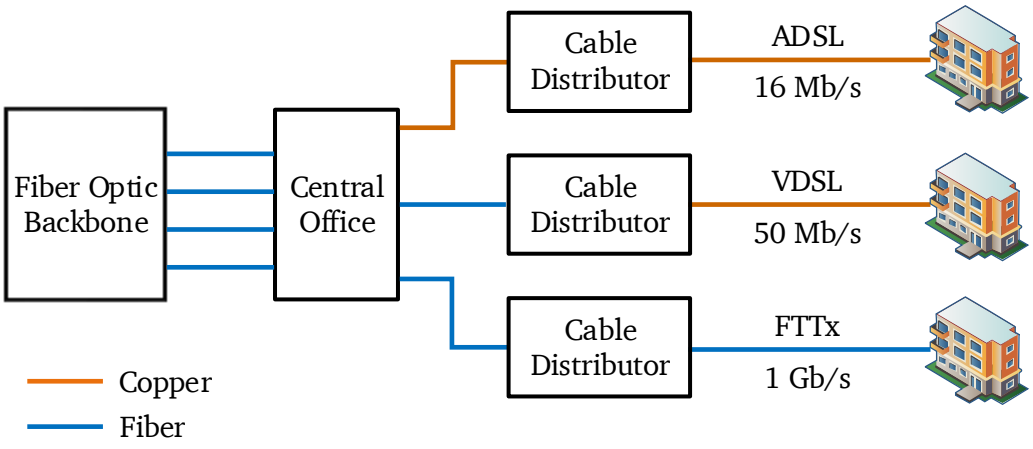

Figure 1.1: Comparison of different access networks.

1.1.1 Fiber-to-the-Home

The most recent market panorama data prepared by IDATE DigiWorld on behalf of FTTH Council Europe showed that as of September 2018, there were 59.6 million FTTH/B subscribers in Europe. Comparing this to the subscriber count of 20 million subscribers in September 2013, it can be observed that there has been a 200 percent growth in the subscriber count. The total coverage of FTTH/B networks was 46.4 percent of total homes in 2018. Market forecasts show that the subscriber count is going to grow further and would be up to 168 million subscribers by 2025. Also interesting to note is the forecast that the ratio of FTTH deployments to FTTB deployments would increase from 55.6 percent in 2018 to 63.8 percent in 2025, signifying that the fiber deployments would get closer to end-users by 2025 [5, 6]. Consumer surveys have also shown that consumer satisfaction is highest with FTTH when compared to other access technologies such as digital subscriber line (DSL), Cable Modem, and wireless access. Studies have also shown that a vast majority of the non-FTTH users would consider subscribing to FTTH services if it was made available in their area [7]. FTTH is, hence, the technology of choice for the future of broadband access networks, and research in this area has taken high prominence in recent times.

1.1.2 Optical Transceiver Modules in FTTx Deployments

Two major FTTx solutions are being widely deployed today: active optical networks (AONs) and passive optical networks (PONs). In both these network topologies, an optical fiber is used to carry the optical signals from a central office, or in other words a local exchange, up to a router or a switch aggregator that distributes the signal to specific end users. In AONs, the switching equipment is electrically powered and hence, the name active optical network. In PONs, the active switch nodes are replaced by passive optical splitters.

Optical transceiver modules are used at the optical network terminations for the conversion of signal between the optical and electrical mediums with the help of laser diodes and photo-diodes. The electrical signals that are received and transmitted need certain post-reception or pre-transmission processing as per the requirements of the application and the deployment conditions. Overall, an optical transceiver module has to support multiple functionalities such as wavelength control, tunable amplification, and gain slope equalization apart from signal conversion between the optical and electrical mediums. As a result, the size of a module and its deployment costs increase. Figures 1.2 and 1.3 show the functionality of an example electronic sub-system of an optical transceiver module when operated in the receiver and transmitter modes of operation. In the receiver mode of operation, the data received from the optical fiber is converted from an optical signal to an electrical signal using a photodetector and then processed by the electronic sub-system. In the transmitter mode of operation, the electrical signal to be transmitted is processed by the electronic sub-system first and then converted to an optical signal by using laser diodes.

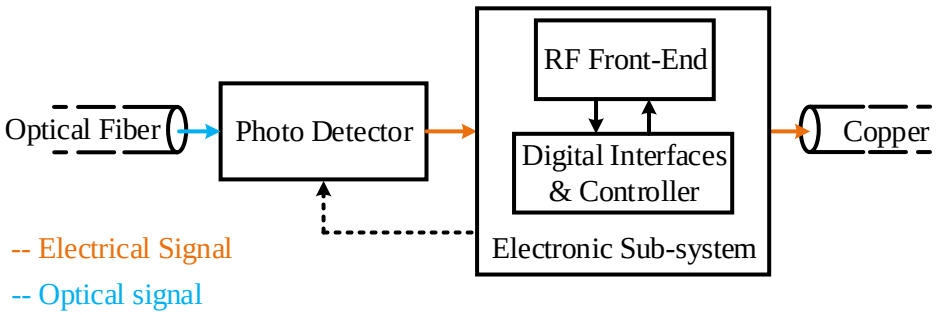

Figure 1.2: Functional block diagram of an optical transceiver module when operated in the receiver mode.

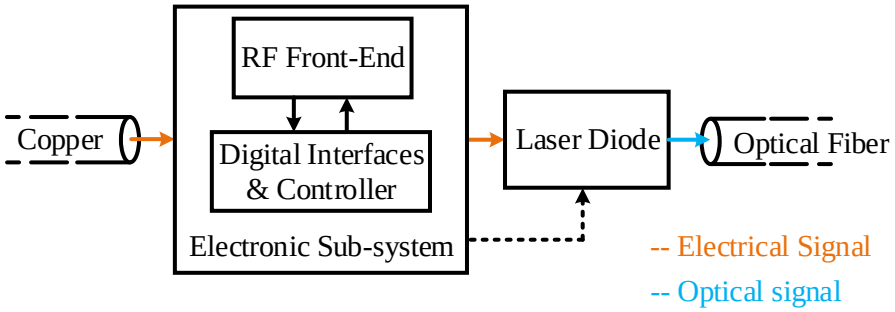

Figure 1.3: Functional block diagram of an optical transceiver module when operated in the transmitter mode.

Cost-effectiveness is an essential feature that could help bolster the widespread deployment of FTTx technology. The costs associated with the technology can be minimized by reducing the required component footprint of, amongst others, the electronic circuitry that is part of an optical transceiver module. Most of the currently available optical transceiver modules adopt a discrete realization using commercially available ICs for the electronic circuitry. The need for an area constrained deployment of a transceiver module makes an integrated implementation of multiple parts of the electronic sub-system highly attractive.

Digital control is finding more and more applications in radio frequency integrated circuits (RFICs) because of the high integration potential of digital circuitry and the high degree of flexibility that a digitally controlled RFIC can provide when interfacing with external circuits and systems. Enabling digital control for the RF circuits in an optical transceiver module will make them suitable for a wide range of deployment conditions, especially when considering the desire to use the same circuitry in both the transmitter and receiver modes of operation.

1.2 Research Objectives

The research in this dissertation focuses on the enhancement of digital controllability in RF front-end integrated circuits (ICs). The research is undertaken within the intended application area of digitally controllable RFICs for optical transceiver modules in FTTx applications. The following major research objectives are investigated in this work:

1. **Investigate the influence of the choice of technology on the design of RF switch attenuators.** Introducing digital controllability in RF front-end ICs influences the performance of individual sub-circuits when realized as a system-on-chip. The limitations that the choice of a semiconductor technology places on the performance of the digital gain control blocks, namely the RF switch attenuators, are evaluated in this work.

2. **Enable digital controllability of gain slope in wideband RF front-end ICs.** The wideband operation of RF blocks such as amplifiers and attenuators result in undesirable performance drops across the bandwidth of interest. The implementation of a digitally controllable gain slope equalizer, to compensate for the degradation of gain with increasing frequency, is explored in this work.

3. **Design of large dynamic range wideband logarithmic power detectors for high sensitivity.** The increase in the dynamic range and the digital control range of the RF front-end also increases the requirements on the sensitivity and dynamic range of the power detectors. Sensitivity-aware design approaches for logarithmic power detectors are investigated in this work. Within this context, the influence of offset cancellation schemes on the performance of wideband logarithmic power

detectors is evaluated. Additionally, the noise contributions from the different sub-circuits are studied, and the factors limiting the sensitivity of wideband large dynamic range RF power detectors are analyzed.

4. **Prototype implementation of an RF front-end with enhanced digital controllability.**
   The feasibility of an integrated implementation of an RF front-end system with enhanced digital controllability is demonstrated with the help of a prototype implementation.

The above-mentioned research aspects are explored for the application area of RFICs for optical transceiver modules in FTTx applications, within the framework of FTTH-ASIC and Mixed-Signal ASIC research projects undertaken at Technische Universität Darmstadt [8, 9]. An extended L-band frequency range of 500 MHz to 2.5 GHz is considered for the RF circuits taking into account the intended application area of satellite communication and broadcast services such as CATV. An architectural diagram of the RF front-end under consideration, highlighting the major research objectives of this work, is illustrated in Figure 1.4.

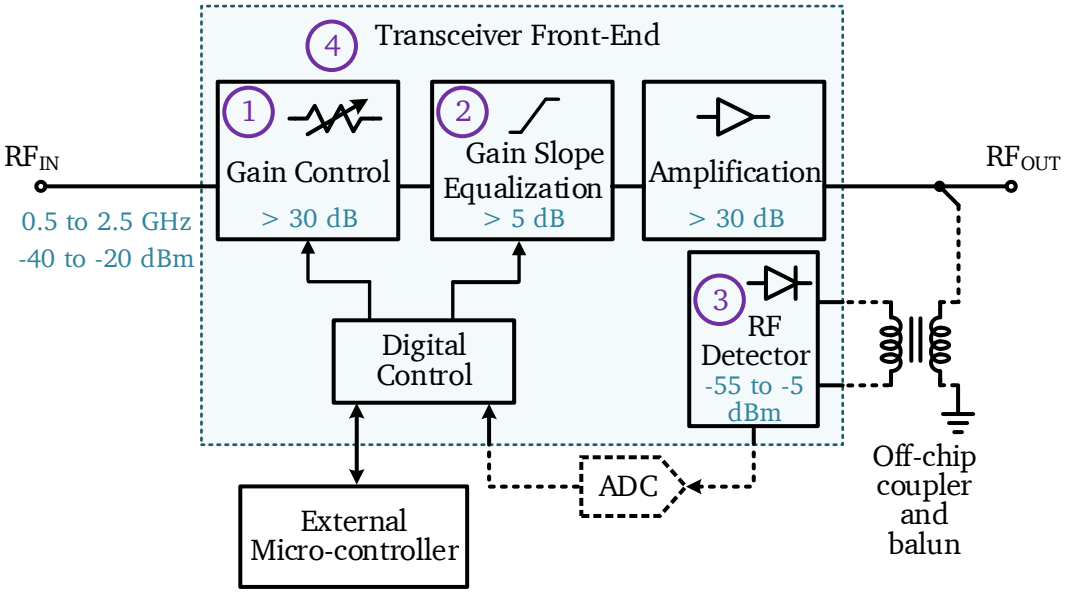

Figure 1.4: Block diagram of the IC implementation of RF transceiver front-end highlighting the research objectives of this thesis. The circled numbers correspond to the numbering in the research objectives listing.

1.3 Outline

This chapter has provided an introduction to the dissertation and stated the research objectives. Chapter 2 describes the system level design considerations of the RF transceiver front-end, with a focus on the architecture, assembly within the package, and the choice of the semiconductor technology for implementation.

Chapter 3 evaluates the influence of the choice of semiconductor technology on the performance of the switched attenuators that are utilized to enable digital control of system gain. Three commonly used switched attenuator topologies are compared with respect to the technology figure of merit that affects the performance of the switched attenuators the most. A design methodology is proposed for this comparison, and the comparison is carried out for different attenuation levels. Finally, digital step attenuators are implemented using switched attenuators to achieve a gain control range larger than 30 dB for the system.

Chapter 4 analyzes the necessity for gain slope equalization in RF front-ends and reviews the state-of-the-art design approaches. The need for a new design approach is described, and a novel digitally controllable gain slope equalizer is proposed. Finally, the design, implementation and results of the proposed gain slope equalizer are presented.

Chapter 5 focuses on the sensitivity-aware design of logarithmic peak power detectors for wideband operation and large dynamic range. The influence of two of the commonly used offset cancellation approaches on the performance of the detector is investigated, and the noise contributions from the different building blocks of the power detector are evaluated. Finally, a wideband logarithmic power detector providing highest sensitivity when compared to other silicon based state-of-the-art wideband large dynamic range logarithmic power detector implementations is presented.

Chapter 6 describes the implementation of an RF front-end system with enhanced digital controllability. An application example of the RF front-end system as part of an RFIC intended for optical transceiver modules in FTTx applications is presented, and the measurement results of the RF front-end system are provided. Chapter 7 presents the conclusion and lists the major contributions of this work.

2 System Level Design Considerations

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An integrated implementation of an RF transceiver front-end calls for focus on specific system-level considerations that help maximize the overall performance of the system. This chapter presents a brief overview of the architectural choices, type of assembly within a package, and choice of semiconductor technology for the realization of the RF front-end being considered in this dissertation.

2.1 Architectural Considerations

A functional block diagram of the RF transceiver front-end system is shown in Figure 2.1. The RF front-end is intended for operation in the receiver mode as well as the transmitter mode. As a result, it needs to be appropriately configurable. Gain control is required to improve the reconfigurability of the RF front-end and to thereby make the system attractive for a wider range of applications.

For analysis purposes, the reconfigurable gain range of a system implementing gain control can be represented by the sum of a fixed part, which is the maximum gain achievable, and a variable part, which is the attenuation range, as given by Equation 2.1.

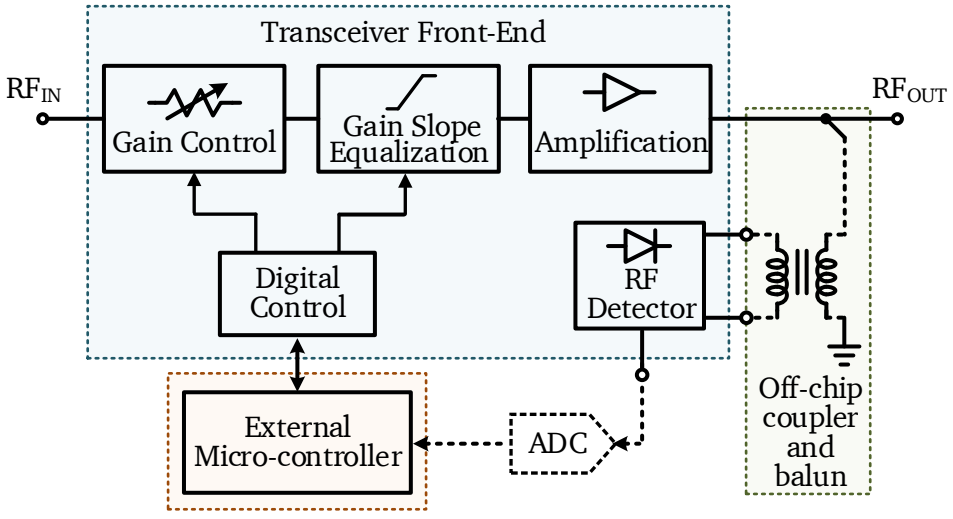

Figure 2.1: Functional block diagram of the RF transceiver front-end.

As the variable part of the system gain increases, the dynamic range at the input and output of the system increases. The input dynamic range is especially important in the receiver mode of operation. A high value for the input dynamic range implies that the range of input powers for which the transceiver provides compression-free output power is also high. Table 2.1 shows the dependence of the input dynamic range on the attenuation range, i.e., the gain control range, for a system with 30 dB fixed gain and 5 dBm compression-free output power.

$$\text{Reconfigurable Gain Range} = \text{Fixed Gain} + \text{Attenuation Range} \tag{2.1}$$

Table 2.1: Influence of attenuation range on system input dynamic range when the fixed part of gain is 30 dB and the compression-free output power is 5 dBm.

Attenuation Range	System input dynamic range
0	-25
10	-25 to -15
20	-25 to -5
30	-25 to 5

The output dynamic range of the system is especially significant in the transmitter mode of operation. A high value for the output dynamic range means that the range of output powers for which the transceiver provides compression-free response is high. Table 2.2 summarizes the dependence of the output dynamic range on the attenuation range when the fixed part of the gain of the system is 30 dB, the maximum compression-free output power is 5 dBm, and the input power is -25 dBm.

Table 2.2: Influence of attenuation range on system output dynamic range when the fixed part of gain is 30 dB and the compression-free input power is -25 dBm.

Attenuation Range	System output dynamic range
0	5
10	-5 to 5
20	-15 to 5
30	-25 to 5

The larger the compression-free input and output dynamic range of the RF front-end, the more attractive it will be to a wider range of deployment conditions. Hence, increasing the gain control range, or attenuation range, of the system is highly desirable.

The selection of the implementation mechanism for the control of gain is important in determining the overall performance of the system. An approach based on active gain control approach or passive gain control can be used to achieve gain reconfigurability through digital control, which is desired here. The following section discusses these approaches and reviews their suitability for the transceiver front-end under consideration.

2.1.1 Active Gain Control

As the name suggests, active gain control approaches use active components for gain control. One approach to the implementation of active gain tuning involves the utilization of variable-gain amplifiers (VGAs), as shown in Figure 2.2. Either of the low-noise amplifier (LNA) or power amplifier (PA) that is part of the RF transceiver front-end could be designed to function as a VGA. The variability in gain can be achieved either by varying the transconductance of the transistors used in the amplifiers, or by employing circuit techniques such as current splitting or current steering [10].

Designing an RF amplifier for variable gain reduces the peak performance of it, and requires trade-offs to certain design specifications. For instance, varying the bias point of a transistor to tune its gain moves it away from the bias point that is required for optimal noise performance in case of a low-noise amplifier. Moreover, to achieve the same linearity performance as that of a design for constant gain, the design for variable gain will consume more power and make the solution power-inefficient [11]. VGA based solutions, hence, compromise the performance of the system. Additionally, digital to analog conversion techniques have to be implemented to convert the digital control signals to analog equivalent control for a VGA implementation.

Another approach to the implementation of active gain tuning is to use variable attenuators that employ active components. Such an approach, however, has the disadvantage that it leads to an increase in the power consumption of the attenuator, apart from also reducing its linearity.

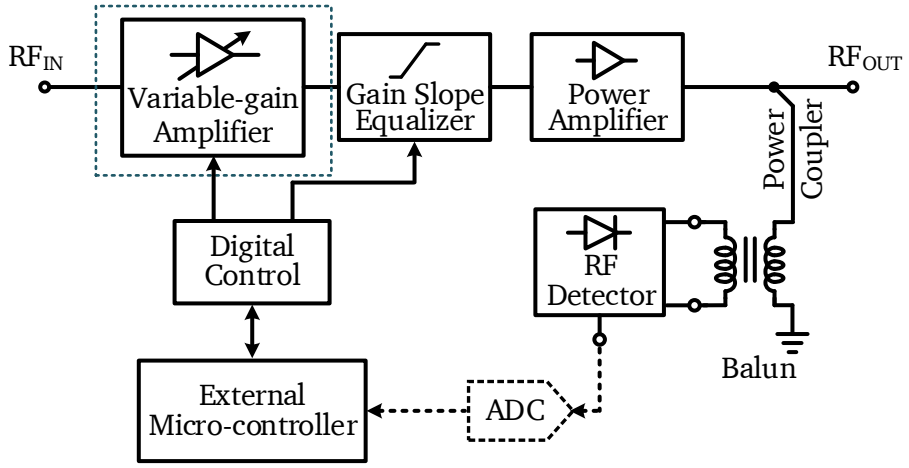

Figure 2.2: RF transceiver front-end with active gain control approach.

2.1.2 Passive Gain Control

A passive network based implementation involves the use of step attenuators to realize the required gain control range, as illustrated in Figure 2.3. Step attenuators consist of cascaded switch attenuation stages and use switches that are controlled by digital control signals to provide the required attenuation level.

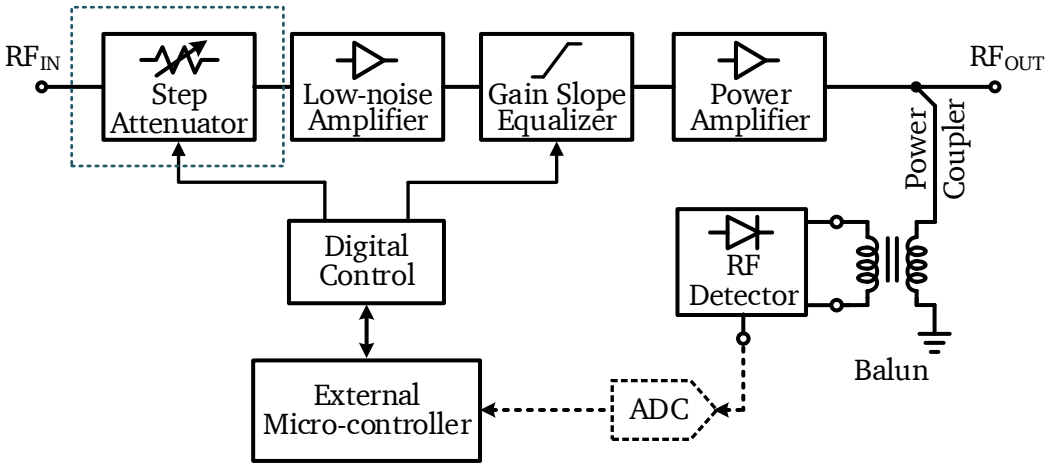

Figure 2.3: RF transceiver front-end with passive gain control approach.

Step attenuators predominantly consist of passive components and the only active components used within them are switches. Transistor switches are used to switch between the attenuation and bypass modes of operation of the individual attenuation stages of a step attenuator. Due to the attenuation itself being achieved using passive components such as resistors, the linearity attainable for the step attenuators is very high. Implementing such a high linearity gain control circuit also helps in improving the overall linearity for the transceiver and reducing the requirements on the linearity of the other circuit blocks that are part of the front-end system. As a result, the power requirements of the overall system reduces. Another advantage that it has, compared to active gain control approaches, is the reduced design complexity. No additional digital to analog interfacing circuits are necessary when step attenuators are employed for gain control. Moreover, passive gain control also provides the possibility to bypass the attenuator circuits when no attenuation is required. These factors make a passive gain control approach more suitable for adoption for the RF transceiver front-end in this work.

2.2 Chip Assembly within a Package

The type of assembly of the chip within a package is another system level design consideration that affects its overall performance. Two different approaches can be considered for the chip assembly, namely a single-chip package based approach or a multi-chip package based approach.

A single-chip package is a chip package that has only one die in it. All the circuit blocks that are part of the system are implemented on this single die, and such an implementation is often referred to as a system-on-chip (SoC). Figure 2.4 illustrates the structural view of a single-chip package. Multi-chip packages, on the other hand, use multiple dies within a package. Different dies are used for the realization of different functional elements on separate semiconductor technologies and they are interconnected within the package to realize a system within a package. A multi-chip package is also known as a system-in-package (SiP). An example illustration of such a system is shown in Figure 2.5.

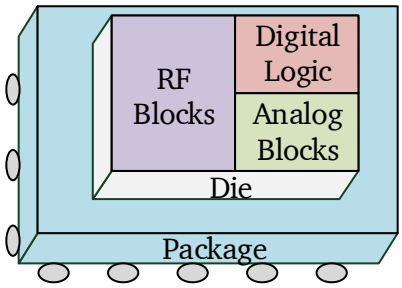

Figure 2.4: Single-chip package or system-on-chip (SoC).

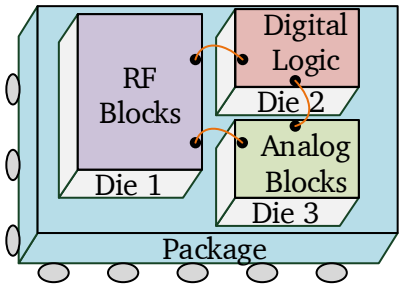

Figure 2.5: Multi-chip package or system-in-package (SiP).

The utilization of multiple dies is advantageous as it facilitates the implementation of different functional elements on technologies more suitable for them. For example, digital technologies could be

realized using an advanced complementary metal oxide semiconductor (CMOS) node, whereas RF circuits could be realized on III-V semiconductor technology nodes that have provision for lower substrate and passive component parasitics and higher breakdown voltages and power handling capabilities.

An evaluation of the different circuit blocks that are part of the architectural block diagram of the RF transceiver front-end under consideration, which is shown in Figure 2.6, is necessary to understand the benefits of a multi-chip package approach for the RF front-end.

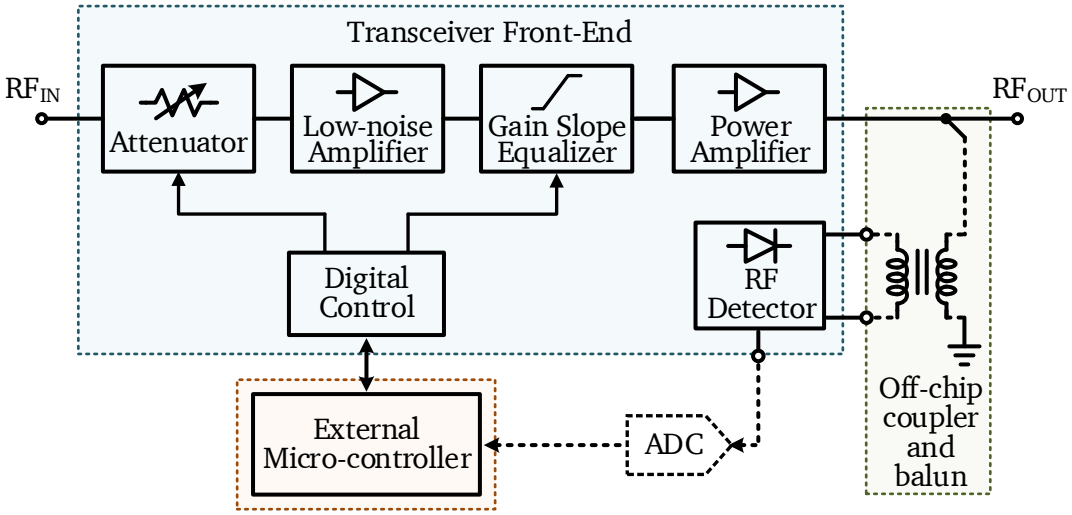

Figure 2.6: Architectural block diagram of the RF transceiver front-end.

The circuit level implementations of the digital gain control and digital gain slope equalization blocks require the utilization of switches. Hence, for these functional blocks, semiconductor technologies having low $R_{on}C_{off}$ values are attractive. The gain in the RF transceiver front-end is provided by two amplifier stages, namely the LNA and PA. For the LNA, a technology that provides transistors with low noise figure and high gain within the bandwidth of interest is attractive. The PA provides high performance when implemented on technologies that provide transistors with high breakdown voltages and high gain within the bandwidth of interest. The digital controller, on the other hand, is best implemented on a low supply voltage CMOS technology.

It can be observed that a multi-chip package implementation using an radio frequency silicon-on-insulator (RF-SOI) technology node for the front-end circuits and the digital logic, and a technology that provides a high breakdown voltage bipolar transistor for PA implementation would be the an attractive solution when considering the performance of the functional blocks of the transceiver. Multi-chip packages, however, require inter-chip connections such as bond-wires, the use of which affects the matching between the different RF circuit blocks and this introduces additional complexity with regards to the modeling effort needed. Moreover, multi-chip packages are costlier if they are not manufactured in a very large scale.

Single-chip package based implementation is more attractive when considering the costs involved and the reduced complexity of realization. Considering these factors, a single-chip packaging approach is preferred in this work.

2.3 Technology Considerations

The choice of a single-chip package or in other words, a SoC implementation for the RF transceiver front-end calls for the selection of a single semiconductor technology for the realization of the die. In

this section, a brief overview of the available technologies and their suitability for the wideband digitally controllable RF front-end is presented.

With the increasing integration of digital control and analog circuits to support RF functionalities, a wide variety of RF systems are being integrated within a single technology. To cater for this demand, research is being driven towards technologies that support the implementation of RFICs with digital control. Silicon based technologies have a distinct advantage for mixed-signal RFICs considering the vastly developed infrastructure that is already in place. Hence, CMOS technologies optimized for RF applications are obvious choices for consideration for the RF transceiver front-end.

Research push is currently also seen in silicon-on-insulator (SOI) technologies that provide attractive opportunities for RF integration in the form of RF-SOI technologies. Silicon-germanium (SiGe) bipolar-complementary metal oxide semiconductor (BiCMOS) technologies, which combine the advantages of silicon (Si) and germanium (Ge) by means of bandgap engineering and provide CMOS as well as bipolar transistors, are also attractive when it comes to RF applications in Si substrates.

RF-SOI technologies are well suited for LNA and RF switch implementations, whereas, SiGe BiCMOS technologies are well suited for RF amplifier implementations and high power applications. Many of the RF-SOI and SiGe BiCMOS technologies also offer digital standard cell libraries that ease the realization of digital logic.

Looking beyond Si, technologies based on compound semiconductors, such as gallium arsenide (GaAs), gallium nitride (GaN), indium phosphide (InP), and indium gallium phosphide (InGaP) are popular choices for high-frequency applications, especially when high power, high gain or low noise performance is the focal point of a design. However, compound semiconductor technologies are less suitable for the integration of digital logic and the cost associated with such an integration is high. As a result, the commercial availability of compound semiconductor technologies with digital logic is constrained. Recent trends have also indicated a tendency for heterogeneous integration of compound semiconductors within Si technologies to combine their respective advantages. However, heterogeneous technologies are not considered for this work as they are still in their emerging phase and their commercial availability is currently limited.

The need for digital controllability and the ease of availability of silicon based digital logic narrows the technology choices for the RF front-end implementation down to RF-SOI, radio frequency complementary metal oxide semiconductor (RF-CMOS), and SiGe BiCMOS technologies. A comparison of the general strengths and weaknesses of these technology classes are provided in Table 2.3.

Table 2.3: Comparison of RF-CMOS, SiGe BiCMOS and RF-SOI technologies.

Technology	Quality of passives	Transistor gain	Suitability for frequencies > 10 GHz	Cost
RF-CMOS	Poor	Good	Limited	Low
SiGe BiCMOS	Poor	Excellent	High	High
RF-SOI	Excellent	Good	Good	High

SiGe BiCMOS and RF-SOI technologies are better suitable for the implementation of the RF transceiver front-end when considering the performance of the overall system, even though the costs associated with them are higher than that of an RF-CMOS based implementation. The SiGe BiCMOS technology is better suitable when the gain and the output power capabilities of the amplifiers are prioritized. Moreover, SiGe HBTs have higher values for unity-current-gain frequency f_{T} and unity-power-gain frequency f_{max}, making them suitable for future bandwidth expansion into frequencies that are higher than that considered in this work. Due to these factors, a commercially available SiGe BiCMOS technology is chosen for this work. In the following sections a brief overview of the SiGe BiCMOS technology is provided.

2.3.1 Overview of SiGe BiCMOS Technology

To improve the current gain of Si bipolar junction transistor (BJT), Ge can be added to the base of the transistors. Ge has a bandgap of 0.66 eV at 300 K, because of a larger lattice constant (approximately 4 percent larger than Si), compared to Si that has a wider bandgap of approximately 1.12 eV at 300K. When Ge is added to the base of the bipolar transistors, the effective bandgap of the SiGe base decreases. The emitter and collector of a SiGe heterojunction bipolar transistor (HBT) remain the same as that of a Si BJT. As a result, the emitter and collector of a SiGe HBT have a wider bandgap than the base. The minority carriers traveling from emitter to base see a drop in bandgap and experience a lower barrier than in a Si BJT. Effectively, more electrons are transported from emitter to collector for the same bias applied to emitter-base junction and the collector current density J_{C} increases. The base current density J_{B} in a SiGe HBT remains the same as that in a Si BJT since the emitter region remains identical for both the devices. The net result is that the current gain β of the transistor, given by Equation 2.2, is higher for a SiGe HBT when compared to a Si BJT [12–15].

$$\beta = \frac{J_C}{J_B} \tag{2.2}$$

Due to the different lattice constants of Si and Ge, the SiGe alloy on a Si substrate has a compressive strain. This compressive strain limits the thickness of the SiGe alloy for a given Ge concentration so as to ensure the stability of the device. A lower thickness is desirable for the base of an npn transistor so that it can provide better high-frequency performance. Hence, the thickness limitation is not an issue in case of the SiGe base realization. However, the thickness limitation usually means that the SiGe bandgap engineering is applied only for the base region [12].

A gradient Ge concentration profile, as shown in Figure 2.7, can be introduced to produce a negative slope in the conduction band from emitter towards collector. The Ge concentration is kept lower near the emitter-base junction and is increased towards the base-collector junction. This gradient profile produces an electric field in the base region. The electrons, which are minority carriers in the base of an npn transistor, are accelerated through this electric field and this drifting effect, which is considerably faster than diffusion, reduces the base transit time significantly. As a result, SiGe HBTs exhibit better high frequency behavior and achieve higher f_{T} and f_{max} when compared to Si BJTs [12], [16, p.30], [17, p.225]. Hence, SiGe HBTs are more suitable for wideband RF amplifier applications.

The important features of SiGe technology, in comparison to other technologies used for high frequency applications, can be summarized as follows [13, 20, 21]:

SiGe devices achieve significantly higher f_{T} and f_{max} values than CMOS devices for a given lithography node, provide higher breakdown voltages, and are more reliable than CMOS devices. To achieve the same performance, SiGe requires lower power than CMOS. Compared to silicon BJTs, SiGe HBTs provide higher current gain due to the increase in collector current resulting from SiGe base.

Compared to compound semiconductor technologies, SiGe technologies have lower cost, and its noise performance is almost comparable to GaAs. SiGe HBTs have lower breakdown voltage compared to GaAs devices and, as a result, the maximum power output is limited. Due to the poorer isolation and increased parasitics of silicon substrate, the quality factor of passives in SiGe technologies is low. At RF frequencies, this becomes an important consideration. RF switches on GaAs, for instance, have extremely low distortion at high RF power compared to silicon based switches. Hence, switching performance is worse on SiGe compared to implementations on GaAs.

When the SiGe HBTs are combined with traditional Si based CMOS on the same process to offer a SiGe BiCMOS technology, the advantages of Si with regards to its integration levels, mature processing

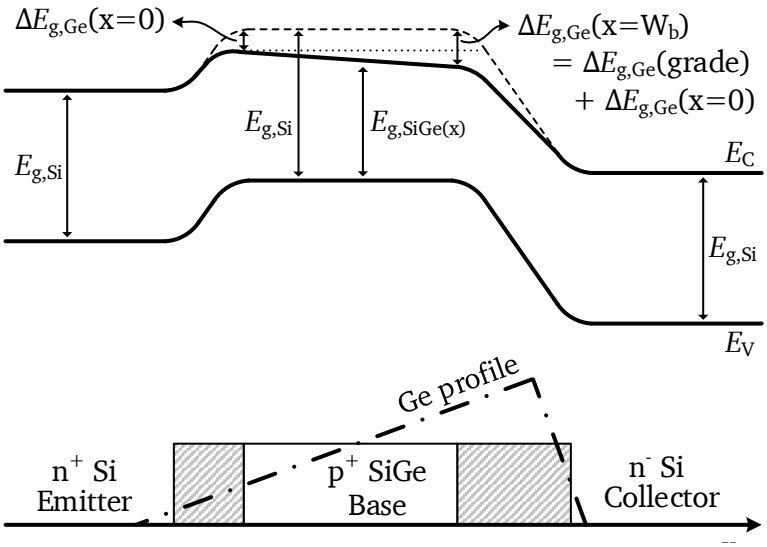

Figure 2.7: Energy band diagram of a SiGe HBT with graded base profile [12, 18, 19].

capabilities, yield, and cost, and the advantages of SiGe with regards to its high performance RF capabilities, are combined together to provide solutions for RF system on chip applications. Considering these factors, a commercially available SiGe BiCMOS technology is chosen for the realization of the RF front-end presented in this work.

2.4 Summary

This chapter has introduced three major system and architectural level design considerations of the RF transceiver front-end. Firstly, the active and passive gain control approaches have been compared to select the optimal solution for the implementation of digital gain control of the system. Secondly, the system-on-chip and the system-in-package assembly type of the chip within a package have been compared with respect to their suitability to the transceiver front-end system under consideration. Thirdly, the selection of the semiconductor technology for the implementation of the transceiver front-end is discussed.

Based on the evaluations presented in the chapter, a passive gain control approach is chosen with the aim of achieving high linearity for the system, and a system-on-chip realization based on a commercially available SiGe BiCMOS technology is chosen considering the high-frequency broadband performance, complexity, and implementation costs of the system.

3 Technology Considerations in the Design of Digitally Controllable Attenuators

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This chapter introduces the different conventionally used switched attenuator topologies and evaluates the influence of the choice of technology on the performance of these attenuators. Based on these evaluations, wideband attenuators intended for passive gain control of the RF transceiver front-end are designed. Parts of this chapter have been published as a research paper in [113].

3.1 Introduction

As described in Section 2.1, the step attenuator based gain control approach is employed in RF transceiver front-ends when digital control and high linearity are desirable. The block diagram of a system utilizing attenuator based gain control is shown in Figure 3.1. Step attenuators introduce a digitally controllable loss in the system and assist in controlling the overall gain. The most commonly used step attenuators adopt switched architectures, wherein digital control is provided using switches.

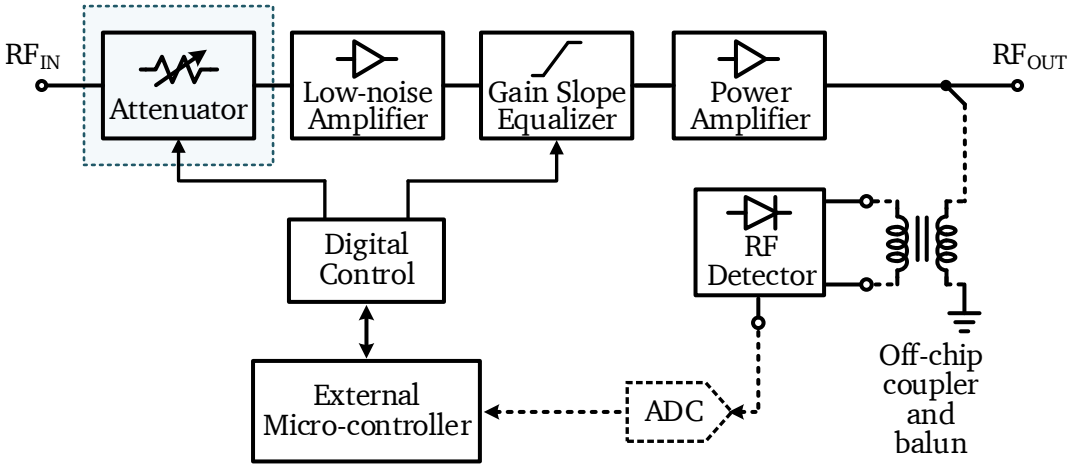


Figure 3.1: Attenuator based gain control in an RF front-end.

The variable gain setting in a step attenuator is realized by using a combination of attenuators designed for different attenuation levels. Each sub-stage is designed for a specific level of attenuation, and when

cascaded together, the overall attenuator system provides levels of attenuation that can be digitally controlled [22–24].

An example of a step attenuator that provides an attenuation range of 7 dB with a step resolution of 1 dB is shown in Figure 3.2. The attenuator is built by cascading three attenuation stages having attenuation levels of 1 dB, 2 dB, and 4 dB in series. Table 3.1 shows the levels of attenuation achievable for different digital control settings for this attenuator. The individual attenuator stages are designed based on the required source and load impedance. Compared to a single attenuator that provides 7 dB attenuation, such a cascaded architecture facilitates finer gain control. This is helpful in many systems where the required step size of gain settings are small. When no attenuation is required, the digital control bits can be set to logic zero, and the attenuator system can be bypassed.

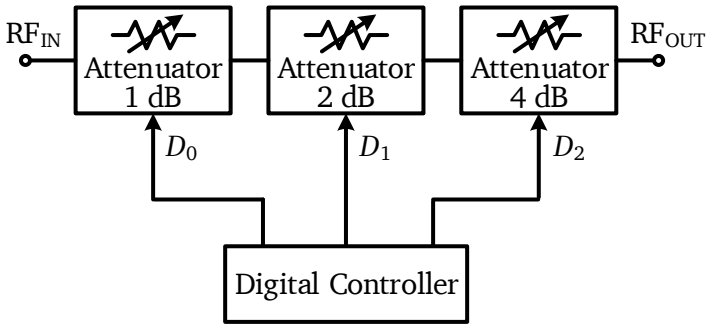


Figure 3.2: Block diagram of a step attenuator with 7 dB attenuation range and 1 dB step resolution.

Table 3.1: Attenuation levels corresponding to different digital settings for the attenuator in Figure 3.2.

D_2	D_1	D_0	Attenuation Level [dB]
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

3.2 Switched Attenuators

The basic building block of a step attenuator system is the so called switched attenuator. As the name suggests, switched attenuators are controlled by switches, and can be switched between two modes of operation, namely, the attenuation mode and the bypass mode. In the bypass mode, the switches are set in such a way that the attenuator provides zero attenuation, whereas, in the attenuation mode, the switches are set to provide the required attenuation level. In real implementations, there will losses associated the both the bypass and attenuation modes. The loss in the bypass mode is known as the insertion loss of the attenuator, whereas the frequency dependent deviation of the attenuation level results in a non-zero attenuation flatness in the attenuation mode.

Three topologies are frequently adopted for switched attenuator implementations, namely, switched Pi attenuators, switched T attenuators, and switched bridged-T attenuators. The switched Pi attenuator utilizes a Pi-network architecture, as shown in Figure 3.3. Assuming the switches to be ideal and the

source and load impedance to be equal to Z_0, the relations between the attenuation level in the attenuation mode and the values of the resistors in the network are given by Equations 3.1 and 3.2.

$$R_{\mathrm{P,Pi}} = Z_0 \cdot \frac{K+1}{K-1} \tag{3.1}$$

$$R_{\mathrm{S,Pi}} = Z_0 \cdot \frac{K^2-1}{2 \cdot K} \tag{3.2}$$

$$K = 10^{\left(\frac{L_{\mathrm{dB}}}{20}\right)} \tag{3.3}$$

where, K is the impedance factor and L_{dB} is the attenuation level in the attenuation mode in decibels.

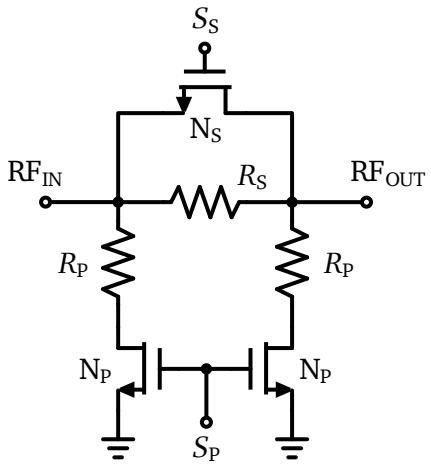


Figure 3.3: Switched Pi attenuator topology.

The switched T attenuator utilizes a T-network, as shown in Figure 3.4. Assuming the switches to be ideal and the source and load impedance to be equal to Z_0, the values of the resistors $R_{\mathrm{P,T}}$ and $R_{\mathrm{S,T}}$ can be determined from the desired attenuation level in the attenuation mode using the relations in Equations 3.4 and 3.5.

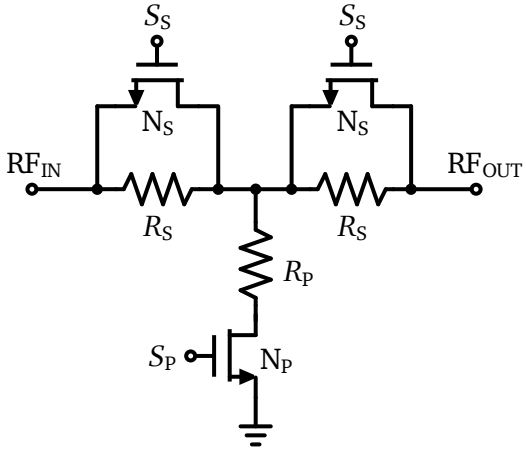


Figure 3.4: Switched T attenuator topology.

$$R_{\text{P,T}} = 2 \cdot Z_0 \cdot \frac{K}{K^2 - 1} \tag{3.4}$$

$$R_{\text{S,T}} = Z_0 \cdot \frac{K - 1}{K + 1} \tag{3.5}$$

The switched bridged-T attenuator uses the network architecture shown in Figure 3.5. Assuming the switches to be ideal and the source and load impedance to be equal to Z_0, the values of the resistors $R_{\text{P,BrT}}$ and $R_{\text{BR,BrT}}$ can be determined from the desired attenuation level using the relations in Equations 3.6 and 3.7.

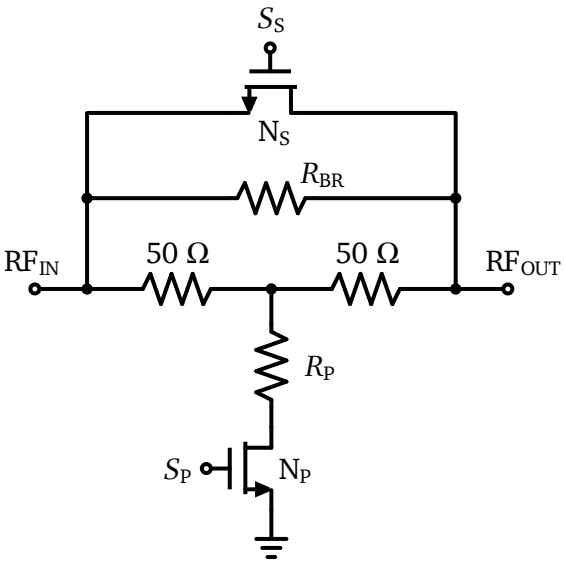


Figure 3.5: Switched bridged-T attenuator topology for 50 Ω source and load impedance.

$$R_{\text{P,BrT}} = \frac{Z_0}{K - 1} \tag{3.6}$$

$$R_{\text{BR,BrT}} = Z_0 \cdot (K - 1) \tag{3.7}$$

A comparative study of the three topologies is important to understand their advantages and disadvantages with respect to specific applications and the design goals that need to be met. The next section evaluates the performance of the three switched attenuator topologies, with considerations for the influence of technology and the required attenuation level.

3.3 Influence of Technology in Integrated Implementations of Switched Attenuators

The technology chosen for an integrated implementation of an RF front-end is not always the technology that could maximize the performance of the attenuator when it is considered independently. If the primary area of focus in an RF front-end IC is towards amplifier performance, as is the case in this work, then the performance of attenuators will have to be compromised. In this section, the limitations that the technology places on the performance of switched attenuator realizations are analyzed. Additionally, a comparative study of the performance of the switched Pi, switched T, and switched bridged-T topologies, with a focus on the technology constraints affecting their performance, is presented.

3.3.1 RF Switches and their Technology Dependence

The component that plays the most decisive role with regards to the achievable performance of a switched attenuator is the RF switch. GaAs and SOI based technologies have been at the forefront of integrated RF attenuator implementations due to the high quality of RF switches realizable using these technologies [25]. These technologies provide a high resistivity substrate and better isolation for switches when compared to CMOS based technologies. However, with the increasing use of CMOS and BiCMOS technologies for RFICs, CMOS based switches are also being widely used for RF switches and switched attenuators [8-10].

While designing switches for switched attenuators, a compromise has to be found between the performance in the bypass state and the performance in the attenuation state. In the bypass state, insertion loss and return loss are the most important performance indicators, whereas, in the attenuation state, the attenuation level, attenuation flatness, and return loss are significant. Due to its attenuating nature, the noise figure of an attenuator is the same as its attenuation level. Phase error and linearity are other relevant performance indicators for a switched attenuator. Phase error has to be minimized in dynamic switching applications. However, in systems where only a static control is needed, similar to the work in focus, the influence of phase error is negligible. The inherently passive resistor based implementation caters for excellent linearity for the switched attenuators. As a result, their linearity and power handling capabilities are sufficiently large for the application under consideration.

To improve the performance of RF switches, large isolation resistors, as shown in Figure 3.6, can be added to the gate and bulk connections [26–28]. Isolated NMOS transistors also help in improving the switch performance as demonstrated in [27]. However, the fundamental performance limitation arises from the so called $R_{on}C_{off}$ figure of merit of the technology. A low value for $R_{on}C_{off}$ will facilitate a low insertion loss and good isolation for RF switches. Minimizing the value of $R_{on}C_{off}$ has been a primary focus in many recent technologies focusing on RF switch based applications. Compared to an $R_{on}C_{off}$ in the range of 400 fs to 500 fs and above for 3.3 V based silicon technologies, recent advances show that $R_{on}C_{off}$ values below 150 fs are available in many advanced technologies [25]. The large range of possible values for $R_{on}C_{off}$ based on the technology selected makes the evaluation of the influence of the technology choice on the performance of switched attenuators of paramount importance.

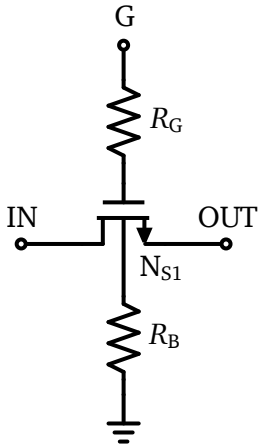


Figure 3.6: NMOS switch with large isolation resistors for high frequency applications.

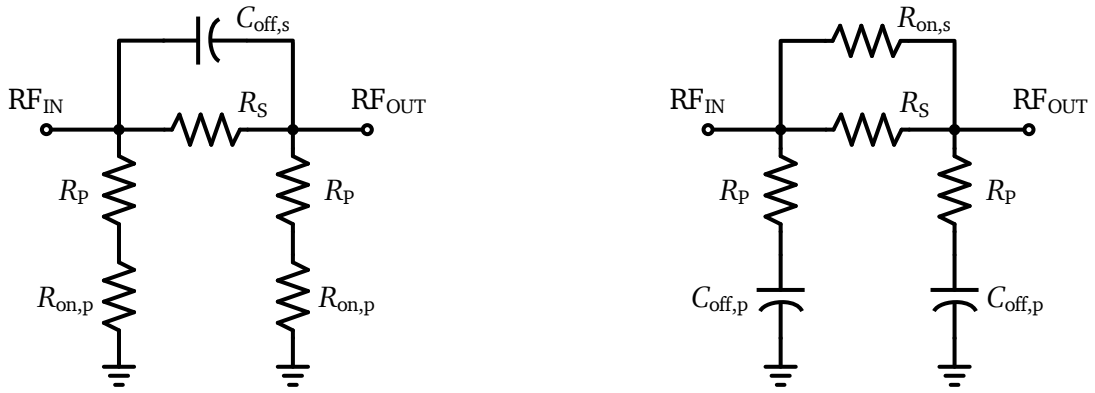
To parameterize the influence of switches on the performance of switched attenuators, a simplified equivalent circuit model of a MOS switch, as shown in Figure 3.7 is used [22]. In the on-state, the switch is approximated by a resistance R_{on} and in the off-state, it is approximated by a capacitance C_{off}. This model assumes that the junction capacitances and the impedances to the substrate are negligibly small.

(a) On-state. **(b)** Off-state.

Figure 3.7: Equivalent model of NMOS switch.

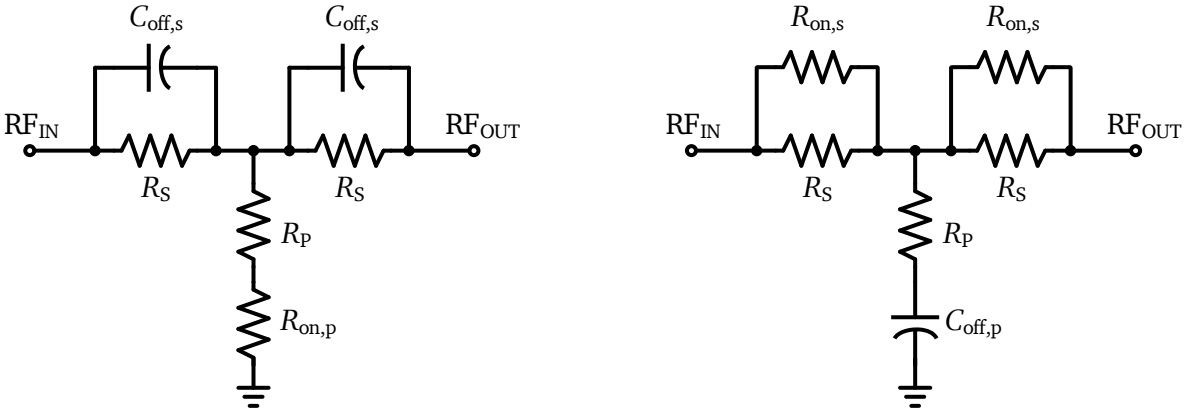
3.3.2 Technology Dependence of Switched Attenuators

Based on the $R_{on}C_{off}$ model of a switch, separate equivalent circuits are created for the bypass state and the attenuation state of the switched Pi, T, and Bridged-T attenuators [22, 28]. Figures 3.8, 3.9, and 3.10 show the equivalent models for the bypass and attenuation states of a switched Pi attenuator, switched T attenuator, and a switched bridged-T attenuator, respectively.



(a) Attenuation state. **(b)** Bypass state.

Figure 3.8: Equivalent model of switched Pi attenuator.

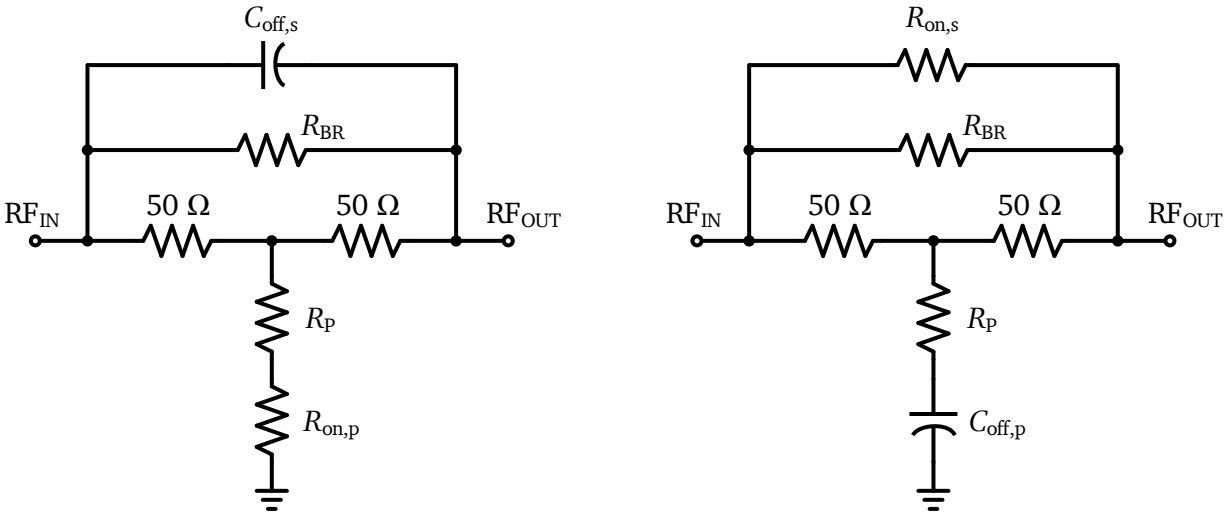


(a) Attenuation state. **(b)** Bypass state.

Figure 3.9: Equivalent model of switched T attenuator.

If the $R_{on}C_{off}$ value of a technology is known, the choice of $R_{on,s}$ and $R_{on,p}$ values would simultaneously also determine the $C_{off,s}$ and $C_{off,p}$ values as given by Equation 3.8.

$$C_{off,s} = \frac{R_{on}C_{off}}{R_{on,s}} \quad ; \quad C_{off,p} = \frac{R_{on}C_{off}}{R_{on,p}} \tag{3.8}$$



(a) Attenuation state. **(b)** Bypass state.

Figure 3.10: Equivalent model of switched bridged-T attenuator.

For the switches that are connected to ground, the value of $R_{on,p}$ influences the attenuation level and the return loss in the attenuation state, and the value of $C_{off,p}$ affects the return loss and the insertion loss in the bypass state. A very low $R_{on,p}$ is not necessary because of the series connection of resistance R_P and $R_{on,p}$ in the attenuation state. $R_{on,p}$ can be even as high as R_P, in which case the resistor R_P is removed from the circuit. However, such a scenario would mean that the shunt resistor is implemented using a transistor alone and it will compromise the linearity of the attenuator.

To achieve high linearity and to maintain a low value for $C_{off,p}$, the value of $R_{on,p}$ is chosen to be K_{SW} times the value of R_P, as given by Equation 3.9, where K_{SW} is a design constant. To ensure that the net resistance of the path to ground is equal to R_P, the value of the degeneration resistor is simultaneously replaced by R'_P, as given by Equation 3.10. This helps in maintaining the attenuation level at its desired value. The value of K_{SW} is found through simulations and set equal to 0.25 in this analysis as it presents a good solution, where the value of $C_{off,p}$ is maintained sufficiently low without having to compromise on the linearity of the system.

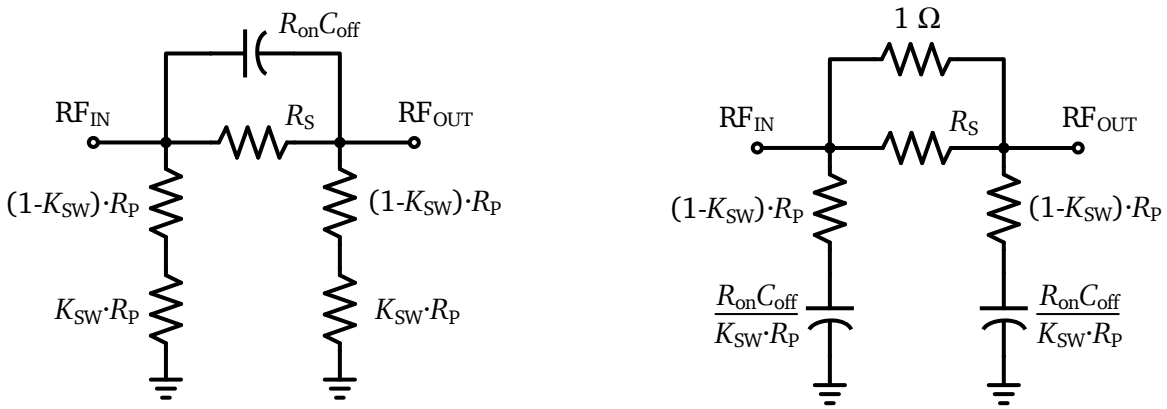
$$R_{on,p} = K_{SW} \cdot R_P \tag{3.9}$$

$$R'_P = (1 - K_{SW}) \cdot R_P \tag{3.10}$$

In the bypass state, the insertion loss of a switched attenuator is predominantly determined by the value of $R_{on,s}$. To achieve a low insertion loss, a very low $R_{on,s}$ is desirable. However, $C_{off,s}$ will increase at the same time, and the attenuation flatness and the return loss in the attenuation state will be degraded. Based on the design requirements, a compromise needs to be found. $R_{on,s}$ is set to 1 Ω in this analysis with the aim of minimizing the insertion loss in the bypass state.

Simplified models are created for the switched Pi, switched T, and switched bridged-T attenuators in the attenuation and bypass modes of operation based on the value of $R_{on,s}$ adopted here. Figure 3.11 shows the models for a switched Pi attenuator. The models for a switched T attenuator and a bridged-T attenuator can be drawn similarly.

Simulations are performed based on the chosen values of $R_{on,s}$ and K_{SW} to analyze the influence of $R_{on}C_{off}$ on the performance of the circuit for attenuation levels from 0.5 dB to 16 dB. A bandwidth of 500 MHz to 2.5 GHz is considered for this analysis. Due to the wideband nature, the average values



(a) Attenuation mode. **(b)** Bypass mode.

Figure 3.11: Simplified equivalent models of a switched Pi attenuator.

of the relevant parameters across the bandwidth of interest are evaluated, and the s-parameters are characterized using their magnitudes instead of their decibel values to keep the performance figures linear. Equation 3.11 is used for the evaluation of attenuation flatness. Lower $\Delta|S_{21}|$ in the attenuation state implies better flatness.

$$\Delta|S_{21}| = |S_{21,high}| - |S_{21,low}| \tag{3.11}$$

where, $|S_{21,high}|$ and $|S_{21,low}|$ are, respectively, the maximum and the minimum values of S_{21} within the bandwidth of interest. Figure 3.12 shows the attenuation flatness at different attenuation levels for the switched Pi, T, and bridged-T topologies. As the value of $R_{on}C_{off}$ is swept from 150 fs to 600 fs, the performance degradation is clearly visible for the switched Pi and switched bridged-T attenuators. However, the degradation in flatness is less prominent for switched T attenuators.

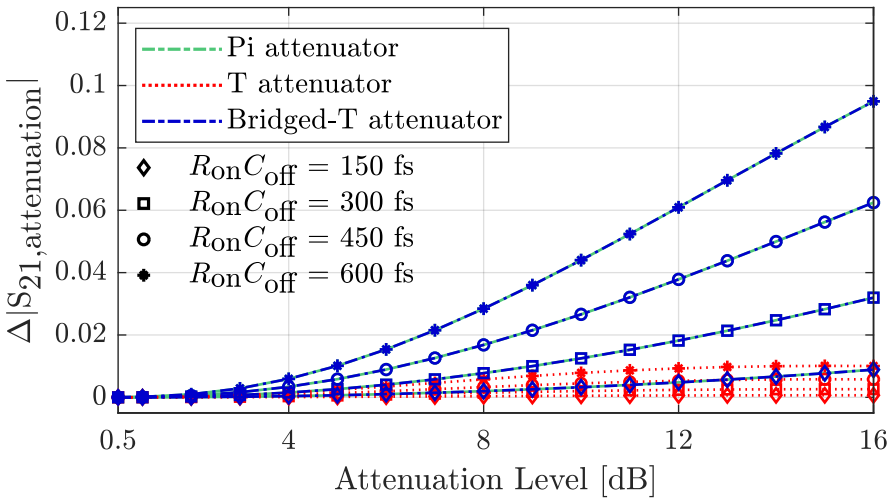


Figure 3.12: Measure of attenuation flatness across 500 MHz to 2.5 GHz in attenuation mode.

Figure 3.13 shows the measure of insertion loss performance at different attenuation levels for the switched Pi, T, and bridged-T topologies in their bypass modes. The insertion loss is minimum when the magnitude of S_{21} is closer to 1. It can be observed that the switched Pi attenuator and the switched bridged-T attenuator have lower insertion loss. As the value of $R_{on}C_{off}$ is swept from 150 fs to 600 fs, there is a small increase in insertion loss for the Pi and T attenuators, and a noticeable increase in insertion loss

for bridged-T attenuators. It can also be observed that the influence of the attenuation level is greater than the influence of $R_{on}C_{off}$ for the insertion loss performance.

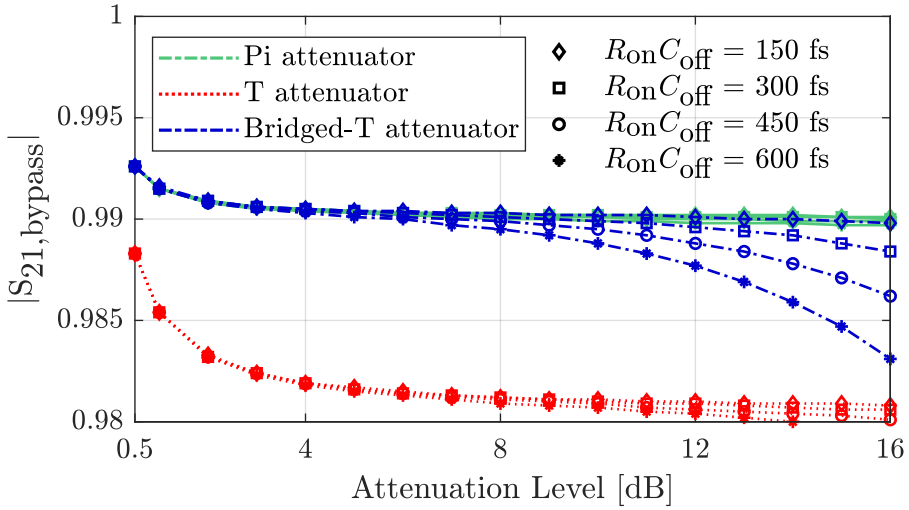


Figure 3.13: Measure of insertion loss across 500 MHz to 2.5 GHz in bypass mode.

The input return loss plots are shown in Figures 3.14 and 3.15, respectively, for the attenuation and bypass modes of operation of the switched attenuators. It can be observed that in the bypass mode of operation, the return loss performance is better for switched Pi attenuators. In the attenuation mode of operation, the performance is better for switched T attenuators. The influence of the value of $R_{on}C_{off}$ is more prominent in the attenuation mode than in the bypass mode of operation.

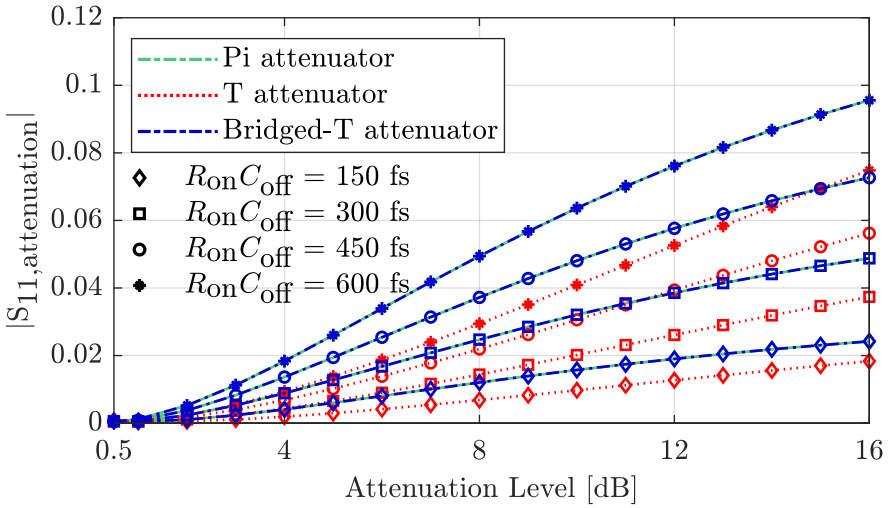


Figure 3.14: Measure of return loss across 500 MHz to 2.5 GHz in attenuation mode.

The evaluations presented here show that at lower attenuation levels, the choice of the particular topology and technology is less critical to the overall performance. However, as the attenuation level increases beyond 4 dB, the influence of the topology choice and the technology of implementation are more significant. At higher attenuation levels, the switched Pi and T topologies show better performance. The Pi-topology provides lower insertion loss and better reflection performance in the bypass state, whereas the T-topology shows better flatness and higher reflection performance in the attenuation state.

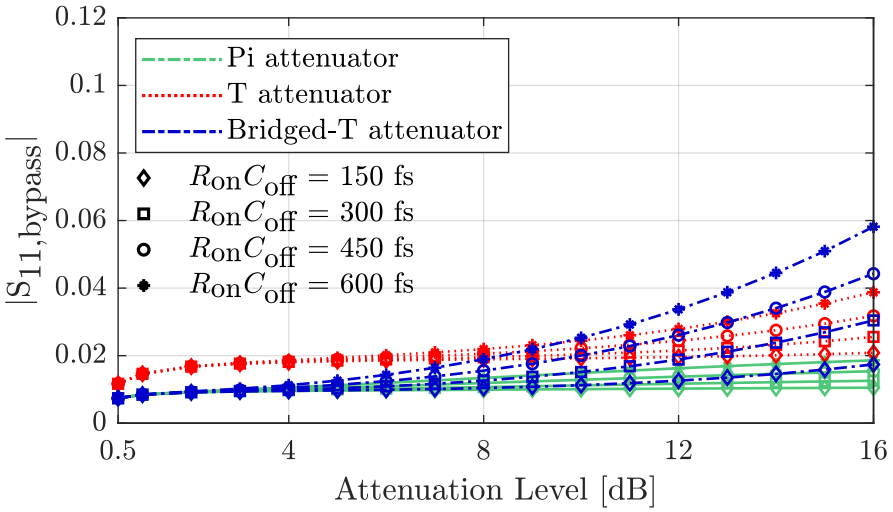


Figure 3.15: Measure of return loss across 500 MHz to 2.5 GHz in bypass mode.

The results presented also highlight how lower values of $R_{on}C_{off}$ are favourable for the overall performance of the switched attenuators.

3.4 Implementation Example of RF Step Attenuator in SiGe BiCMOS Technology

For the RF front-end implementation in this work, a lower insertion loss is desirable in order to maintain the influence of the attenuator circuits minimal when they are bypassed. As a result, the switched Pi attenuator has been chosen for the attenuator implementation. At least six attenuation stages are necessary to achieve a dynamic range larger than 30 dB and a step resolution of 0.5 dB for the step attenuator. The individual attenuation stages implemented here adopt binary scaling from 0.5 dB to 16 dB, and the combination of attenuation stages are 0.5 dB, 1 dB, 2 dB, 4 dB, 8 dB, and 16 dB. Instead of implementing a single cascade of six stages to achieve the total attenuation range, a split-attenuator architecture has been employed in this work. As the number of stages in the cascade is increased, the difficulty in achieving the desired impedance matching increases due to the difference in return loss performance of the different sub-stages. To simplify the matching requirements and to maintain a high value for the input return loss of the overall RF front-end, the coarse attenuator is placed before the LNA, and the fine attenuator is placed after the LNA. The high isolation of the LNA circuit helps in reducing the influence of the lower return loss of the fine attenuator at the input port of the RF front-end system.

A coarse attenuator comprising of a cascade of 8 dB and 16 dB attenuation sub-circuits and a fine attenuator comprising of a cascade of 0.5 dB, 1 dB, 2 dB, and 4 dB sub-stages are designed using the switched Pi topology. The schematic diagrams of the implemented coarse and fine attenuators are shown in Figures 3.16 and 3.17, respectively. Input matching inductors and coupling capacitors are added at the input and output ports of the fine and coarse attenuators to improve the return loss performance and for direct current (DC) blocking, respectively. The inductors had an inductance of 800 pH and were synthesized with the help of electro-magnetic (EM) modeling software. Patterned ground shield was added in the metal 1 layer underneath the inductors to help maintain a high inductor Q-factor. The inductor itself was realized as orthogonal structures using thick top metals having a width of 13 µm. Number of turns was set to two to reduce the overall area of the inductors.

The design focused on achieving attenuation levels relative to the insertion loss in bypass mode instead of focusing on the absolute values of attenuation levels. The expected relative attenuation levels and the corresponding digital states of the coarse and fine attenuators are given in Tables 3.2 and 3.3, respectively.

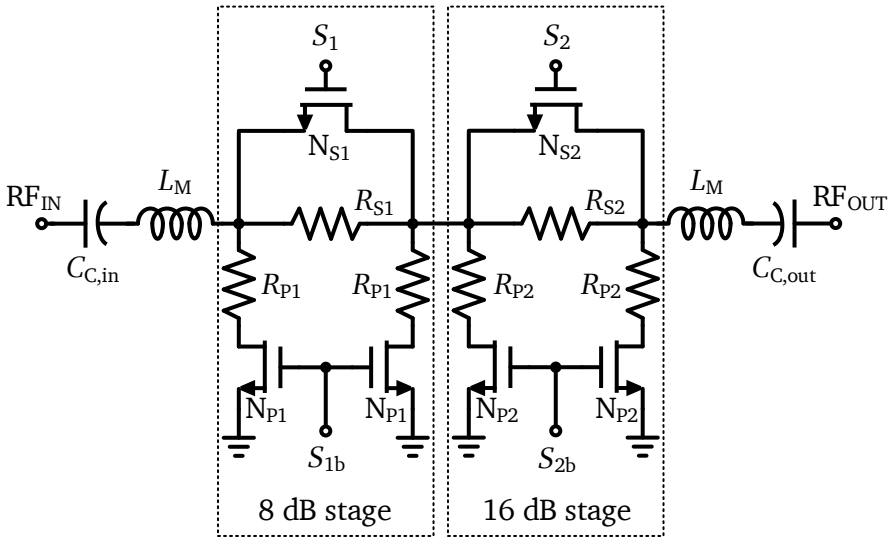


Figure 3.16: Schematic of the implemented coarse attenuator. S_{1b} and S_{2b} are inverted logic of S_1 and S_2, respectively.

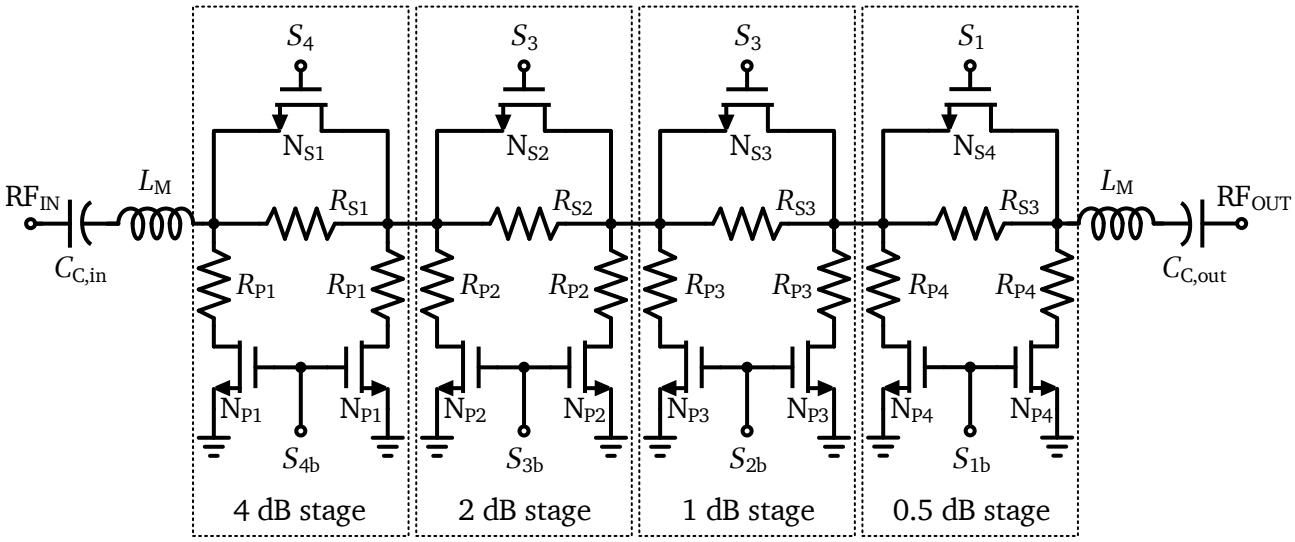


Figure 3.17: Schematic of the implemented fine attenuator. Here, S_{ib} denotes the inverted logic of S_i, where i = 1, 2, 3, 4.

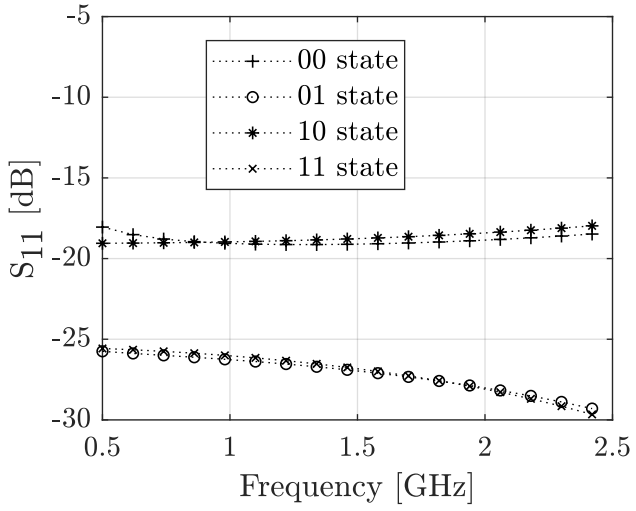
Table 3.2: Target attenuation levels for the coarse attenuator.

S_2	S_1	Attenuation Level [dB]
0	0	0
0	1	8
1	0	16
1	1	24

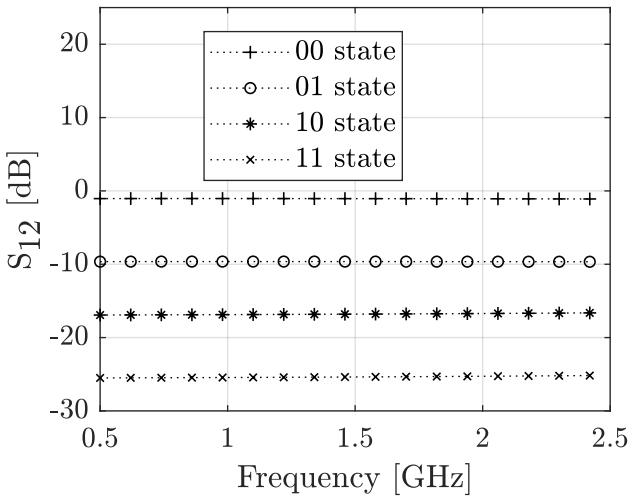
Parasitic-extracted post-layout simulation results of the s-parameters of the coarse and fine attenuators are illustrated in Figure 3.18 and 3.19, respectively. The coarse and fine attenuators have input and output return loss larger than 12 dB across the bandwidth of interest. The coarse attenuator has an insertion loss less than 1.24 dB, whereas the fine attenuator has an insertion loss less than 2.17 dB across the bandwidth of interest.

Table 3.3: Target attenuation levels for the fine attenuator.

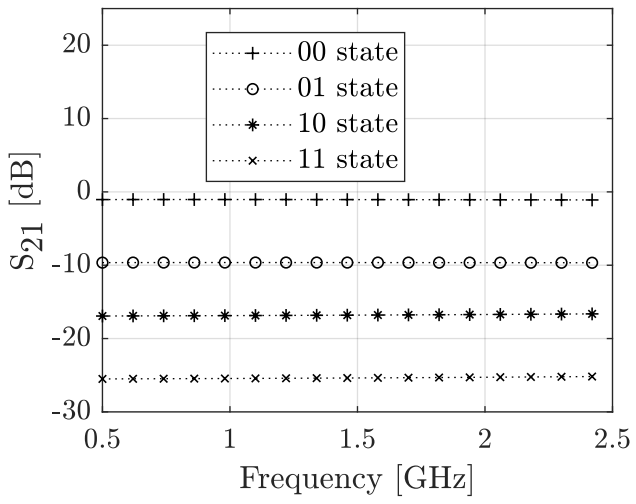
S_4	S_3	S_2	S_1	Attenuation Level [dB]
0	0	0	0	0
0	0	0	1	0.5
0	0	1	0	1
0	0	1	1	1.5
0	1	0	0	2
0	1	0	1	2.5
0	1	1	0	3
0	1	1	1	3.5
1	0	0	0	4
1	0	0	1	4.5
1	0	1	0	5
1	0	1	1	5.5
1	1	0	0	6
1	1	0	1	6.5
1	1	1	0	7
1	1	1	1	7.5



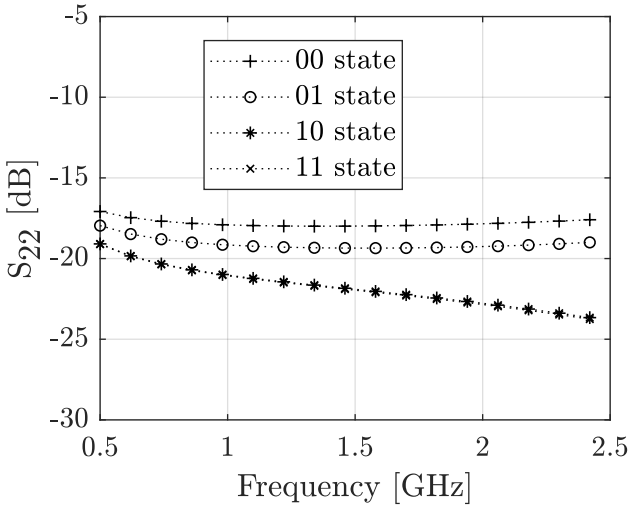
(a) Input return loss S_{11}.



(b) Reverse transmission gain S_{12}.

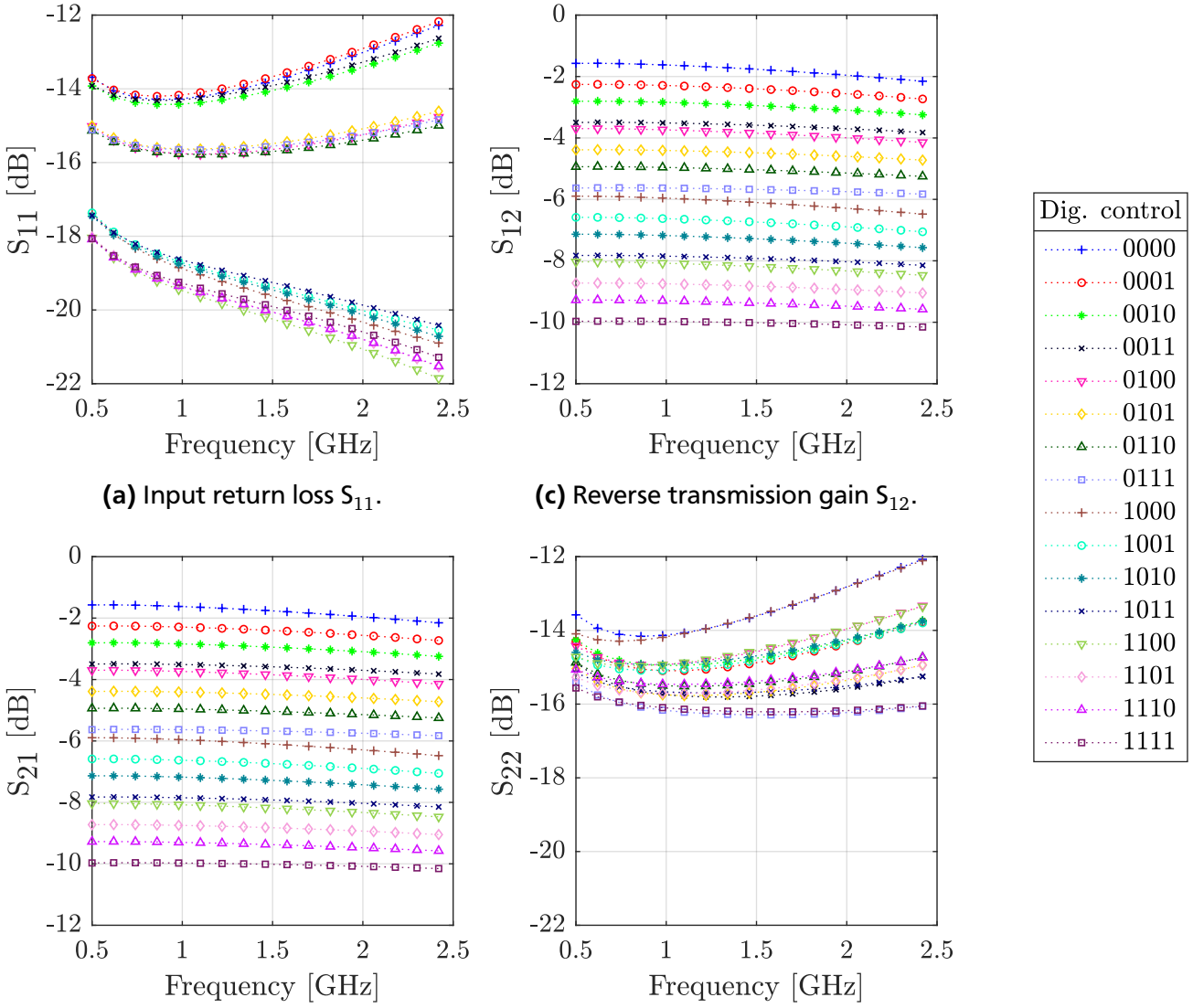


(c) Forward transmission gain S_{21}.



(d) Output return loss S_{22}.

Figure 3.18: Parasitic-extracted post-layout s-parameter simulation results of coarse attenuator.



(a) Input return loss S_{11}.

(c) Reverse transmission gain S_{12}.

(b) Forward transmission gain S_{21}.

(d) Output return loss S_{22}.

Figure 3.19: Parasitic-extracted post-layout s-parameter simulation results of fine attenuator.

Two-tone simulations were performed to measure the linearity performance of the designed attenuators. The two tones were separated by an offset of 50 MHz, and the simulations were performed at the center frequency of 1.5 GHz, and 1.55 GHz. Based on parasitic-extracted post-layout simulations, it was observed that the coarse attenuator achieves an input intercept point larger than 34.91 dBm across the different attenuation settings, whereas, the fine attenuator achieves an input intercept point larger than 36.97 dBm across the different attenuation settings. The large values of input intercept points were designed to facilitate sufficient linearity performance for the overall RF front-end.

3.5 Summary

This chapter investigated the constraints that the choice of technology places on the performance of wideband RF switched attenuators. The performance of three commonly used switched attenuators, namely the switched Pi attenuator, the switched T attenuator and the switched bridged-T attenuator, were evaluated using the simplified equivalent circuit model of an NMOS RF switch. A methodology was then introduced to compare the switched Pi, switched T and switched bridged-T attenuator topologies for wireline applications, where the influence of phase variations can be neglected.

The comparative simulations demonstrated that the switched Pi attenuator provides the lowest insertion loss and return loss in bypass mode, whereas the switched T attenuator provides the best attenuation flatness and return loss in attenuation mode across the wide bandwidth of interest. Based on the comparative analysis, it was also found that the switched bridged-T attenuator showed the poorest performance when considering the return loss, insertion loss, and attenuation flatness achievable. Additionally, the evaluations also showed that the attenuation flatness, insertion loss, and return loss of the switched attenuators become poorer as the attenuation level increases.

Finally, switched Pi attenuator based coarse and fine attenuators were designed for integration into the RF front-end of an RFIC that is realized using a SiGe BiCMOS technology. The two attenuators provide an overall attenuation range larger than 30 dB, with a minimum step size of 0.5 dB. Switched Pi attenuators were employed considering their low insertion loss and high return loss in the bypass mode of operation.

4 Digitally Controllable Gain Slope Equalizers

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This chapter introduces the working principle of gain slope equalizers and discusses the various state-of-the-art implementations before highlighting the need for a new design approach suitable for mixed-signal RFICs. Thereafter, a novel design technique is presented, and its various design considerations and performance criteria are analyzed. Finally, a wideband digitally controllable gain slope equalizer implementation is presented, and its results are evaluated. Parts of this chapter have been published as a research paper in [114].

4.1 Introduction

A common issue in RF applications is the degradation of the signal along its path. Various factors could influence the degradation of the signals at higher frequencies. These include, among others, losses due to the channel, skin effect losses, losses due to the cascaded placement of dissipative components, mismatches between the terminations of the components in the signal path, and variations in temperature. The frequency-dependent degradation of the gain of the signal is commonly known as gain slope variation, sometimes also referred to as gain tilt.

Gain slope variation can lead to several undesirable effects. In digital transmission channels, gain slope variations could lead to effects such as distortion, inter-signal interference (ISI), and inter-channel interference (ICI) [29–32]. Equalizer circuits like continuous-time linear equalizers, decision feedback equalizers, and discrete-time linear equalizers are incorporated in these applications to overcome these effects and to provide bandwidth extension. In fiber links, gain tilt leads to distortion effects [33]. Kikushima et. al. analyzed the distortion, prominently the composite second order (CSO) distortion, which results from the coupling between the gain tilt of the fiber amplifier and the laser chirp [34]. CSO distortion degrades the ability of an erbium-doped fiber amplifier (EDFA) to be used in an amplitude modulation frequency division multiplexing (AM-FDM) optical analog video transmission system. In broadband radio frequency applications, the gain roll-off with frequency predominantly influences the

gain flatness of the system. This roll-off, in turn, has a negative influence on the system's dynamic range and overall performance. Compensation of gain slope variations is often required to stabilize the gain slope and to improve the gain flatness. In some applications, gain slope compensation is needed before digitization to ensure flat performance across the bandwidth of interest [35].

Gain slope equalizers, also referred to as gain tilt equalizers, are slope equalization circuits that are used to correct the gain slope variations. The principle of gain slope equalization is illustrated in Figure 4.1. It shows that the gain slope equalizer introduces an opposite slope characteristic to the slope response of the system without an equalizer. This way, the flatness of the overall gain response across the frequency band of interest is improved.

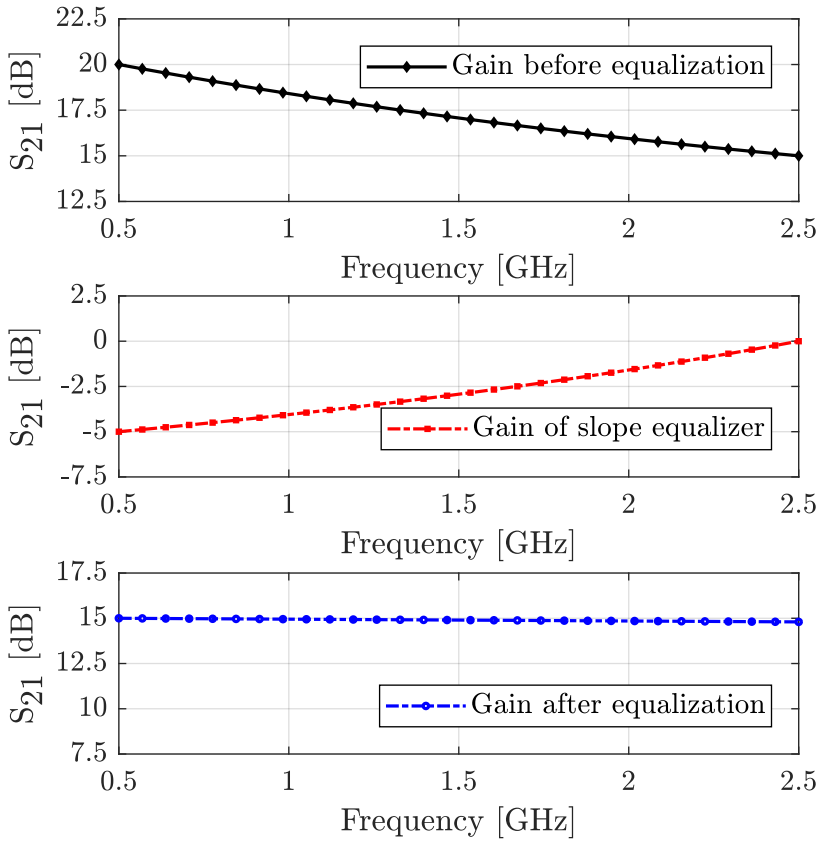


Figure 4.1: Representational image describing the principle of gain slope equalization.

The tunability of the gain slope is another aspect that is important for many applications. By controlling the slope, the required compensation levels can be manipulated during the operation of an IC or in circumstances where the application demands static or dynamic adaptive control. Digital controllability is being increasingly employed in complex mixed-signal RFICs. Digital control of gain slope will increase the range of applications in which an equalizer circuit could find deployment. These factors are driving the research in novel design approaches for the implementation of gain slope equalizers with high integration potential and digital control. The RF transceiver front-end under consideration in this work, shown in Figure 4.2, utilizes such a gain slope equalizer.

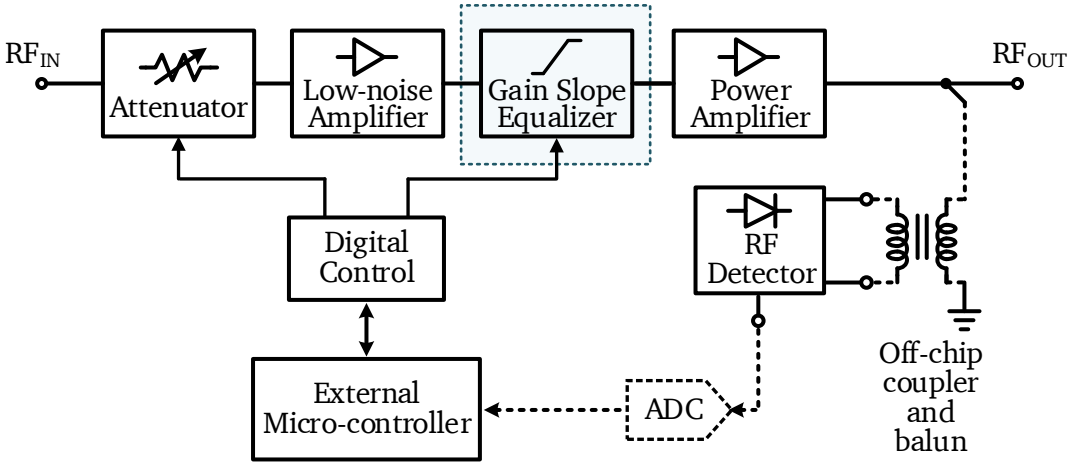


Figure 4.2: Gain slope equalizer as part of the RF transceiver front-end.

The next section reviews the state-of-the-art integrated implementations of gain slope equalizers.

4.2 Literature Review

Different approaches to the implementation of gain slope equalizers have been reported in literature.

4.2.1 State-of-the Art Implementations Suitable for Microwave Applications

A gain tilt equalizer for EDFAs was presented by Kikushima in [33]. An optical fiber bandpass filter was used for this purpose. Goosen et. al. presented another optical power equalizer to equalize the power levels of different wavelength channels and used micro-electro-mechanical system (MEMS) structures for the realization [36].

A p-type intrinsic n-type (PIN) diode based gain slope equalizer was presented by Bera in [37]. The paper demonstrated the equalizer's capability to provide temperature and gain slope compensation by generating positive and negative slopes. However, PIN diodes are bulky and not commonly available in Silicon-based integrated technologies.

Transmission lines have found widespread use for gain slope equalizer implementations in very high-frequency applications [35]. Various implementations based on coplanar or substrate integrated waveguides [38, 39], microstrip transmission lines and resonators [35, 40–42] have been reported. However, these solutions are bulky and mostly used in microwave applications. They are less suitable for integration in silicon substrate based RFICs.

4.2.2 State-of-the Art Implementations Suitable for Silicon RFICs

Integrated solutions for gain slope equalization have also been presented in academic literature. A GaAs millimetre-wave integrated circuit (MMIC) traveling-wave amplifier (TWA) utilizing a thermistor as part of a microwave attenuator for gain equalization was presented by Fejzuli et. al. in [43]. Thermistors are, however, not convenient for RFIC integration on silicon substrates.

Sun et. al. introduced a GaAs metal-semiconductor field effect transistor (MESFET) based MMIC implementation of gain slope equalizer utilizing on-chip resonators [44]. Another implementation based on resonator circuits was presented by Turkmen et. al. in [45]. Resonator circuits need multiple inductors

for their realization and implementations based on them would push the overall area to undesirable values when considering their integration potential for complex SoC RFICs.

An active gain slope equalizer was described by Çalışkan et. al. in [46]. Active equalizers consume more power and have lower linearity when compared to their passive counterparts. Passive approaches are also better when high power handling capability is desirable.

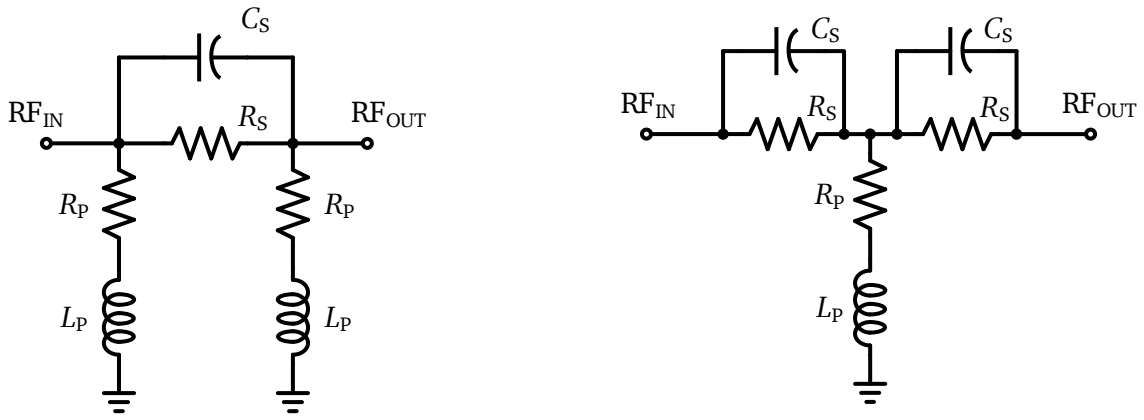
The state of the art design approaches are not conducive for integrated implementation in applications where high linearity, high power handling capability, and digital controllability are required. The rest of the chapter describes approaches to the design of gain slope equalizers that are better suited to these applications.

4.3 Cascaded Attenuators based Equalization

Digitally controllable gain slope equalization can be achieved by using cascaded attenuator stages, where each of the individual stages is designed to provide a frequency-dependent attenuation having a different slope. By cascading the stages, the different slopes are combined to achieve a large gain slope equalization range. These approaches have traditionally been used in board-level implementations and have limitations when considering their silicon integration potential. An overview of the approach is provided in the next section before its merits and demerits are discussed.

4.3.1 Overview of the Design Approach

Different types of resistive attenuator networks could be used for the cascaded gain slope equalization design, namely the Pi attenuator, the T attenuator or the bridged-T attenuator. To achieve a frequency-dependent gain slope, a simple Pi attenuator could be modified as illustrated in Figure 4.3a, by the addition of the capacitor C_S and inductor L_P to the resistive network. The attenuation of such a network decreases with frequency and the slope of the attenuation characteristic depends on the value of C_S and L_P. Similarly, a simple T attenuator could be modified as illustrated in Figure 4.3b to provide a frequency-dependent gain slope.



(a) Pi-stage gain slope equalizer.

(b) T-stage gain slope equalizer.

Figure 4.3: Single stage gain slope equalizers.

In a cascaded architecture, each of the individual stages can be designed to have different attenuation slope characteristics. Each of these stages is designed for input and output matching to the required characteristic impedance. When these individual stages are connected in series, the overall circuit provides

a digitally controllable attenuation slope. For example, for a given bandwidth if the gain slope of N individual stages are designed to be GS_1, GS_2, up to GS_N, respectively in decibels, then the overall gain slope range of the cascaded structure, in decibels, would be given by:

$$GS_{TOTAL} = GS_1 + GS_2 + ... + GS_N \tag{4.1}$$

If s_1, s_2, up to s_N are the control bits used to switch each of the N individual stages between the equalization mode and the bypass mode of operation, then the overall gain slope for the cascaded circuit, in decibels, can be represented as:

$$GS_{TOTAL} = s_1 \cdot GS_1 + s_2 \cdot GS_2 + ... + s_N \cdot GS_N \tag{4.2}$$

where,

$$s_i = \begin{cases} 1 & \text{when stage i is operated in gain equalization mode} \\ 0 & \text{when stage i is operated in bypass mode} \end{cases}$$

Multi-stage gain slope equalizers can be designed based on the cascaded architecture. An example implementation of such a multi-stage gain slope equalizer is discussed in the following section.

4.3.2 Example Implementation based on Three-stage Attenuation

An example cascaded gain slope equalizer based on the T attenuator network is shown in Figure 4.4. Three stages of T attenuators are cascaded to achieve a gain slope equalization range of 7.5 dB across a bandwidth of 300 MHz to 2.5 GHz using this circuit. The attenuation characteristic of the circuit is shown in Figure 4.5.

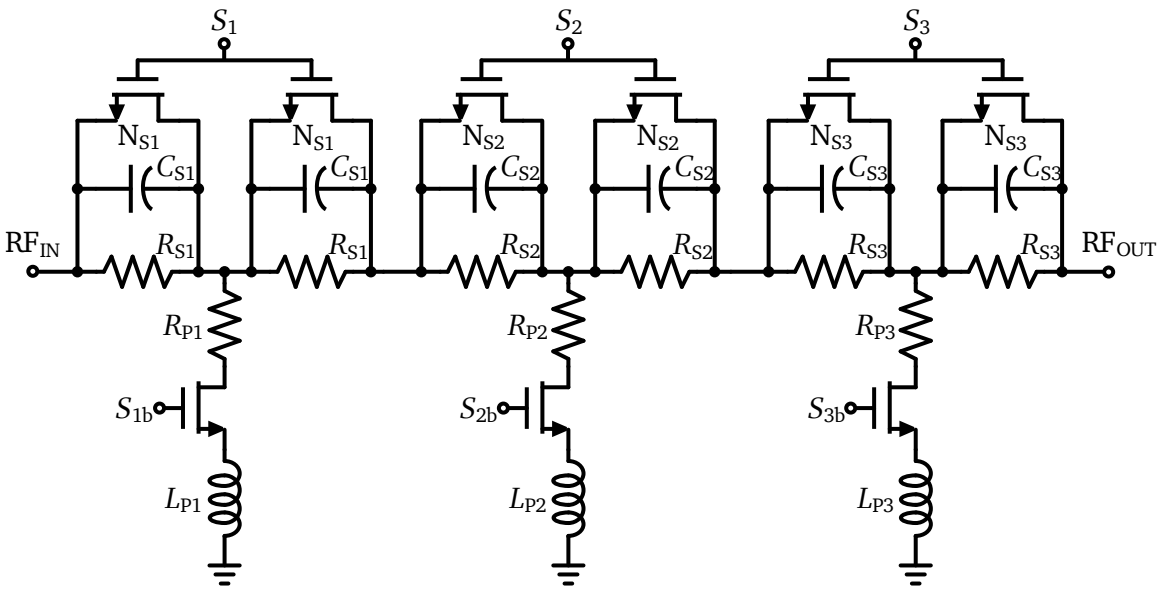


Figure 4.4: Schematic of a three-stage switched T attenuator based gain slope equalizer. Here, S_{ib} denotes the inverted logic of S_i, where i = 1, 2, 3.

Each attenuator stage in the cascade needs a different value of bridge capacitor C_S and degeneration inductor L_P to achieve the required slope characteristic. The multiple degeneration inductors that are required for this implementation makes the realization area intensive. A more area-efficient approach based on a single-stage network is proposed in the following section.

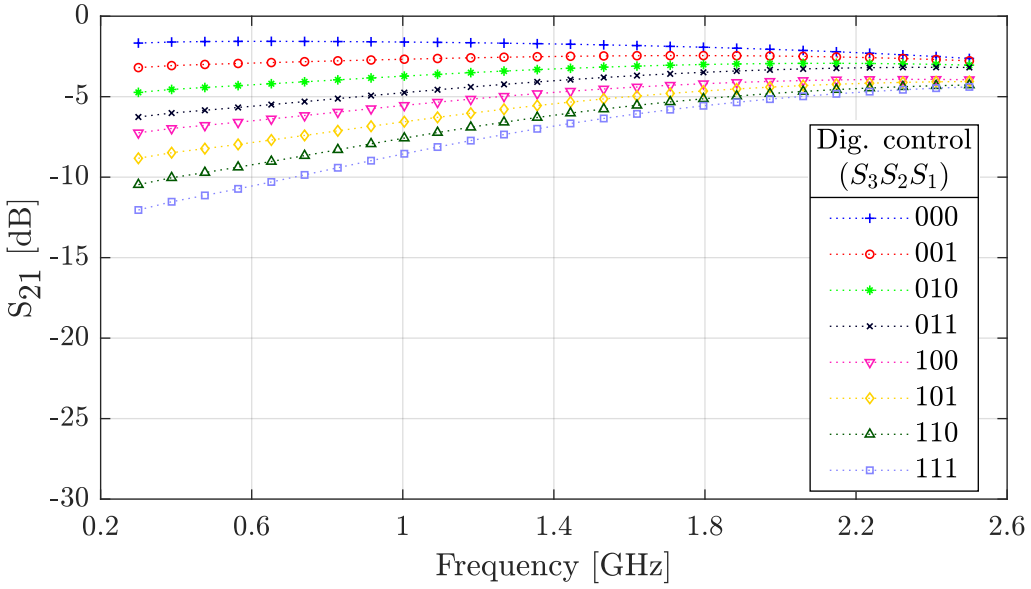


Figure 4.5: Attenuation characteristic of the three-stage switched T attenuator based gain slope equalizer.

4.4 Modified Bridged-T Network based Equalization

Bridged-T networks are commonly used as attenuator stages and are particularly suitable for utilization when the input (or source) and the output (or load) impedances are equal. A bridged-T impedance network is shown in Figure 4.6. Due to its passive nature, the bridge-T network is attractive for high linearity applications. The impedances Z_{S1} and Z_{S2} are kept equal to the characteristic impedance to achieve good impedance matching performance, Z_{BR} is the bridge impedance, and Z_P is the degeneration impedance of the branch to ground.

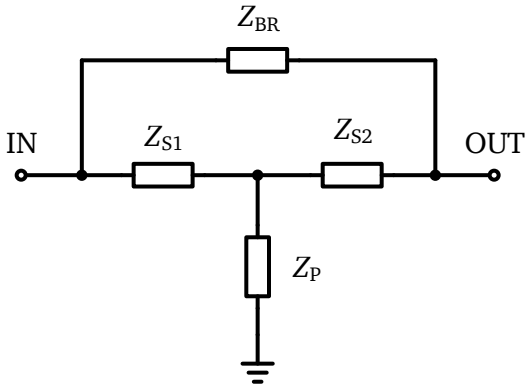


Figure 4.6: Schematic of a bridged-T impedance network.

S-parameters are more measurement friendly for high-frequency applications, compared to other two-port network parameters due to the comparative ease of achieving termination with known impedance as opposed to the short circuits or the open circuits that are necessary for conventional z, y, h or g-

parameters. As a result, the s-parameter representation shown in Equation 4.3 is of interest for the bridged-T impedance network. The voltage transfer function of the network is given by Equation 4.7.

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \frac{1}{\Delta_1} \begin{bmatrix} (Z'_{11}-1)(Z'_{22}+1) - Z'_{12}Z'_{21} & 2Z'_{12} \\ 2Z'_{21} & (Z'_{11}+1)(Z'_{22}-1) - Z'_{12}Z'_{21} \end{bmatrix} \tag{4.3}$$

where,

$$Z'_{11} = \frac{Z_{11}}{Z_0}; Z'_{12} = \frac{Z_{12}}{Z_0}; Z'_{21} = \frac{Z_{21}}{Z_0}; Z'_{22} = \frac{Z_{22}}{Z_0} \tag{4.4}$$

$$\Delta_1 = (Z'_{11}+1)(Z'_{22}+1) - Z'_{12}Z'_{21} \tag{4.5}$$

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_P + \dfrac{Z_2(Z_{BR}+Z_3)}{Z_{BR}+Z_2+Z_3} & Z_P + \dfrac{Z_2 Z_3}{Z_{BR}+Z_2+Z_3} \\ Z_P + \dfrac{Z_2 Z_3}{Z_{BR}+Z_2+Z_3} & Z_P + \dfrac{Z_3(Z_{BR}+Z_2)}{Z_{BR}+Z_2+Z_3} \end{bmatrix} \tag{4.6}$$

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{Z_{\text{BR}}Z_{\text{P}} + Z_{\text{S1}}Z_{\text{S2}} + Z_{\text{S1}}Z_{\text{P}} + Z_{\text{S2}}Z_{\text{P}}}{Z_{\text{BR}}Z_{\text{S1}} + Z_{\text{BR}}Z_{\text{P}} + Z_{\text{S1}}Z_{\text{S2}} + Z_{\text{S1}}Z_{\text{P}} + Z_{\text{S2}}Z_{\text{P}}} \tag{4.7}$$

4.4.1 Resistive Bridged-T Attenuation

Only resistors are used in the network when the bridged-T network is designed for a flat attenuation characteristic across frequency. In such scenarios, Z_{BR}, Z_{S1}, Z_{S2}, and Z_{P} are replaced with R_{BR}, R_{S1}, R_{S2}, and R_{P}, respectively. The resistors R_{S1} and R_{S2} are replaced with 50 Ω resistors when impedance matching to 50 Ω is considered at the input and output. The resulting network is shown in Figure 4.7.

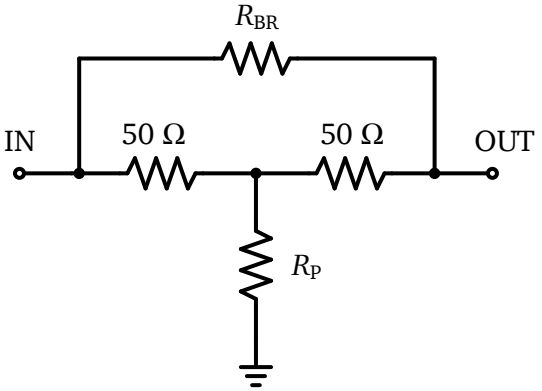


Figure 4.7: Bridged-T resistive attenuator matched to 50 Ω characteristic impedance.

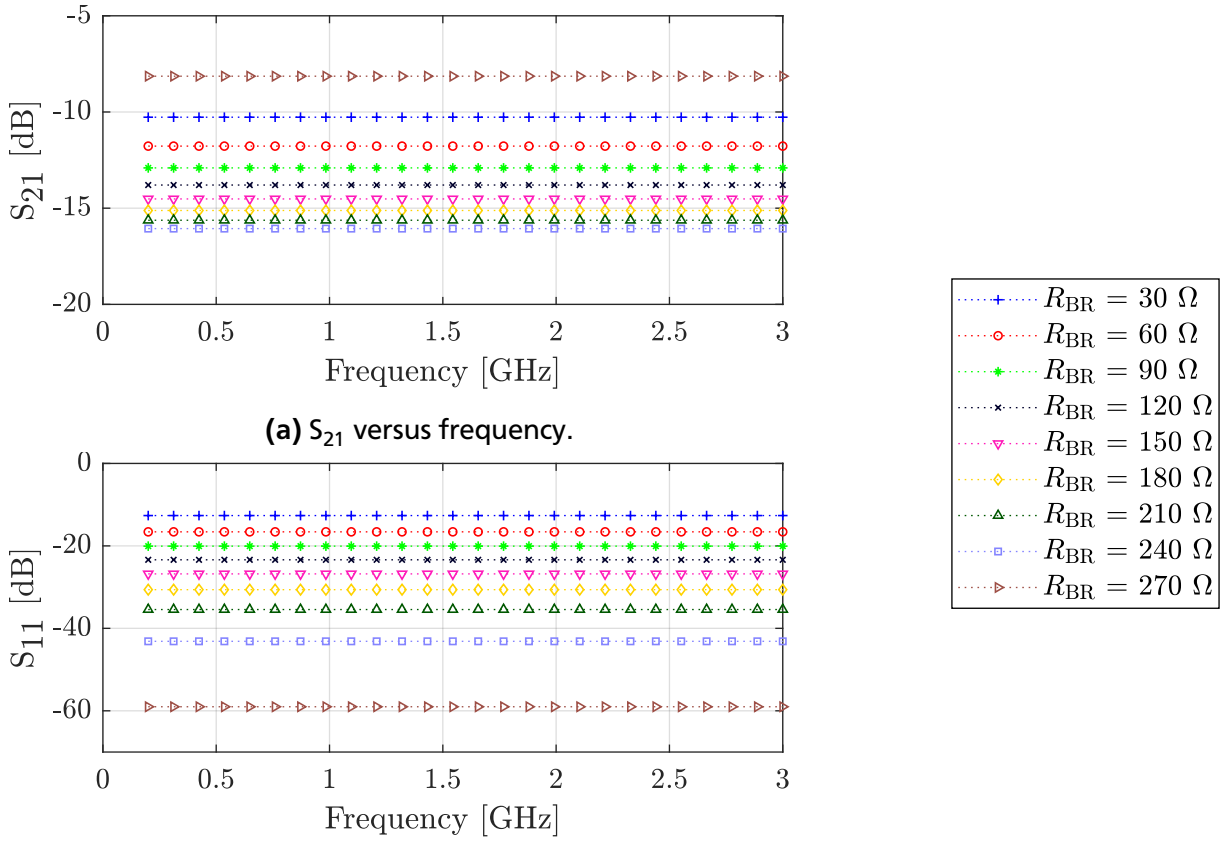
The s-parameters of the circuit can be derived from Equations 4.3, 4.4 and 4.5. The transfer function of the circuit is given by Equation 4.8. The resistors R_{BR} and R_{P} are selected depending upon the required attenuation level. Table 4.1 shows selected values for R_{BR} and R_{P} to achieve different attenuation levels under 50 Ω impedance matching conditions. Varying one of R_{BR} or R_{P} when keeping the other constant changes the attenuation level and return loss of the network.

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{R_{\text{BR}}R_{\text{P}} + 100R_{\text{P}} + 2500}{R_{\text{BR}}R_{\text{P}} + 50R_{\text{BR}} + 100R_{\text{P}} + 2500} \tag{4.8}$$

Table 4.1: Attenuation levels and resistor values of an ideal resistive bridged-T network under 50 Ω impedance matching conditions.

R_{BR} [Ω]	R_P [Ω]	Attenuation [dB]
6.10	409.77	1
12.94	193.10	2
29.24	85.48	4
75.59	33.07	8
265.48	9.41	16

As illustrated in Table 4.1, a 16 dB attenuation is achieved if R_{BR} is equal to 265.48 Ω and R_P is equal to 9.41 Ω. To understand the effect of varying the value of R_{BR}, it is varied from 270 Ω to 30 Ω in 30 Ω steps. It can be observed from Figure 4.8a that the attenuation level decreases as R_{BR} is reduced from 270 Ω to 30 Ω. Similarly, the input return loss decreases as the value of R_{BR} reduces from 270 Ω to 30 Ω, as depicted in the plot in Figure 4.8b. Because of the symmetric nature of the circuit, the same behavior is true for the output return loss. For most practical considerations, a return loss in the order of 12 dB is acceptable and hence, the variation of the bridge resistor does not compromise the matching of the system considerably. The results presented here demonstrate that the resistive bridged-T network can be configured as a tunable attenuator by adjusting the value of R_{BR}.



(a) S_{21} versus frequency.

(b) S_{11} versus frequency.

Figure 4.8: Variation of (a) forward transmission gain S_{21} and (b) input return loss S_{11} with frequency for different values of bridge resistor R_{BR}. R_P is equal to 9.41 Ω.

4.4.2 Reactive Bridged-T Frequency-Dependent Attenuation

The circuit and the results considered in Section 4.4.1 were purely resistive. The attenuation response of such a resistive bridged-T network is flat and frequency-independent. When passive structures such as capacitors and inductors are added to the network, the attenuation becomes frequency-dependent. Such networks can be configured to provide gain slope equalization.

For the bridged-T network presented so far, the addition of a capacitor in parallel to the bridge resistor R_{BR} or an inductor in series to the degeneration resistor R_P, as shown in Figure 4.9a, leads to a frequency-dependent attenuation characteristic. More complex RLC resonator networks could be considered to build the bridged-T network. However, the addition of resonator networks makes the network area-intensive. Therefore, resonator networks are avoided in this work to maintain the implementation area-efficient. The focus on a tunable attenuation characteristic, in turn, leads us to the modified attenuator network having a variable R_{BR} as shown in Figure 4.9b. In the following sections, this circuit is referred to analyze the influence of adding a capacitor in parallel to R_{BR} and/or adding an inductor in series with R_P.

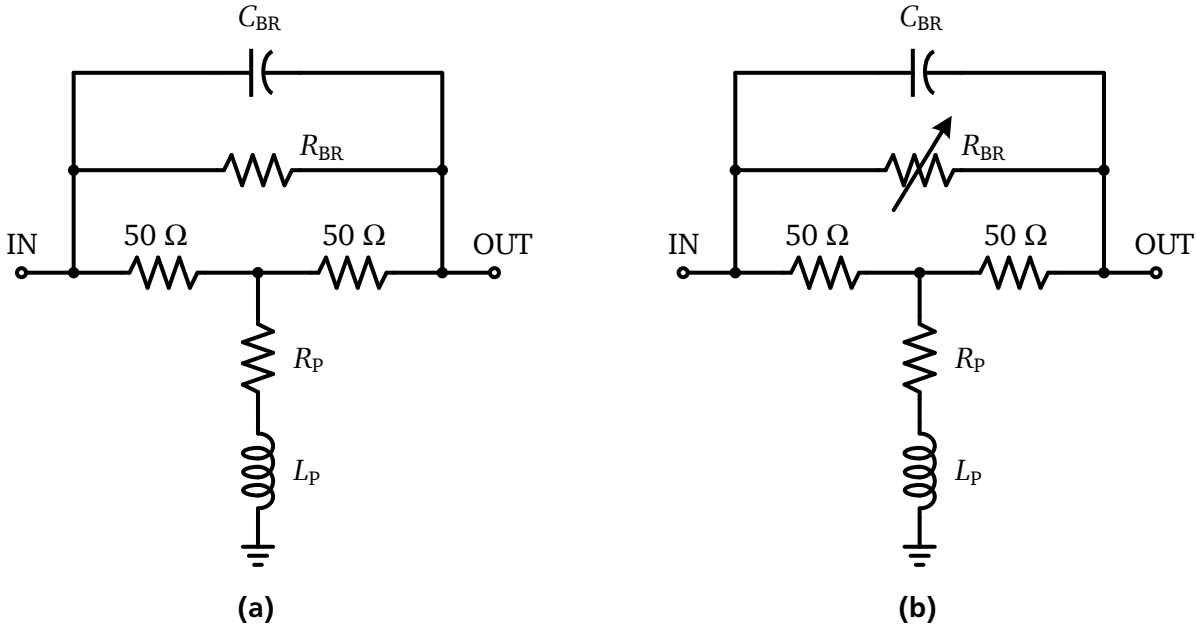


Figure 4.9: Model of a gain slope equalizer based on bridged-T attenuator network (a) with a fixed bridge resistor and (b) with a variable bridge resistor.

4.4.2.1 Capacitor in Parallel to Bridge Resistor R_{BR}

This section discusses the influence of adding a capacitor in parallel to bridge resistor R_{BR} on the response of the network. The schematic of the network with a capacitor C_{BR} added in parallel to R_{BR} is shown in Figure 4.10.

The addition of C_{BR} modifies the effective impedance Z_{BR} of the bridged path, as represented in Equation 4.9. The capacitor presents a high impedance path for low frequency signals. Hence, at low frequencies the resistor R_{BR} dominates the parallel connection of R_{BR} and $Z_{C,BR}$, where $Z_{C,BR}$ is the impedance due to the capacitor, given by Equation 4.10. As the frequency increases, the impedance of the C_{BR} decreases and the dominance of R_{BR} starts decreasing. Consequently, the effective parallel impedance Z_{BR} becomes more dependent on C_{BR} and the value of attenuation changes. This is illustrated in Figure 4.11, which shows the ideal gain response for different values of C_{BR} for $R_{BR} = 265.48\Omega$. It has to be noted that no degeneration inductance is used in this analysis.

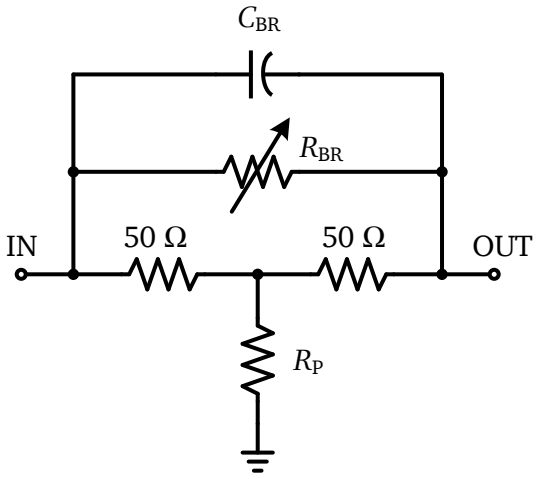


Figure 4.10: Model of a tunable gain slope equalizer based on bridged-T attenuator network having a bridge capacitor.

$$Z_{BR} = R_{BR} \,||\, Z_{C,BR} \tag{4.9}$$

where,

$$Z_{C,BR} = \frac{1}{sC_{BR}} \tag{4.10}$$

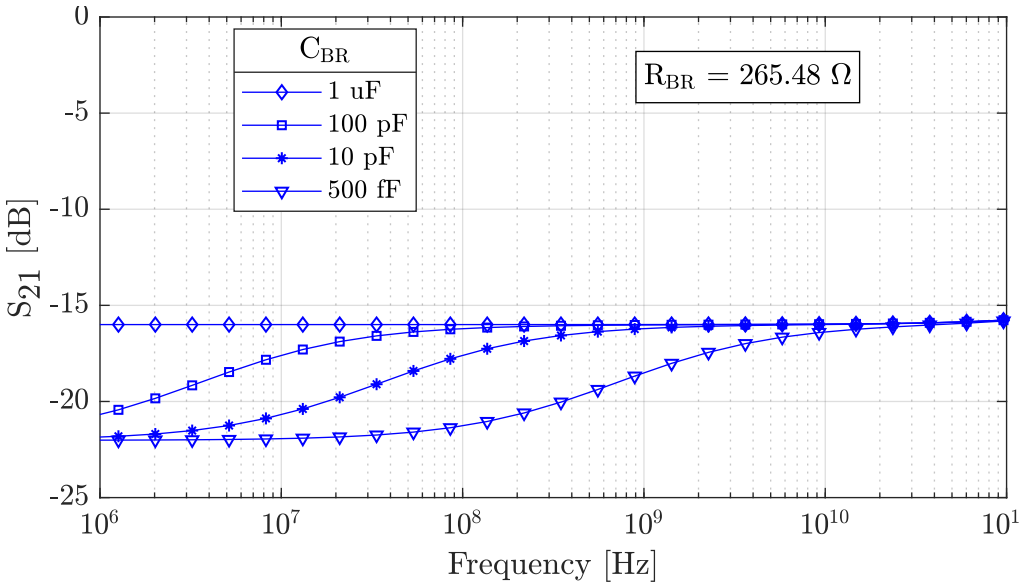
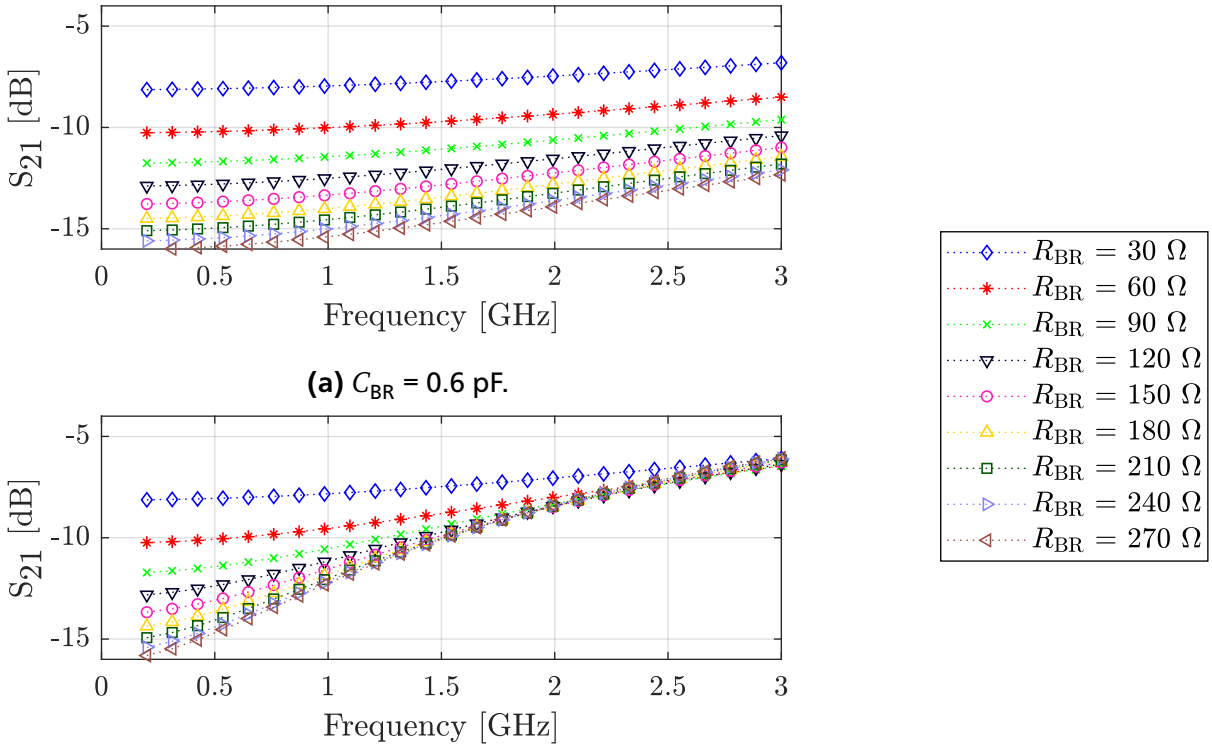


Figure 4.11: Influence of the value of bridge capacitor C_{BR} on the gain response of a bridged-T attenuator.

The schematic in Figure 4.9b is used to analyze the influence of C_{BR} in the presence of a finite degeneration inductor L_P. The value of L_P is maintained at 1.1 nH. The change in attenuation levels for different values of C_{BR} when R_{BR} is swept from 30 Ω to 270 Ω is plotted in Figure 4.12 for a frequency range of 200 MHz to 3 GHz. As illustrated in the figure, the slope of the attenuation curves vary as the value of C_{BR} changes. Figure 4.13 shows the slope variation with respect to R_{BR} value for four different values of C_{BR} when a wide bandwidth of 200 MHz to 3 GHz is considered. It can be observed that increasing the value of C_{BR} increases the range and maximum value of gain slope. The gain slope range does not vary significantly when the value of C_{BR} is increased beyond 1.0 pF. However, the maximum attainable value varies slightly.



(a) C_{BR} = 0.6 pF.

(b) C_{BR} = 1.2 pF.

Figure 4.12: Variation of forward transmission gain S_{21} with frequency for different values of bridge resistor R_{BR} and bridge capacitor C_{BR}. L_P = 1.1 nH.

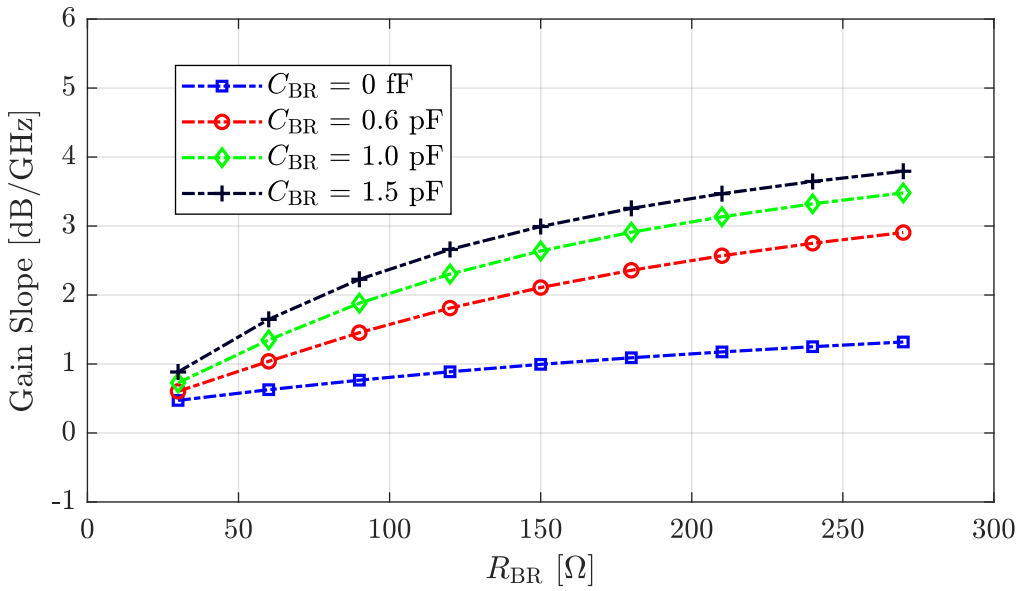
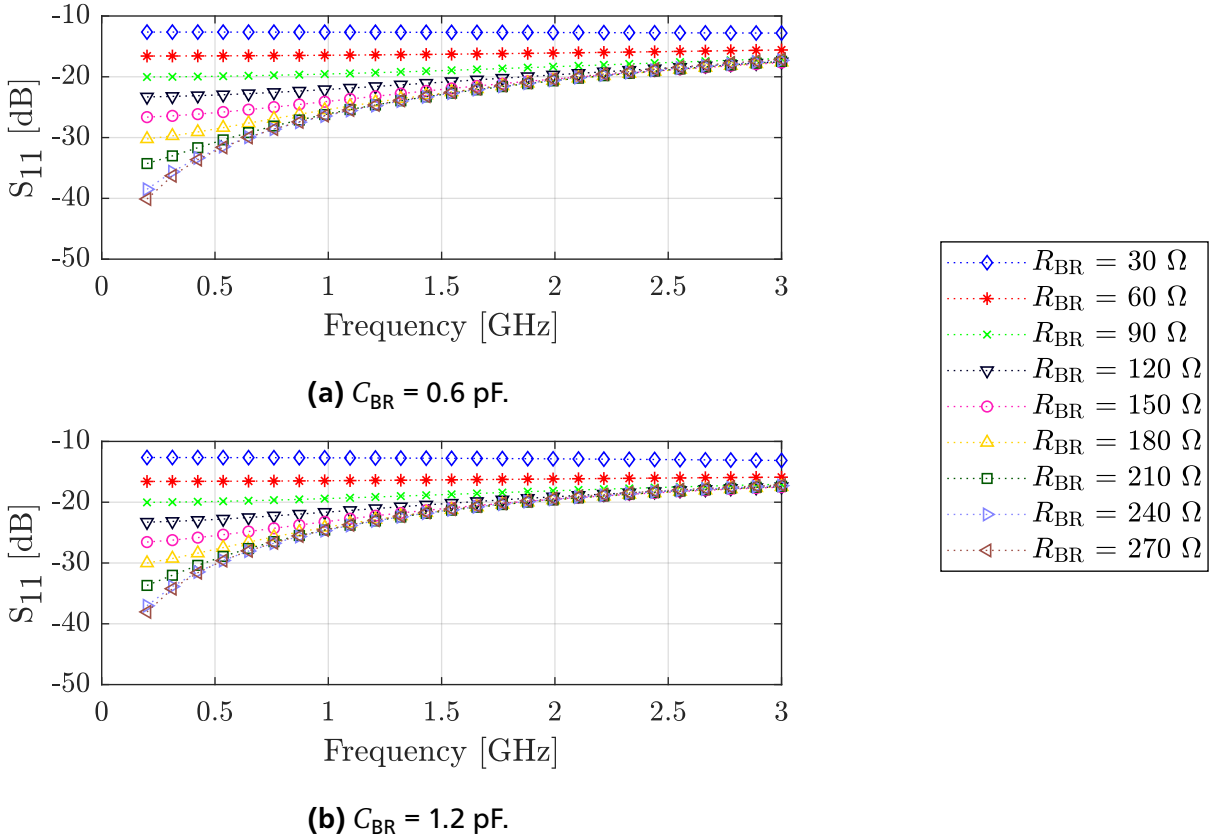


Figure 4.13: Variation of gain slope with value of bridge capacitor C_{BR}.

As the bridge parallel impedance Z_{BR} decreases, the impedance matching at the input (and output) of the bridged attenuator network to the characteristic source (and load) impedance of 50 Ω is modified. The resultant variation in the response of the input return loss is shown in Figure 4.14 for different values of C_{BR}. The plots show that the influence of the choice of C_{BR} on the return loss performance is minimal. Because of the symmetric nature of the circuit, the same behavior is true for the output return loss.



(a) C_{BR} = 0.6 pF.

(b) C_{BR} = 1.2 pF.

Figure 4.14: Input return loss S_{11} for different values of bridge resistor R_{BR} and bridge capacitor C_{BR}. L_P = 1.1 nH.

This section has illustrated that the addition of a capacitor C_{BR} in parallel to the variable bridge resistor R_{BR} helps in providing variable gain slope equalization. It can also be observed that increasing the value of C_{BR} effectively compresses the linear range of the gain slope characteristic to lower frequencies. Hence, the higher end of the bandwidth of interest plays an important role in the design of C_{BR}. In high bandwidth applications, a lower value of C_{BR} is desirable, whereas, in low bandwidth applications, a higher C_{BR} is preferable.

The gain slope range could be further increased by the addition of a degeneration inductor L_P in series with resistor R_P, which is explained in the following section.

4.4.2.2 Inductor in Series with Degeneration Resistor R_P

This section analyzes the influence of adding an inductor in series with R_P to the performance of the gain slope equalizer. The modified bridged-T attenuator network shown in Figure 4.15 is used for the initial analysis without the presence of a bridge capacitor.

The presence of inductor L_P modifies the impedance looking from the input and the output side of the network. The inductor provides a high-impedance path for high-frequency signals, and a low impedance path for low frequency signals. The addition of L_P modifies the impedance Z_P of the branch to ground as follows:

$$Z_P = R_P + Z_{L,P} \tag{4.11}$$

where,

$$Z_{L,P} = sL_P \tag{4.12}$$

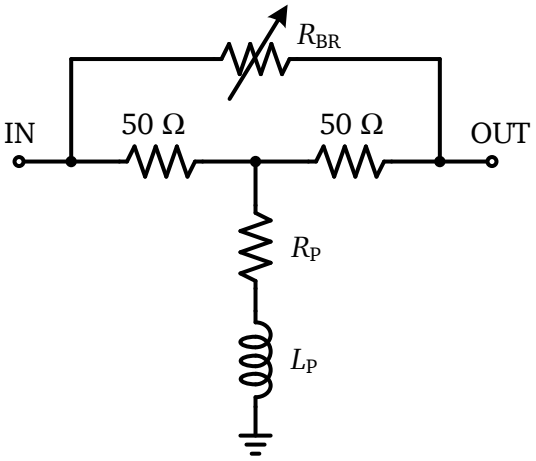


Figure 4.15: Model of gain slope equalizer based on bridged-T attenuator network with variable bridge resistor and degeneration inductor.

As a result, the s-parameter response of the network gets modified. Figure 4.16 shows the response of forward transmission characteristic for different values of L_P when $R_{BR} = 265.48\Omega$. As the value of L_P increases, the bandwidth in which the gain slope equalization is visible shifts to higher frequencies. L_P has to be designed based on the frequency range required for the application.

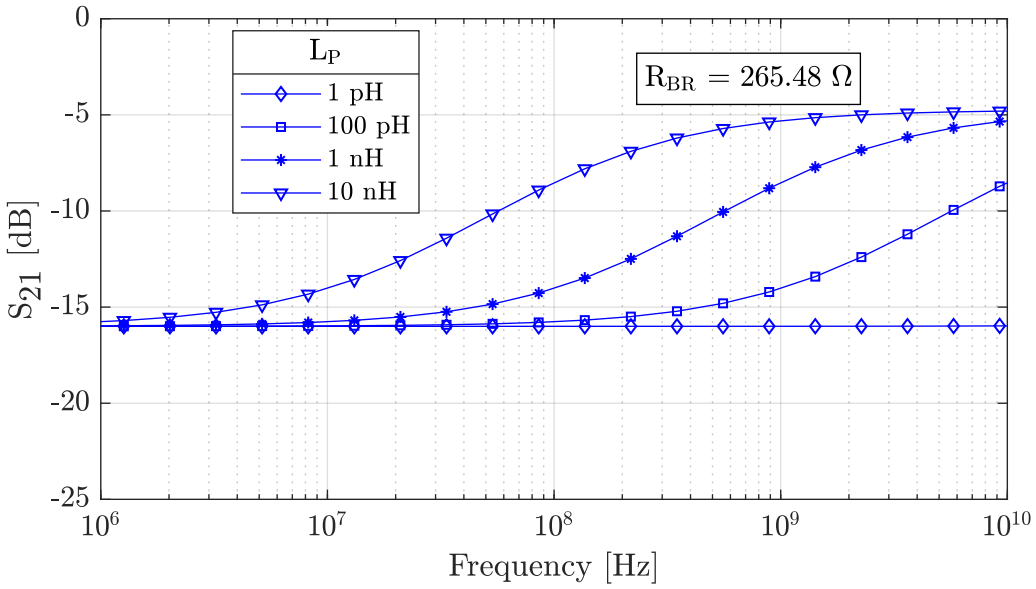
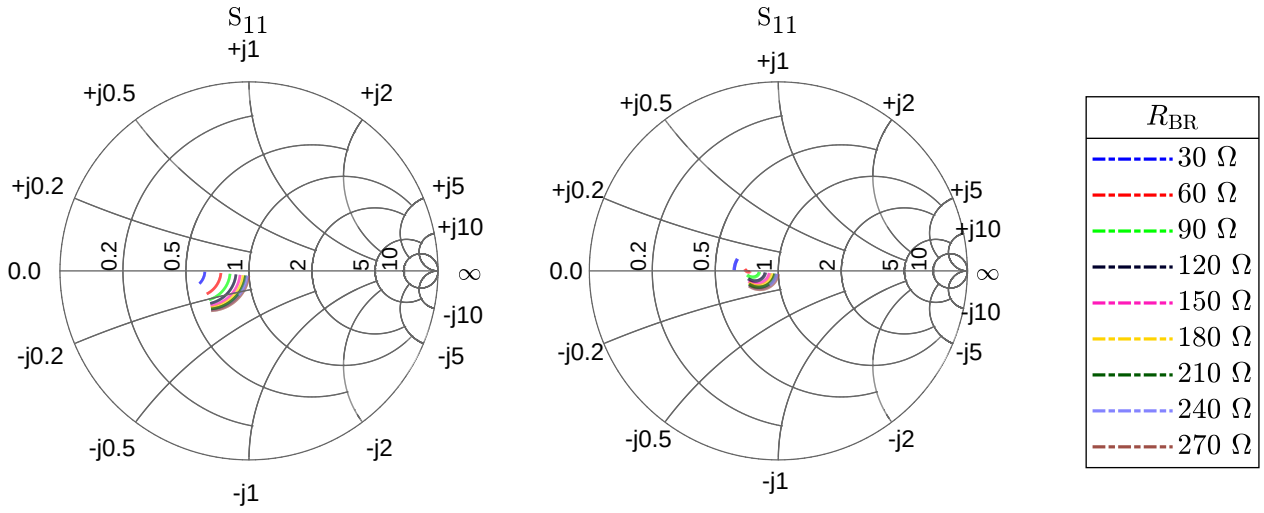


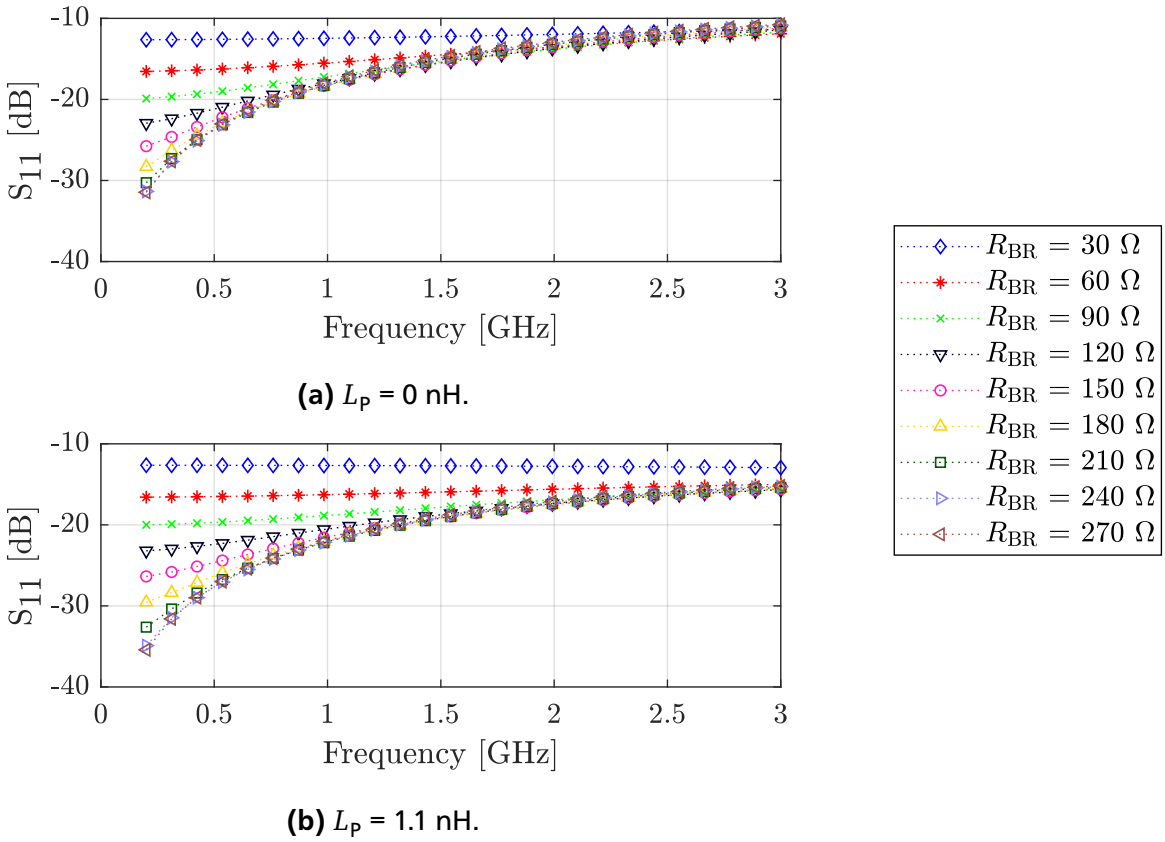
Figure 4.16: Influence of degeneration inductor on the gain response.

The effect of adding an inductor L_P in series with R_P is further illustrated by the smith-chart representation of the input reflection coefficient in Figure 4.17. The network consisting of bridge capacitor C_{BR} and degeneration inductor L_P, as shown in Figure 4.9b, is considered for this analysis. Compared to the input reflection coefficient plot for the circuit without L_P, the circuit with L_P illustrates a response that folds closer to 50 Ω. Figure 4.18 plots the input return loss in the decibel magnitude scale. It can be observed that the input return loss improved due to the addition of L_P. Because of the symmetric nature of the circuit, the same behavior is true for the output return loss.



(a) L_P = 0 nH. **(b)** L_P = 1.1 nH.

Figure 4.17: Smith chart representation of the input reflection coefficient for different values of bridge resistor R_{BR} and degeneration inductor L_P. A bandwidth of 200 MHz to 3 GHz is considered. C_{BR} = 1.2 pF.



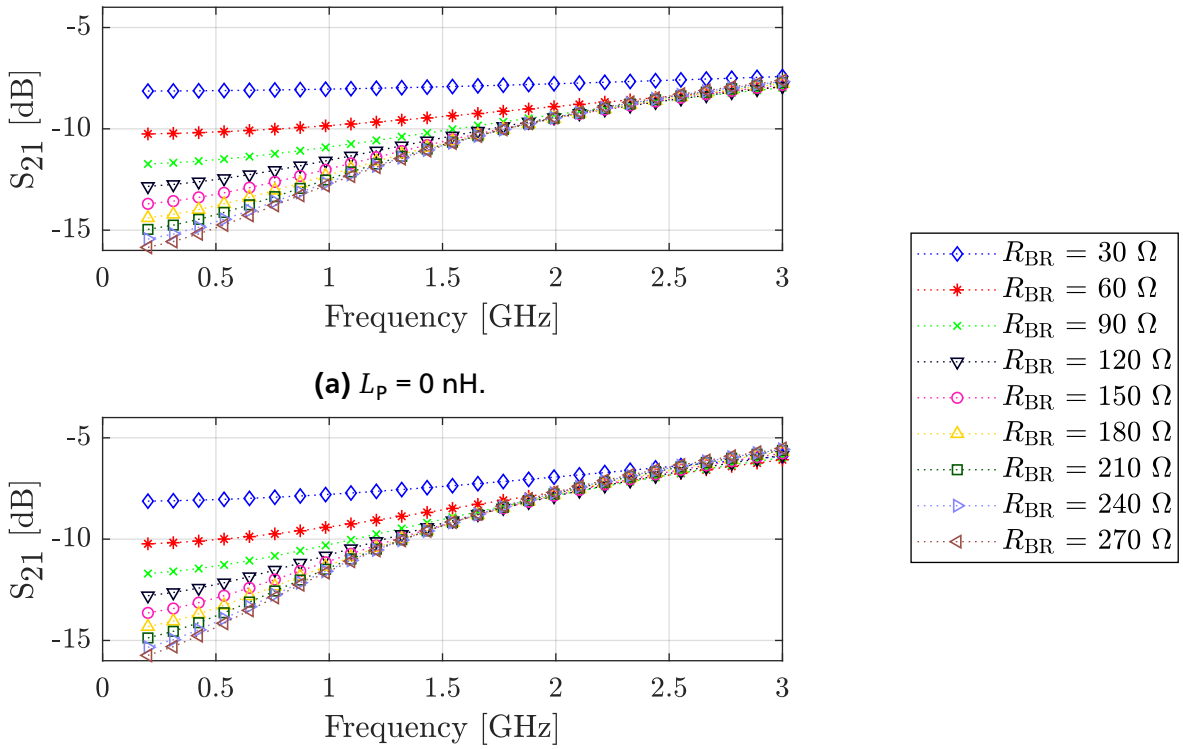
(a) L_P = 0 nH.

(b) L_P = 1.1 nH.

Figure 4.18: Input return loss for different values of bridge resistor R_{BR} and degeneration inductor L_P. C_{BR} = 1.2 pF.

Addition of L_P modifies the frequency profile of the attenuation of the equalizer circuit as illustrated in Figure 4.19. Compared to the case when L_P is zero, the attenuation decreases at higher frequencies when

the value of L_P is 1.1 nH. This helps in increasing the gain slope value. Figure 4.20 illustrates the gain slope variation with respect to R_{BR} values for four different values of L_P when a wide bandwidth of 200 MHz to 3 GHz is considered. Introduction of L_P helps in increasing the range and maximum value of gain slope for L_P values up to 1.1 nH. The range of gain slope attainable does not vary significantly when the value of L_P is increased beyond 1.1 nH. However, the maximum attainable value varies slightly.



(a) L_P = 0 nH.

(b) L_P = 1.1 nH.

Figure 4.19: Variation of forward transmission gain with frequency for different values of bridge resistor R_{BR} and degeneration inductor L_P. C_{BR} = 1.2 pF.

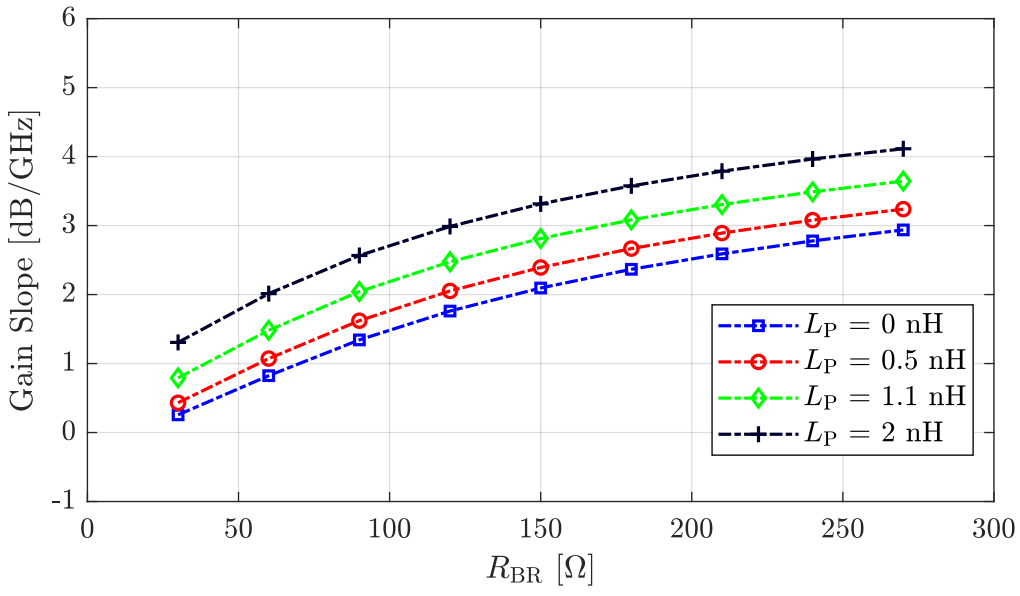


Figure 4.20: Variation of gain slope with degeneration inductor L_P.

Based on the above observations, it can be summarized that the frequency range, slope of the attenuation responses, range of gain slope values, insertion loss, and return loss performance of the network varies depending upon the chosen values of R_{BR}, C_{BR} and L_P. Here, the insertion loss is defined as the loss at the highest frequency of interest, assuming a positive slope response, where the absolute value of attenuation decreases with increasing frequency. When the gain slope equalizer is integrated into RF front end systems, it is preferable to keep the insertion loss as low as possible. A high value of insertion loss would increase the gain requirements from the amplifier circuits and thereby, also increase the power consumption and reduce the linearity of the system.

4.5 Digitally Controllable Gain Slope Equalizer (DCGSE)

The bridged-T attenuator circuit employing bridge resistor R_{BR}, bridge capacitor C_{BR}, and degeneration inductor L_P, presented in section 4.4 are utilized to design a novel gain slope equalizer employing digital controllability, the implementation of which is described in this section.

The digital controllability of the variable gain slope equalizer is incorporated by realizing the bridge resistor R_{BR} in Figure 4.9b using digital control. For this purpose, the total resistance required for the bridge resistor R_{BR} is realized using a series connection of four resistors. Each of these series resistors that contribute towards the bridge resistance is connected in parallel to a switch. Depending upon the state of the parallel switch that is connected to an individual resistor, the resistor will either be part of the bridge resistance or be bypassed. The schematic of a 4-bit digitally controllable version of the gain slope equalizer is presented in Figure 4.21.

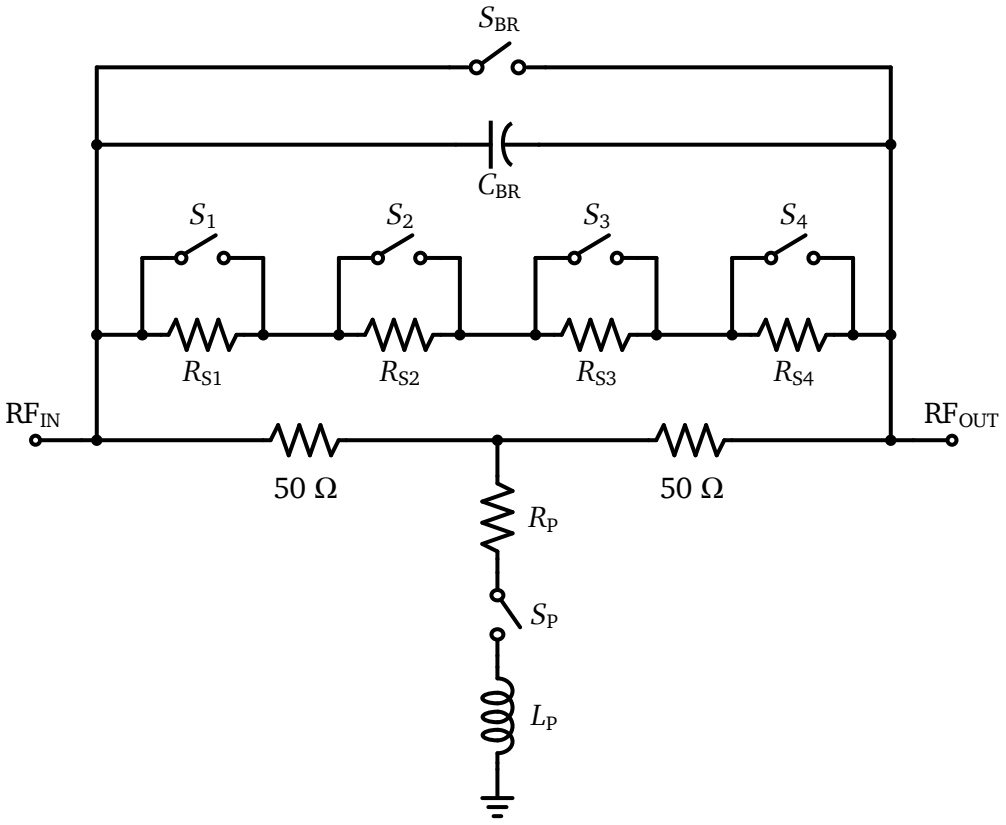


Figure 4.21: DCGSE circuit model.

Additional bypass/attenuate switches are added to the circuit to enable two different modes of operation, namely the bypass mode and the gain equalization mode. In the bypass mode of operation,

the switches S_{BR}, S_1, S_2, S_3, and S_4 are closed whereas the switch S_P is open. That is, the equalization is turned off and if the switches are ideal, the gain slope equalizer is completely bypassed and zero insertion loss is introduced in the overall system because of the presence of this circuit.

The switch S_{BR} is added to ensure that the on-resistance of the bridged path remains as low as possible during the bypass mode of operation. This helps in minimizing the insertion loss of the circuit when real switches are utilized. The control signals needed for the switches S_{BR} and S_P are generated from the 4 bit control signals used for the switches S_1 to S_4.

In the equalization mode of operation, the switch S_P is closed and S_{BR} is opened. The switches S_1, S_2, S_3, and S_4 are then controlled to set the required gain slope equalization for the circuit. Ideally, an open switch would act as an infinite resistance with zero reactance. Referring to Equation 4.7 and considering the switches to be ideal, the transfer function of the circuit is given by,

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_{BR}Z_P + 100Z_P + 2500}{Z_{BR}Z_P + 50R_{BR} + 100Z_P + 2500} \tag{4.13}$$

The terms Z_{BR} and Z_P in the transfer function of the circuit shown in Figure 4.21 can be represented as:

$$Z_{BR} = \frac{R_{EQ}}{1 + sR_{EQ}C_{BR}} \tag{4.14}$$

$$Z_P = R_P + sL_P \tag{4.15}$$

where,

$$R_{EQ} = S_{BR}\left(R_{S1}S_1 + R_{S2}S_2 + R_{S3}S_3 + R_{S4}S_4\right) \tag{4.16}$$

$$S_i = \begin{cases} 1 & \text{when switch i is closed} \\ 0 & \text{when switch i is open} \end{cases} \tag{4.17}$$

Equations 4.13 to 4.17 show that by controlling the switches that are connected in parallel to the resistors R_{S1} to R_{S4}, the equivalent resistance of the bridge resistor R_{EQ} in the bridged-T network can be varied. As the equivalent resistance varies, the gain slope of the network varies as described in sections 4.4.1 and 4.4.2. The resistors R_{S1} to R_{S4} have to be designed in such a way that, for different switching states, the circuit provides different gain slope and satisfies the required compensation range and resolution.

The overall schematic of the implemented digitally controllable gain slope equalizer (DCGSE) is illustrated in Figure 4.22. The switches in the gain slope equalizer are implemented using NMOS transistors as shown in Figure 4.23. These transistors are realized as triple well devices to make the body terminal independent and available for biasing. Large resistors are connected to the isolated body terminal and the gate terminal to increase their isolation. The high impedance seen by the RF signal improves the insertion loss performance at high frequencies, the power handling capability of the transistors, as well as the linearity of the equalizer [11, 47].

Inductors are added at the input and output nodes to improve the return loss performance of the circuit. The inductors compensate for the capacitance introduced by the large switches connected to the input and output of the bridged-T network. The inductance L_P is realized using the bond-wire ground connection. Hence, the need for integrating an additional on-chip inductor is avoided and the area occupied by the circuit is minimized.

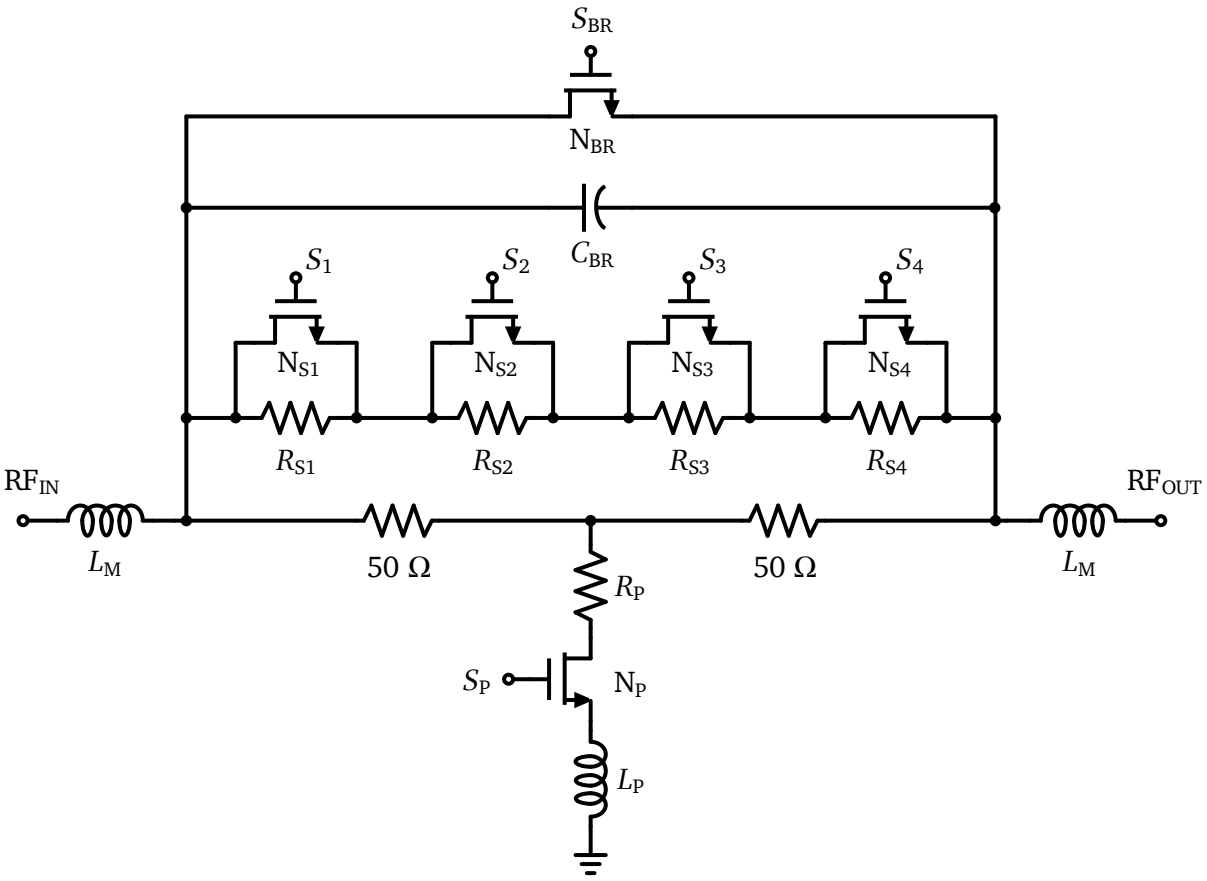


Figure 4.22: Schematic of the implemented DCGSE. The high resistive connections at the gate and base terminals of the NMOS switches are not shown here.

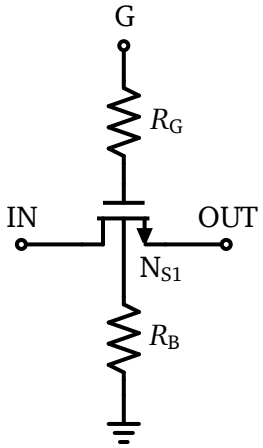


Figure 4.23: NMOS switch with high resistive connections at the gate and base terminals.

4.6 Implementation Results

The DCGSE is realized using a SiGe BiCMOS technology, corresponding to the requirements of the RF front-end in which it is employed. Unsalicided p-doped gate polysilicon resistors, metal insulator metal (MIM) capacitors, octagonal shielded inductors with thick top metal layers, and 3.3 V CMOS transistors available in the technology are utilized for the circuit implementation.

A patterned ground shield is added in the Metal 1 layer below the inductor to provide good isolation from substrate coupling effects. Bond-wires, pads and package leads are modeled using commercially available EM simulation tools to study their influence on the circuit performance.

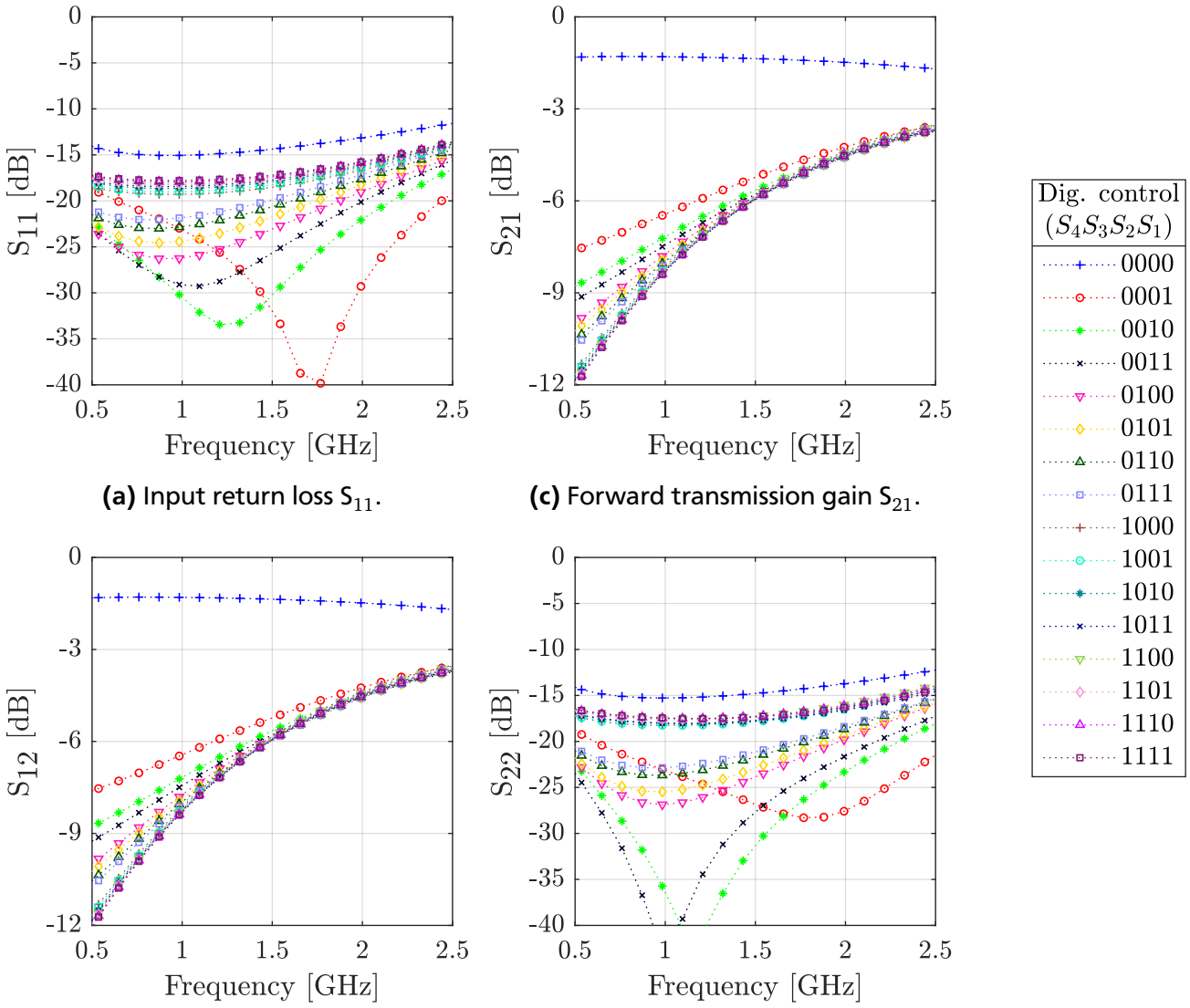
Due to the passive nature of the circuit, the modified bridged-T based DCGSE has a low power consumption of 3.78 μW. The circuit is optimized for a frequency range of 500 MHz to 2.5 GHz as per the requirements of the RF transceiver front-end system in which it is employed. Parasitic-extracted post-layout simulation results of the s-parameters of the DCGSE for different control settings are illustrated in Figure 4.24.

In the bypass mode of operation, the insertion loss is less than 1.69 dB, and in the equalization mode, the gain slope varies from 2.03 dB/GHz to 4.18 dB/GHz for a frequency range of 500 MHz to 2.5 GHz, and 2.09 dB/GHz to 4.8 dB/GHz for a frequency range of 200 MHz to 2.5 GHz. A return loss greater than 12 dB is achieved across the operating bandwidth both at the input and output ports when considering 50 Ω terminations. The results for the gain slope and input 3rd order intercept point (IIP3) values for the circuit at different digital control settings are tabulated in Table 4.2.

The circuit has an IIP3, calculated using two-tone measurements at 1.5 GHz and 1.51 GHz, larger than 36.83 dBm across all gain slope settings. The compression point results of the DCGSE for the bypass and full equalization modes are plotted in Figure 4.25 and Figure 4.26, respectively. The circuit occupies 0.429 mm^2 in silicon area. A performance comparison of the proposed gain slope equalizer circuit with other state-of-the-art gain slope equalizers is provided in Table 4.3. The proposed equalizer provides the required digital control with low power and area overhead, and achieves high linearity and return loss performance. The low area requirement makes the implementation attractive for silicon based RFIC implementations.

Table 4.2: Gain slope equalization and input intercept point values of the DCGSE for different digital settings.

S_4	S_3	S_2	S_1	Gain Slope 0.5 to 2.5 GHz [dB/GHz]	Gain Slope 0.2 to 2.5 GHz [dB/GHz]	IIP3 [dBm]
0	0	0	0	0.20	0.17	36.83
0	0	0	1	2.03	2.09	39.19
0	0	1	0	2.55	2.61	39.06
0	0	1	1	2.76	2.83	38.73
0	1	0	0	3.17	3.30	39.49
0	1	0	1	3.27	3.43	39.16
0	1	1	0	3.44	3.63	39.05
0	1	1	1	3.51	3.74	38.81
1	0	0	0	4.04	4.52	40.11
1	0	0	1	4.03	4.53	39.92
1	0	1	0	4.08	4.61	39.84
1	0	1	1	4.07	4.62	39.7
1	1	0	0	4.17	4.75	39.73
1	1	0	1	4.17	4.75	39.59
1	1	1	0	4.18	4.80	39.56
1	1	1	1	4.18	4.80	39.44



(a) Input return loss S_{11}.

(c) Forward transmission gain S_{21}.

(b) Reverse transmission gain S_{12}.

(d) Output return loss S_{22}.

Figure 4.24: Parasitic-extracted post-layout s-parameter simulation results of the DCGSE.

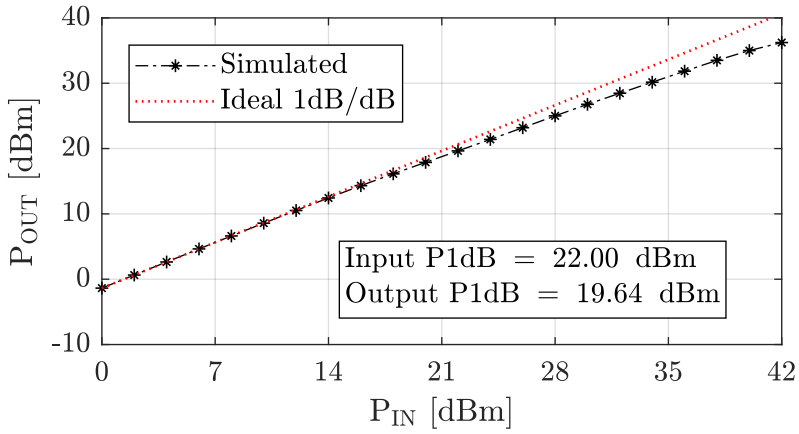


Figure 4.25: Simulated 1dB compression point of the DCGSE at 1.5 GHz for bypass mode.

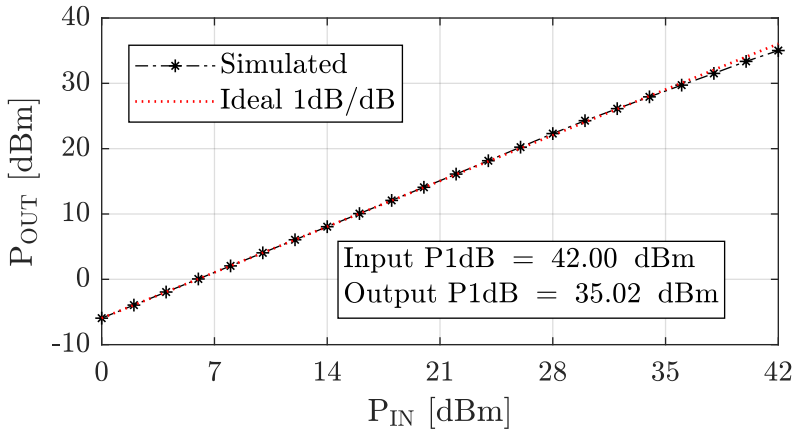


Figure 4.26: Simulated 1dB compression point of the DCGSE at 1.5 GHz for maximum equalization mode.

Table 4.3: Performance comparison of the DCGSE with other state-of-the-art gain slope equalizers [114]

	Technology	DC Power [mW]	Supply [V]	Operating Freq. [GHz]	Linearity (IIP3/IP1dB) [dBm]	S_{11} [dB]	S_{22} [dB]	Gain Slope [dB/GHz]	Area [mm^2]
This Work	**SiGe BiCMOS**	**0.003**	**3.3**	**0.5 - 2.5**	**$36.83^{1}/22^{1}$; $39.44^{2}/42^{2}$ (at 1.5 GHz)**	**≤ -12**	**≤ -12**	**2.03 to 4.18**	**0.429 (core)**
TCAS II 2019 [45]	SiGe BiCMOS	n.a.	n.a.	8 - 12.5	n.r.	≤ -10	≤ -10	1	0.31 (die)
TCAS II 2019 [46]	SiGe BiCMOS	46	3.3	8 - 12	n.r./-1.5	≤ -14^{+}	≤ -7^{+}	1.13	1.07 (die)
APMC 2018 [48]	SiGe HBT + Varactor Diode	n.r.	2	0.1 - 0.8	n.r.	n.r.	n.r.	-6.7 to +13.2	n.a.
J. Sensors 2016 [38]	Coplanar waveguide + MEMS	n.a.	n.a.	17 - 19	n.r.	≤ -16	≤ -16	1.75 to 2.5^{+}	n.a.
IMaRC 2014 [49]	Broadside coupled lines	n.a.	n.a.	1 - 18	n.r.	≤ -9.6	≤ -9.6	0.35	n.a.
MWCL 2011 [37]	P-I-N diodes	n.a.	5	3 - 5	n.r.	≤ -15	≤ -15	-4 to +4	n.a.
IMS 2007 [35]	MMIC	n.a.	n.a.	2 - 4	n.r.	n.r.	n.r.	-8.5 to 8	n.r.
APMC 2007 [41]	Micro-strip line	n.a.	n.a.	2 - 18	n.r.	≤ -10	≤ -10	0.625	n.a.

n.a. Not available/applicable [1] Bypass mode [2] Max gain slope mode [+] Calculated from graph

4.7 Summary

This chapter presented the principle, design and implementation of a novel digitally controllable gain slope equalizer circuit intended for integration within area constrained RF front-ends in system-on-chip applications.

The equalizer utilizes a modified switched bridged-T network architecture. The bridge resistor in the bridged-T network is digitally controlled to set its effective resistance and thereby vary the attenuation level. The frequency dependent attenuation characteristic required for gain slope equalization is provided by the addition of a capacitor in parallel to the bridge resistor and a degeneration inductor, realized using a bond-wire connection, in the path to ground. The combination of the variable attenuation and the frequency dependent characteristic result in a variable gain slope equalization range for the circuit. Based on parasitic-extracted post-layout simulation results, the equalizer achieves a gain slope range tuning range of 2.03 dB/GHz to 4.18 dB/GHz within the bandwidth of interest of 500 MHz to 2.5 GHz, and the input and output return loss are larger than 12 dB.

The presented gain slope equalizer is the first of its kind digitally controllable gain slope equalizer that is suitable for integration in high-frequency and high-power RF system-on-chip applications realizable on silicon. The proposed equalizer achieves the digital controllability at the expense of low power and silicon area, and provides high linearity and good return loss performance. These features make the implementation attractive for integration as part of RF front-ends in silicon based SoC RFIC implementations.

5 Design of Wideband Large Dynamic Range RF Power Detectors for High Sensitivity

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This chapter focuses on the sensitivity-aware design and implementation of wideband large dynamic range peak power detectors suitable for SoC integration as part of RF transceiver front-ends. Particular focus is applied in evaluating the effect of two frequently used offset cancellation approaches on the performance of the detector. Noise contributions from individual sub-circuits of the detector are characterized to understand their effect on the sensitivity of the detector. Thereafter, a high sensitivity large dynamic range wideband logarithmic power detector is prototyped and measurement results are presented. Parts of this chapter have been published as research papers in [112, 116].

5.1 Introduction

Power detectors are one of the most commonly used building blocks in RF transceivers and are employed to measure the power of the received signal at the receiver side or the power of the transmitted signal at the transmitter side. Monitoring the power of the transmitted and received signal is vital due to a multitude of reasons. At the transmission side, power detection assists not only in monitoring the transmitted power but also in adaptively controlling it. In applications where there are strict regulations

in place with regards to the power that is transmitted at a particular frequency, a power detector plays a crucial role as a facilitating circuit that aids in satisfying the regulations. In such applications, a power detector can be used to identify an aberration and initiate adaptive control when the transmitted power exceeds a particular threshold. Furthermore, power monitoring and feedback loop based adaptive control can be utilized to maintain the operating point of a power amplifier near its desirable bias conditions and to avoid breakdown mechanisms. Important power amplifier performance parameters like linearity and output power can be thereby regulated.

At the receiver end, power detectors act as enabling circuits for automatic gain control. The dynamic range at the input of the system can be controlled by employing VGAs or digital step attenuators to implement the gain control. By operating the sub-circuits at close to their optimal bias conditions, the overall power consumption and linearity of the RF front-end IC can be managed. The block diagram of a transceiver system with adaptive control is shown in Figure 5.1. The output from the transceiver is coupled through power couplers and fed to the power detector for detection. The detector output is then converted to digital bits to control the attenuation level of the attenuators in the transceiver. This feedback mechanism helps in regulating the output power and the gain of the system.

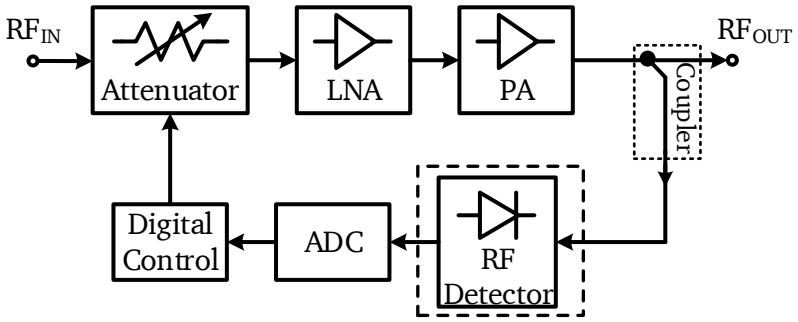


Figure 5.1: Block diagram of an RF transceiver system utilizing a power detector for digital power control.

5.1.1 Losses Associated with Power Couplers

In many RFIC implementations, power coupling is implemented using lossy couplers as area requirements of the low-loss power coupling alternatives are excessive. Lossy power couplers lower the level of the power that needs to be detected. The minimum power that needs to be detected, is thereby reduced. This poses a challenge on the specification of the minimum detectable power of the detector, also known as its sensitivity. A high sensitivity, or in other words a low minimum detectable power, is needed for the detector.

A sense amplifier is added to negate the losses associated with the power coupler if the sensitivity of the detector is not high enough to meet the system requirements. The block diagram of a system utilizing sense amplifiers to compensate for coupling losses is shown in Figure 5.2. The sense amplifier needs to have a high saturated output power and high linearity and requires high power for its realization. The sense amplifier will consume a significant portion of the power budget of the transceiver IC, making its addition undesirable. One way to operate the system without utilizing a sense amplifier would be to improve the sensitivity and the dynamic range of the power detector such that the whole range of the output power from the lossy power coupler is detectable. The block diagram of such a system is illustrated in Figure 5.3.

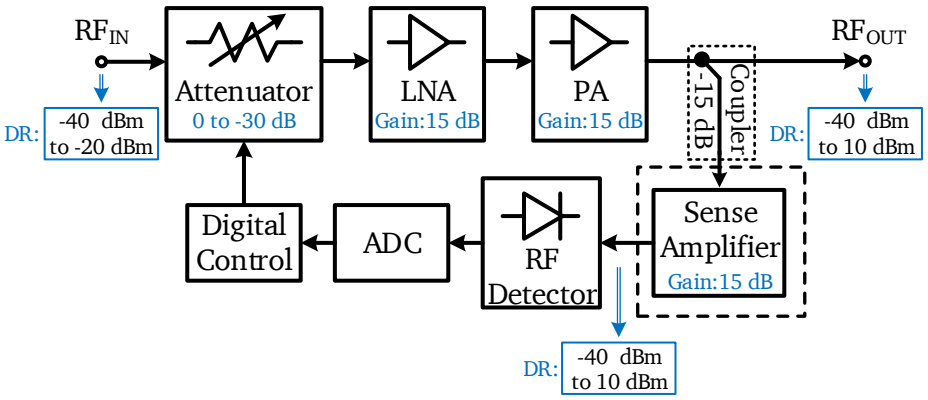


Figure 5.2: A large dynamic range RF front-end system with a sense amplifier in the power control loop. DR denotes the dynamic range of power at a particular node.

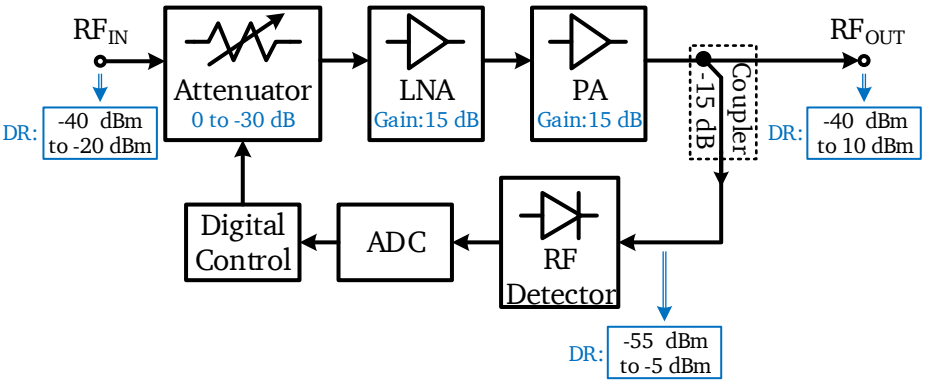


Figure 5.3: A large dynamic range RF front-end system without a sense amplifier in the power control loop. DR denotes the dynamic range of power at a particular node.

Large dynamic range wideband power detectors have been a major area of focus in recent times. The desire to have a high sensitivity along with the large dynamic range poses challenges in such wideband power detector realizations. This chapter focuses on the challenges in designing a wideband power detector for high sensitivity and large dynamic range. The bandwidth considered for the power detector is from 500 MHz to 2.5 GHz, corresponding to the operating bandwidth of the transceiver IC considered in this work.

The chapter is structured as follows: section 5.2 reviews the commonly used power detector architectures and their suitability for high sensitivity large dynamic range wideband applications. Section 5.3 reviews the design considerations of the successive detection logarithmic amplifier power detectors. Section 5.4 investigates the influence of offset cancellation and noise on the achievable sensitivity of successive detection logarithmic amplifiers. Section 5.5 presents the design and the measurement results of a high sensitivity large dynamic range wideband power detector providing state-of-the-art performance. Section 5.6 concludes the chapter.

5.2 Power Detector: State of the Art

Different approaches have been presented for the design of power detectors in the published literature. In this section, a short overview of these approaches is provided, and the approaches that are most suitable for large dynamic range high sensitivity wideband power detection with moderate area and power consumption are investigated.

5.2.1 RMS Detectors vs Peak Detectors

Power detectors can be classified into two types based on the signal characteristic being detected - root-mean square (RMS) power detectors and peak power detectors.

RMS detectors produce an output that is proportional to the RMS, i.e., the average value of the instantaneous magnitude, of the input signal. They are also called true detectors and are preferred when the input is a dynamic signal having varying amplitude and high peak-to-average power ratio (PAPR). Peak detectors, on the other hand, produce an output that is proportional to the peak value of the input signal. These detectors are preferable for constant envelope or low peak to average power ratio applications.

This work focuses on the detection of signals having a low peak to average power ratio. Hence, only peak detectors are considered here.

5.2.2 Types of Power Detectors

Based on the principle applied for detection, power detectors can be classified as thermal detectors, diode detectors, Bipolar or MOS transistor device characteristic based detectors, translinear detectors, and logarithmic detectors. The following subsections provide a summary of these detection techniques.

5.2.2.1 Thermal or Joule Heating Based RMS Power Detectors

Thermal power detectors use thermal power or Joule heating principle for RMS detection [50–52]. The input power is converted to thermal power with the help of resistive components. The generated thermal power is compared to the heating power generated by a known reference input to obtain the measure of the unknown input signal. Thermal power detectors achieve wide bandwidth and provide good accuracy along with low error. However, the realization of such detectors is tricky, and they require complex packaging, which increases the costs of realization.

5.2.2.2 Diode Power Detectors

Diode based power detection is one of the most straightforward approaches to power detector implementation. Schottky diodes or PIN diodes or PN junction diodes are frequently used in this approach. PN junction diode based detectors utilize the square-law characteristic of a diode in the small-signal region for power detection. These detectors are cheaper and are suitable for high-frequency applications. However, the diode characteristic is temperature dependent, and compensation techniques need to be implemented to overcome this limitation. Moreover, the dynamic range achievable is also limited [50, 53]. The need for large signal levels to overcome the uncertainties in the determination of diode turn-on performance, the high power consumption during high-frequency operation, and the dependence of the precision of the detector on high-freq gain variations limit the applicability of diode detectors [54]. For RF implementations, a Schottky diode is preferred considering their low-loss characteristic. However, Schottky diodes are widely available in modern integration processes. Additionally, CMOS realizations of Schottky diode are prone to the presence of parasitic capacitances, which limit their applicability [51, 55–57]. An example implementation of Schottky diode for power detection can be found in reference [58]. An alternative to using Schottky diodes would be to use Bipolar or MOS transistors and utilize their small-signal characteristics. This approach is introduced in the following subsection.

5.2.2.3 Bipolar/MOS Transistor Device Characteristic Based Power Detectors

These detectors provide power detection based on the device characteristic of Bipolar and MOS transistors. An example realization based on bipolar transistors can be found in reference [54], whereas approaches

based on the MOS transistor either utilizing the characteristic behavior in the strong inversion region or the weak inversion region or the ohmic region have been presented in [51, 56, 59, 60].

5.2.2.4 Translinear Power Detectors

Translinear detectors utilize the translinear principle for RMS power detection. In most cases, they use voltage-to-current conversion followed by a squarer circuit and a low pass filter to produce a DC output voltage, which is proportional to the RMS power of the input. Bipolar based implementations [50, 61] as well as MOS transistor based implementations [62] are available in the literature. In bipolar implementations, the translinear principle is based on the exponential law describing the bipolar transistors large-signal behavior. For MOS transistor based translinear principle implementation, the exponential characteristic of a MOS transistor operating in the weak inversion region is employed. The disadvantage of translinear principle based RMS detection is the limited bandwidth achievable, the limited bandwidth of the voltage-to-current converter being the dominant factor.

5.2.2.5 Successive Detection Logarithmic Amplifiers (SDLA)

Logarthmic amplfier based detectors are the most commonly used integrated RF signal power detectors. They achieve a large dynamic range compared to other types of detectors and show a linear-in-dB response, two important features that are desirable in many RF applications.

A commonly adopted approach uses a logarithmic amplifier in a successive detection architecture. The linear-in-dB function is realized by using equally weighted taps from a cascade of limiting gain stages. The tap voltages are converted into current, and in some cases, demodulated by using rectifiers realized as detector cells. The output currents from these rectifier cells are summed together and low pass filtered to produce a DC output voltage that is proportional to the input amplitude (in dB scale). The dynamic range of the detector is determined by the number of cascading limiting gain stages and the gain of each stage. The bandwidth of the cascaded configuration of the limiting gain stages restricts the range of operating frequencies of the detectors that are implemented based on the successive detection architecture. The limiting gain stages have to be designed to provide high bandwidth and high gain at the same time, posing is a significant design challenge. As a result, most implementations include low gain high bandwidth solutions.

CMOS based as well as bipolar transistor based realizations of such power detectors are available in the published literature [63, 64]. CMOS logarithmic detector designs have the advantage of low cost and high integration level. However, they cannot achieve the same performance that the bipolar implementations provide.

The large dynamic range and high sensitivity requirements of the power detector that is considered in this work makes the logarithmic amplifier detection approach the most suitable option.

5.2.2.6 Other Power Detector Architectures

In recent years, other architectural solutions have been presented for power detection. Reference [53] describes one such approach based on the Meyer detector [54], whereas, a transformer based RMS power detection approach is presented in [65]. A linear-in-dB power detector that uses a mixer to down-convert the RF signal to lower frequencies before using the successive detection logarithmic amplifier principle is presented in [55].

5.3 Design of Successive Detection Logarithmic Amplifier based Power Detectors

In the previous section, it has been shown that a successive detection based logarithmic power detector is the most suitable type of detector for the detection of peak power in a wideband high sensitivity

large dynamic range application. This section introduces the architecture of a successive approximation logarithmic power detector and describes its working principle. The design considerations are analyzed with an emphasis on maximizing the dynamic range and sensitivity.

5.3.1 Successive Detection Logarithmic Amplifier: Working Principle

A successive detection logarithmic amplifier (SDLA) power detector works based on the principle of successive approximation and piece-wise logarithmic summation [66–68]. When a certain number of limiting gain cells are connected in cascade, and the outputs from each of the gain cells in the cascaded network are summed together, the resulting output voltage has a piece-wise logarithmic characteristic. When implemented on the circuit level, rectifying transconductors are typically used to convert the outputs from the gain cells to current, and a low-pass filter is added at the output to reduce the alternating current (AC) ripples in the output. A resistor within the low-pass filter acts as the summing node for the output currents from the rectifiers. Figure 5.4 depicts the architecture of such a power detector. For high-frequency applications, an additional network will be added at the input to achieve the required impedance matching.

The cascaded arrangement of limiting gain stages is frequently referred to as a logarithmic amplifier due to its piece-wise logarithmic behavior. This nomenclature will be followed in the rest of this work. A power detector utilizing logarithmic amplifiers for power detection will be denoted as an SDLA power detector, a limiting gain stage will also be simply referred to as a gain cell, and a rectifying transconductor will be referred to as rectifier for simplicity. The input power will be expressed in dBm scale. The expression to convert input RMS voltage to input power for 50 Ω termination is given in Equation 5.1.

The limiting gain stages that are connected in cascade are equally weighted. For low input signals, a limiting gain stage acts as a simple amplifier of gain A_S. As the input signal amplitude increases beyond a specific limiting voltage, namely its knee voltage $V_{KNEE,A}$, the output saturates. Any further increase in the input voltage does not influence the output as it remains saturated. If the input signal to the cascaded gain cells is small enough, it will be amplified by all the gain cells. As the amplitude of the input signal increases, at a certain point, the last stage of the cascade starts limiting, and the overall amplification seen by the input signal reduces. As the input signal increases further, the stages that are farther away from the source start limiting one after the other. The limiting gain stage that is closest to the input source limits at the end, at which point the output stops responding to an increase in input amplitude.

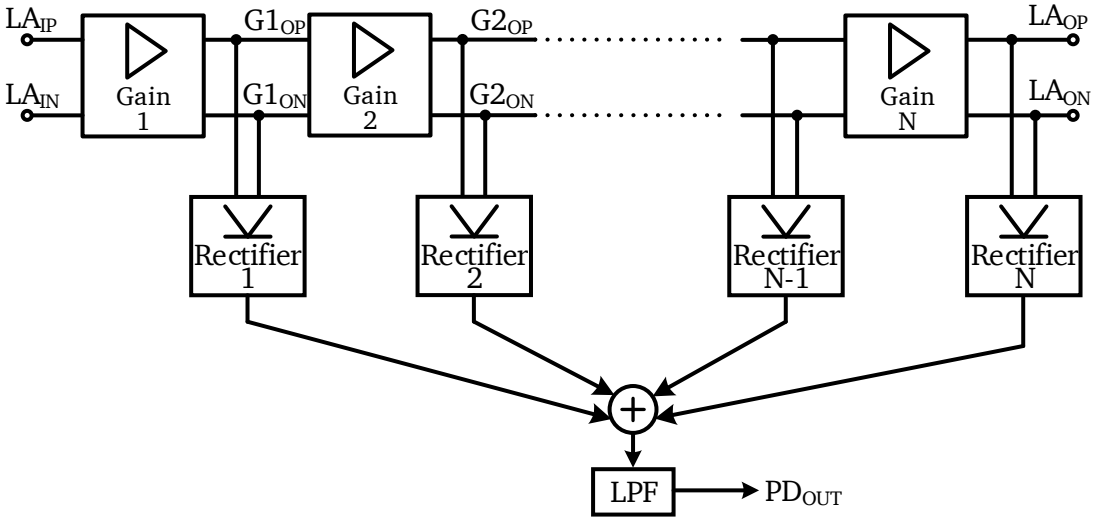


Figure 5.4: Architecture of a successive detection logarithmic amplifier based power detector.

$$P_{\mathrm{dBm}} = 20 \cdot \log_{10}(V_{\mathrm{RMS}}) + 13 \tag{5.1}$$

The phenomenon described above implies that the higher amplitude input signals are amplified by fewer gain cells, whereas the lower amplitude input signals are amplified by more number of stages. This characteristic results in a large input signal range being compressed to a small output voltage range, and the system shows a piece-wise logarithmic behavior. An illustration of the piece-wise logarithmic response of an SDLA utilizing gain cells with hard-limiting behavior is provided in Figure 5.5. Hard-limiting gain stages have the characteristic given by Equation 5.2. MOS or bipolar transistor based gain cells have a more softer limiting behavior as reported by Koli et. al. in [66] and Holdenried et. al. in [69].

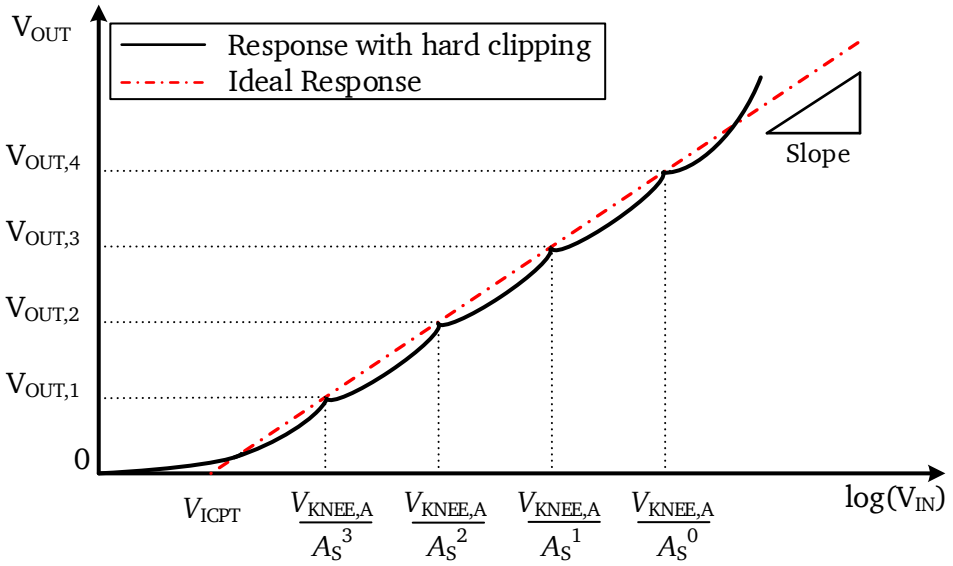


Figure 5.5: Piece-wise summation and linear-in-dB characteristic of a four-stage logarithmic amplifier with hard-limiting characteristic.

$$\mathrm{Gain} = \begin{cases} A_S & \text{when } V_{\mathrm{IN}} \leq V_{\mathrm{KNEE,A}} \\ 0 & \text{when } V_{\mathrm{IN}} > V_{\mathrm{KNEE,A}} \end{cases} \tag{5.2}$$

The input of the logarithmic amplifier can be added to the summation circuitry to extend the top-end dynamic range of the logarithmic amplifier. Figure 5.6 shows the block diagram of a four-stage logarithmic amplifier, and Figure 5.7 illustrates the effect that adding the rectified version of input to the summation node has on the dynamic range of this logarithmic amplifier. The input is expressed in terms of power in the figure, considering a 50 Ω input termination. Figure 5.8 shows a power detector utilizing a top-end dynamic range extension rectifier and a four-stage logarithmic amplifier. Impedance matching to 50 Ω is achieved through an input matching network.

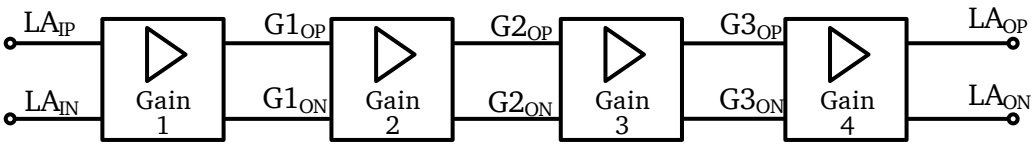


Figure 5.6: Block diagram of a four-stage logarithmic amplifier. The gain cells represent limiting amplifier stages.

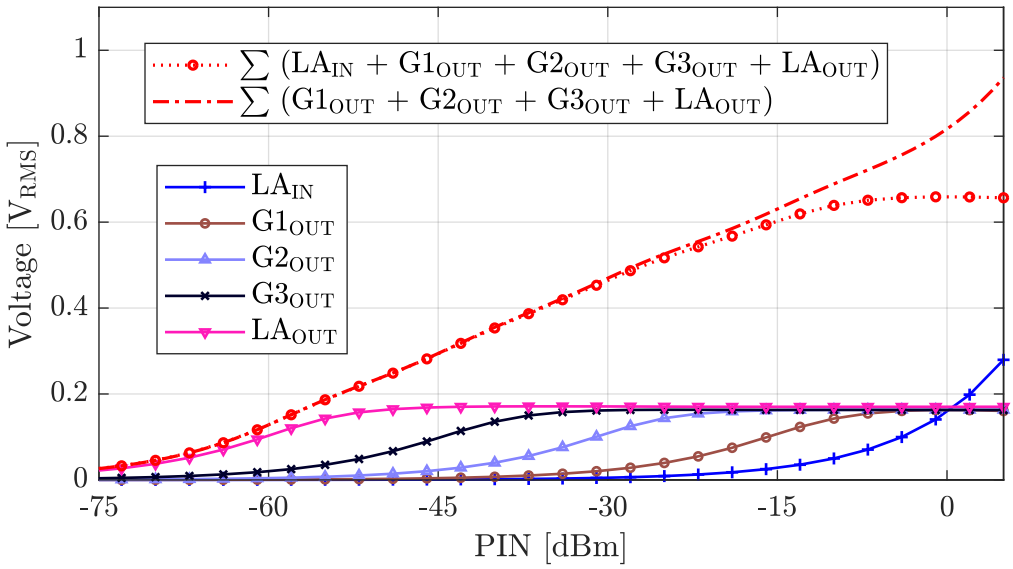


Figure 5.7: Piece-wise summation and linear-in-dB characteristic of the four-stage logarithmic amplifier shown in Figure 5.6 when soft-limiting gain cells are used. Each gain cell has a gain A_S of 14.75 dB and an input-referred limiting voltage $V_{KNEE,A}$ of 40.86 mV_P. Differential voltages are used for summation.

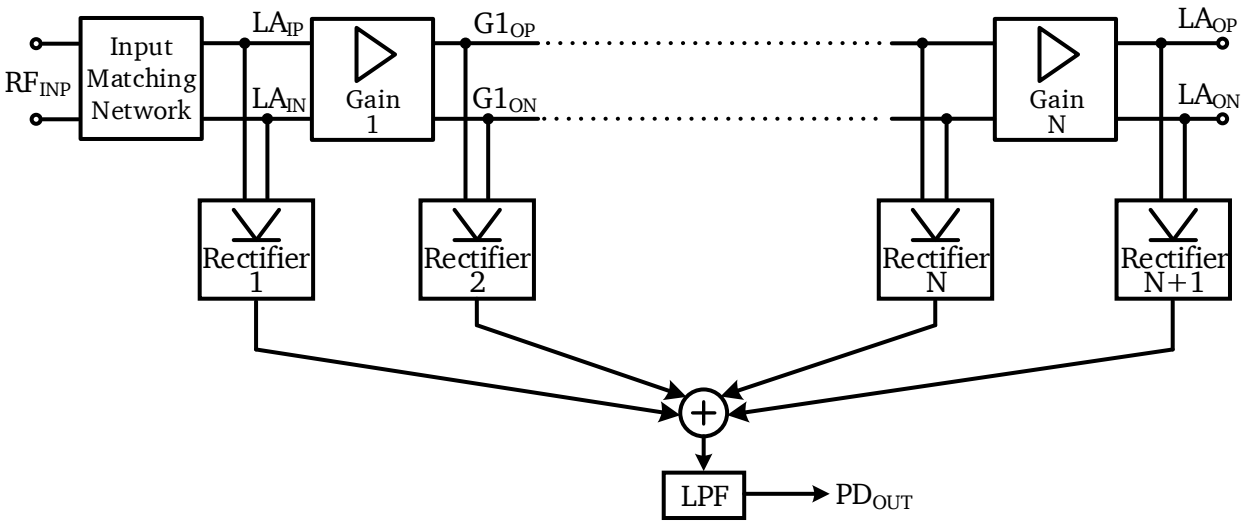


Figure 5.8: Successive detection logarithmic amplifier architecture with input matching network.

This section has presented the principle of operation and architecture of SDLA power detectors. The following sections introduce the design approach for an SDLA power detector keeping in mind the major area of focus in this work, namely achieving a high sensitivity and a olarge dynamic range across a wide frequency range.

5.3.2 Logarithmic Amplifier: Design Choices for Limiting Gain Stages

The cascaded gain stages need to be designed for high gain and high bandwidth because of the large dynamic range, high sensitivity and wide bandwidth requirements of the power detector. This section focuses on the architectural and design choices to simultaneously achieve high gain and high bandwidth for logarithmic amplifiers.

Gain versus bandwidth trade-off is a well-known aspect of amplifiers. Different approaches have been presented in the published literature to achieve high gain-bandwidth product. These techniques include designs based on Cherry-Hooper amplifiers, inductive peaking, active feedback, negative miller capacitance, negative impedance, and scaling of stages [70].

The approaches utilizing alternate series-shunt stages or the so-called Cherry-Hooper amplifier and modified versions of it have been described in various publications [69, 71–78]. The major drawback of this approach is the limited voltage headroom available at the output. Inductive peaking approaches have been reported in [79–81]. The use of inductive peaking has the drawback that the area requirements for the peaking inductor is large. Active inductors could be used to reduce the area. Works based on this solution has been demonstrated in [82–86] and present an alternative to modified Cherry-Hooper topologies when large voltage swings are required. However, the utilization of active feedback topologies comes with additional supply voltage requirements. Negative miller capacitance or negative impedance based gain-bandwidth extension have been presented in [82, 87]. Active inductor load techniques and interstage scaling techniques have also been previously proposed. A good summary of all the solutions mentioned above have been provided by Muller and Leblebici in [70, sec. 7.3], and Razavi in [88, sec. 5.2].

In this work, the focus will be on the modified Cherry-Hooper amplifiers to enhance the gain-bandwidth of the gain cell and thereby, facilitate wideband operation and sufficient gain per stage. As mentioned above, the major limitation of a modified Cherry-Hooper amplifier is the restricted voltage swing and common-mode dynamic range at its output [70]. However, as shown in the following section, for limiting gain cells used in high sensitivity power detectors, the limited output swing and common-mode range are not disadvantageous because of the dependence of the sensitivity of the logarithmic power detector on the limiting voltage of the gain cells.

5.3.2.1 Dependence of Detector Sensitivity on Limiting Voltage and Number of Stages

In Figure 5.5, it was shown that the logarithmic amplifier has a piece-wise logarithmic behavior. The limiting points in the figure, when joined together and extrapolated, provide the approximation for an ideal logarithmic behavior, and the logarithmic amplifier satisfies the equation of the ideal response line at the limiting points. From the ideal response line, two important parameters could be defined for the logarithmic amplifier, namely, slope and intercept voltage [89, p. 150]. The intercept voltage is the input voltage at which the output is equal to zero. In high-frequency applications, where the input is terminated to a given characteristic impedance, the intercept power of the ideal response can be found from the intercept voltage using the relation in Equation 5.1.

The slope and the intercept power of the piece-wise logarithmic response of the logarithmic amplifier are dependent on the number of stages, the gain per stage, and the input-referred limiting voltage of the gain stage, as given by Equations 5.3 and 5.4.

$$\text{Slope} = \frac{R_{\text{LPF}} \cdot G_{\text{S}} \cdot V_{\text{KNEE,A}}}{\log_{10} A_{\text{S}}} \tag{5.3}$$

$$\text{Intercept Power} = P_{\text{ICPT}} = 20 \cdot \log_{10} \left(\frac{V_{\text{KNEE,A}}}{A^{\left(N + \frac{A_{\text{S}}}{A_{\text{S}}-1}\right)}} \right) + 13 \tag{5.4}$$

where, R_{LPF} is the resistance used for summing the output currents from the rectifiers, G_{S} is the transconductance of the rectifier, and the characteristic source impedance is 50 Ω.

The intercept power sets the theoretical ideal limit of the achievable sensitivity for a logarithmic power detector. The mathematical dependence of the intercept power on the limiting voltage and the number

of stages is plotted in Figure 5.9 for a logarithmic amplifier with an overall gain of 60 dB is considered. Based on these results, it can be observed that minimizing the number of stages and the limiting voltage of the gain cells helps in improving the intercept power.

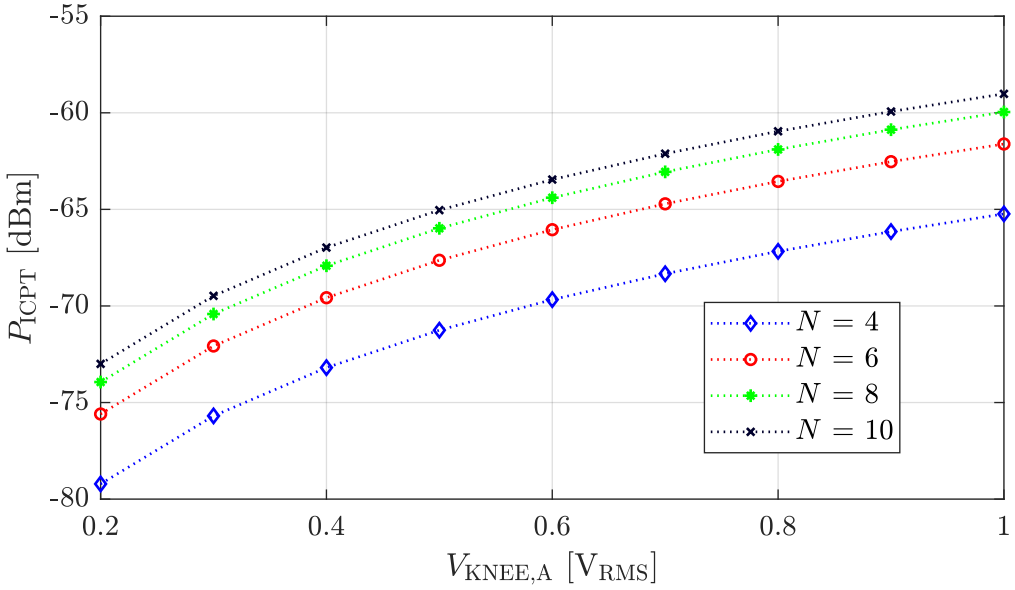


Figure 5.9: Dependence of intercept power on N and $V_{\mathrm{KNEE,A}}$ for a gain of 60 dB for the logarithmic amplifier.

It is important to note that these results hold when an ideal logarithmic behavior is considered. In real implementations, the sensitivity is limited by the piece-wise logarithmic response of the SLDA detector and the noise contributions from the component circuits and supply and ground interconnects. As a result, the actual sensitivity of an SDLA would not meet the ideal values provided here. The actual sensitivity can only be appropriately ascertained once the noise floor of the circuit is known. Nonetheless, the ideal response line based model provides an insight into the design approach for high sensitivity logarithmic power detectors.

5.3.3 Designing for Optimum Number of Stages

The choice of the number of stages N in the cascaded logarithmic amplifier, is critical in extracting the highest possible performance from the SDLA power detector. As N varies, the gain per gain stage A_{S}, the 3dB frequency of a stage f_{S}, the unity gain frequency of a stage f_{US}, the overall DC power consumption P_{T}, the total noise, and the maximum log-conformity error (LCE) LCE_{MAX} of the cascaded stages vary.

There have been previous works focused on deriving the equations concerning the choice of N for a single-pole system [90–92]. These relations describe the trade-offs associated with the choice of N when the limiting gain cell is realized as a dominant pole system.

The modified Cherry-Hooper topology that will be used in this work shows a two-pole characteristic. As such, this work will focus on the two-pole behavior for the choice of N. The relations involved in the analysis of the effect of N on the performance of the logarithmic amplifier are different for a two-pole system compared to that of a single-pole system. The relations for a two-pole system were studied by Chen et al. for a gain cell exhibiting Butterworth response in [93].

For a gain stage with two dominant poles, the gain response can be represented as a general second-order filter transfer function, as given by Equation 5.5 [93], [94, p. 468].

$$\begin{aligned} A(s) &= \frac{A_S}{\frac{s^2}{\omega_O^2} + \frac{s}{\omega_O Q} + 1} \\ &= \frac{A_S \cdot \omega_O^2}{s^2 + \frac{\omega_O}{Q} \cdot s + \omega_O^2} \end{aligned} \tag{5.5}$$

where, Q is the pole quality factor and ω_O is the pole frequency.

From the gain response, the dependence of the 3dB cut-off frequency of a single stage f_S and the 3dB cut-off frequency of the logarithmic amplifier f_{LogA} on the natural frequency can be deduced from Equations 5.6 and 5.7, respectively.

$$f_S = \frac{\omega_O}{2\pi} \cdot \left\{ 1 - \frac{1}{2Q^2} + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1} \right\}^{1/2} \tag{5.6}$$

$$f_{LogA} = \frac{\omega_O}{2\pi} \cdot \left\{ 1 - \frac{1}{2Q^2} + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 - 1 + 2^{(1/N)}} \right\}^{1/2} \tag{5.7}$$

The locations of the poles are given by Equation 5.8. When Q equals 1/2, it is called the critically damped condition, wherein the poles are real and equal. If Q is less than or equal to 1/2, the poles are real, i.e., they lie on the real axis. If Q is negative, the poles are in the right half of the s-plane, and the system is unstable and produces oscillations. As Q decreases from 1/2 towards zero, the poles move farther apart along the real axis. For Q greater than 1/2, the poles are complex conjugates. As the value of Q increases from 1/2 towards infinity, the poles start moving towards the imaginary axis.

$$\begin{aligned} P_1, P_2 &= -\frac{\omega_O}{2Q} \pm \sqrt{\omega_O^2 \cdot \left(\frac{1}{4Q^2} - 1\right)} \\ &= -\frac{\omega_O}{2Q} \pm j\omega_O \cdot \sqrt{1 - \frac{1}{4Q^2}} \end{aligned} \tag{5.8}$$

For a stable system, the poles of the transfer function have to lie in the left half of the complex s-plane. The amplifier provides high gain-bandwidth product when the poles are complex conjugates. Therefore, stable complex conjugate poles are preferable for the gain cells used in the logarithmic amplifier. The condition given by Equation 5.9 is of interest in this regard.

$$\begin{aligned} 1 - \frac{1}{4Q^2} &> 0 \\ \Rightarrow Q &> \frac{1}{2} \end{aligned} \tag{5.9}$$

5.3.3.1 Designing for Maximally Flat Gain Response

Depending upon the value of Q, the type of the magnitude and the group delay responses of the gain stage varies. The maximally flat gain response occurs at Q equal to $1/\sqrt{2}$, which corresponds to a second-order Butterworth response [69]. Q equal to $1/\sqrt{3}$ corresponds to a second-order Bessel response and provides a maximally flat group delay response. In this work, group delay is of less significance. Hence, the gain stages will be designed for maximally flat gain response.

For Q equal to $1/\sqrt{2}$, Equations 5.6 and 5.7 simplify and result in Equations 5.10 and 5.11, respectively.

$$f_{\mathrm{S}} = \frac{\omega_{\mathrm{O}}}{2\pi} \tag{5.10}$$

$$f_{\mathrm{LogA}} = \frac{\omega_{\mathrm{O}}}{2\pi} \cdot \left(2^{1/N} - 1\right)^{1/4} \tag{5.11}$$

When f_{S} is rewritten in terms of f_{LogA}, Equations 5.10 and 5.11 result in Equation 5.12. The gain of a single-stage, in terms of the gain of the logarithmic amplifier is given in Equation 5.13.

$$f_{\mathrm{S}} = \frac{f_{\mathrm{LogA}}}{\left(2^{1/N} - 1\right)^{1/4}} \tag{5.12}$$

$$A_{\mathrm{S}} = \left(A_{\mathrm{LogA}}\right)^{1/N} \tag{5.13}$$

The magnitude of the transfer function A(s) in Equation 5.5 is given by Equation 5.14. The unity gain frequency of a single stage f_{US} can be represented in terms of the 3dB frequency of the cascaded logarithmic amplifier f_{LogA} by deducing the results when the magnitude of the transfer function A(s) is equal to one.

$$|A(s)| = |A(jw)| = \frac{A_S}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_{\mathrm{O}}}\right)^2\right)^2 + \left(\frac{\omega}{Q \cdot \omega_{\mathrm{O}}}\right)^2}} \tag{5.14}$$

For a maximally flat response, f_{US} is given by Equation 5.15. Equations 5.11, 5.13, and 5.15 can be combined together to derive Equation 5.16, which represents f_{US} as a function of N when the gain and the 3dB frequency of the logarithmic amplfier are known. The total power consumption P_{LogA} of the logarithmic amplifier can be approximated by Equation 5.17 [93]. The maximum log-conformity-error LCE_{MAX} is defined by Equation 5.18 based on the observations by Melamed et. al. in [95].

$$f_{\mathrm{US}} = \frac{\omega_{\mathrm{O}}}{2\pi} \cdot \left(A_S^2 - 1\right)^{1/4} \tag{5.15}$$

$$f_{\mathrm{US}} = f_{\mathrm{LogA}} \cdot \left(\frac{1}{2^{1/N} - 1}\right)^{1/4} \cdot \left(A_{\mathrm{LogA}}^{2/N} - 1\right)^{1/4} \tag{5.16}$$

$$P_{\mathrm{T}} \propto N \cdot (f_{\mathrm{US}})^2 \tag{5.17}$$

$$LCE_{\mathrm{MAX}} = 10 \cdot \log_{10} A_{\mathrm{S}} \cdot \left[\frac{\log_{10}\left(\frac{A_{\mathrm{S}}-1}{\ln A_{\mathrm{S}}}\right)}{\log_{10} A_{\mathrm{S}}} - \frac{1}{\ln A_{\mathrm{S}}} + \frac{1}{A_{\mathrm{S}} - 1}\right] \tag{5.18}$$

For given specifications of dynamic range and bandwidth for the power detector, the value of N can be chosen based on Equations 5.12, 5.13, 5.16, 5.17 and 5.18.

Figures 5.10, 5.11 and 5.12 illustrate these dependencies when the overall gain for the logarithmic amplifier is 60 dB and the 3dB bandwidth is 3 GHz. The plots show that for a cascaded gain of 60 dB and a 3dB bandwidth of 3 GHz for the logarithmic amplifier employing modified Cherry-Hooper limiting gain cells, the total power consumption has an approximately broad minima for N values ranging from 4 to 6.

As the value of N increases, the unity-gain frequency required per stage decreases, thereby making the gain-bandwidth requirements less stringent. However, beyond a value of 6, the decrease in unity-gain frequency is not significant, and the decrease in the unity-gain frequency is moderated from N equal to four to N equal to 6. From the conditions for total power consumption and single-stage unity-gain frequency, values of 4 to 6 present a good range for N.

It has to be noted that for higher values of N, the degradation in the DC stability of the system is more prominent, and the requirements on the offset cancellation circuit increase. This leads to an additional trade-off in the choice of N, concerning the noise contribution from an offset cancellation circuit, and its influence on the detector sensitivity. Offset cancellation circuits and their significance on the design are described in Section 5.4.

Increasing the number of stages also decreases the gain per stage, and results in a higher input-referred noise for the logarithmic amplifier. Considering the above-mentioned trade-offs, the value of N has been chosen as four in this work. This value decreases the power consumption, and the maximum LCE is also within the required value of 1.5 dB. It has to be noted that the LCE_{MAX} is defined for the hard-clipping model of gain cell. As discussed in Section 5.3.1, MOS based, and Bipolar transistor based implementations have a softer limiting action. As a result, the actual maximum error will be lesser for designs based on MOS or Bipolar transistors.

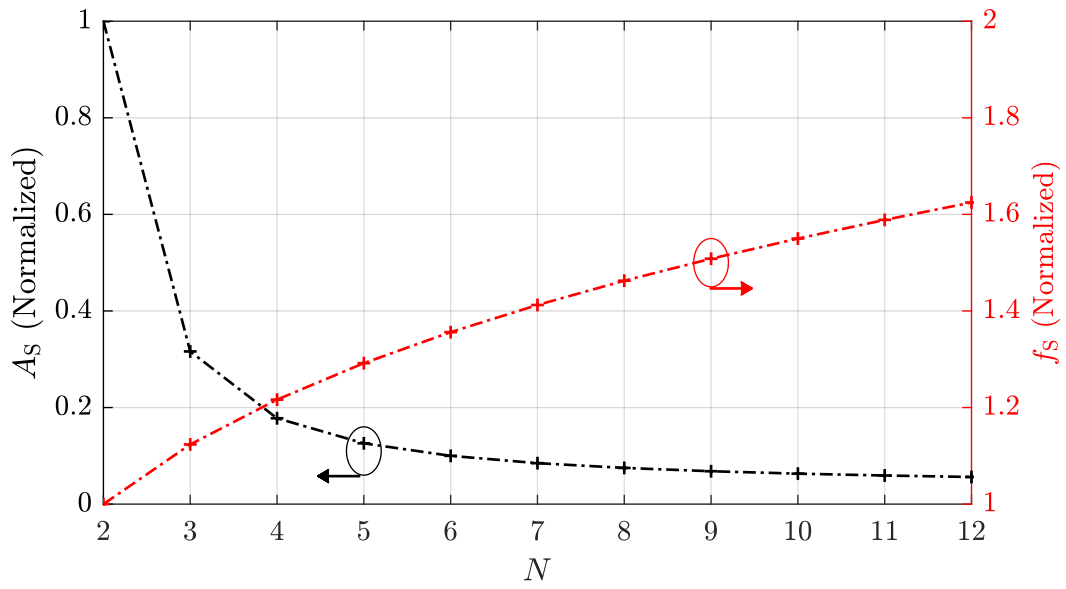


Figure 5.10: Dependence of normalized gain per stage A_S and 3dB frequency per stage f_S on the number of stages N for an overall gain of 60 dB and a 3dB frequency of 3 GHz for the logarithmic amplifier. The values are normalized with respect to the value of the corresponding parameter at N equal to 2.

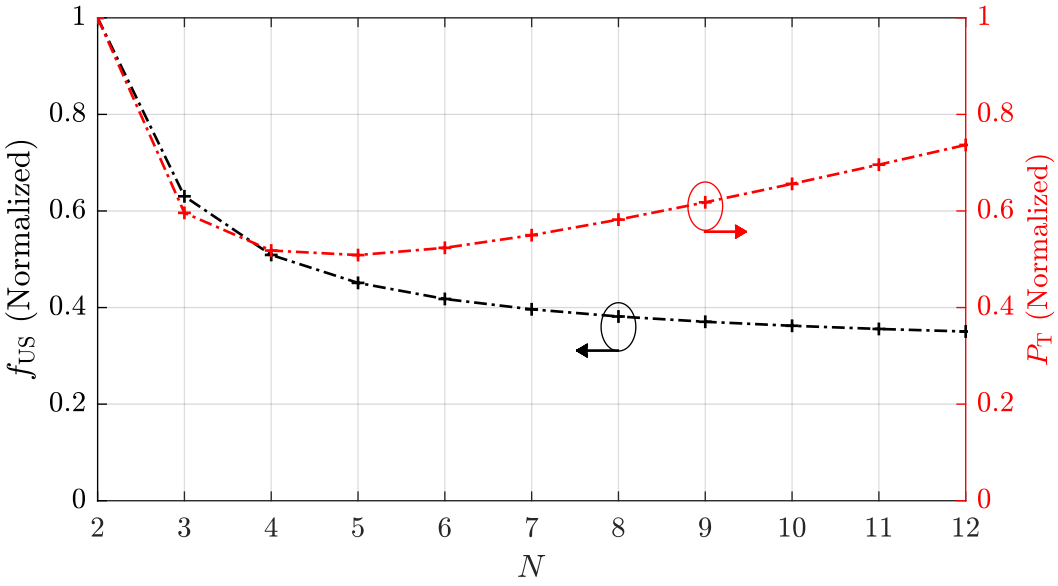


Figure 5.11: Dependence of normalized values of unity-gain frequency per stage f_{US} and total power P_T on the number of stages N for an overall gain of 60 dB and a 3dB frequency of 3 GHz for the logarithmic amplifier. The values are normalized with respect to the value of the corresponding parameter at N equal to 2.

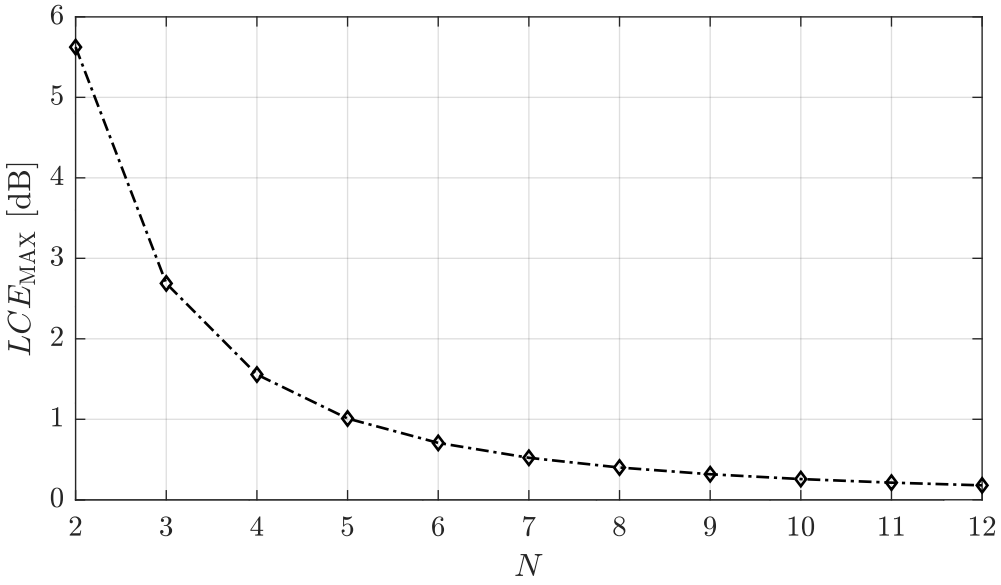


Figure 5.12: Dependence of the log-conformity error range LCE_{MAX} on the number of stages N for an overall gain of 60 dB and a 3dB frequency of 3 GHz for the logarithmic amplifier. The values are normalized with respect to the value of the corresponding parameter at N equal to 2.

5.3.4 Logarithmic Amplifier: Implementation

The optimal value for the number of stages in the cascaded logarithmic amplifier arrangement has been determined to be four in the previous section. The logarithmic amplifier can be implemented once the limiting gain stage has been designed.

5.3.4.1 Limiting Gain Stage Implementation

Section 5.3.2 evaluated the different choices for the realization of the limiting gain stage and ascertained that the modified Cherry-Hooper amplifier would a good choice for this work. This section presents the implementation of a limiting gain cell based on the modified Cherry-Hooper topology.

The Cherry-Hooper amplifier was first proposed in [71] as a technique that uses alternate series- and shunt feedback stages to tune the gain and bandwidth of an amplifier independently from one another. The Cherry-Hooper amplifier, however, introduced a trade-off with respect to the gain-bandwidth and the dynamic range. Many implementations of modified Cherry-Hooper amplifiers employing emitter-follower feedback or source-follower feedback have been reported that alleviate this trade-off [69, 72, 73]. Figure 5.13 depicts the schematic of the designed limiting gain stage [69] based on the modified Cherry-Hooper amplifier architecture employing emitter-follower feedback. A BiCMOS implementation is preferred for the modified Cherry-Hooper amplifier due to the higher transconductance of a SiGe HBT and the higher gain-bandwidth product that can be achieved for the same power, when compared to a MOS transistor based implementation. Moreover, bipolar transistors are more robust against process variations, and provide better matching between the transistors in the differential pair, and minimize the DC offset of the limiting gain stage. A high DC offset will be detrimental to the logarithmic amplifier because of the cascaded open-loop nature of the gain stages, and minimizing the input-referred offset of the gain stages reduces the requirements on the offset cancellation range of the logarithmic amplifier.

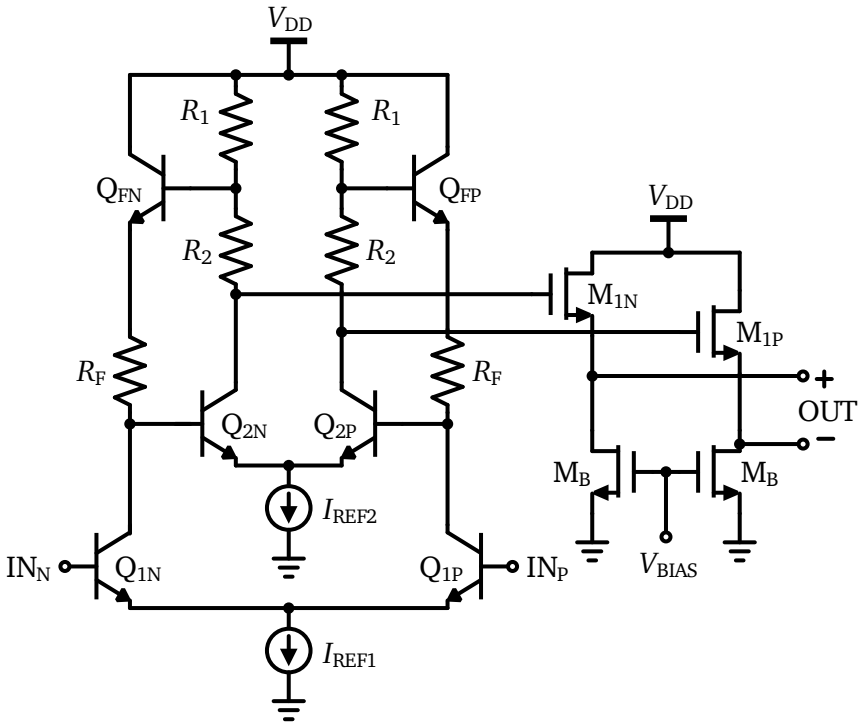


Figure 5.13: Schematic of the limiting gain cell.

The transistors Q_1, Q_2, and Q_F are designed to limit the noise and power consumption of the circuit. The transistor Q_1 is sized for low noise and I_{REF1} is chosen to provide close to peak f_T current density for Q_1. The choice of I_{REF2} affects the output swing of the circuit and the current density of Q_2. Once the value of I_{REF2} is determined, R_1 is chosen based on the required output swing.

The value of resistors R_1, R_2, and R_F determine the gain, bandwidth, output swing, and pole quality factor of the circuit. As reported in [73], the gain of the circuit can be increased significantly by increasing

R_2 while maintaining the ratio R_2/R_1 in the range of 0 to 2.5, which ensures that the variation in bandwidth is very little. For given values of I_{REF1} and I_{REF2}, the choice of R_F/R_1 determines the pole quality factor, 3dB bandwidth and gain of the circuit.

A buffer stage is added to the modified Cherry-Hooper amplifier output to increase the slew rate. The buffer is realized using source follower NMOS transistors. The bias voltage, V_{BIAS}, for the source follower is generated using a Brokaw cell based bandgap reference circuitry to ensure minimal variations due to supply and temperature variations [96]. The schematic diagram of the implemented bandgap reference circuit is illustrated in Figure 5.14. The limiting gain cell has been designed to provide a DC gain higher than 15 dB so that the four gain cells in the cascade can provide 60 dB total gain. The AC response of the gain cell is plotted in Figure 5.15.

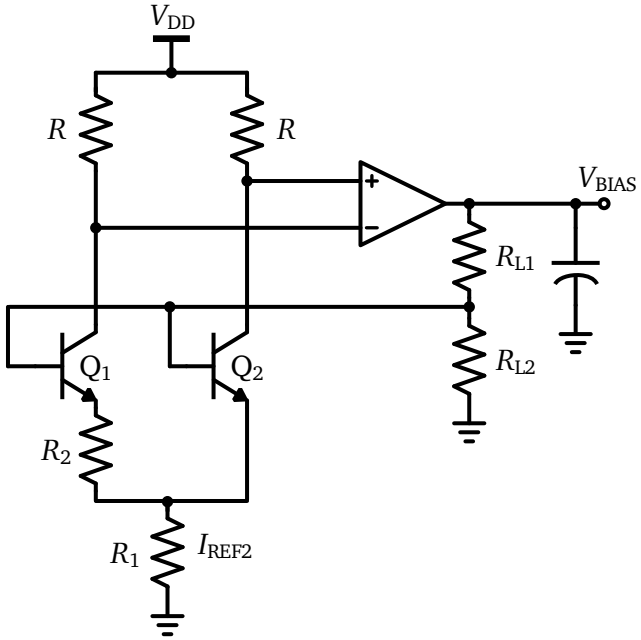


Figure 5.14: Schematic of the bandgap reference circuit.

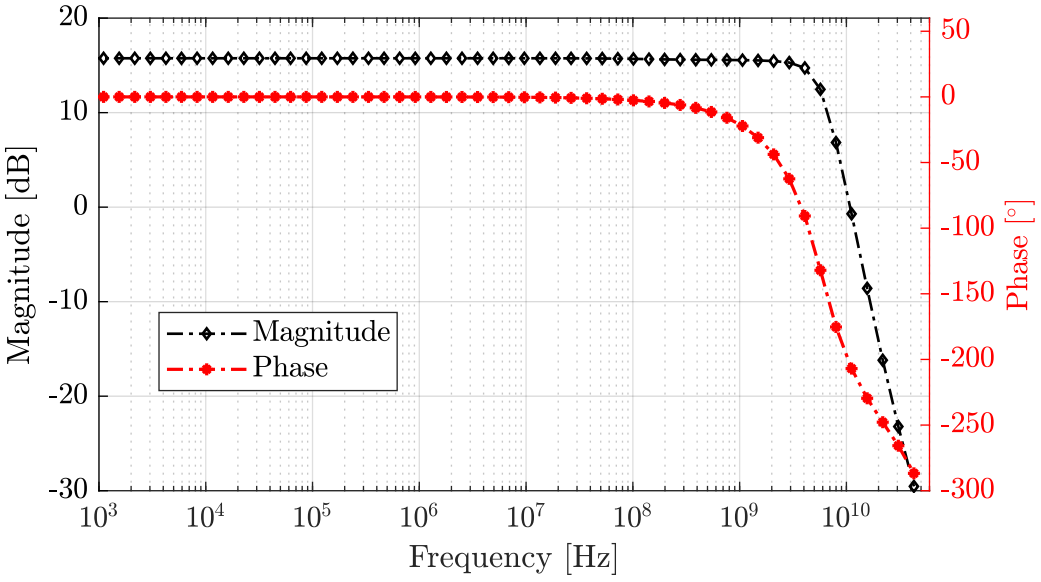


Figure 5.15: AC response of the limiting gain cell.

The limiting action of the gain cell is verified through transient simulations, and the response is plotted in Figure 5.16. The variation of the RMS value of the output voltage as the input peak value varies is shown in Figure 5.17 for 1 GHz input frequency.

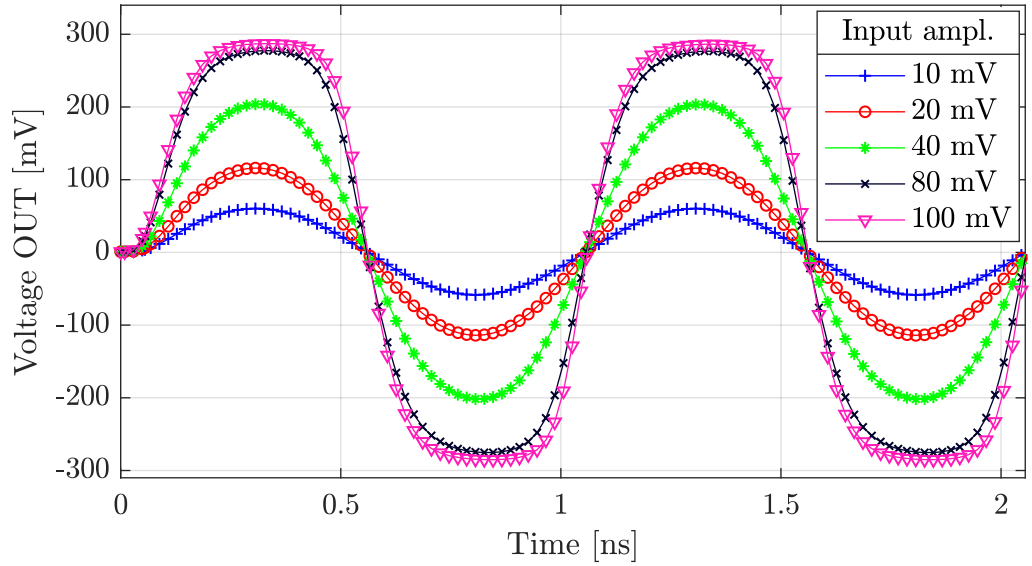


Figure 5.16: Transient response of the gain cell for different values of input amplitude at 1 GHz input frequency.

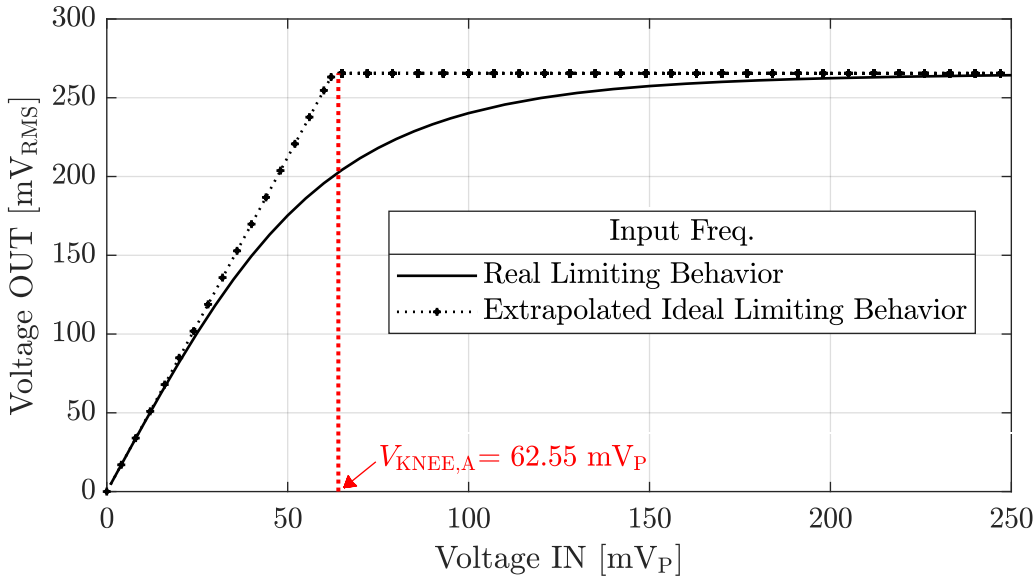


Figure 5.17: Soft-limiting behavior of the gain cell. The RMS voltage characteristic is plotted here for 1 GHz input frequency.

The limiting voltage $V_{KNEE,A}$, varies slightly as the frequency of the input signal is varied. This is illustrated in Figure 5.18 for five different frequencies within the frequency range of interest of the power detector. The resultant deviation of the limiting voltage of the limiting gain cells results in a frequency-dependent variation of the slope and the sensitivity of the SDLA power detector, which were presented by Equations 5.3 and 5.4.

A low value for the input-referred limiting voltage is essential to keep the sensitivity of the power detector as high as possible. The noise from the gain stage is predominantly due to the input differential

pair transistors Q_{1N} and Q_{1P}. These transistors have been designed in such a way that their minimum noise figure F_{MIN} is kept as low as possible. i.e., transistor gain has been sacrificed for low noise in this design.

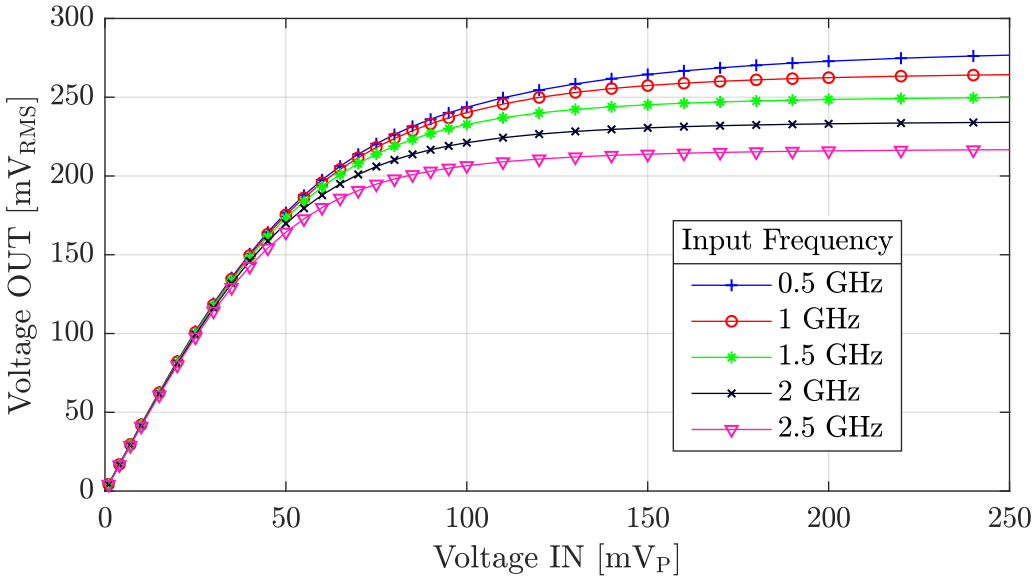


Figure 5.18: Soft-limiting behavior of the gain cell for different input frequencies.

Parasitic-extracted post-layout simulation results of the important performance indicators of the gain cell are summarized in Table 5.1. The simulations are set up with the gain stages loaded by one gain stage and one rectifier to reflect the load of the gain stage when it is employed within an SDLA power detector. From the simulation results, it can be observed that the input-referred DC offset of the limiting gain stage is high at 136 µV. This makes the cascaded arrangement of four limiting gain stages prone to DC stability issues. The total integrated input-referred noise of the limiting gain stage is also rather high at 337 µV.

Table 5.1: Parasitic-extracted post-layout simulation results of the limiting gain cell.

Parameter	Value	Unit
DC Gain (A_S)	15.58	dB
3dB frequency (f_S)	5.583	GHz
Unity-gain frequency (f_{US})	10.86	GHz
Input-referred noise at 1 GHz	3.257	$\frac{nV}{\sqrt{Hz}}$
Integrated input-referred noise in pass-band	337	µV
Input-referred limiting voltage ($V_{KNEE,A}$) at 1 GHz	62.55	mV_P
Output-referred limiting voltage at 1 GHz	265.96	mV_{RMS}
Settling time (high/low)	149.5 / 149	ps
Slew-rate (rise/fall)	4.391 / 4.535	$\frac{V}{\mu s}$
Input-referred DC offset	146.38	µV
DC power consumption	8.474	mW

Four of these gain stages are cascaded to implement the logarithmic amplifier. The AC response of the logarithmic amplifier is illustrated in Figure 5.19 for two different test cases. In the first test case, the DC bias to the differential inputs are maintained at the same level, i.e., DC input offset of the circuit is not

canceled. In the second test case, differential input bias is maintained at different levels to negate the DC input offset. Parasitic-extracted post-layout simulation results of the logarithmic amplifier without any offset cancellation are summarized in Table 5.2. For these simulations, the logarithmic amplifier is loaded with a dummy gain stage, and the individual gain stage outputs are loaded with rectifiers to imitate the real loading conditions when used in an SDLA power detector. The DC power consumption, including the power consumption due to the bias circuitry and the dummy gain stage, is 37.79 mW.

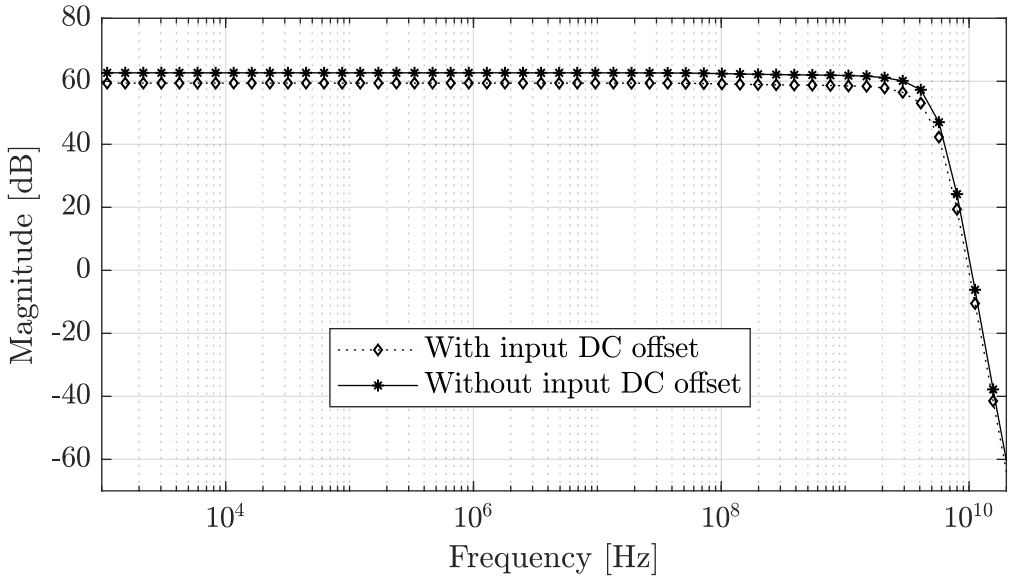


Figure 5.19: AC response of the logarithmic amplifier with and without compensation of input DC offset.

Table 5.2: Parasitic-extracted post-layout simulation results of the four-stage logarithmic amplifier with no offset cancellation.

Parameter	Value	Unit
DC Gain (A_{LogA})	59.415	dB
3dB frequency (f_{LogA})	3.189	GHz
Unity-gain frequency (f_{ULogA})	9.97	GHz
Input-referred noise at 1 GHz	3.327	$\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$
Integrated input-referred noise in pass-band	579.9	µV
DC power consumption	37.79	mW

5.3.5 Input Matching Network Implementation

The input of the power detector needs to have good impedance matching to the output of the power amplifier to ensure low-loss power transfer into the detector. At the input of the power detector, an impedance matching network needs to be added for this purpose. Due to the large area requirements of a passive implementation, an active matching network, as shown in Figure 5.20, is designed for 50 Ω impedance matching [97, 116].

The return loss performance of the input matching network is shown in Figure 5.21. The circuit is optimized to provide the best performance across the frequency range of 500 MHz to 2.5 GHz. The return loss is larger than 10 dB across this bandwidth.

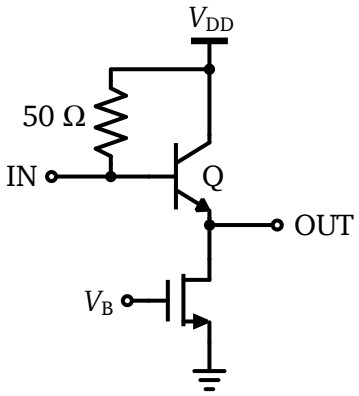


Figure 5.20: Schematic of the implemented input matching circuit.

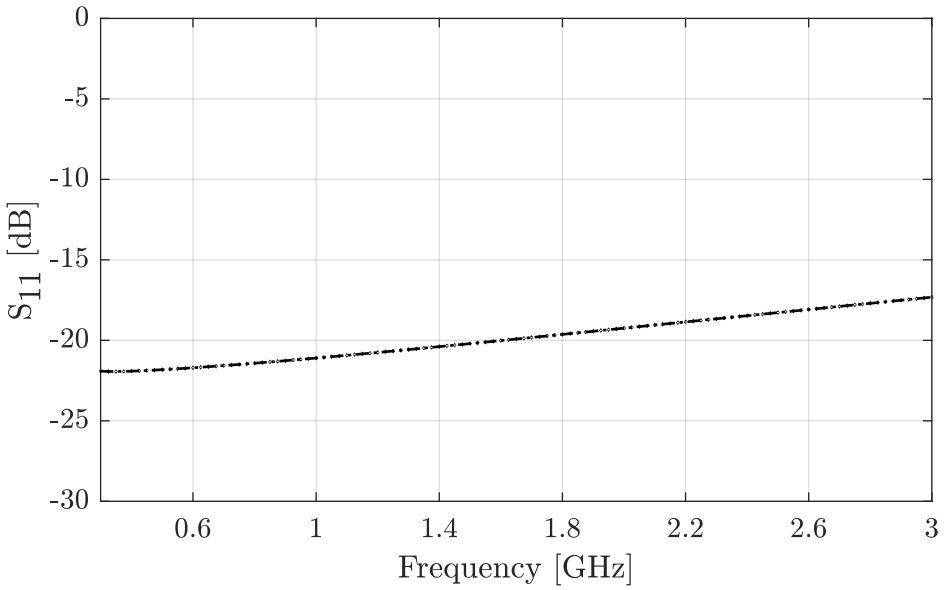


Figure 5.21: Input return loss of the input matching circuit.

5.3.6 Rectifier Implementation

The rectifying transconductor is used as part of the SDLA power detector to convert the differential output signals from the gain stages of the logarithmic amplifier to single-ended current signals that are proportional to the amplitude of the input signal. These cells act as the detector cells for peak power detection. They detect the envelope of the RF input signal and generate a DC output that is a measure of the peak value of the input.

Unlike a limiting gain stage, a rectifier doesn't need to have a substantial bandwidth. If the gain of a rectifier rolls off with frequency, the full-scale output current will be decreased. However, this is not detrimental to the dynamic range of the power detector [63]. Also, compared to the gain stages, the noise contribution from the rectifying stages is minimal. In this work, a modified version of the balanced source-coupled pair rectifier reported in [98] is implemented. It has a single-ended output as opposed to the differential nature of the output in the original work. The circuit is based on the detector cell that was originally proposed by Gilbert in [99].

The schematic of the implemented rectifier, together with the load, is shown in Figure 5.22. Balanced source-coupled NMOS differential pairs are used, with one differential pair connected to the differential

input and the other differential pair connected to the average of the differential input. This average is generated by connecting the differential terminals of the input through resistors.

The currents at the two differential pairs are summed up, and the resulting current relation is given by Equation 5.19. The NMOS transistors are operated in the strong inversion region and Equation 5.20 defines the behavior of the output current with respect to the input voltage [98, 112].

$$\mathrm{I_O} = \mathrm{I_{SCP1}} - \mathrm{I_{SCP2}} \tag{5.19}$$

$$\mathrm{I_{OUT}} = \mathrm{I_O} = \begin{cases} \frac{\mu_n C_{OX} \frac{W}{L}}{4} \cdot V_{IN,D}^2 & \text{if } |\mathrm{V_{IN}}| < V_{knee,D} \\ I_{REF,D} & \text{if } |\mathrm{V_{IN}}| \geq V_{knee,D} \end{cases} \tag{5.20}$$

where, $V_{knee,D}$ denotes the input referred knee voltage, $I_{REF,D}$ denotes the reference current, μ_n denotes the electron mobility, C_{OX} denotes the gate oxide capacitance per unit area and $\frac{W}{L}$ denotes the dimensions of the source-coupled transistors.

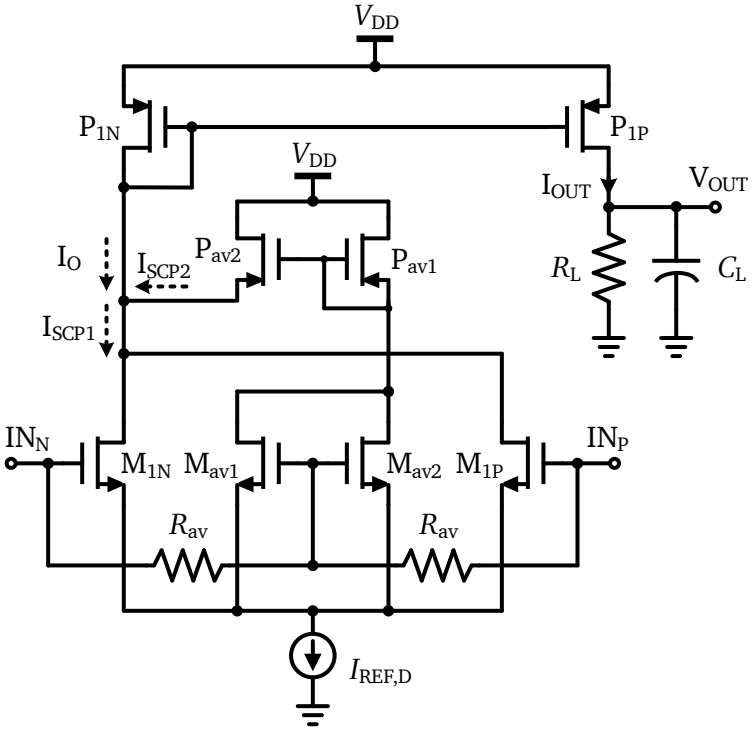


Figure 5.22: Schematic of the implemented rectifier.

The output current of the rectifier for different input signal amplitudes is plotted in Figure 5.23 for two different input signal frequencies. The response of the rectifier shows negligibly small deviation for the two different frequencies considered.

Figure 5.24 depicts the transient response of the implemented rectifier for different values of peak input voltage. As the input amplitude increases from 0 to the knee voltage of the rectifier, the rectifier output settles to higher values. Beyond the knee voltage, the output level starts saturating, as is evident in the transient response. The knee voltage of the rectifier $V_{knee,D}$ is 247 mV_P and is maintained higher than the knee voltage of the limiting gain stages $V_{knee,A}$.

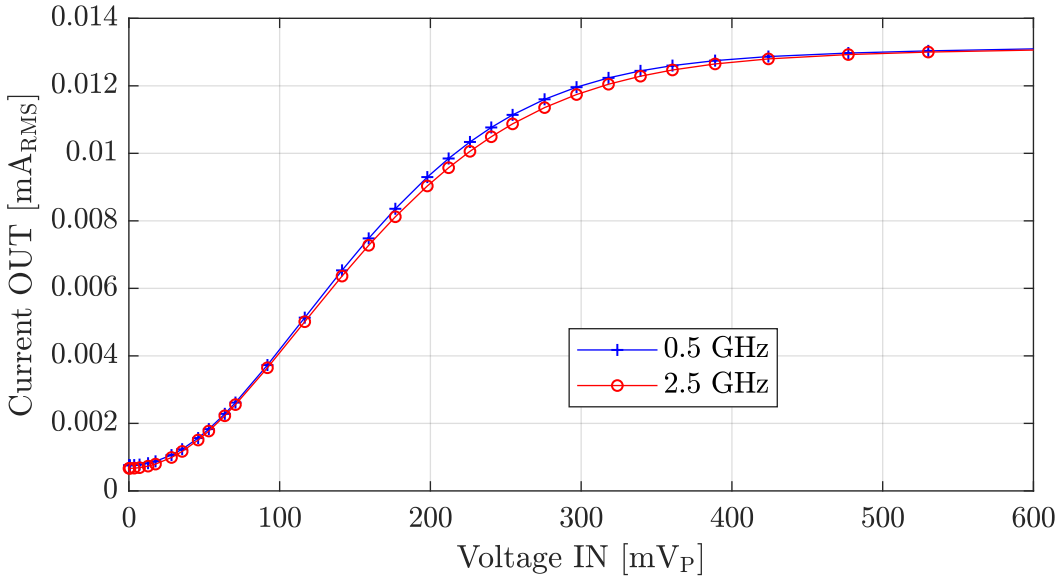


Figure 5.23: Output characteristic of the current from the rectifier cell.

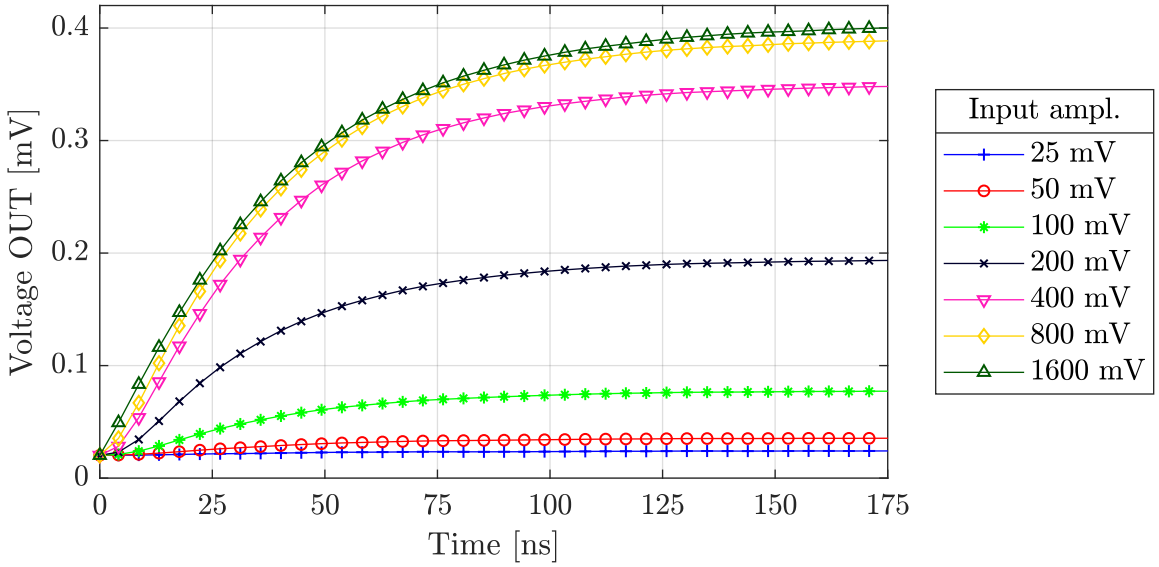


Figure 5.24: Output voltage of the rectifier when connected to load resistor and capacitor.

5.3.7 Power Detector Implementation without Offset Cancellation

The logarithmic amplifier, the rectifier, and the input matching network are employed to implement an SDLA power detector, as shown in Figure 5.25. The negative terminal is connected to an internally generated common-mode voltage that is required for the limiting gain stages. Such a pseudo-differential approach is undertaken considering the single-ended nature of the output of the power coupler in the power control loop that is shown in Figure 5.3. The rectifier currents are summed up at the resistor R_L to generate the DC output voltage of the detector. No in-built offset cancellation circuit is added to this detector.

Parasitic-extracted post-layout simulation results of the detector output voltage and the corresponding LCE are plotted in Figures 5.26 and 5.27, respectively. MATLAB function to calculate LCE from detector output voltage is given in Appendix A. The results demonstrate that the sensitivity of the detector varies

from a maximum of -56 dBm at 500 MHz to a minimum of -48 dBm at 3 GHz when considering a ±1 dB error range. The detector has a maximum dynamic range of 58.5 dB at 1 GHz and a minimum dynamic range of 47 at 3 GHz. At frequencies higher than 2.5 GHz, the gain roll-off and the increase in $V_{KNEE,A}$ of the limiting gain stages reduce the sensitivity and dynamic range. At 3 GHz, the sensitivity is -48 dBm and the dynamic range is 47 dB. The total power consumption of the detector is 40.92 mW. Parasitic-extracted post-layout simulation results of the power detector with no offset cancellation are tabulated in Table 5.3.

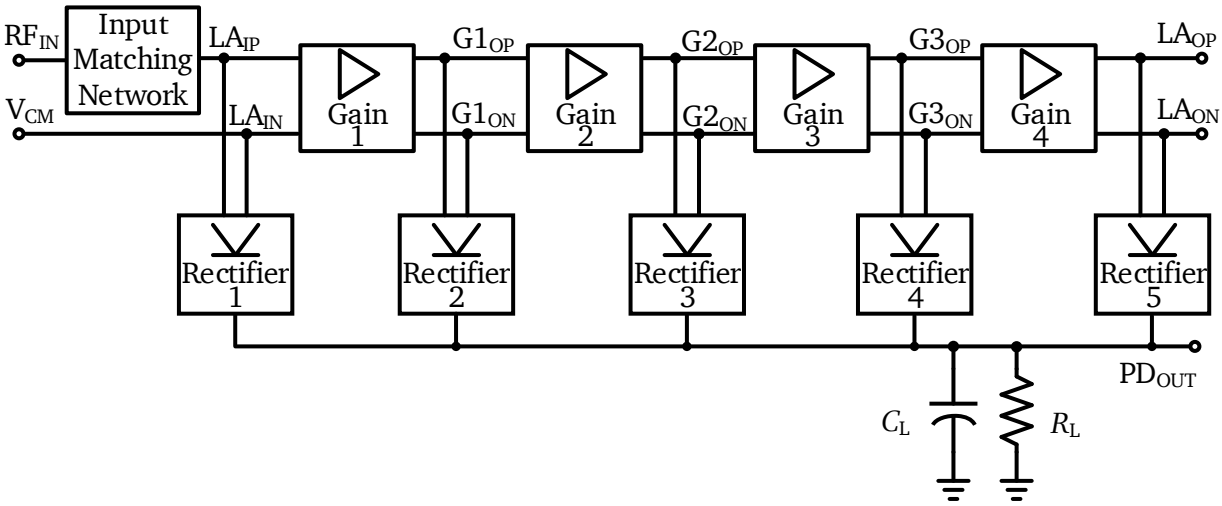


Figure 5.25: Block diagram of the SDLA power detector having no offset cancellation circuit.

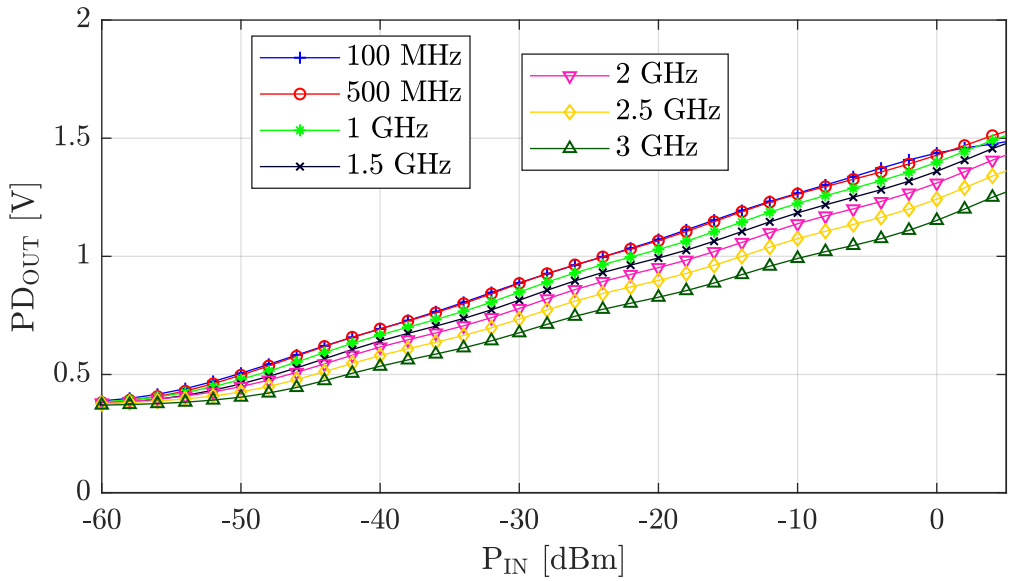


Figure 5.26: Output response of the SDLA power detector having no offset cancellation circuit.

Separate transient simulations are performed with noise contribution from selected sub-circuits alone turned on, in order to study the influence of noise generated from individual sub-circuits. LCE plots based on these simulations for an input signal frequency of 2.5 GHz are shown in Figure 5.28. Due to the limiting characteristic of the cascaded gain cells, the overall gain of the cascaded amplifiers and consequently output noise is maximum for lower input power levels. Figure 5.29 shows a magnified version of the results, with a focus on the low input power region.

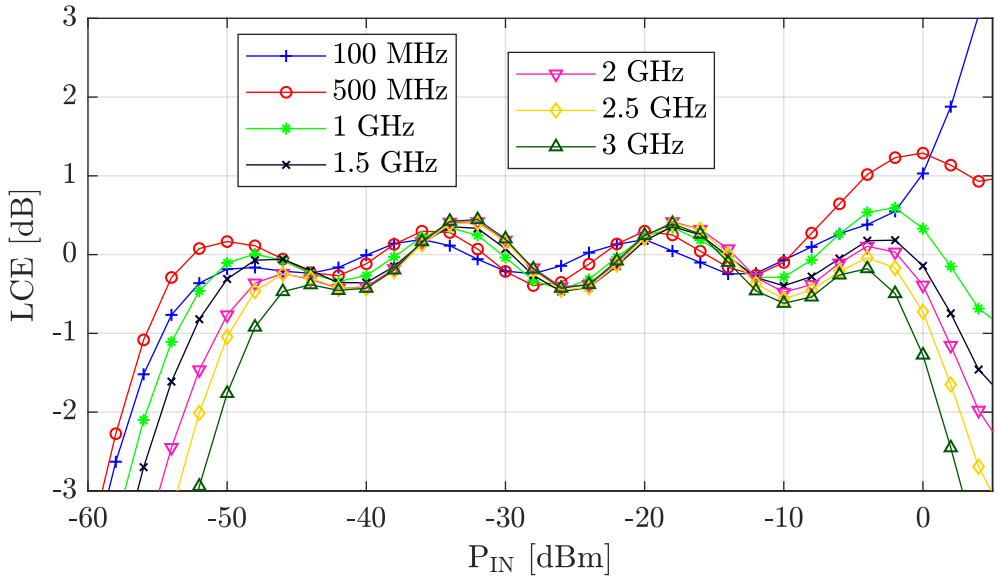


Figure 5.27: Log-conformity error of the SDLA power detector having no offset cancellation circuit.

Table 5.3: Parasitic-extracted post-layout simulation results of the power detector with no offset cancellation for ±1 dB log-conformity error range.

Frequency [GHz]	Sensitivity [dBm]	Dynamic Range [dB]
0.1	-54.5	54.5
0.5	-56	52
1	-53.5	58.5
1.5	-52.5	55
2	-50.5	52
2.5	-50	50.5
3	-48	47

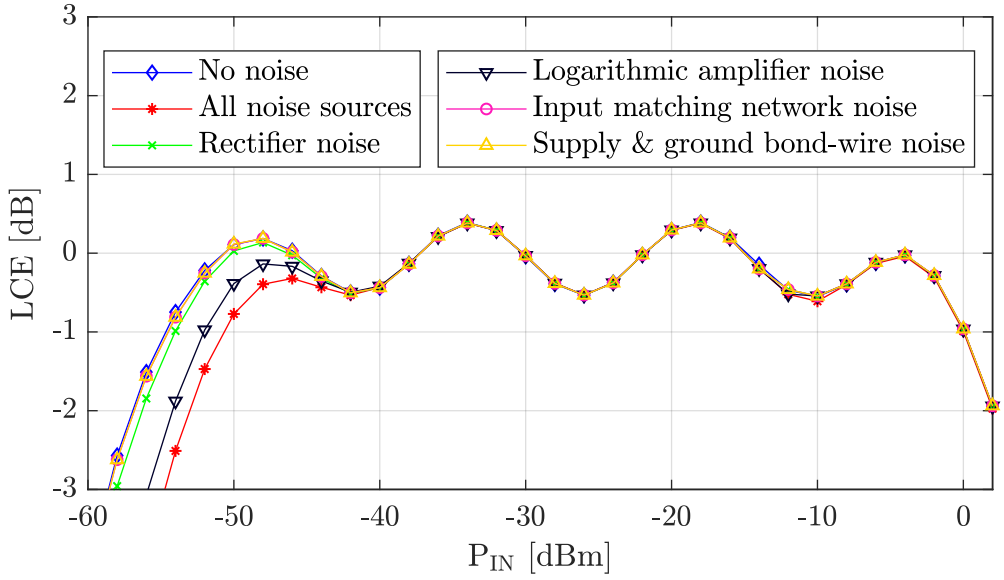


Figure 5.28: LCE plot at 2.5 GHz showing noise contributions of the SDLA power detector when no offset cancellation circuitry is employed.

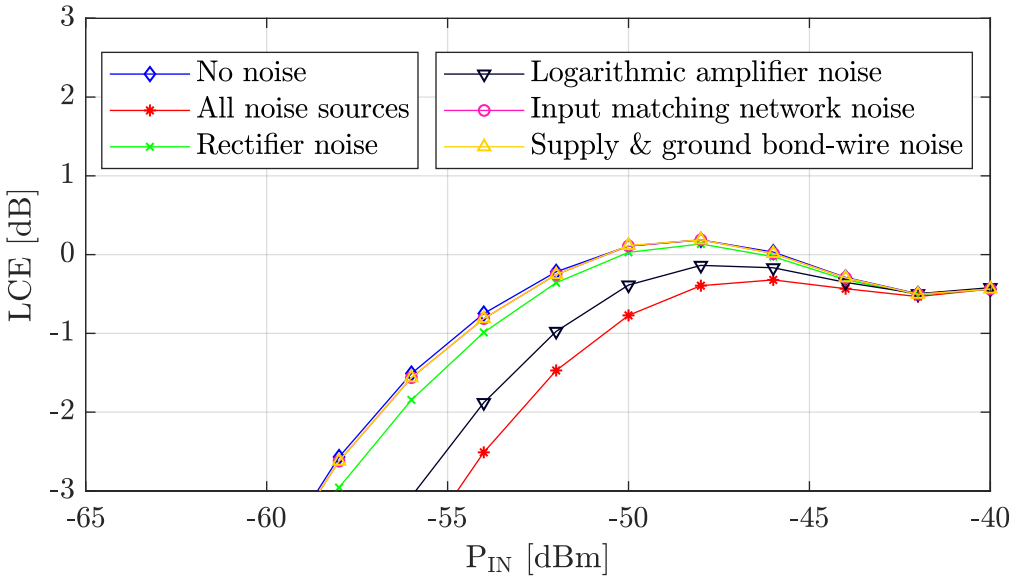


Figure 5.29: Magnified view of the LCE plot at 2.5 GHz showing noise contributions and their effect on the sensitivity of the SDLA power detector when no offset cancellation circuitry is employed.

It can be observed that the logarithmic amplifier is the major noise contributing source within the power detector and limits the achievable sensitivity. Due to the peak detecting nature of the rectifiers, the noise from the entire pass-band of the logarithmic amplifier gets integrated into the DC output. As a result, low-frequency noise sources, such as the flicker noise of the transistors, also remain significant.

The input-referred DC offset of the four-stage cascaded logarithmic amplifier having no in-built offset cancellation mechanism is 146.4 µV. As the input offset increases beyond this value, the performance of the logarithmic amplifier starts deteriorating. Hence, it is imperative to study the offset cancellation range of the logarithmic amplifier. This is done by varying the offset between the differential input rails and observing the performance of the logarithmic amplifier simultaneously. A plot of the variation in the logarithmic amplifier gain at 2.5 GHz, as the input offset varies, is shown in Figure 5.30.

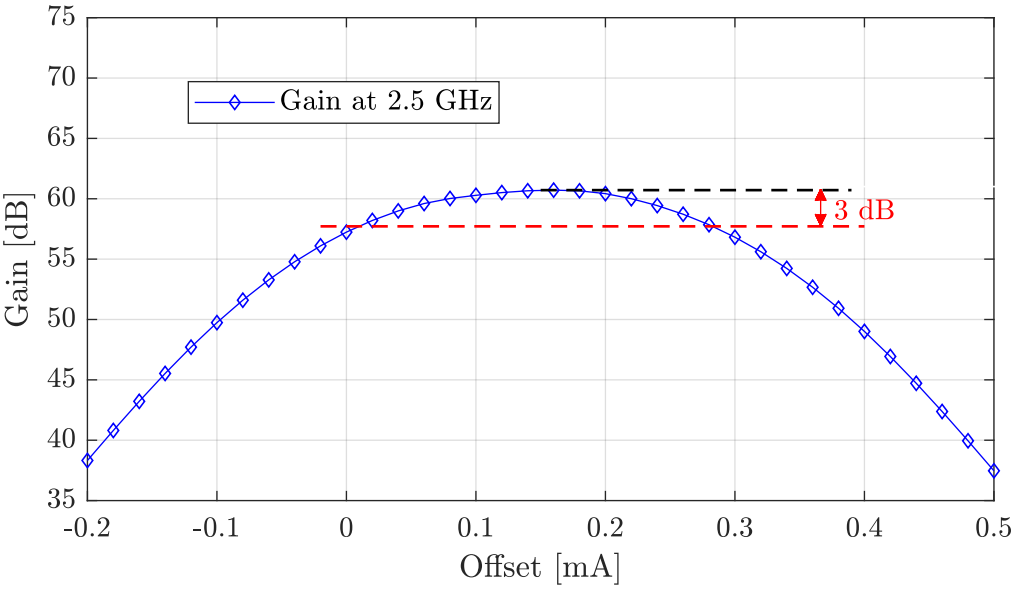


Figure 5.30: Variation in gain for different values of input offset for the logarithmic amplifier when no offset cancellation circuitry is employed.

For input offset voltages larger than 284 μV and for input offsets lesser than 15 μV, the gain of the logarithmic amplifier drops below the -3dB threshold when compared to the maximum achievable performance. Such a low offset range, within which the logarithmic amplifier performance remains close to nominal performance, makes the power detector extremely prone to saturation errors. As a result, it is paramount that an offset cancellation circuit is added to the implemented power detector.

The next section introduces certain commonly used offset cancellation approaches. Two of these approaches will be implemented for the presented power detector, and their influence on the system performance will be analyzed.

5.4 Offset Cancellation Approaches and Their Influence on Detector Performance

Different factors, such as process variations, device mismatches, layout parasitics, and biasing non-idealities, contribute towards the offset of a circuit. These offset inducing sources could be either within the circuit or external to it. In this section, initially, a review of the different offset cancellation methodologies is presented. Thereafter, logarithmic amplifiers employing two of the commonly adopted approaches are implemented and the influence of these approaches on the performance of power detectors based on these implementations is evaluated.

5.4.1 Offset Cancellation Approaches

Different approaches have, traditionally, been utilized to reduce offset in a circuit. These include device trimming, design and layout optimization approaches as well as employment of additional circuits meant for offset cancellation. Trimming is a post-processing technique, and it is limited by the need for additional processing steps and the costs associated with these steps. Design and layout optimization approaches meant for inherently low offset in the circuit are limited by the range of offset that can be suppressed. When a large offset cancellation range is desirable, the addition of specialized circuitry meant for offset suppression is preferred. The commonly used circuit-based offset cancellation approaches are AC-coupled offset cancellation, DC feedback offset cancellation, auto-zero based offset cancellation, and chopper-modulator offset cancellation. Auto-zeroing and chopper-modulation are dynamic approaches that involve the utilization of switches. This work concentrates on the AC-coupling based and DC feedback based offset cancellation approaches.

5.4.2 Power Detector Implementation with AC-coupled Offset Cancellation

AC-coupled offset cancellation circuits utilize DC blocking capacitors and resistive voltage dividers to ensure that any DC offset in a limiting gain stage does not propagate to the following cascaded stages. The capacitors block the DC voltage at the output, and the resistive divider provides the required common-mode voltage at the output. If the compensation circuit is not designed carefully, the gain of the stage could be compromised. The coupling capacitors need to be large enough to maintain the desired bandwidth of operation for the gain stage. Whereas, the resistors need to be chosen carefully to reduce their noise contribution and power consumption.

The schematic of the limiting gain stage with the AC-coupling offset cancellation circuit at its output is shown in Figure 5.31. The modified Cherry-Hooper circuit and the buffer circuits remain the same as the ones presented in Section 5.3.4.1. The lower frequency at which the logarithmic amplifier crosses unity-gain is designed to be 6 MHz. A lower value for this lower unity-gain frequency will help in extending the pass-band frequency range. However, the noise contributions within the pass-band frequencies will increase.

Four limiting gain stages are cascaded together to implement a logarithmic amplifier with AC-coupled offset cancellation. Parasitic-extracted post-layout simulation results of the logarithmic amplifier with

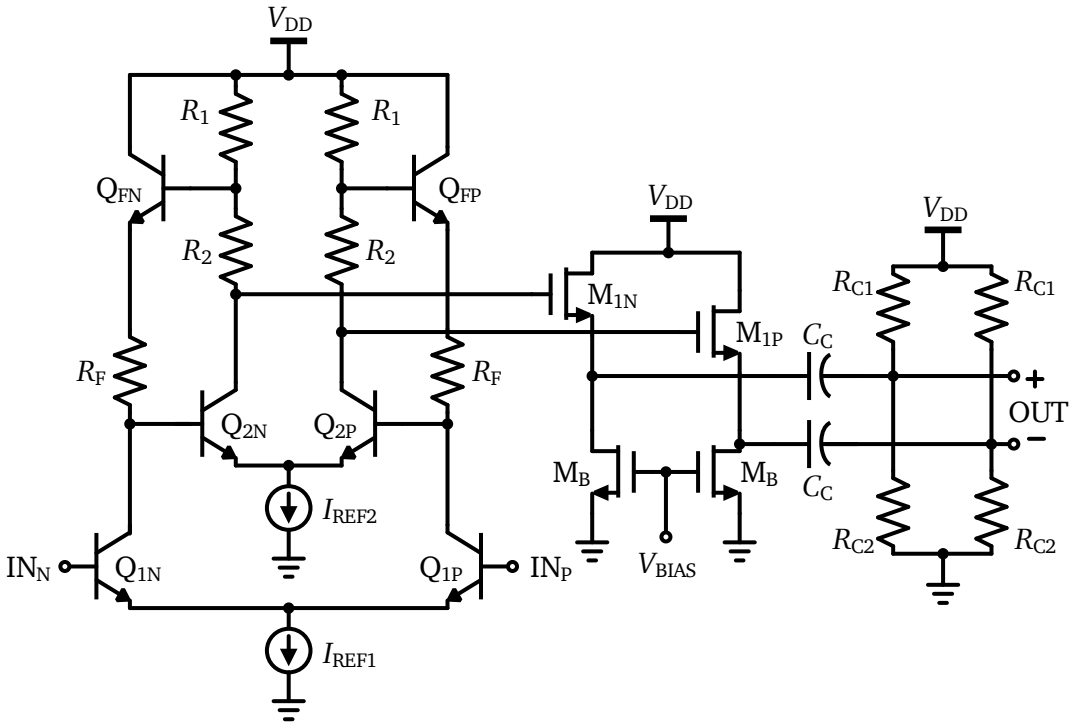


Figure 5.31: Schematic of the limiting gain cell with AC-coupled offset cancellation [112].

AC-coupled offset cancellation are summarized in Table 5.4. For these simulations, the logarithmic amplifier is loaded with a dummy gain stage, and the individual gain stage outputs are loaded with rectifiers to imitate the real loading conditions when used in an SDLA power detector. The total DC power consumption of the logarithmic amplifier, including the biasing circuits and the dummy gain stage, is 39.94 mW. The frequency response plots for the limiting gain stage and the logarithmic amplifier are shown in Figure 5.32.

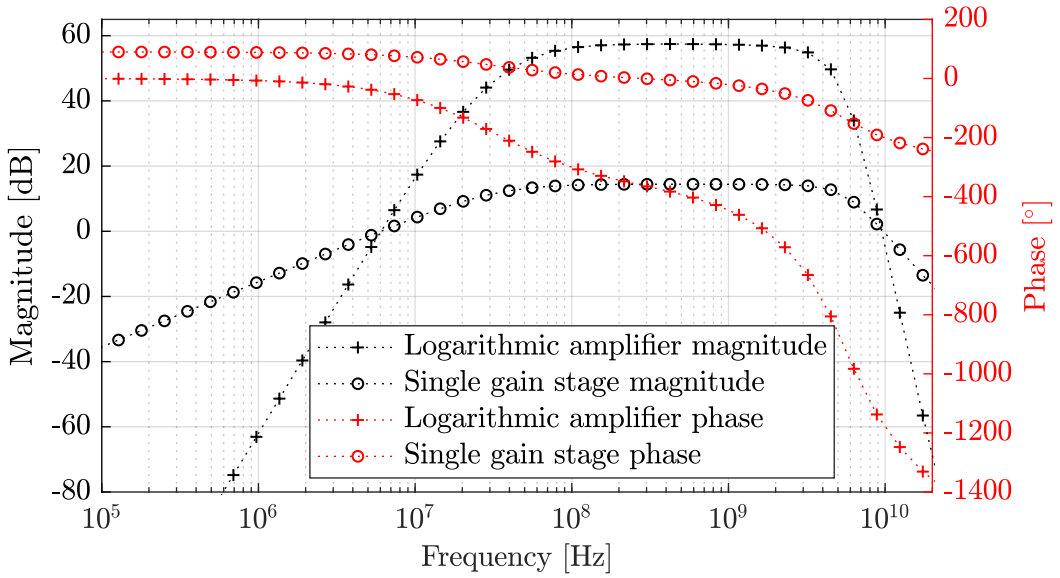


Figure 5.32: AC response of the limiting gain cell and the logarithmic amplifier with AC-coupled offset cancellation.

Table 5.4: Parasitic-extracted post-layout simulation results of the four-stage logarithmic amplifier with AC-coupled offset cancellation.

Parameter	Value	Unit
Maximum gain between 500 MHz and 2.5 GHz (A_{LogA})	57.44	dB
3dB frequency (f_{LogA})	3.37	GHz
Unity-gain frequency (low/high) (f_{ULogA})	0.006 / 9.53	GHz
Input-referred noise at 1 GHz	3.393	$\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$
Integrated input-referred noise in pass-band	532.7	µV
DC power consumption	39.94	mW

The offset cancellation range of the logarithmic amplifier is maintained larger than ± 30 mV. In this work, the offset cancellation range is defined as the range of input offsets within which the circuit still provides a gain that is within a -3dB threshold compared to the maximum achievable gain of the circuit. Since the maximum frequency of interest for the power detector design is 2.5 GHz, the gain at 2.5 GHz is considered for the offset cancellation range evaluation. Figure 5.33 shows the gain variation with input offset for the implemented logarithmic amplifier employing AC-coupled offset cancellation.

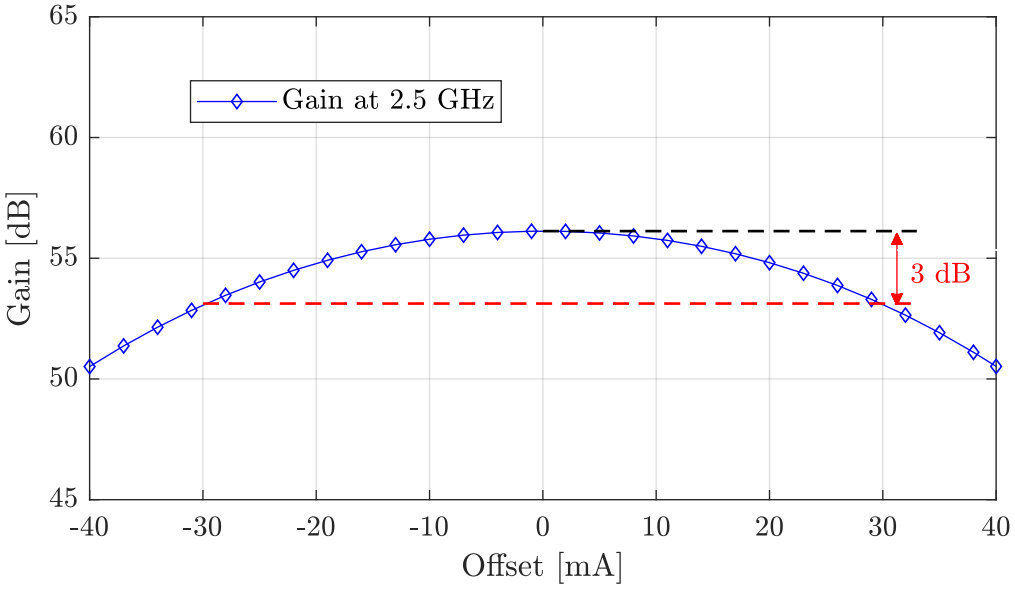


Figure 5.33: Four stage logarithmic amplifier with AC-coupled offset cancellation: Gain variation with input offset at 2.5 GHz input frequency.

Based on the implemented logarithmic amplifier, a power detector is realized as shown in Figure 5.34. The rectifiers and the input matching network utilized in this implementation are the same as the ones presented in 5.3.6 and 5.3.5, respectively. Parasitic-extracted post-layout simulation results of the detector output voltage and LCE are plotted in Figures 5.35 and 5.36, respectively.

The sensitivity of the detector with AC-coupled offset cancellation varies from a maximum of -56 dBm at 500 MHz to a minimum of -48.5 dBm at 3 GHz when considering a ±1 dB error range. The detector has a maximum dynamic range of 59 dB at 1 GHz and a minimum dynamic range of 46.5 at 3 GHz. The total power consumption of the detector is 43.692 mW. Parasitic-extracted post-layout simulation results of the power detector with AC-coupled offset cancellation are tabulated in Table 5.5.

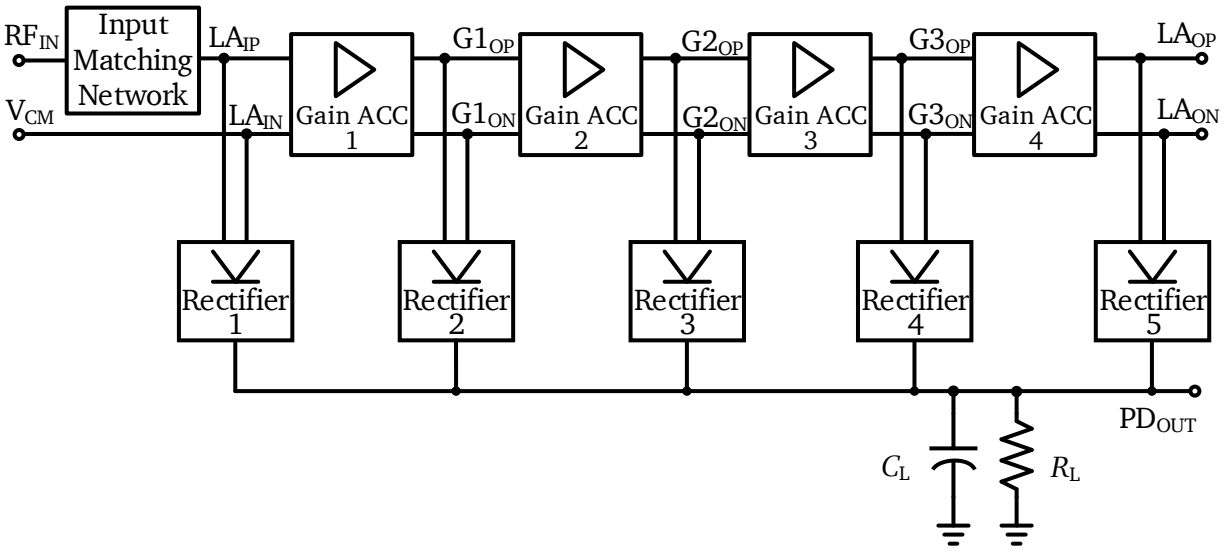


Figure 5.34: Block diagram of the SDLA power detector with AC-coupled offset cancellation.

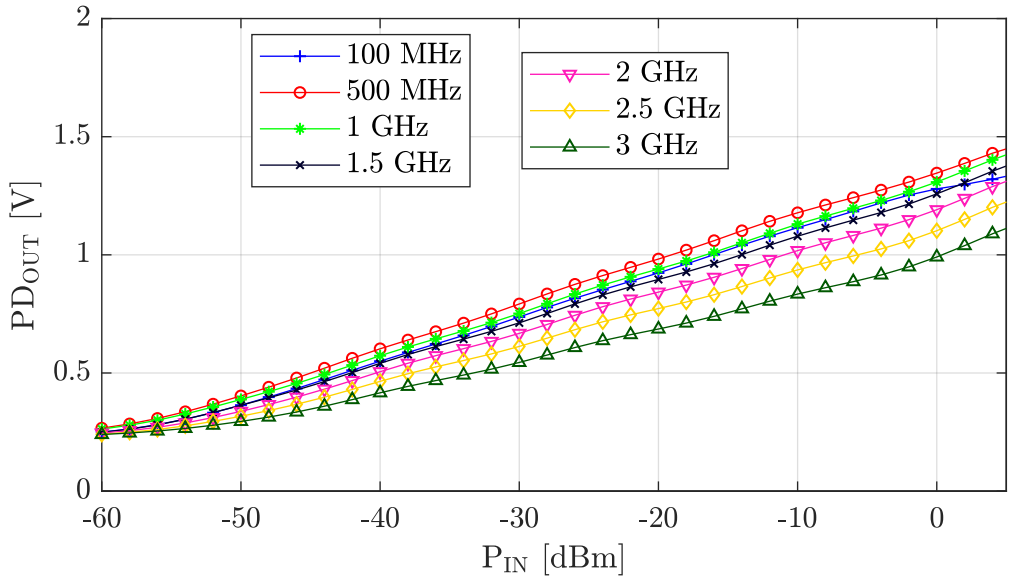


Figure 5.35: Output response of the SDLA power detector with AC-coupled offset cancellation.

Table 5.5: Parasitic-extracted post-layout simulation results of the power detector with AC-coupled offset cancellation for ±1 dB log-conformity error range.

Frequency [GHz]	Sensitivity [dBm]	Dynamic Range [dB]
0.1	-54	53
0.5	-56	52
1	-54	59
1.5	-54	56.5
2	-53	54
2.5	-50.5	50.5
3	-48.5	46.5

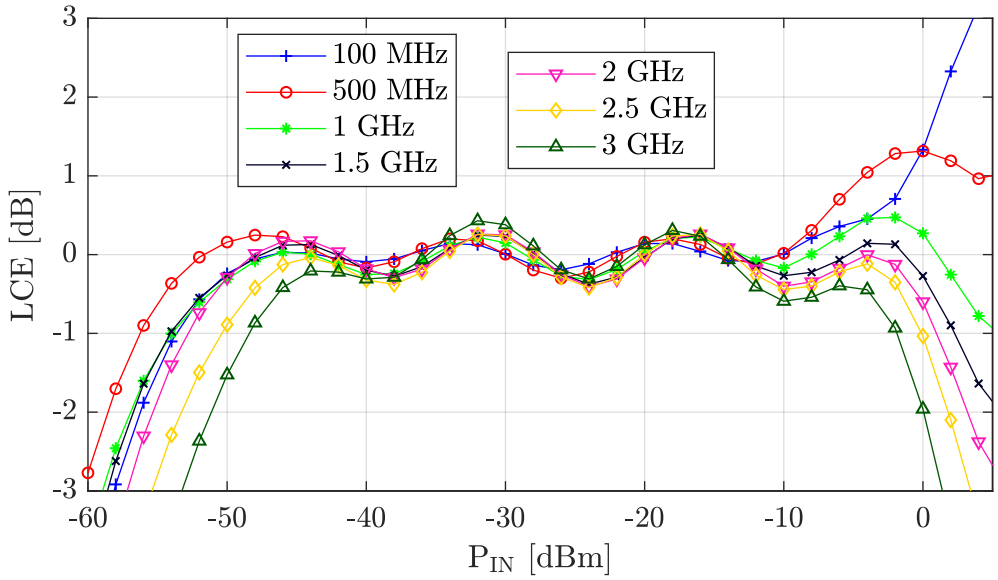


Figure 5.36: Log-conformity error of the SDLA power detector with AC-coupled offset cancellation.

Separate transient simulations are performed with noise contribution from selected sub-circuits alone turned on, in order to study the influence of noise generated from the individual sub-circuits. LCE plots based on these simulations for an input signal frequency of 2.5 GHz are shown in Figure 5.37. Figure 5.38 shows a magnified version of the results from the noise simulations, with a focus on the low input power region to visualize the effect of noise from sub-circuits on the sensitivity.

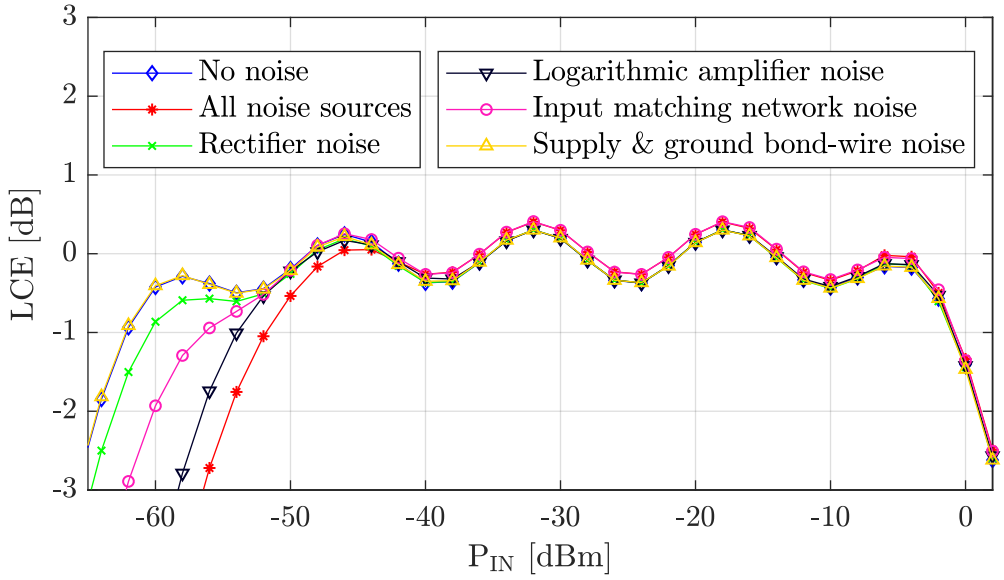


Figure 5.37: LCE plot at 2.5 GHz showing noise contributions of the SDLA power detector when AC-coupled offset cancellation circuitry is employed.

The addition of the AC-coupled offset cancellation circuit has reduced the range of frequencies at which the logarithmic amplifier provides amplification. As a result, noise sources such as flicker noise that originate below the lower cut-off frequency of the logarithmic amplifier get attenuated. At the same time, the AC-coupling circuit introduces noise and increases the high-frequency noise sources such as white noise. From the simulation results, it can be seen that there is, effectively, a reduction in overall pass-band noise and a slight improvement in the sensitivity of the power detector.

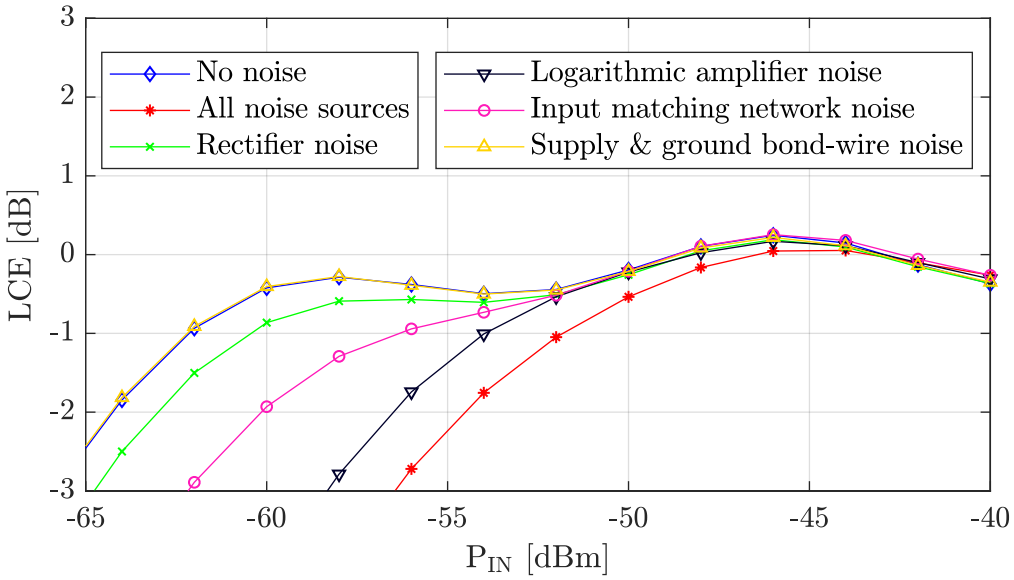
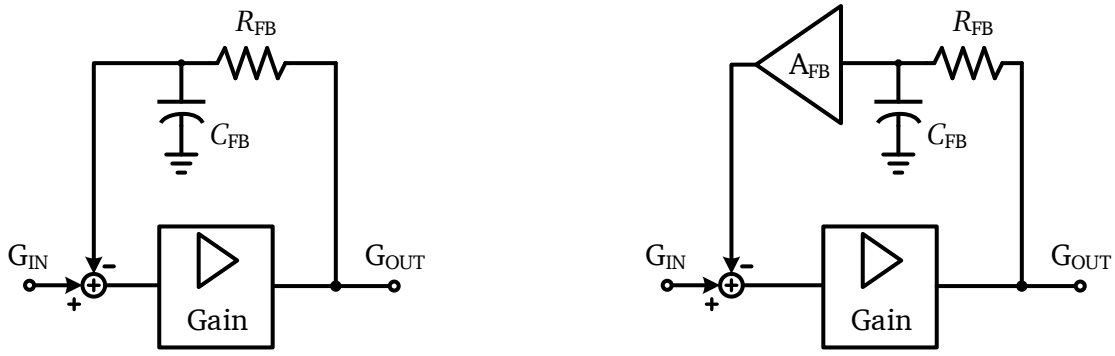


Figure 5.38: Magnified view of the LCE plot at 2.5 GHz showing noise contributions and their effect on the sensitivity of the SDLA power detector employing AC-coupled offset cancellation.

5.4.3 Power Detector Implementation with Feedback Offset Cancellation

As the name suggests, a DC feedback offset cancellation circuit employs a feedback loop for offset cancellation. The low-pass filtered output signal is fed back and subtracted at the input to cancel out the low-frequency signals. As a result, any DC offset at the output will be compensated for by the feedback loop.

The block diagram of an amplifier utilizing a feedback loop for offset cancellation is shown in Figure 5.39a. The resistor R_{FB} and the capacitor C_{FB} together constitute the low-pass filter in the feedback loop. A feedback amplifier can be added to increase the gain of the feedback path, as shown in Figure 5.39b. Any increase in the gain of the feedback path will increase the low-frequency attenuation of the amplifier employing the feedback path for offset cancellation and thereby helps in extending the offset cancellation range of the system [81, 82, 100]. A plot of the variation in the low-frequency gain-suppression of the system as the gain of the feedback amplifier increases is shown in Figure 5.40. The corresponding variation in the offset cancellation range of the system is depicted in Figure 5.41.



(a) Without amplification in the feedback path.

(b) With amplification in the feedback path.

Figure 5.39: Block diagram of an amplifier employing DC feedback offset cancellation (a) without amplification in the feedback path and (b) with amplification in the feedback path.

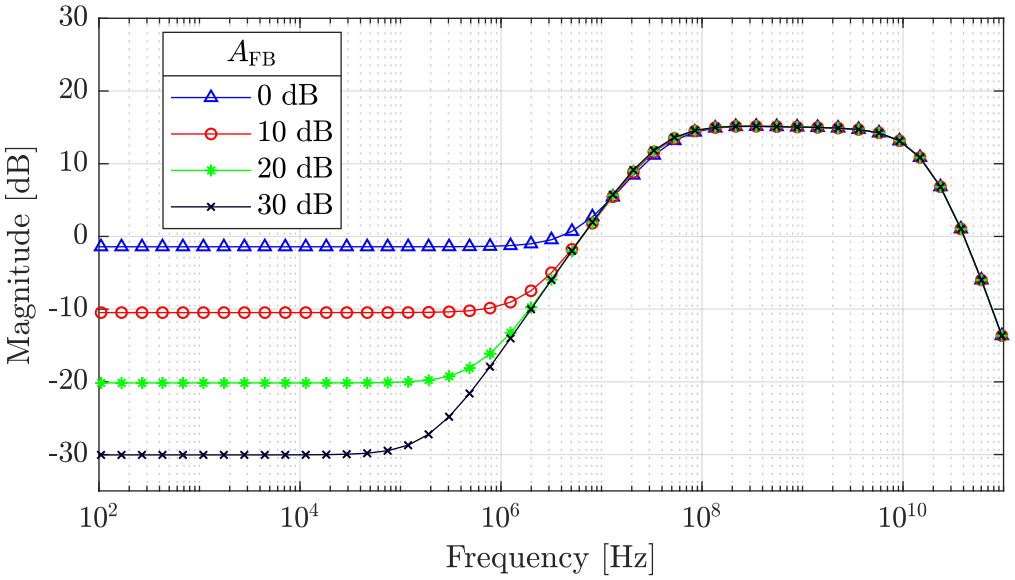


Figure 5.40: Dependence of low-frequency gain-suppression of the system on the gain of the feedback loop. A dominant-pole feedback amplifier is considered and its gain-bandwidth is kept constant at 1 MHz. A_{FB} is the low-frequency gain of the feedback amplifier.

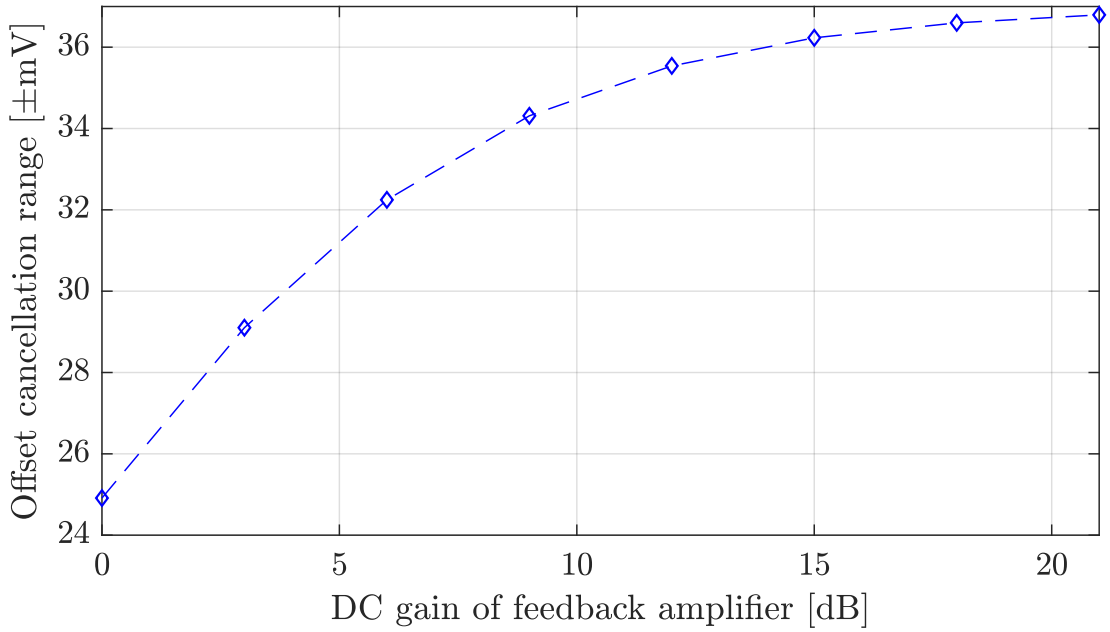


Figure 5.41: Dependence of offset cancellation range of the system on the gain of the feedback loop. A dominant-pole feedback amplifier model is considered and its gain-bandwidth is kept constant at 1 MHz.

Similar to the logarithmic amplifier with AC-coupled offset cancellation, an offset cancellation range larger than ± 30 mV is specified for the logarithmic amplifier that is to be designed using feedback offset cancellation. The modified Cherry-Hooper circuit and the buffer circuits to be used for the logarithmic amplifier remain the same as the ones presented in Section 5.3.4.1.

Due to the high gain of the open-loop cascade of limiting gain stages, and the high offset cancellation range needed, the requirements on the feedback loop are extremely high. A single feedback loop based

approach requires a very large feedback capacitance, which will have to be realized off-chip, to maintain the lower cut-off frequency sufficiently small. To avoid off-chip capacitors, multiple feedback loops can be used as reported in [101–103].

A dual feedback loop based approach is utilized for the logarithmic amplifier under consideration. One feedback loop is added around the first two amplifiers, and a second feedback loop is added around the third and the fourth amplifiers. The first and the third limiting gain stages of the logarithmic amplifier are modified to include an additional source-coupled differential pair for offset subtraction, as depicted in Figure 5.42 [116]. The feedback amplifiers are designed as simple differential pairs, as shown in Figure 5.43. The logarithmic amplifier employing this dual feedback loop approach is shown in Figure 5.44.

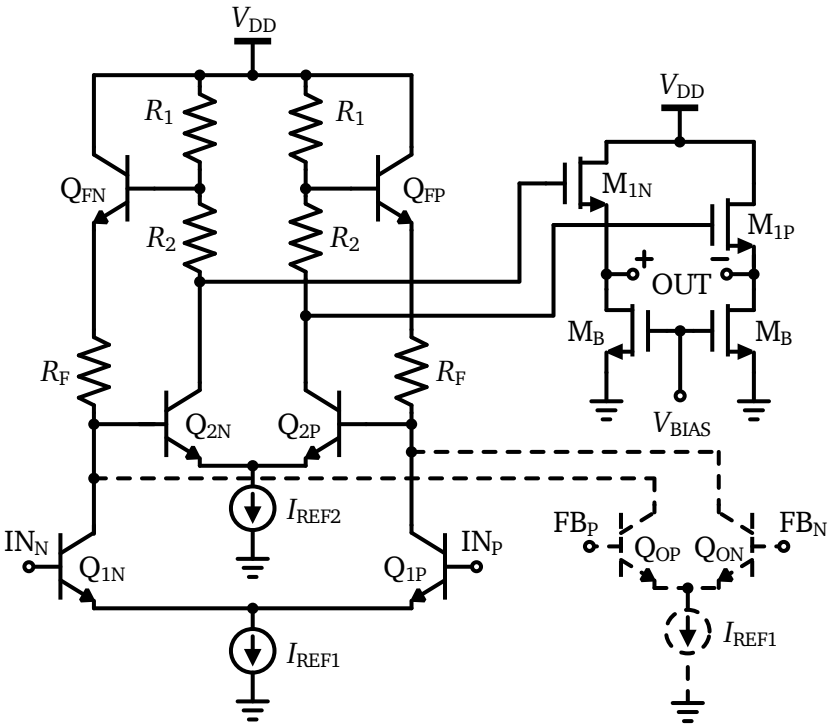


Figure 5.42: Schematic of the limiting gain cell with offset subtractor [116].

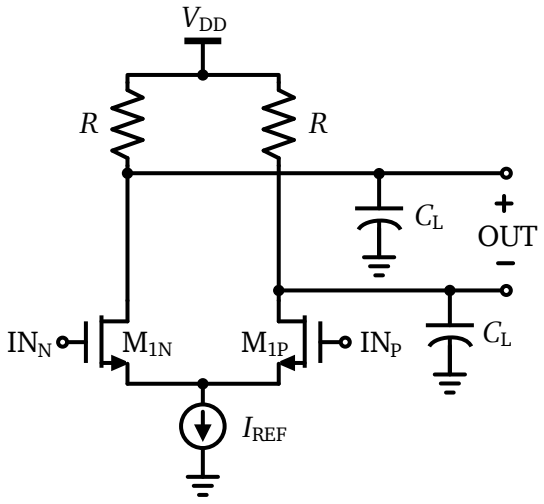


Figure 5.43: Schematic of the feedback amplifier for DC feedback offset cancellation.

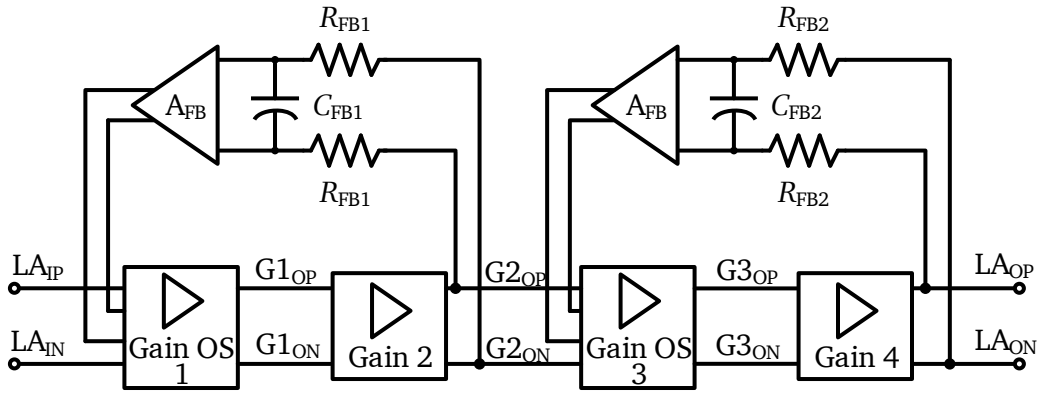


Figure 5.44: Logarithmic amplifier with dual feedback loop offset cancellation.

The pole-frequencies of the amplifier and the low-pass filter in the feedback loop need to be far away from each other to ensure a dominant-pole characteristic for the feedback loop. The lack of a dominant-pole response will lead to a large peak in the frequency response of the overall system and could lead to stability issues. In this design, the poles of the feedback amplifier and the low-pass RC filter are kept sufficiently separated. Due to the large area requirements of the load capacitor C_L that is used to reduce the pole frequency of the feedback amplifier, some peaking is allowed. Nonetheless, it is ensured that the peaking does not affect the flatness of the magnitude response of the system considerably. The lower frequency at which the logarithmic amplifier crosses unity-gain is designed to be 1 MHz. Additionally, the loop is designed to have a phase margin larger than 40 deg to ensure loop stability. The plots for the frequency response of the logarithmic amplifier and the loop gain of the feedback loop are shown in Figures 5.45 and 5.46, respectively. Parasitic-extracted post-layout simulation results of the

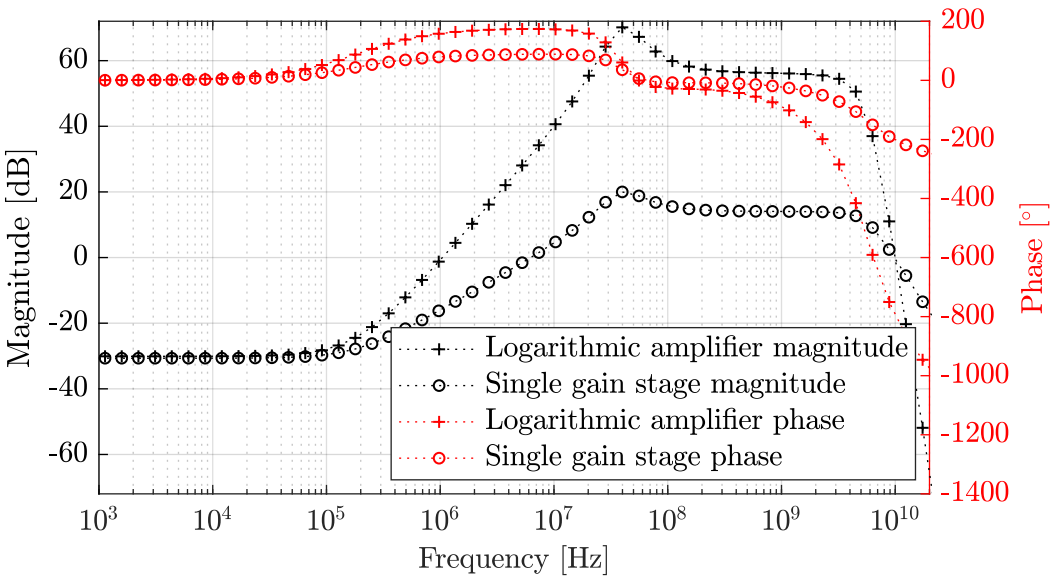


Figure 5.45: AC response of the limiting gain cell and the logarithmic amplifier with dual feedback loop offset cancellation.

logarithmic amplifier with dual feedback loop offset cancellation are summarized in Table 5.6. For these simulations, the logarithmic amplifier is loaded with a dummy gain stage, and the individual gain stage outputs are loaded with rectifiers to imitate the real loading conditions when used in an SDLA power detector. The total DC power consumption of this logarithmic amplifier, including its bias circuitry and dummy gain stage is 38.76 mW.

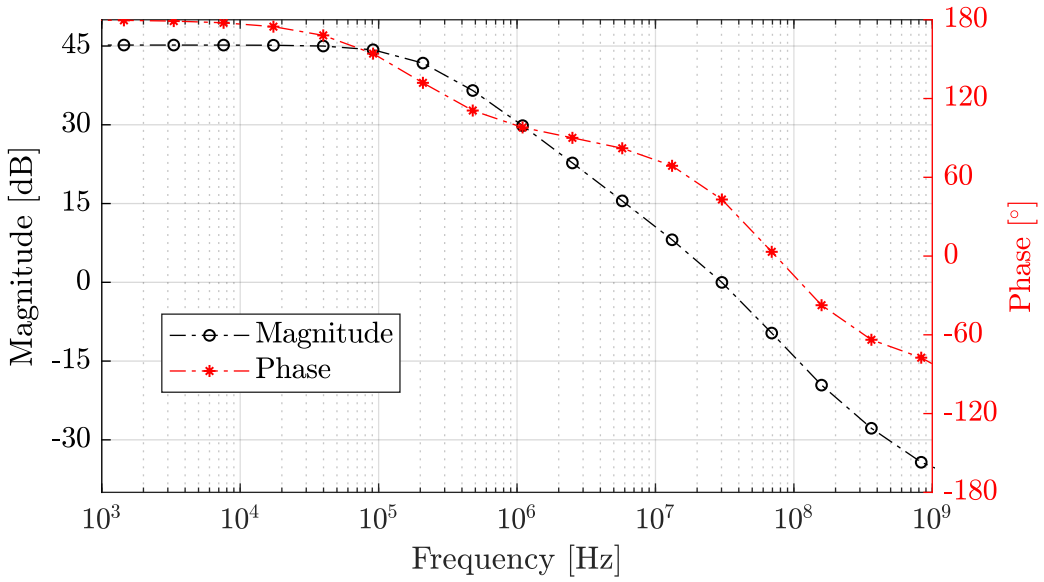


Figure 5.46: Loop response of a single DC feedback offset cancellation loop.

Table 5.6: Parasitic-extracted post-layout simulation results of the four-stage logarithmic amplifier with dual DC feedback loop offset cancellation.

Parameter	Value	Unit
Maximum gain between 500 MHz and 2.5 GHz (A_{LogA})	56.4	dB
3dB frequency (f_{LogA})	3.567	GHz
Unity-gain frequency (low/high) (f_{ULogA})	0.001 / 9.99	GHz
Input-referred noise at 1 GHz	4.678	$\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$
Integrated input-referred noise in pass-band	646.4	µV
DC power consumption	38.76	mW

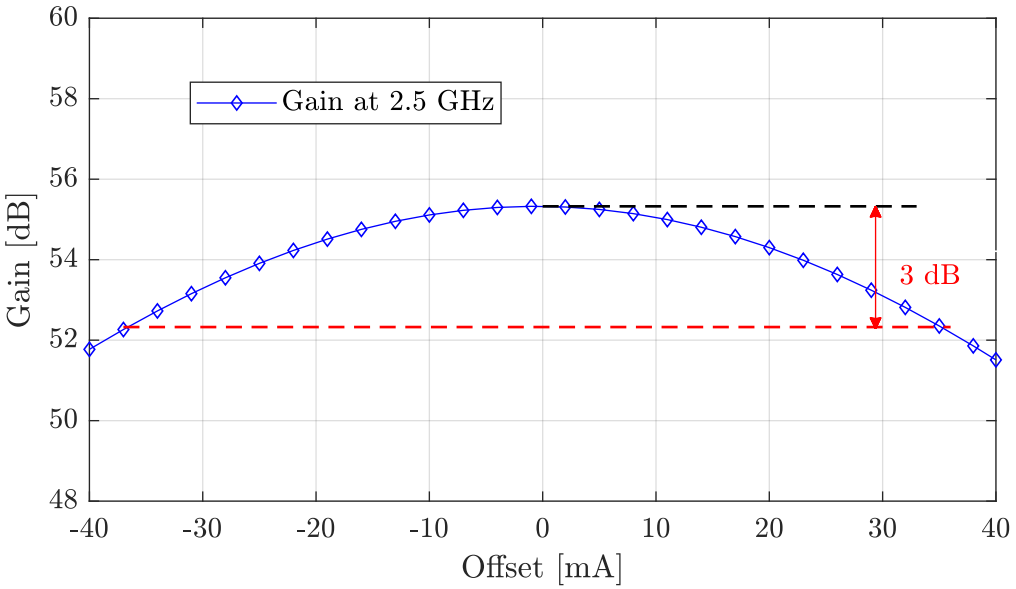


Figure 5.47: Four stage logarithmic amplifier with dual DC feedback offset cancellation: Gain variation with input offset at 2.5 GHz input frequency.

Based on the implemented logarithmic amplifier, a power detector is realized as shown in Figure 5.48 [116]. The rectifiers and the input matching network utilized in this implementation are the same as the ones presented in Sections 5.3.6 and 5.3.5, respectively. Parasitic-extracted post-layout simulation results of the detector output voltage and LCE are plotted in Figures 5.49 and 5.50, respectively.

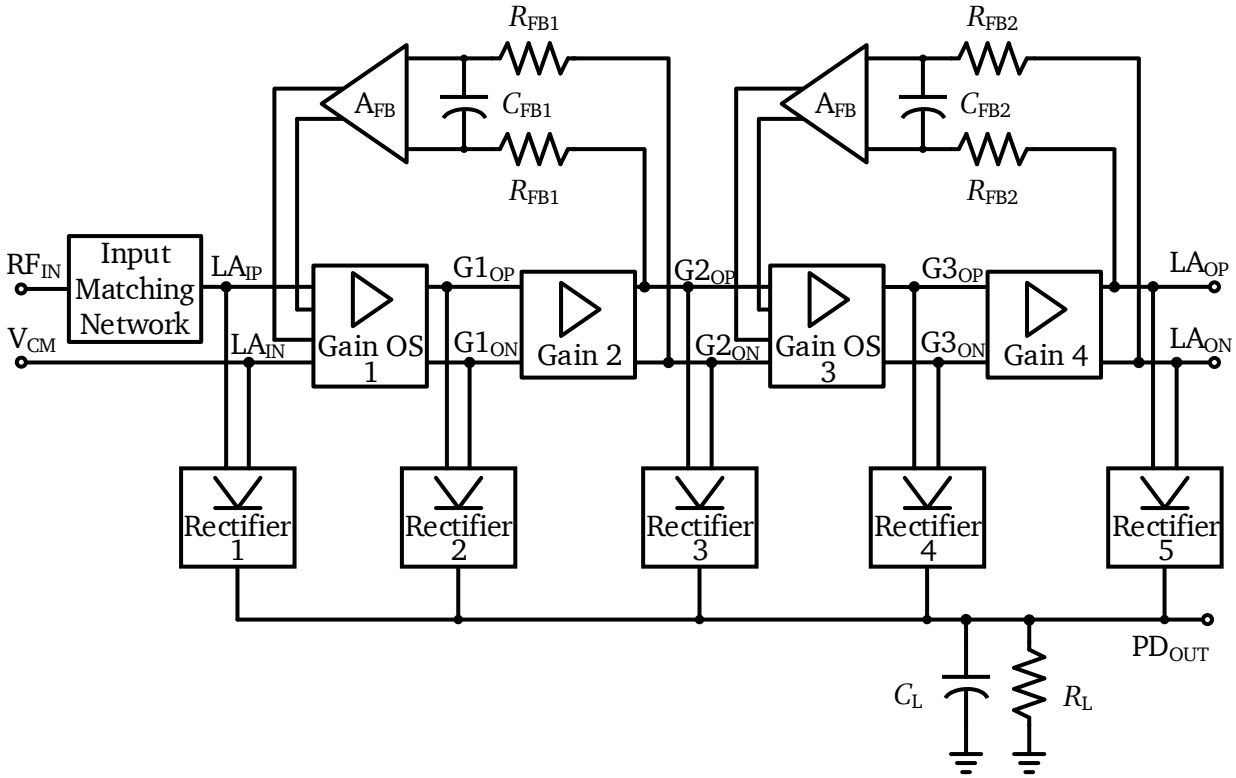


Figure 5.48: Block diagram of the power detector with dual DC feedback offset cancellation [116].

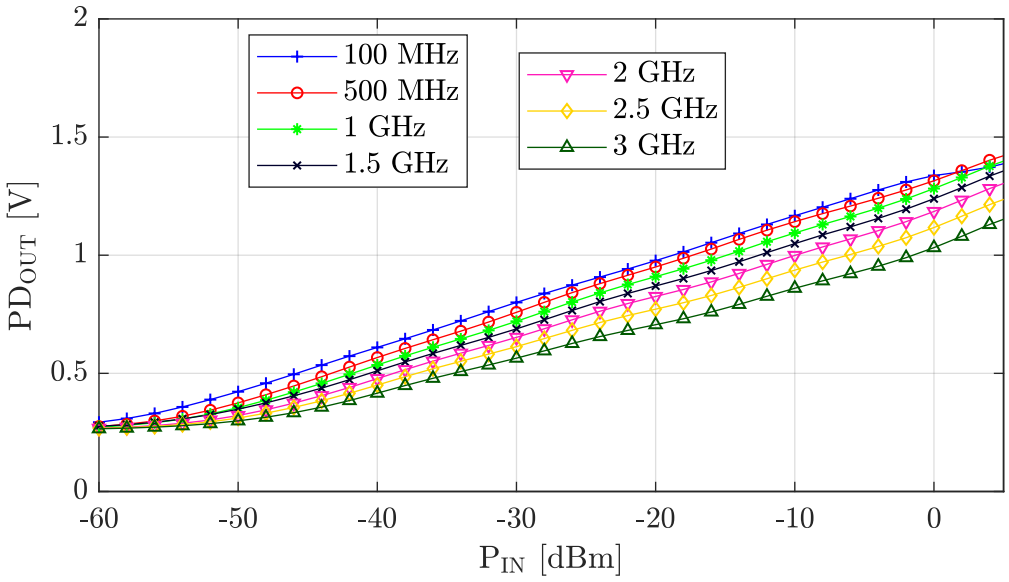


Figure 5.49: Output response of the SDLA power detector with dual DC feedback offset cancellation [116].

The sensitivity of the detector with dual feedback offset cancellation varies from a maximum of -57 dBm at 100 MHz to a minimum of -48 dBm at 3 GHz when considering a ±1 dB error range. The detector

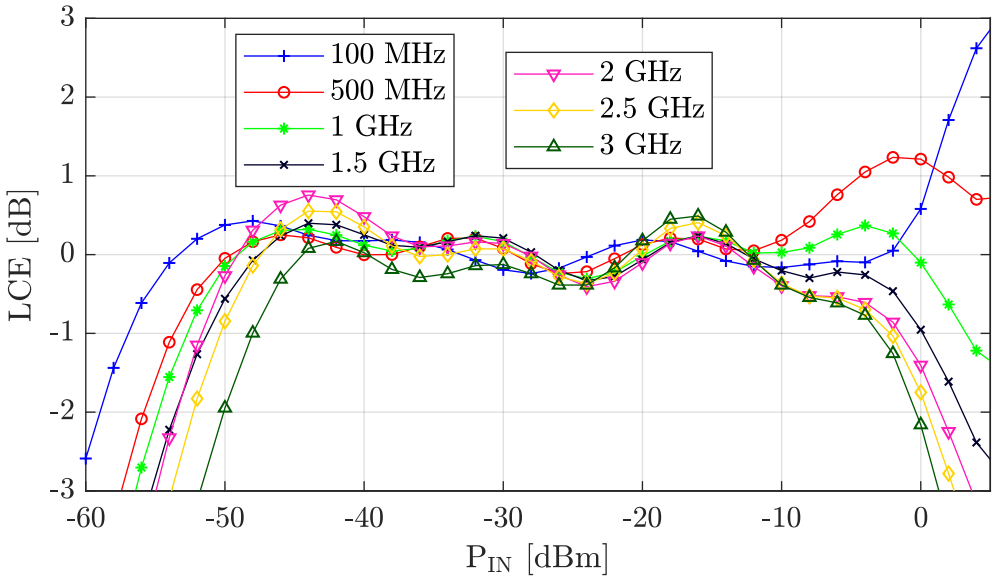


Figure 5.50: Log-conformity error of the SDLA power detector with dual DC feedback offset cancellation [116].

has a maximum dynamic range of 57.5 dB at 100 MHz and a minimum dynamic range of 45 at 3 GHz. The total power consumption of the detector is 42.405 mW. Parasitic-extracted post-layout simulation results of the power detector with dual DC feedback loop based offset cancellation are tabulated in Table 5.7.

Table 5.7: Parasitic-extracted post-layout simulation results of the power detector with dual DC feedback loop based offset cancellation for ±1 dB log-conformity error range.

Frequency [GHz]	Sensitivity [dBm]	Dynamic Range [dB]
0.1	-57	57.5
0.5	-54	50
1	-53	56.5
1.5	-51.5	51.5
2	-51.5	50
2.5	-50	48
3	-48	45

Separate transient simulations are performed with noise contribution from selected sub-circuits alone turned on, in order to study the influence of noise generated from the individual sub-circuits. LCE plots based on these simulations are shown in Figure 5.51 for an input signal frequency of 2.5 GHz. Figure 5.52 shows a magnified version of the results from the noise simulations, with a focus on the low input power region to better visualize the effect of noise from sub-circuits on the sensitivity.

The noise sources, such as flicker noise, that are significant below the lower cut-off frequency of the logarithmic amplifier get attenuated because of the low-frequency gain-suppression due to the offset cancellation circuit. At the same time, the feedback loop introduces noise in the pass-band frequencies.

Simulation results show that the dual feedback offset cancellation mechanism provides slightly lower performance than the AC-coupled offset cancellation mechanism for a similar offset cancellation range and power consumption. Considering the performance at the center frequency of interest of 1.5 GHz,

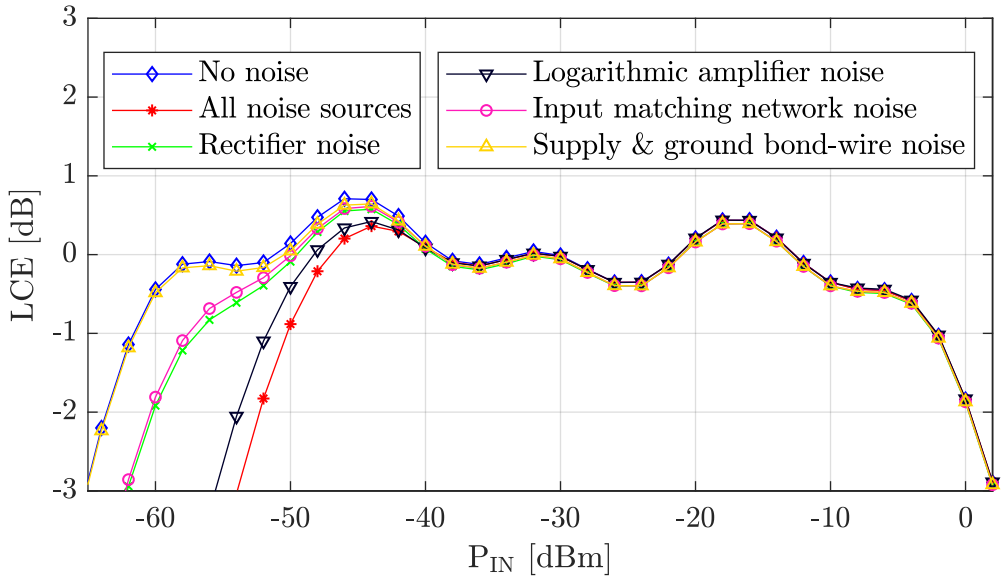


Figure 5.51: LCE plot showing noise contributions of the SDLA power detector when dual DC feedback offset cancellation circuitry is employed [116].

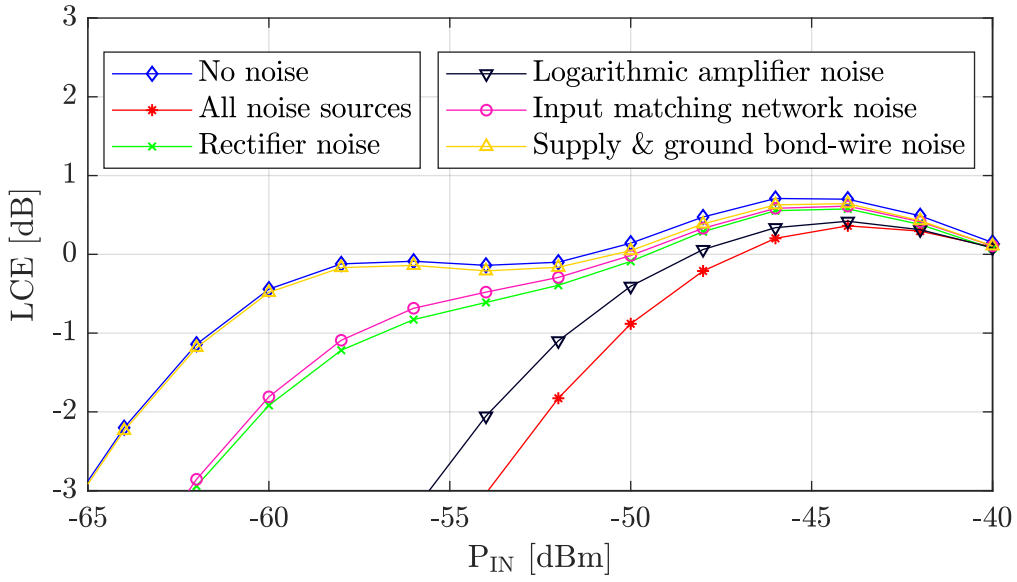


Figure 5.52: Magnified view of the LCE plot showing noise contributions and their effect on the sensitivity of the SDLA power detector when dual DC feedback offset cancellation circuitry is employed.

the sensitivity of the detector is -51.5 dBm when employing dual feedback loop based offset cancellation, compared to -54 dBm when employing AC-coupled offset cancellation. The drop in performance is due to the fact that the noise introduced by the feedback amplifier that is added to achieve the necessary offset cancellation range is higher than the noise introduced by the AC-coupling network. The AC-coupled offset cancellation approach is also more robust considering its non-reliance on a feedback mechanism, making it more attractive for the power detector under consideration.

The next section presents the implementation and measurement results of a prototype power detector realized based on the observations presented so far in this chapter.

5.5 Prototype Power Detector and Measurement Results

The analysis presented in the previous section has been shown that the sensitivity is higher when employing an AC-coupled offset cancellation mechanism for the detector under consideration. As such, AC-coupling is used to fine-tune the performance of the detector.

Results summarized in Tables 5.2 and 5.4 showed that the pass-band gain of the logarithmic amplifier employing the AC-coupled offset cancellation mechanism dropped by around 2 dB compared to the implementation without any offset cancellation circuitry. To overcome this drop in gain, the limiting gain stages are redesigned. The design is also optimized to provide lower input-referred noise for the limiting gain stages. The increase in gain and the reduction in noise come at an acceptable deviation from the maximally flat characteristic. The pole locations are modified to allow slight peaking within the pass-band frequencies. This peaking helps in maintaining a high bandwidth for the limiting gain stage when the improvements in the gain and noise performance are undertaken.

The gain plots of a single limiting gain stage and the logarithmic amplifier are displayed in Figure 5.53. A single limiting gain stage has a limiting voltage of 400 mV and provides a gain of 17.46 dB at 0.5 GHz and 17.86 dB at 2.5 GHz. The maximum gain is 18.23 dB at 3.61 GHz. The lower 3dB frequency is 63.7 MHz, whereas the upper 3dB frequency is 5.08 GHz. The logarithmic amplifier provides a gain of 69.6 dB at 500 MHz, 71.3 dB at 2.5 GHz, and a maximum gain of 72.7 dB at 3.61 GHz. It has a lower 3dB frequency of 269.5 MHz and an upper 3dB frequency of 4.41 GHz. Parasitic-extracted post-layout simulation results of the optimized logarithmic amplifier design used for prototyping are summarized in Table 5.8.

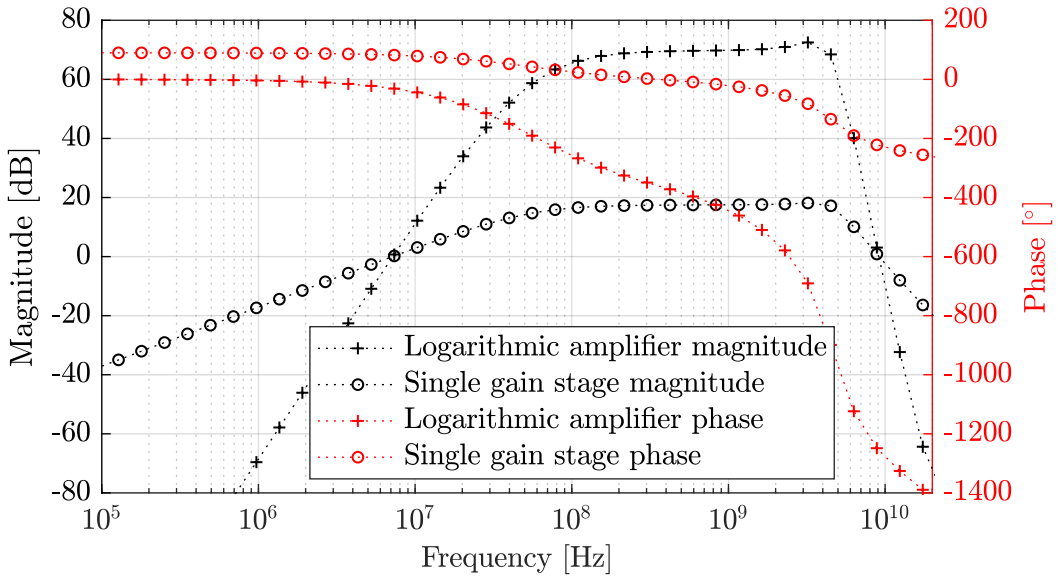


Figure 5.53: AC response of the limiting gain cell and the logarithmic amplifier used for prototyping.

Figure 5.54 shows the gain variation with input offset at 2.5 GHz for the logarithmic amplifier used for prototyping. It can be observed that the circuit provides a gain that is within a -3dB threshold compared to the maximum gain of 71.3 dB for input offsets from -40 mV to +40 mV, which corresponds to an offset cancellation range of ± 40 mV.

The single-ended to differential conversion of the power detector is performed off-chip and the on-chip input matching network is designed for fully-differential operation, as shown in Figure 5.55 [112]. The block diagram of the fabricated power detector is shown in Figure 5.56 [112].

Table 5.8: Parasitic-extracted post-layout simulation results of the four-stage logarithmic amplifier with AC-coupled offset cancellation used for fabrication.

Parameter	Value	Unit
Maximum gain between 500 MHz and 2.5 GHz (A_{LogA})	71.3	dB
3dB frequency (f_{LogA})	4.4	GHz
Unity-gain frequency (low/high) (f_{ULogA})	0.0072 / 9.12	GHz
Input-referred noise at 1 GHz	4.17	$\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$
Integrated input-referred noise in pass-band	823	µV
DC power consumption	21.8	mW

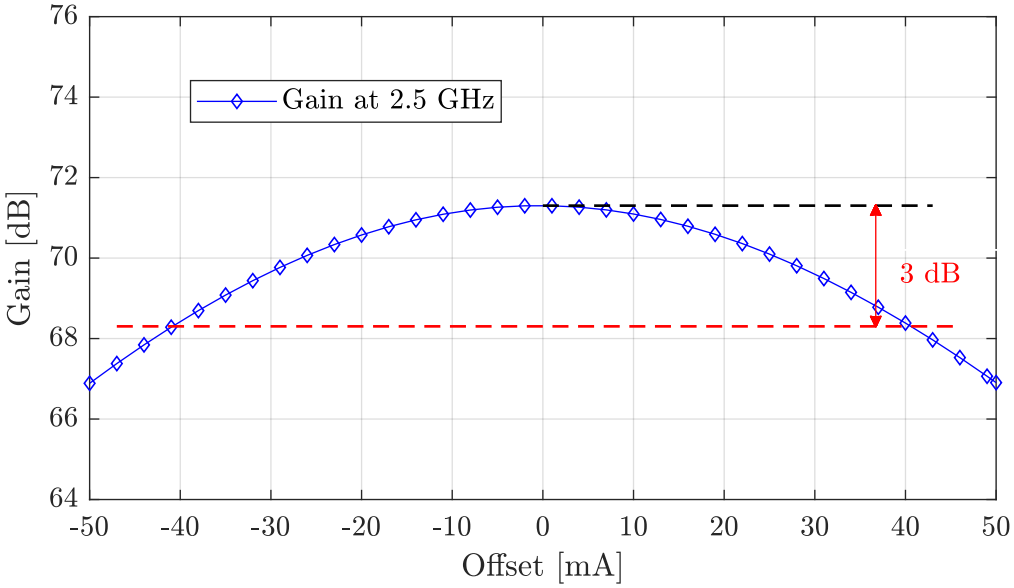


Figure 5.54: Four stage logarithmic amplifier used for prototyping: Gain variation with input offset at 2.5 GHz input frequency.

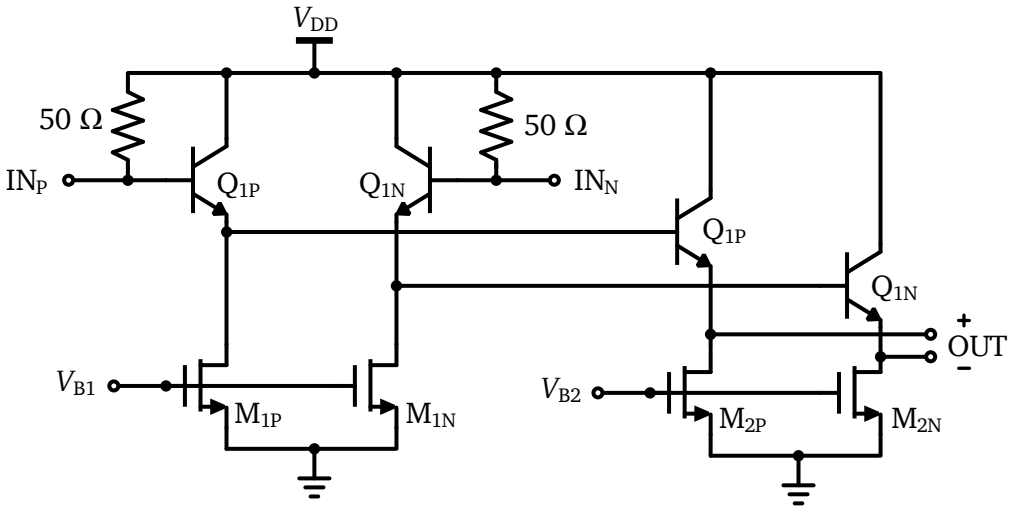


Figure 5.55: Schematic of the fully differential input matching network used for fabrication [112].

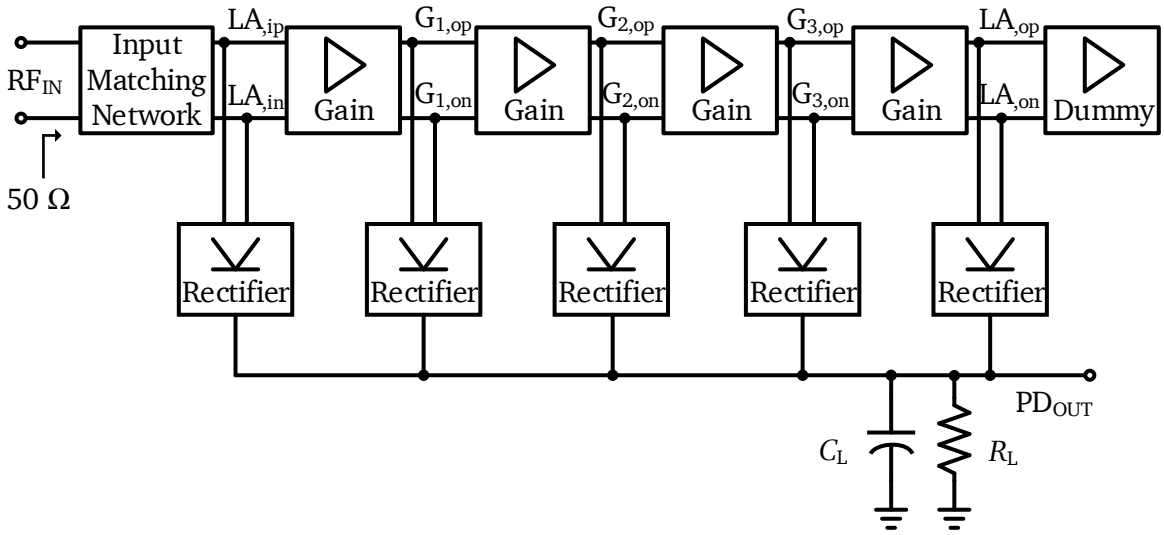


Figure 5.56: Block diagram of the prototype power detector [112].

The implemented power detector is incorporated within an RF transceiver ASIC chip that is packaged using a quad flat no-lead (QFN) 9mm x 9mm 64 pin package, and the packaged chip is mounted on a test printed circuit board (PCB) for measurement purposes [112].

5.5.1 Measurement Results

Measurement results of the detector output voltage are plotted for varying input powers in Figure 5.57, and the corresponding log-conformity error plots are shown in Figure 5.58. The detector has an input signal detection range of -56 dBm to 8 dBm at its 1.5 GHz center frequency, which corresponds to a dynamic range of 64 dB. Within this input signal range, the error is within ± 1 dB compared to an ideal linear-in-dB response. The sensitivity varies from -58 dBm at 500 MHz to -50.5 dB at 2.5 GHz, whereas the dynamic range varies from 64.5 db at 500 MHz to 60 dB at 2.5 GHz.

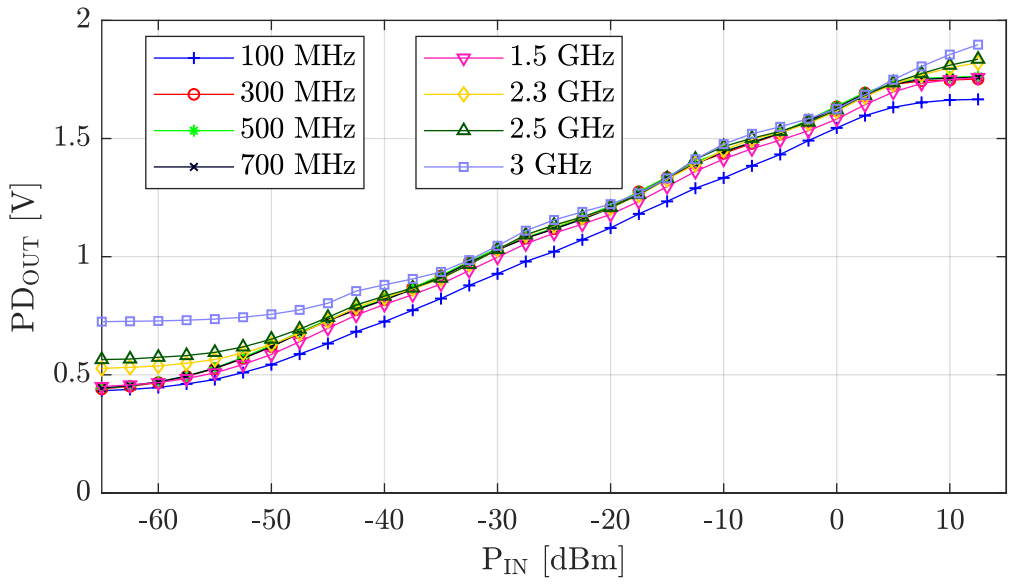


Figure 5.57: Measurement results for detector output-voltage [112].

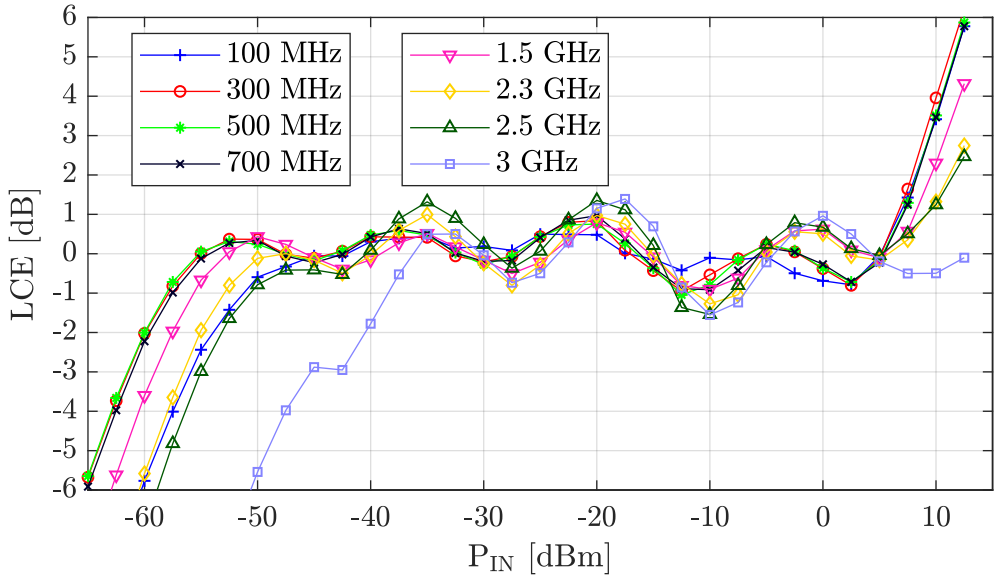


Figure 5.58: Measurement results for log-conformity error [112].

The input return loss of the prototype power detector is plotted in Figure 5.59. The detector provides a return loss larger than 7 dB across the bandwidth of 500 MHz to 2.5 GHz. The power detector has a power consumption of 9.91 mA from a 3.3 V supply and occupies 0.064 mm^2 in area.

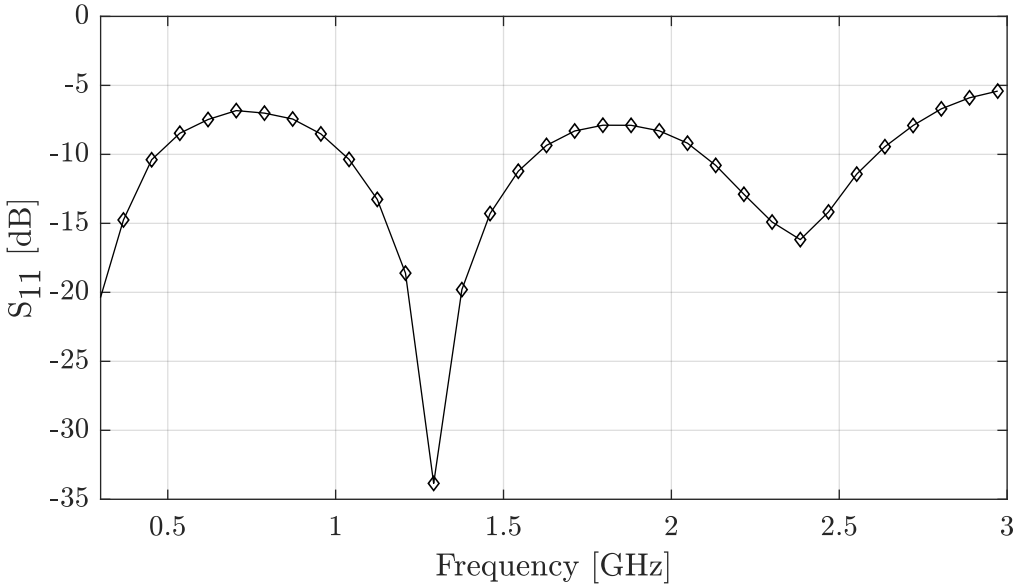


Figure 5.59: Measurement results for input matching performance.

The measurement results are summarized and compared to other state-of-the-art logarithmic power detectors in Table 5.9. Compared to other silicon based state-of-the-art logarithmic wideband power detectors with large dynamic range, the proposed detector achieves the highest sensitivity when considering a ± 1 dB error range. The high sensitivity, large dynamic range and wideband characteristic make power detector suitable for integration in a wide variety of applications.

Table 5.9: Performance comparison of the fabricated power detector with other state-of-the-art logarithmic power detectors [112]

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	Process	DC Power [mW]	Supply [V]	Operating Freq. [GHz]	Sensitivity [dBm]	Dynamic Range [dB]	LCE [dB]	Area [mm^2]
This Work	SiGe BiCMOS	32.72	3.3	0.3 - 3	-58 (0.5 GHz) -56 (1.5 GHz) -50.5 (2.5 GHz)	64 (0.5 GHz) 64 (1.5 GHz) 60 (2.5 GHz)	± 1	0.064 (core)
MTTT 2016 [104]	28 nm CMOS	5.8-11.8	1.8	0.7 - 4	-35 (@ 1.9 GHz; PS mode 3) $^{+}$	40	± 0.8	0.15 (core)
ISCAS 2015 [105]	180 nm CMOS	0.55	3.3	0.3 - 10	-12 *	42 *	± 1 *	0.113 (core)
MWCL 2013 [106]	130 nm CMOS	35.2	2	up to 16	-35	43 (up to 14 GHz)	± 1	0.75 (die)
MTT 2011 [107]	180 nm CMOS	70	2.8	up to 8	-54 (3.6 GHz) -39 (8 GHz)	53 (3.6 GHz) 40 (8 GHz)	± 1	0.98 (die)
JSSC 2009 [108]	180 nm CMOS	10.8	1.8	3.1 - 10.6	-40	20	± 2.4	0.36 (core)
APMC 2009 [109]	180 nm CMOS	16	1.8	0.9 - 1.8	-43 (0.9 GHz)	39 (0.9 GHz) 29 (1.8 GHz)	± 1	0.479 (die)
ISCAS 2007 [59]	180 nm CMOS	8	1.8	3 - 10	-54 $^{*+}$	40 *	± 3 *	0.25 (core)
ISCAS 2006 [56]	SiGe BiCMOS	17	2.5	up to 6	-45 *	40 *	± 1 *	n.r

n.r - not reported * Simulation result $^{+}$ Calculated from graph

5.6 Summary

This chapter focused on the sensitivity-aware design and implementation of a wideband large dynamic range peak power detector suitable for system-on-chip integration as part of RF transceiver front-ends.

Initially, the approaches for the design of a power detector without any in-built offset cancellation mechanism for high sensitivity, large dynamic range and high bandwidth was presented. The detector was realized using a successive-detection logarithmic amplifier architecture consisting of four limiting gain stages, five rectifiers and an input matching network. The limiting gain stages were realized using a modified Cherry-Hooper amplifier topology employing SiGe HBTs to achieve high gain-bandwidth product. The rectifier was realized using a balanced source-coupled pair topology and the input matching network was realized using an active architecture.

Next, two of the frequently used offset cancellation approaches, namely the AC-coupled offset cancellation approach and the DC feedback offset cancellation approach, were implemented and analyzed for their suitability to the detector implementation. Comparative results showed that the AC-coupling offset cancellation approach provided better performance for the detector under consideration.

Finally, a successive detection logarithmic amplifier based power detector employing AC-coupled offset cancellation was implemented on a SiGe BiCMOS technology and fabricated. The prototype detector achieves a sensitivity of -56 dBm and a dynamic range of 64 dBm at 1.5 GHz center frequency for an error range of ± 1 dB. It consumes 32.72 mW power from a 3.3 V supply and the core area, excluding pads, is 0.064 mm^2. A comparison with other state-of-the-art publications achieving similarly large dynamic range and bandwidth shows that the realized power detector achieves a higher sensitivity at the expense of

relatively little power consumption and area compared to the other existing published works. This makes the power detector suitable for integration in a wide variety of applications. The results presented also demonstrate the feasibility and attractiveness of employing SiGe HBTs for high sensitivity, large dynamic range wideband power detectors.

6 System Implementation: Wideband Digitally Controllable RF Transceiver Front-End

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The previous three chapters dealt with three different aspects concerning the system-on-chip implementation of digitally controllable RF transceiver front-ends. This chapter presents the implementation of an RF transceiver front-end, referred to as RFFE, that employs the implementations presented in those chapters.

The chapter is structured as follows: an overview of the RFFE is presented in Section 6.1. An application example of the RFFE as part of an RFIC system is presented in Section 6.2. The measurement results of the RFFE are provided in Section 6.3, and a summary of the chapter is presented in Section 6.4. Parts of this chapter have been published as a research paper in [111].

6.1 Overview of the RF Front-end (RFFE)

The RFFE consists of coarse attenuator, LNA, gain slope equalizer, fine attenuator, and PA blocks along with a power detector and an on-chip digital controller. Figure 6.1 shows the block diagram of the RFFE.

The coarse attenuator and the fine attenuator circuits presented in Chapter 3 have been utilized to achieve digital gain control. The coarse attenuator is placed at the input of the RFFE and helps in reducing the linearity requirements of the LNA. Consindering the situation when the input to the RFFE is 0 dBm, the LNA will see an input power of 0 dBm if placed directly at the input of the RFFE. To avoid operation in the compression region of the power characteristic curve, the input P1dB compression point of the LNA will have to be higher than 0 dBm, which would increase the power consumption requirements of the LNA. The presence of the coarse attenuator at the input makes it possible to provide an attenuation of 8 dB, 16 dB or 24 dB to the input signal, and thereby reduce the input power seen by the LNA to below its input compression point. Additionally, the attenuator circuit has the characteristic of attenuating any noise at the input, and the noise figure of an attenuator is the same as its attenuation level. As a result, placing the coarse attenuator at the input, instead of the LNA, does not degrade the noise figure of the RFFE.

The LNA provides a gain larger than 14 dB and has a noise figure lower than 3.7 dB. The low noise figure and the high gain that it provides help in maintaining the overall noise figure of the system below 7.5 dB. The gain slope equalizer presented in Chapter 4 is placed after the LNA to facilitate digital gain slope equalization. The fine attenuator is placed after the gain slope equalizer and is followed by the

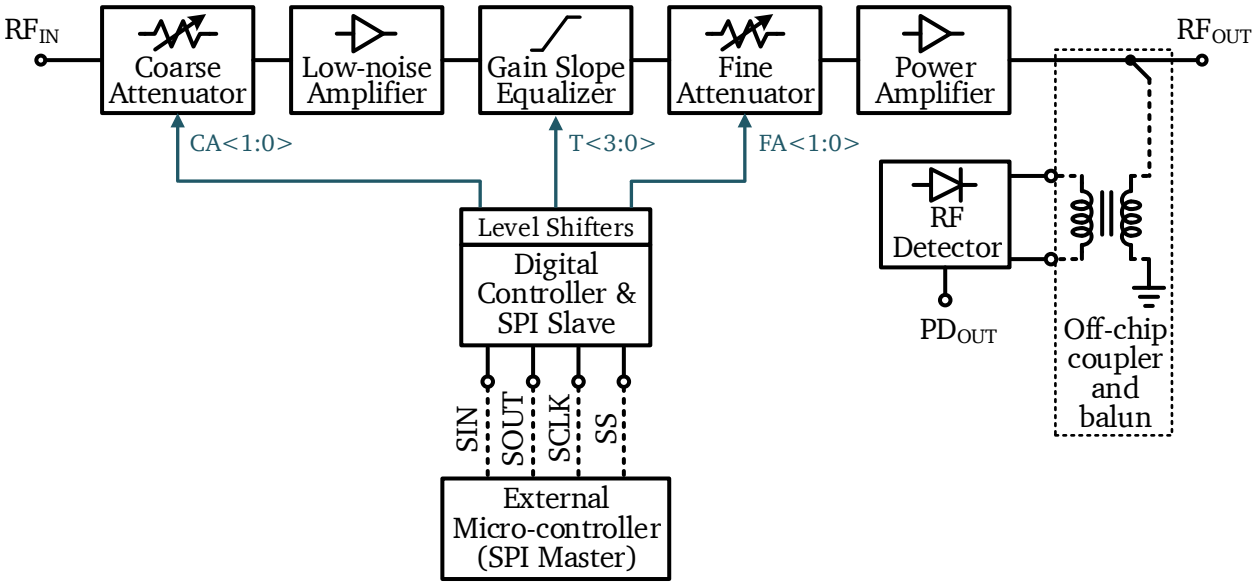


Figure 6.1: Block Diagram of the radio frequency front-end (RFFE).

power amplifier at the output. The PA provides a gain larger than 14 dB and an output power larger than 5 dBm. The power detector implemented in Chapter 5 is employed for power detection.

The next section briefly introduces the LNA and PA that are part of the system.

6.1.1 Wideband RF Low-Noise Amplifier

The schematic diagram of the implemented LNA is shown in Figure 6.2.

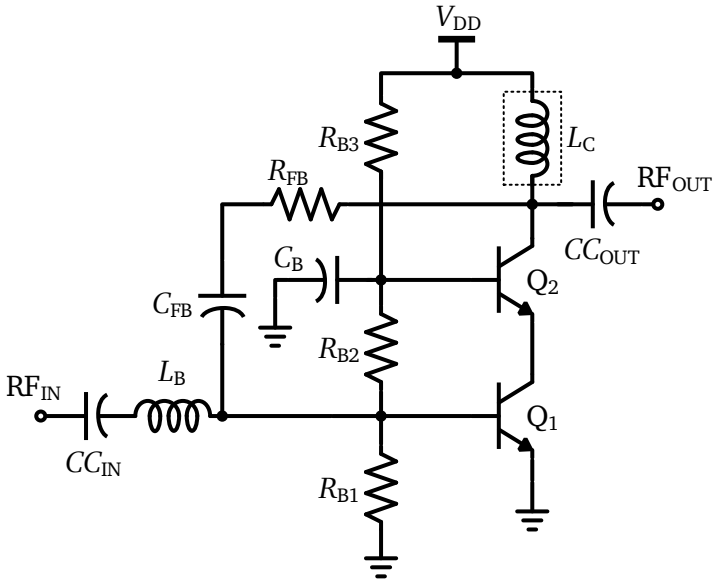
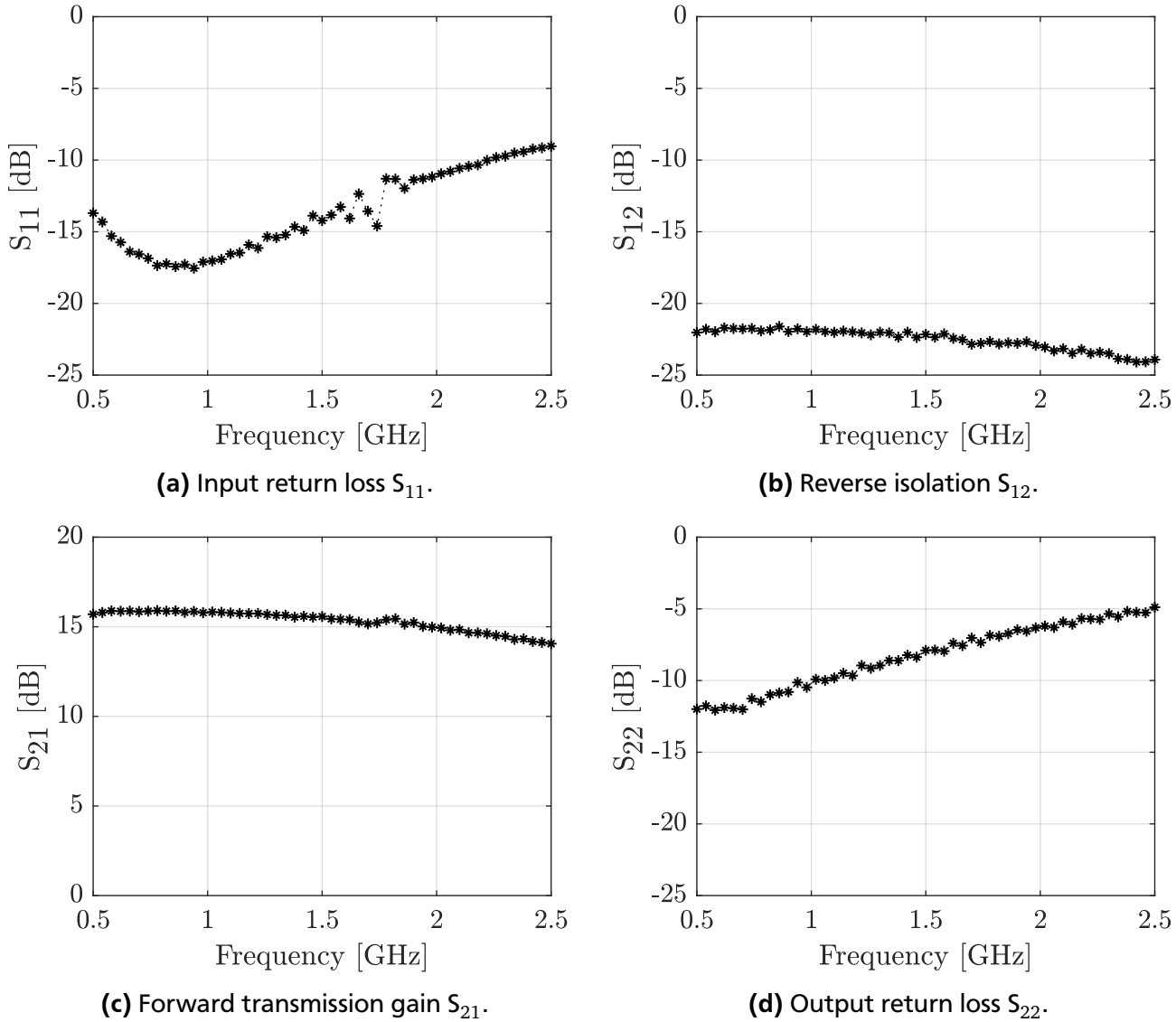


Figure 6.2: Schematic of the implemented low-noise amplifier.

The LNA utilizes a cascode configuration of high-performance SiGe HBTs to provide the required amplification. Passive input matching networks are used to provide good impedance matching performance for the LNA. At the input, a DC blocking capacitor is used to isolate the DC bias point of the circuit from

the DC of the output of the coarse attenuator. An on-chip inductor is used to compensate the capacitive contribution of the large transistor Q_1, and thereby bring the imaginary part of the impedance seen from the input closer to the zero. The implementation incorporates a compromise with respect to the design of transistor Q_1 for maximum gain, minimum noise figure, and optimal input impedance matching. The cascode transistor helps in minimizing the miller capacitance of the transistor and in improving the wideband performance. The shunt feedback resistor R_{FB} is employed to improve the gain flatness of the amplifier. Additionally, it influences the input and the output matching of the LNA. The capacitor C_{FB} is added to block any DC current in the feedback path from flowing into the base of the transistor Q_1 and affecting its biasing conditions. The cascode transistors are biased using a simple resistive divider circuit. Output impedance matching is provided using an LC output matching stage consisting of an off-chip inductor L_C, and capacitor CC_{OUT} that also acts as an output DC blocking capacitor.

On-wafer measurements are carried out to evaluate the performance of the low-noise amplifier. S-parameter results based on the on-wafer characterization of the LNA are depicted in Figure 6.3.



(a) Input return loss S_{11}.

(b) Reverse isolation S_{12}.

(c) Forward transmission gain S_{21}.

(d) Output return loss S_{22}.

Figure 6.3: S-parameter measurement results of the implemented low-noise amplifier.

The LNA achieves a maximum gain of 16 dB, a gain flatness of 2 dB, reverse isolation larger than 22 dB, and input return loss larger than 8.7 dB in the frequency range of 500 MHz to 2.5 GHz. The output

return loss drops below 8 dB for frequencies higher than 1.5 GHz. Optimization of the output return loss could be considered for future work, as it will help improve the inter-stage matching between the LNA and gain slope equalizer in the RF transceiver front-end. The LNA consumes 28.05 mW power from a 3.3 V supply. Post-layout co-simulation results of the LNA show that its noise figure is lower than 3.7 dB.

6.1.2 Wideband RF Power Amplifier

The power amplifier utilizes a cascode configuration of high-voltage SiGe HBTs to provide the required amplification and output power across the wide bandwidth of interest. A two-stage design approach is employed to isolate the noise figure and input impedance matching requirements of the PA from the high gain and output power requirements of the wideband realization. The schematic diagram of the implemented PA is shown in Figure 6.4.

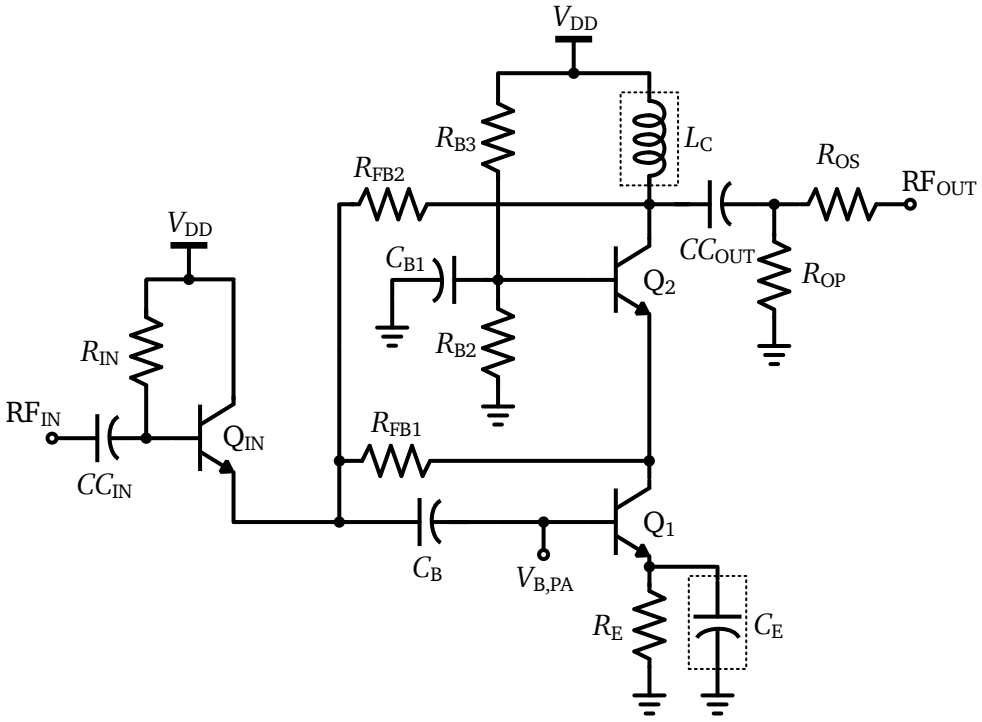


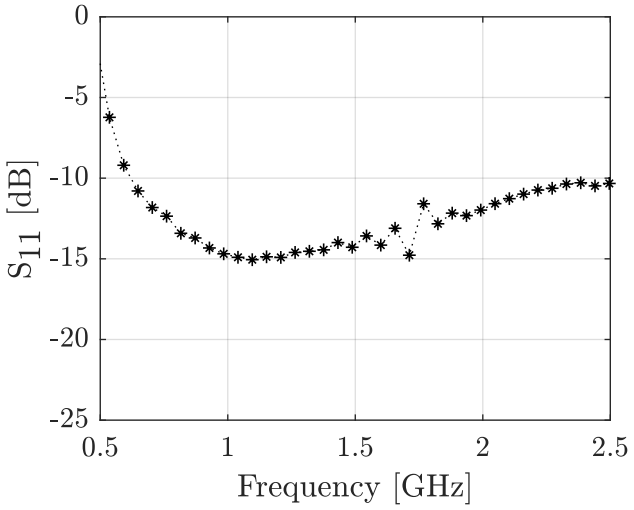
Figure 6.4: Schematic of the implemented power amplifier.

An active input matching network is employed as the first stage, as an alternative realization employing a passive input matching network was found to be area intensive. At the input, a DC blocking capacitor is used to isolate the DC bias point of the circuit from the output of the fine attenuator. The combination of resistor R_{IN} and transistor Q_{IN} sets the impedance of the circuit when seen from the input. Transistor Q_1 is designed to provide high amplification and high output power. Dual shunt feedback resistors R_{FB1} and R_{FB2} are added to improve the gain flatness and help with the input and output impedance matching requirements of the circuit. The cascode configuration minimizes the miller effect and improves the wideband performance.

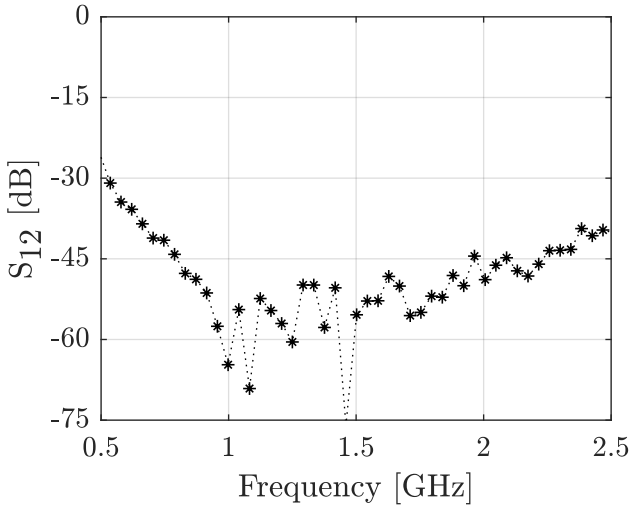
The capacitor C_B is added to block any DC current in the feedback path from flowing into the base of the transistor Q_1 and affecting its biasing conditions. An off-chip bias is utilized in order to avoid the area overhead of an on-chip realization. Capacitor CC_{OUT}, inductor L_C and resistors R_{OS} and R_{OP} together form the output matching network. The emitter degeneration resistor R_E is added to improve the linearity of the circuit. The off-chip bypass capacitor C_E helps in improving the stability and high-frequency gain of the circuit.

The power amplifier consumes 156.1 mW power from a 3.3 V supply. On-wafer measurements are carried out to evaluate the performance of the power amplifier. S-parameter measurement results of the PA are depicted in Figure 6.5. From the s-parameter measurement results, it can be observed that the gain flatness of the amplifier is 6 dB within the frequency range of 500 MHz to 2.5 GHz. The input return loss is larger than 10 dB from 625 MHz to 2.5 GHz. At frequencies lower than 625 MHz, the input return loss drops below 10 dB. The reverse isolation of the power amplifier is very good at above 28 dB across the bandwidth of interest, and the output return loss is larger than 10 dB across the bandwidth of interest. The measured output power characteristic of the amplifier is illustrated in Figure 6.6. The output P1dB compression point is 6.25 dBm at 1.5 GHz input signal frequency.

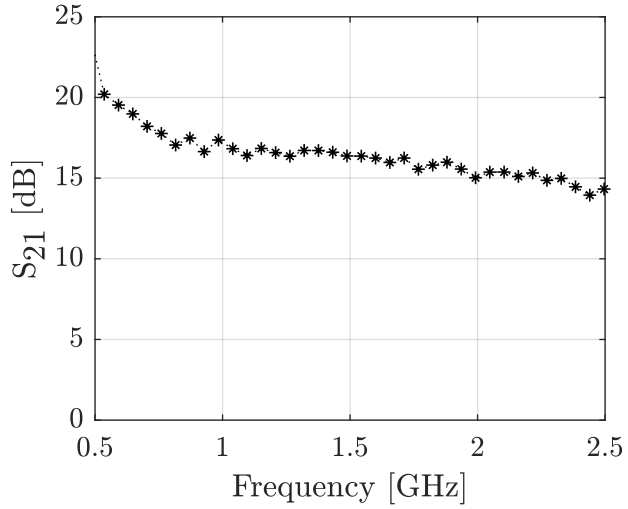
Since the primary focus of this work has been on enhancing the digital controllability of the RFFE, the results achieved for the PA are satisfactory. However, there is good potential for future research work with a focus on reducing the gain flatness to below 2 dB and improving the input return loss to levels higher than 10 dB across the bandwidth of interest.



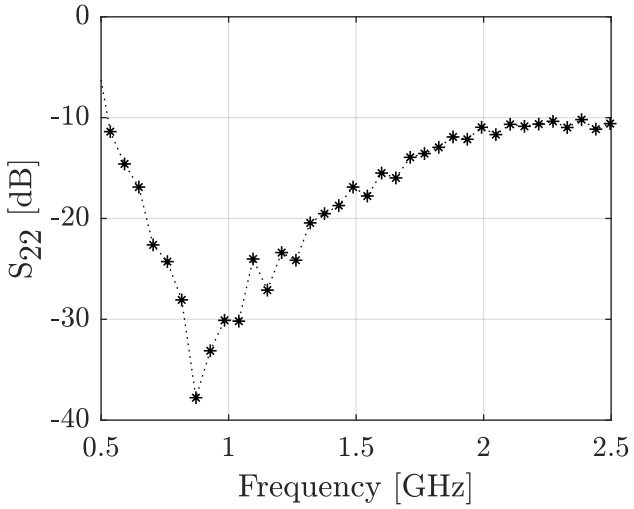
(a) Input return loss S_{11}.



(b) Reverse isolation S_{12}.



(c) Forward transmission gain S_{21}.



(d) Output return loss S_{22}.

Figure 6.5: S-parameter measurement results of the implemented power amplifier.

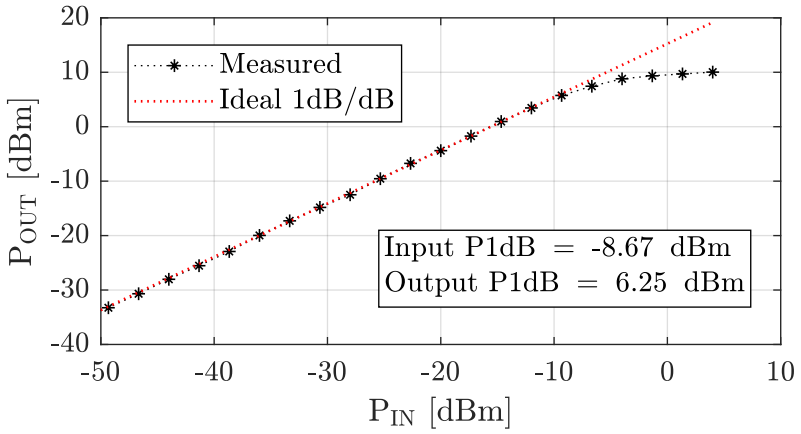


Figure 6.6: Measured output power of power amplifier at 1.5 GHz input frequency.

6.2 Application Example: Digitally Controllable RFIC with BiST and Wavelength Control for FTTx Applications

The RFFE is employed as part of an RFIC that provides digital control of gain, gain slope equalization, wavelength tuning, and built-in self-test (BiST) functionalities for optical transceiver modules in FTTx applications [111]. The block diagram of the implemented RFIC is shown in Figure 6.7.

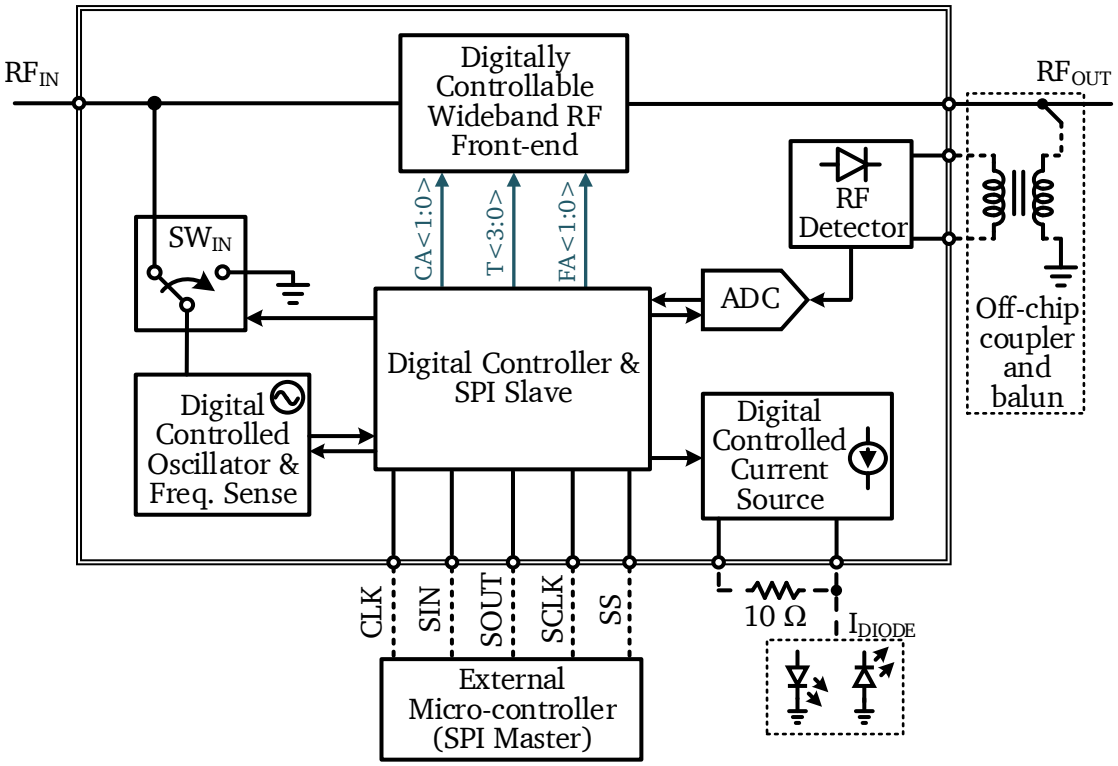


Figure 6.7: RFIC block diagram showing the important blocks.

The RFIC can be operated in two modes, the normal operation mode and the test mode. In the normal mode of operation, the RF switch SW_{IN} is turned off and the input to the RF circuit chain is provided at

the input pin of the RFIC. In the test mode of operation, the external input is decoupled and the switch SW_{IN} is set to pass the output from a digitally controllable oscillator (DCO) to the RF circuit chain.

The DCO generates an output signal that has close to -22 dBm output power and seven frequencies that cover the lower, middle, and top end of the frequency range, and are digitally controllable through the on-chip digital controller and the external micro-controller [111]. A frequency sense circuit is used to the DCO to approximately gauge the generated frequency. An analog-to-digital converter (ADC) is added to convert the detector output to digital signals for transmission to the external micro-controller.

The digitally controllable current source (DCCS) is meant for current control of the laser diodes and photodiodes that are used within the optical transceiver module in FTTx applications for the signal conversion between the optical and electrical mediums [111, 115]. By controlling the current through the diodes, the wavelength of the signal can be tuned.

The architectural diagram and timing diagram of the digital controller are shown in Figures 6.8 and 6.9, respectively, and the signals used within these diagrams are described in Table 6.1. The serial-parallel interface (SPI) slave is controlled by an external micro-controller. The slave has a 24-bit input data and a 24-bit output data and reads/writes these data one bit at a time serially.

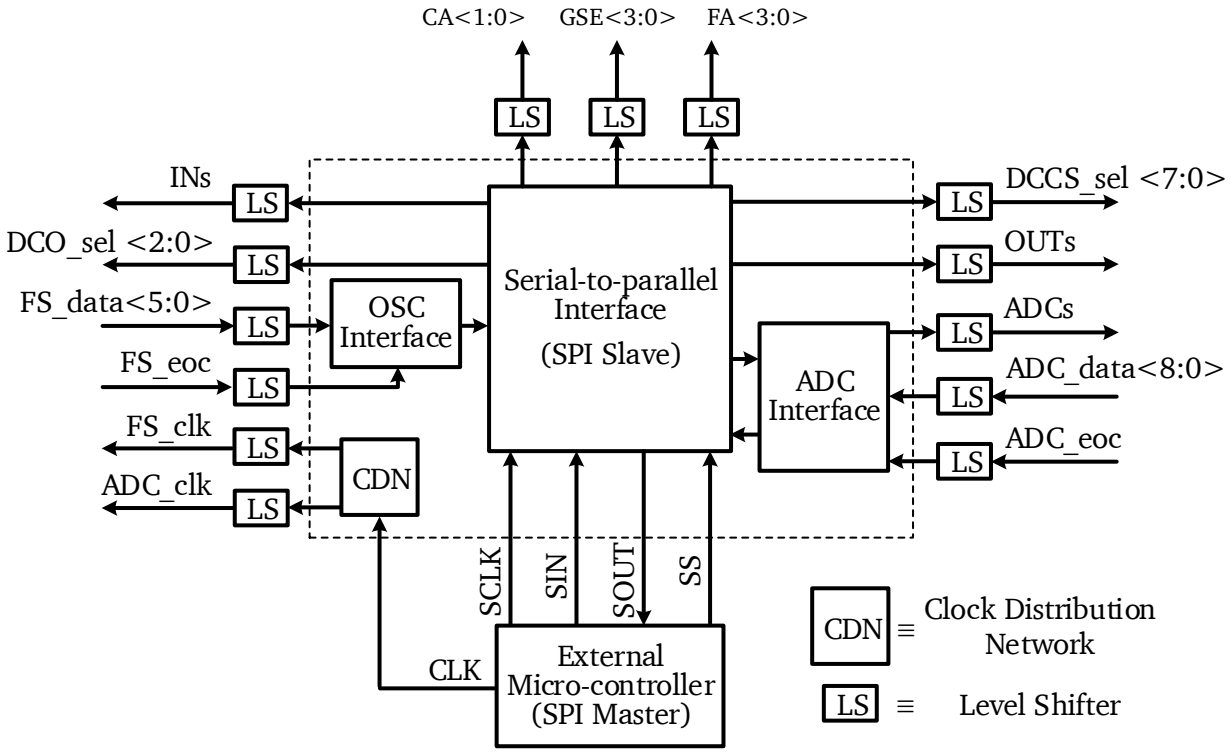


Figure 6.8: Digital controller architectural diagram.

The die photograph of the overall RFIC is shown in Figure 6.10. The die has dimensions of 2.9 mm x 1.76 mm and the overall area is 5.104 mm^2. The die is mounted on a QFN package and wire bonded for chip level interconnection. To lower the length of the bond-wires connecting the RF pads to package pins, the die is placed asymmetrically with respect the x-axis within the package, with the top edge of the die placed closer to the package edge. A 6mm x 6mm 40 pin QFN package is used for packaging. EM simulations are performed to extract the s-parameter models for the chip interconnects and these models are then utilized in design phase for co-simulation purposes.

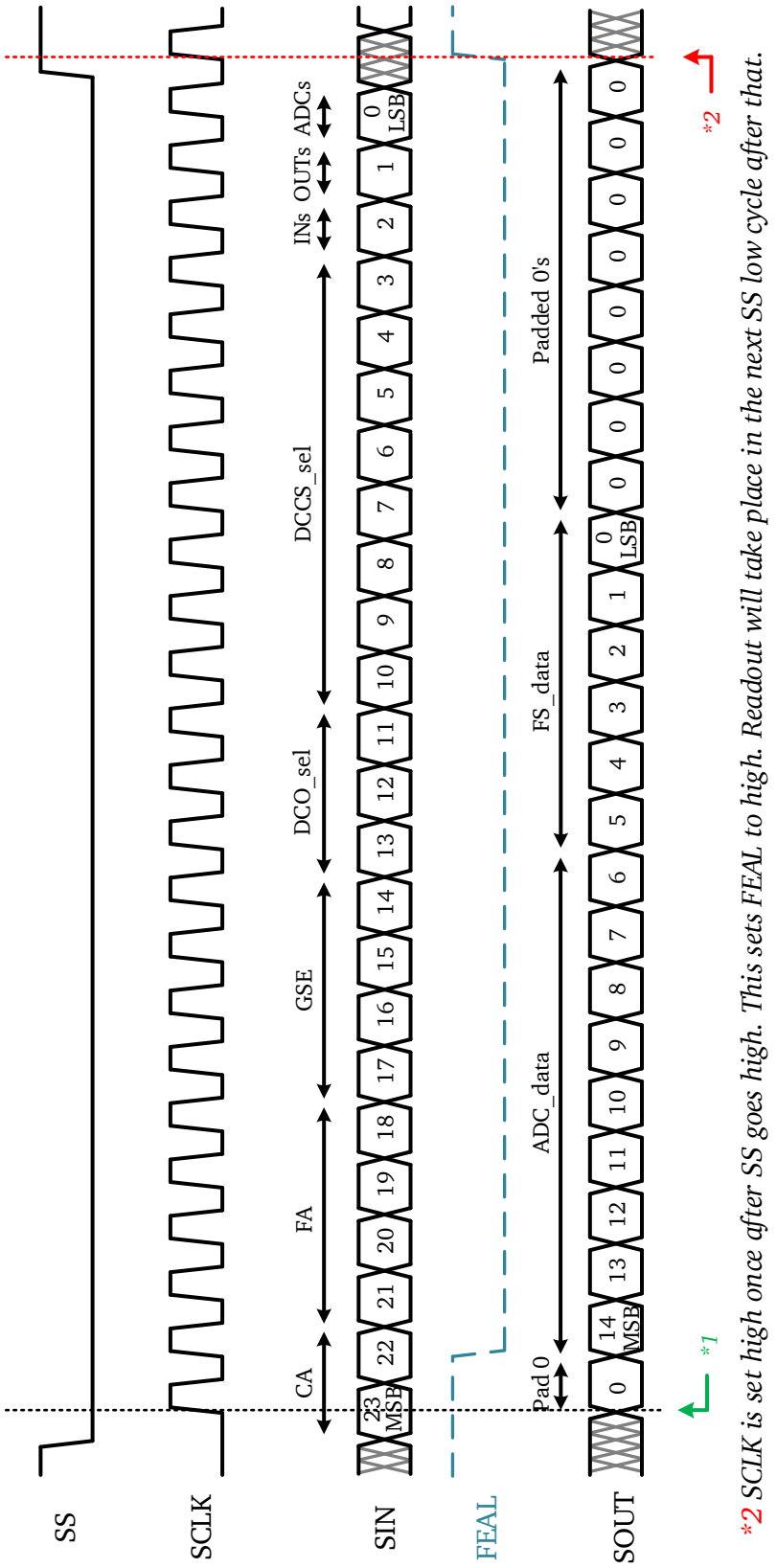


Figure 6.9: Digital interface timing diagram.

Table 6.1: Overview of RFIC naming conventions.

Signal Name	Description	Remarks
SW_{IN}	RF input switch for BiST	-
SW_{OUT}	RF output switch for BiST	-
SW_{ADC}	Switch at ADC input to select between detector output and on-chip temperature sensor output	-
CA	Control bits for coarse attenuator	2 bits
GSE	Control bits for gain slope equalizer	4 bits
FA	Control bits for fine attenuator	4 bits
DCO_sel	Control bits for DCO	3 bits
DCCS_sel	Control bits for DCCS	8 bits
INs	Control bit for SW_{IN}	1 bit
OUTs	Control bit for SW_{OUT}	1 bit
ADCs	Control bit SW_{ADC}	1 bit
ADC_data	ADC output	9 bits
ADC_eoc	ADC end of conversion	1 bit
ADC_clk	Clock for ADC	2.5 MHz
FS_data	Frequency sense circuit output	6 bits
FS_eoc	Erequency sense end of conversion	1 bit
FS_clk	Clock for frequency sense circuit	5 MHz
SCLK	SPI slave clock	-
SIN	SPI slave input	-
SOUT	SPI slave output	-
SS	SPI slave select	-
CLK	External clock to clock distribution network (CDN)	10 MHz

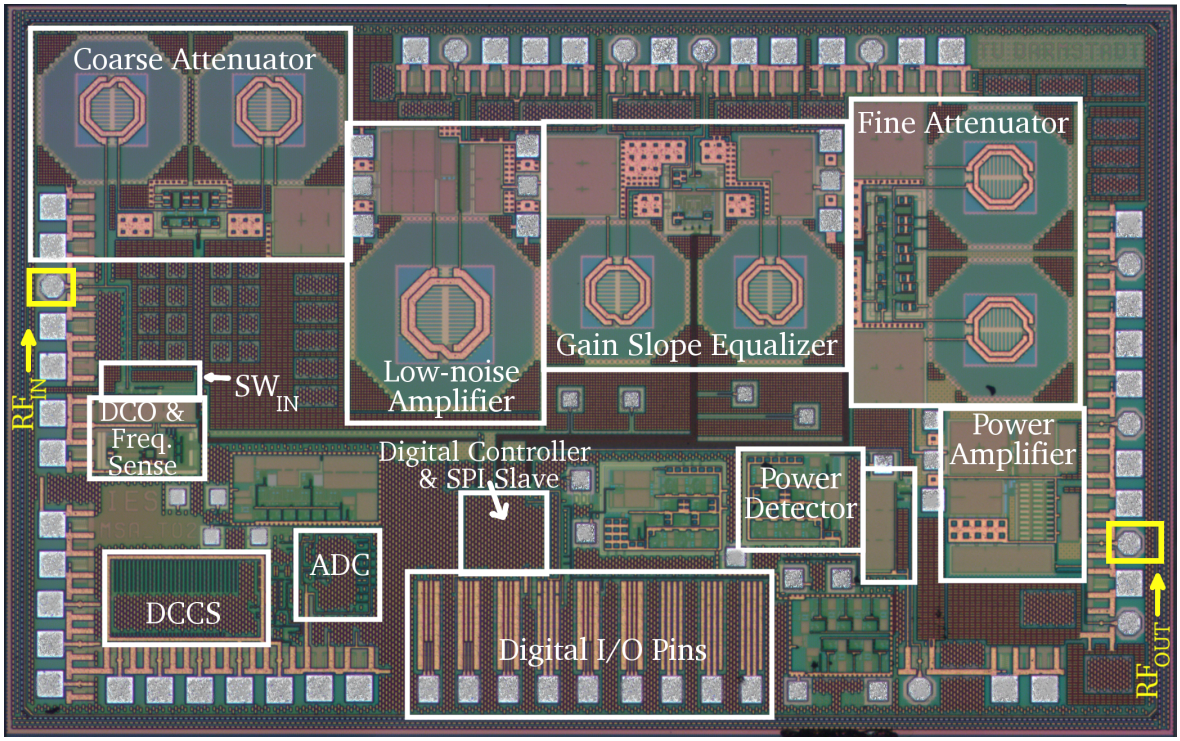
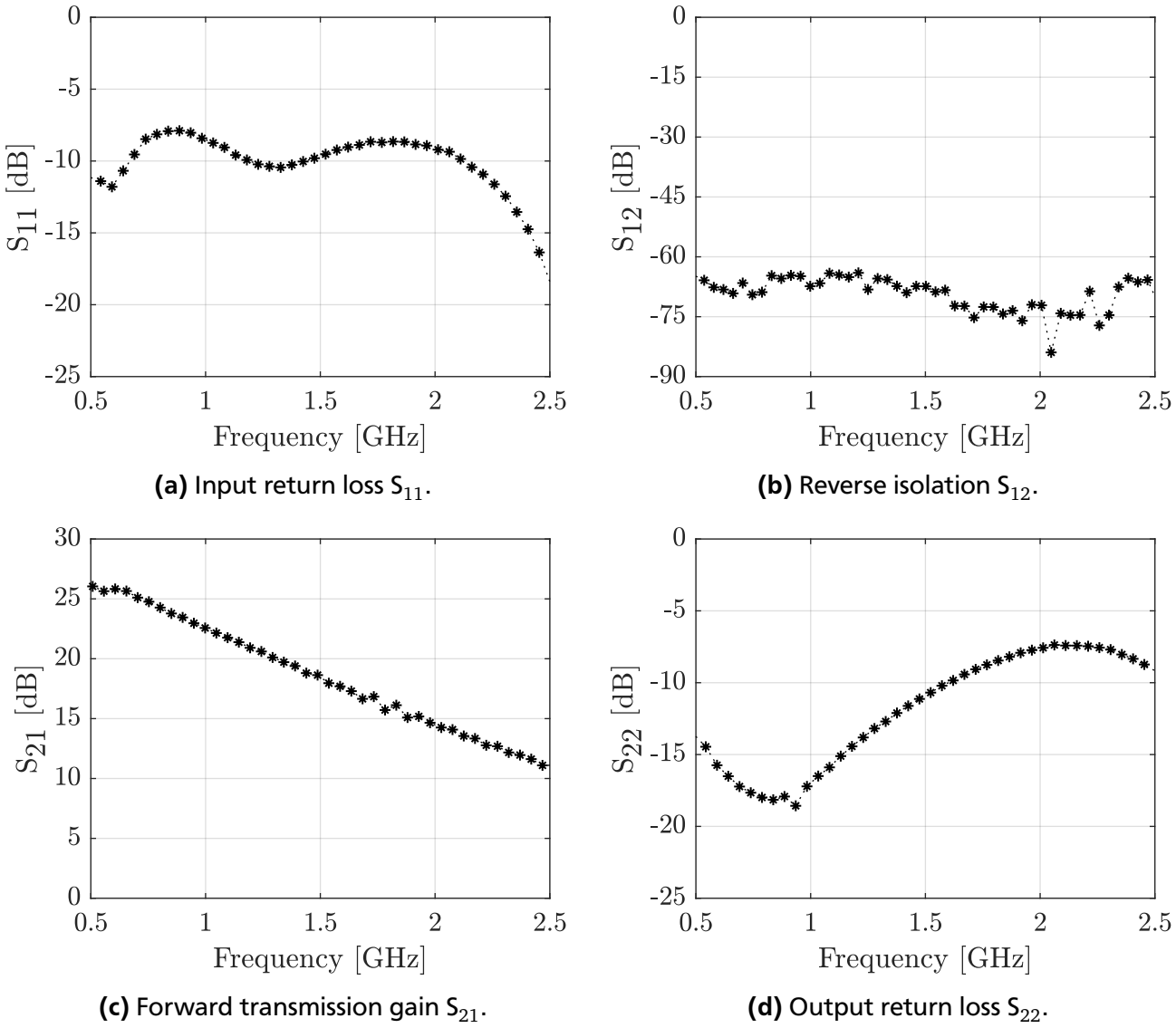


Figure 6.10: RFIC die photograph. Die area = 5.104 mm^2.

6.3 RF Front-End Measurement Results

The packaged IC is mounted on evaluation boards for measurement purposes. The RFFE can be operated under different digital control settings for the coarse attenuator, gain slope equalizer and fine attenuator. As a result, there are 512 different digital settings possible. Selected measurement results are summarized in this section.

The s-parameter measurement results of the RFFE are illustrated in Figure 6.11 for the case when the gain slope equalizer is set to operate in the bypass mode and an overall attenuation of 0.5 dB is provided. The stability factors, K and B_1, are calculated from the s-parameters and plotted in Figure 6.12. The necessary and sufficient conditions for unconditional stability, $K > 1$ and $B_1 > 0$, are satisfied across the bandwidth of interest, ensuring the stability of the RFFE [110, p. 222].



(a) Input return loss S_{11}.

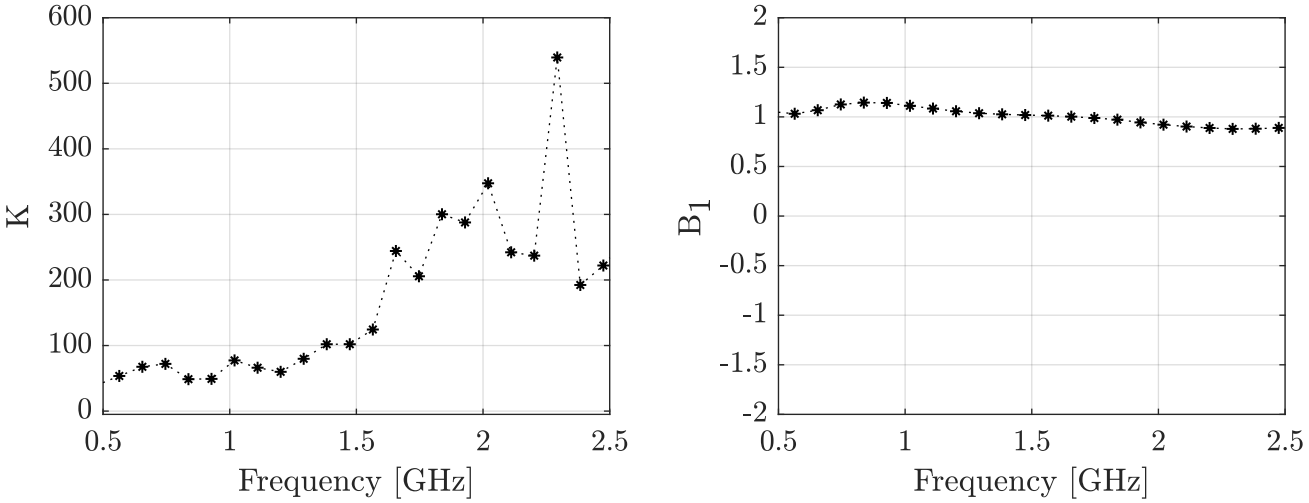
(b) Reverse isolation S_{12}.

(c) Forward transmission gain S_{21}.

(d) Output return loss S_{22}.

Figure 6.11: S-parameter measurement results of RFFE for 0.5 dB attenuation setting.

To observe the effectiveness of the gain control circuitry, the S21 plots for all attenuation settings from 0.5 dB to 31.5 dB are plotted in Figure 6.13. Figure 6.14 shows the performance of the RFFE when only one switched attenuator within the coarse and fine attenuators is turned on at a time. Figure 6.15, depicts



(a) Stability factor K. **(b)** Stability factor B_1.

Figure 6.12: Stability plots of RFFE for 0.5 dB attenuation setting.

the performance for selected attenuation settings across the attenuation range to display the effectiveness of the gain control circuitry.

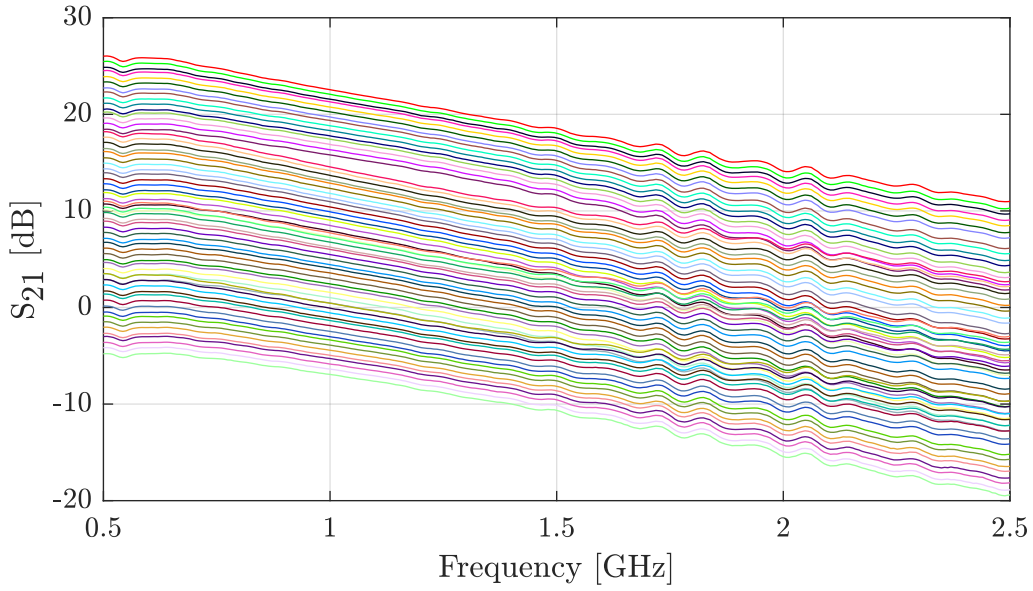


Figure 6.13: Measurement results for gain of RFFE for all attenuation settings from 0.5 dB to 31.5 dB when gain slope equalizer is bypassed.

The effectiveness of the gain slope equalizer circuitry is verified by keeping the attenuation state constant and varying the gain slope equalization setting. The gain and the normalized gain responses for different gain slope equalization settings based on the measurement results for three different attenuation settings are shown in Figure 6.16. Normalized gain for a particular gain slope equalization setting is the gain relative to the gain when the gain slope equalizer is operated in the bypass state. The digital control of gain slope equalization helps in improving the flatness of the RFFE, as observable from the results. For higher attenuation states, the gain slope equalization is clearly visible across the bandwidth of interest. However, when the attenuation is low, the high-frequency equalization is limited. This can be attributed to mismatches in the inter-stage matching performance under different attenuation settings.

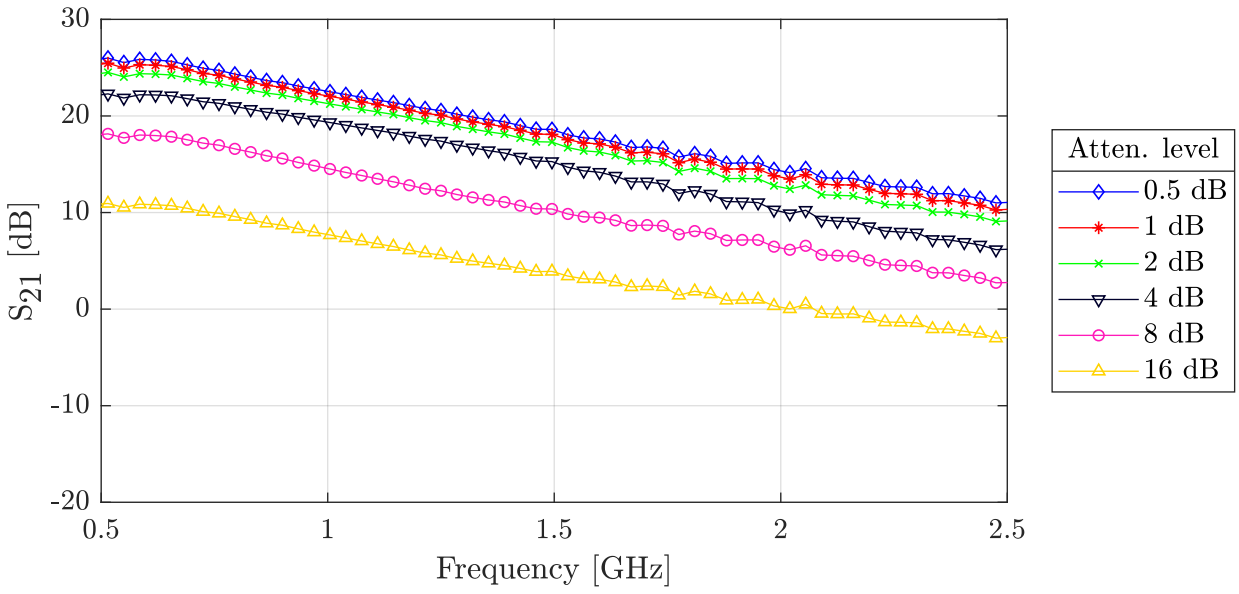


Figure 6.14: Measurement results for gain of RFFE for binary weighted attenuation level settings when gain slope equalizer is bypassed.

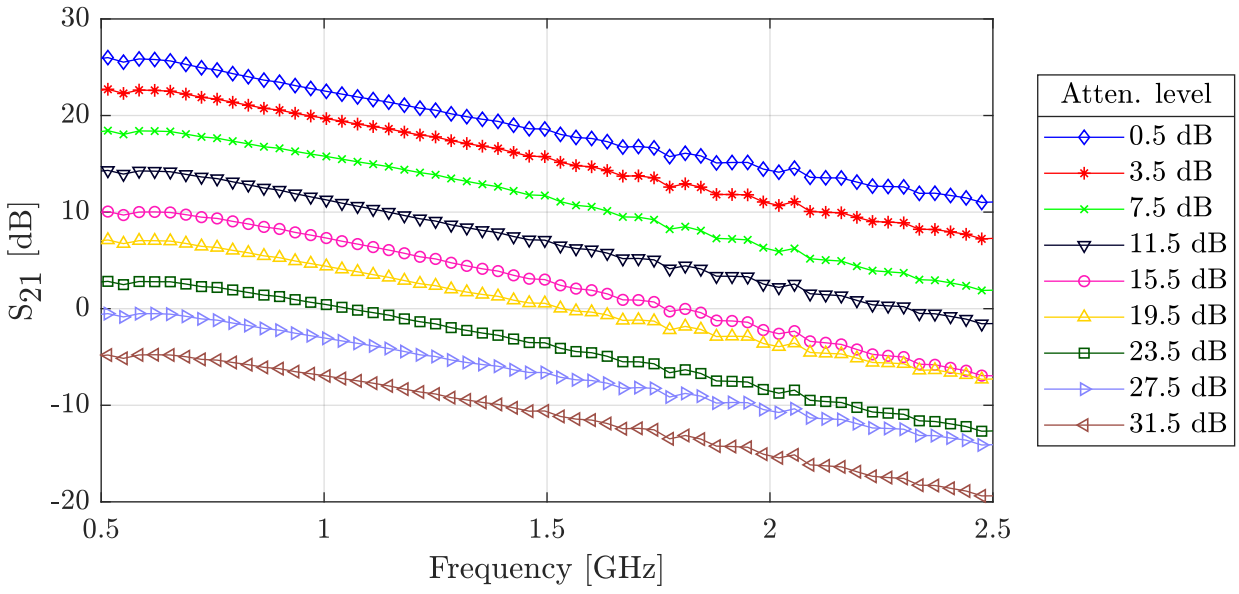
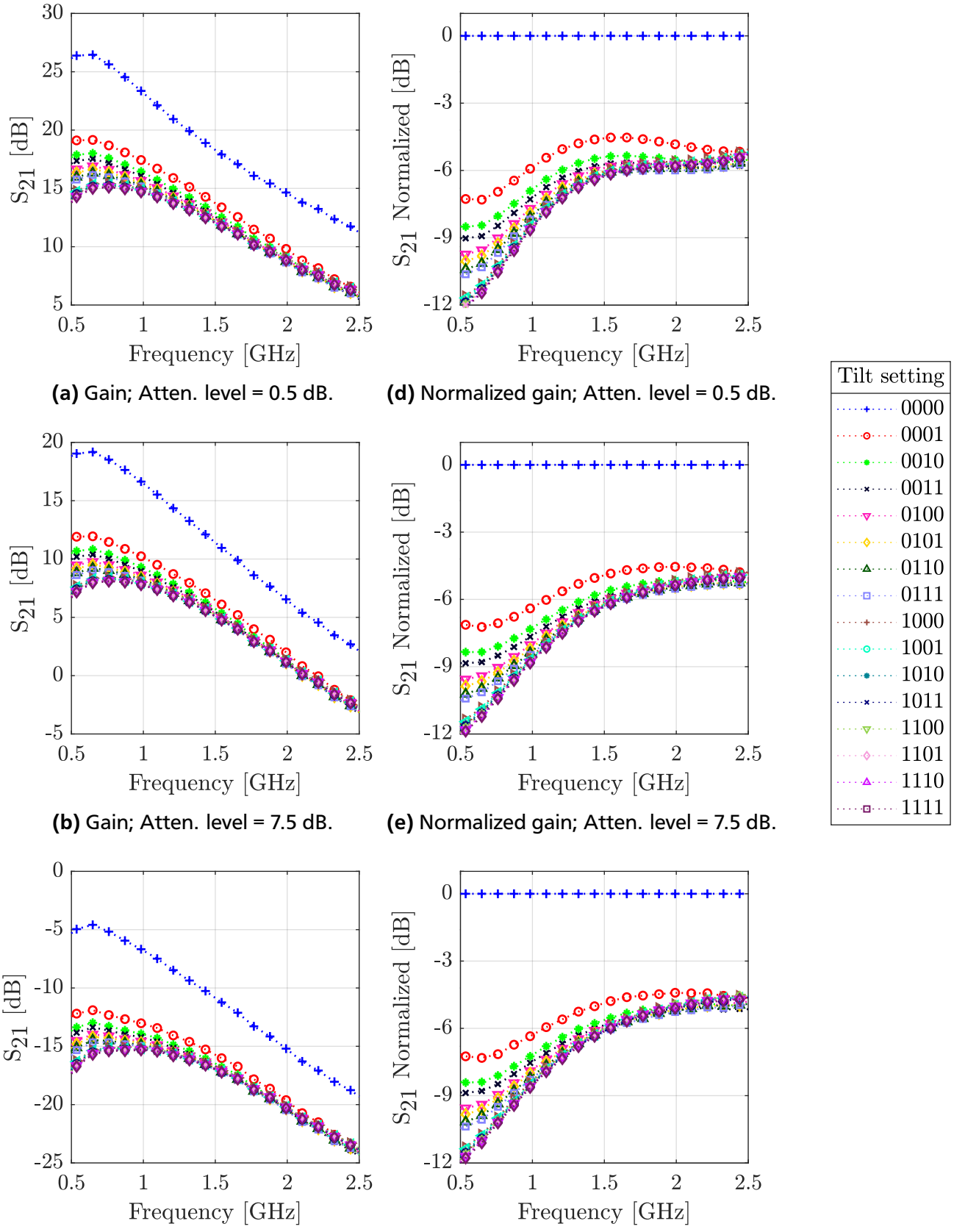


Figure 6.15: Measurement results for gain of RFFE for selected attenuation level settings across the gain control range of the RFFE when gain slope equalizer is bypassed.

Future research work could concentrate on understanding these mismatches and methods to overcome them. The gain slope equalization provided by the equalizer circuit as part of the RFFE is tabulated in Table B.1 in Appendix B for five different attenuation settings.

The measurement results of the noise figure of the RFFE is shown in Figure 6.17. The minimum value of noise figure is 7.125 at 1.33 GHz. At certain frequencies, the noise figure is higher than 10 dB. Further improvements to the noise performance of the RFFE is a potential future research direction that could be undertaken. The RFFE achieves a compression-free output power higher than 5 dBm. The power characteristic of the RFFE is shown in Figure 6.18 for an input frequency of 1.6 GHz.



(a) Gain; Atten. level = 0.5 dB.

(d) Normalized gain; Atten. level = 0.5 dB.

(b) Gain; Atten. level = 7.5 dB.

(e) Normalized gain; Atten. level = 7.5 dB.

(c) Gain; Atten. level = 31.5 dB.

(f) Normalized gain; Atten. level = 31.5 dB.

Figure 6.16: Measurement results of RFFE for different gain slope equalization (tilt) settings. (a), (b) and (c) depict gain at attenuation levels 0.5 dB, 7.5 dB and 31.5 dB, respectively. (d), (e), and (f) are normalized gain plots at attenuation levels 0.5 dB, 7.5 dB and 31.5 dB, respectively.

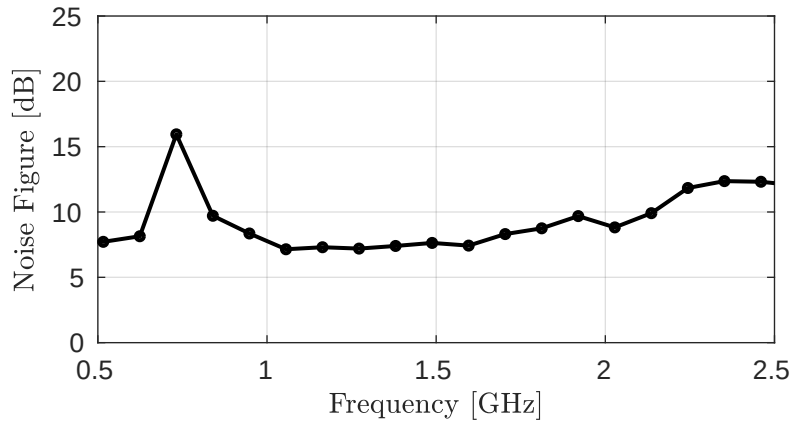


Figure 6.17: Measurement results of noise figure of RFFE for attenuation = 0.5 dB.

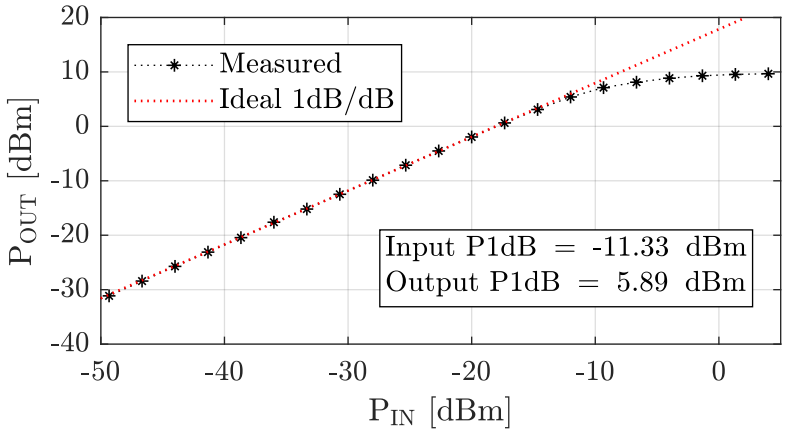


Figure 6.18: Measurement results of output power characteristic of RFFE at 1.6 GHz for attenuation = 0.5 dB.

6.4 Summary

A wideband RF transceiver front-end, RFFE, employing digital control of gain and gain slope equalization across an operating bandwidth of 500 MHz to 2.5 GHz is presented in this chapter. The RFFE employs the coarse attenuator and fine attenuators presented in Chapter 3 for digital gain control and the DCGSE presented in Chapter 4 for gain slope equalization. The SDLA power detector presented in Chapter 5 is included for power detection. Additionally, this chapter also presented the implementation results of a low-noise amplifier and a power amplifier added within the RFFE for signal amplification purposes are presented.

An application example of the RFFE, as part of an RFIC, was also presented in this chapter. Apart from the RFFE, the RFIC incorporates digital control for built-in self-test and wavelength control functionalities for the optical transceiver module for which it is intended. The digital control is provided through an on-chip digital controller that is controlled by an external micro-controller through an SPI interface. Overall, the RFIC occupies an area of 5.104 mm^2 when realized on a commercially available SiGe BiCMOS technology and it is packaged using a QFN 6mm by 6mm package.

Measurement results show that the RFFE achieves a digital gain control range larger than 30 dB with the help of the coarse and fine attenuators. The digital control of gain slope equalization is also verified from measurements. At its lowest attenuation setting of 0.5 dB, the RFFE has a gain slope equalization

range from 1.44 dB/GHz to 3.6 dB/GHz across the bandwidth of 500 MHz to 2.5 GHz for different digital settings. At its highest attenuation setting of 31.5 dB, it has a gain slope equalization range from 1.49 dB/GHz to 3.78 dB/GHz across the bandwidth of 500 MHz to 2.5 GHz for different digital settings

7 Conclusion

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Digital control is being increasingly utilized in radio frequency integrated circuits to widen the range of deployment conditions and utility of such systems within a system-on-chip environment. The increase in digital control in an integrated RF front-end also introduces additional challenges concerning the realization of the system. Three major aspects associated with the design and implementation of such systems have been focused upon in this work, and a wideband RF transceiver front-end has been presented to demonstrate the findings and propositions concerning these three research aspects.

7.1 Contributions

The research aspects and the results of this work can be formulated in the form of these major contributions:

- **The influence of the choice of technology in a single technology based system-on-chip realization of digital gain control in RF front-ends has been evaluated.**
  The influence of the choice of technology on the performance of RF switched attenuators has been evaluated. A methodology to compare the effect of technology $R_{on}C_{off}$ value and the choice of attenuator topology on the performance of the attenuator has been proposed. Technologies with lower $R_{on}C_{off}$ values are better suitable for high performance switched attenuators, especially at higher attenuation levels. Choosing a technology more suited to the low-noise amplifier and power amplifier restricts the performance of switched attenuators.

- **An approach to implementing digital control for gain slope equalization suitable for system-on-chip integration has been proposed.**
  The proposed design has been implemented and verified for its functionality based on a realization using a SiGe BiCMOS technology. To the best of the author's knowledge, this is the first such digital gain slope equalization integration in a system-on-chip realization in published literature.

- **A large dynamic range and high sensitivity SiGe BiCMOS technology based wideband logarithmic power detector with state-of-the-art performance has been presented.**
  A state-of-the-art wideband large dynamic range RF power detector has been implemented to enable power detection across a large output power range that corresponds to the large input dynamic range and wide gain control range of the transceiver. Additionally, design approaches for high sensitivity were adopted, and the influence of noise contributions from circuit blocks were studied. AC coupling and DC feedback offset cancellation mechanisms were investigated for their suitability for a sensitivity-aware design of logarithmic power detectors having a wide input offset cancellation range.

- **A novel wideband RF front-end with digital control of gain and gain slope equalization, and intended for optical transceiver modules in FTTx applications, has been presented.**
  A gain control range larger than 30 dB gain is achieved by utilizing two step attenuators that consist of cascaded switched attenuation stages. The equalizer facilitates gain slope settings from

2.03 dB/GHz to 4.18 dB/GHz for the RF front-end. The digital control in the RF front-end is implemented using an on-chip digital controller and a SPI slave interface that is controlled by an off-chip micro-controller. The transceiver front-end has an input power range of -40 dBm to -20 dBm and a frequency range from 500 MHz to 2.5 GHz. The wide bandwidth is chosen to serve the extended L-Band frequency range that facilitates the FTTx deployment in broadcast and satellite communications such as CATV applications. A prototype implementation of the front-end system has been presented as part of an RFIC realized using a commercially available SiGe BiCMOS technology and packaged using a QFN package.

7.2 Future Research Scope

Different interesting questions arise based on the observations and results presented in this work. Many of these questions could be further explored with a view of further improving the circuit level or system level performance. The following

- **System-in-package implementation.**
  The implementation presented in this dissertation was based on the system-on-chip approach. As a result, all the circuit blocks of the RF transceiver front-end were realized using a single semiconductor technology. SiGe perspectives could be considered to carry forward the research presented in this work: BiCMOS technology was chosen as a compromise considering the high gain and comparatively high output power that could be provided by the SiGe HBTs and the ease of integration of digital logic. The choice of a choice technology, in turn, affects the performance of the RF circuits such as the step attenuators and the gain slope equalizer. Switches implemented using this technology demonstrate lower performance compared to a technology with a lower value for $R_{\mathrm{on}}C_{\mathrm{off}}$. Similarly, the minimum noise figure of the low-noise amplifier and the quality of the passives such as on-chip inductors, and the output power of the power amplifier are limited by the technology. A system-in-package implementation based on multiple semiconductor technologies suitable for different types of blocks of the RF transceiver front-end could be focused upon, and the performance of such a system-in-package implementation could be compared to the system-on-chip realization presented in this work.

- **RF-SOI based implementation.**
  An implementation based on an RF-SOI technology could be considered to achieve higher performance from the RF step attenuators, low-noise amplifier, and digitally controllable gain slope equalizer. Moreover, the improved isolation and reduced parasitics of SOI technologies could be made use of to reduce the frequency-dependent losses across the bandwidth.

- **Chip-on-board packaging.**
  This work employed a QFN package considering its excellent thermal characteristics and suitability for high-frequency applications compared to traditional packages with leads. The costs associated with QFN packages are also not on the higher side. However, the use of bond-wires affects the high-frequency performance of the IC. Alternative packaging technologies, such as chip-on-board, could be considered to reduce the interconnect losses, especially at the high power and supply and ground nodes.

- **Attenuator implementation using low voltage transistors.**
  This work concentrated on the maintenance of a single supply voltage for all the RF blocks. A 3.3 V supply was chosen considering the requirements of the SiGe HBTs and the high output power for the power amplifier. The switches in the attenuator were implemented using a 3.3 V high voltage CMOS transistors. A low voltage CMOS variant, which has been reported to provide a lower $R_{\mathrm{on}}C_{\mathrm{off}}$ value, could be used to realize the switches in the attenuators and thereby the performance of the switched attenuators could be improved.

- **Studying the high-frequency loss in gain slope equalization behavior.**
  The measurements carried out during the work concentrated on the PCB-level characterization of the whole RF front-end and the on-wafer measurements for low-noise amplifier and power amplifier. On-wafer characterization of the gain slope equalizer and the RF step attenuators could be carried out to study the achievable performance of the individual RF circuits in detail.

- **Modeling of inter-stage impedance matching.**
  Inter-stage matching is an important criterion in many RF systems with cascaded circuit blocks. However, it is not always possible to examine the inter-stage impedance matching in detail due to time and cost constraints. In this work, each block has been independently characterized for good impedance matching for 50 Ω terminations. The input and output return loss of the individual sub-circuits could be investigated further with a view of increasing the performance of the system further.

- **More intensive modeling for high-frequency characterization.**
  At higher frequencies, it is important to model the parasitics associated with the circuit interconnects, be it within the circuit level, or on the packaging level, or even on the board level. In this work, the modeling on the circuit level was limited to the two thick top metal layers of the technology, because their feature sizes are closer to the wavelength under consideration. Including the lower metal layers increases the simulation run times significantly. Also, the EM models of the packaging interconnects (bond-wires, package leads) and PCB routing were generated separately to the models of the on-chip metal routing. A future research exploration could be on the lines of extracting the models of all interconnects together with all the metal layers and substrate, and studying the differences that such a modeling approach would make to the system performance.

A MATLAB Function for Power Detector LCE Calculation

```
function [LCE_arr]=fn_LCE_calc2(Pin_arr,PDout_arr,Pin_sensvty_low,
  Pin_sensvty_high)
  % Function to read input data from ADExl csv
  % Author           : Sreekesh Lakshminarayanan
  % Version Date       : 03.08.2019
  % Version No.        : 2
  % Version Source : fn_LCE_calculator

  n_PIN_vals            = length(Pin_arr);
  PDout_ideal           = zeros(1,n_PIN_vals);
  LCE_arr               = zeros(1,n_PIN_vals);
  i_Pin_sense_low       = -1;
  i_Pin_sense_high      = -1;
  Pin_stepSize          = (Pin_arr(2) - Pin_arr(1));

  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  %--- Calc indices for high and low sensitivity range ---%
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  for i = 1:n_PIN_vals
    if Pin_arr(i)    >= Pin_sensvty_low
      i_Pin_sense_low        = i;
      break
    end
  end
  if i_Pin_sense_low == -1
    disp(['Error..!! Pin low value for sensitivity check not found']);
  end
  for i = 1:n_PIN_vals
    if Pin_arr(i)    > Pin_sensvty_high
      i_Pin_sense_high       = i-1;
      break
    end
  end
  if i_Pin_sense_high == -1
    disp(['Error..!! Pin high value for sensitivity check not found');
  end
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  %--- Recursively calculate minLCE case ---%
  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
  iBestH                = i_Pin_sense_high;
  iBestL                = i_Pin_sense_low;
  delLCE_min            = 100;
  for iH = (i_Pin_sense_low + 6):i_Pin_sense_high
```

```
        for iL = i_Pin_sense_low:(i_Pin_sense_high - 5)
            if iH >= iL + 5
                slope=(PDout_arr(iH)-PDout_arr(iL))/(Pin_arr(iH)-Pin_arr(iL));
                for j = 1:n_PIN_vals
                    PDout_ideal(1,j)=PDout_arr(1)+(j-1)*slope*Pin_stepSize;
                end
                LCE                            = (PDout_ideal(1,:) - PDout_arr)/
                    slope;
                LCE_inSenseRange = LCE(i_Pin_sense_low:i_Pin_sense_high);
                LCE_inSenseRange = LCE_inSenseRange - mean(LCE_inSenseRange);
                delLCE           = abs(max(LCE_inSenseRange) - min(
                    LCE_inSenseRange));
                if delLCE < delLCE_min
                    delLCE_min       = delLCE;
                    iBestH           = iH;
                    iBestL           = iL;
                end
            end
        end
    end
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    %--- Calculate LCEarr for delLCE_min ---%
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    slope = (PDout_arr(iBestH)-PDout_arr(iBestL))/(Pin_arr(iBestH)-Pin_arr(
        iBestL));
    for j = 1:n_PIN_vals
        PDout_ideal(1,j)           = PDout_arr(1) + (j-1) * slope *
            Pin_stepSize;
    end
    LCE    = (PDout_ideal(1,:) - PDout_arr) / slope;
    LCE_arr = LCE - mean(LCE(iBestL:iBestH));   %--- normalize LCE ---%
end
```

B Gain Slope Equalization Results of the RF Front-End

Table B.1: Gain slope equalization results in dB/GHz for the RFFE for different attenuation settings. S_4, S_3, S_2 and S_1 denote the digital control bits of the gain slope equalizer.

S_4	S_3	S_2	S_1	Attenuation = 0.5 dB	Attenuation = 7.5 dB	Attenuation = 15.5 dB	Attenuation = 23.5 dB	Attenuation = 31.5 dB
0	0	0	1	1.44	1.35	1.41	1.42	1.49
0	0	1	0	1.66	1.67	1.72	1.74	1.85
0	0	1	1	1.78	1.83	1.88	1.91	2.00
0	1	0	0	2.26	2.29	2.34	2.38	2.49
0	1	0	1	2.35	2.38	2.43	2.48	2.57
0	1	1	0	2.53	2.59	2.64	2.69	2.77
0	1	1	1	2.64	2.68	2.71	2.75	2.81
1	0	0	0	3.44	3.45	3.48	3.52	3.61
1	0	0	1	3.43	3.44	3.48	3.52	3.6
1	0	1	0	3.47	3.50	3.53	3.57	3.68
1	0	1	1	3.47	3.50	3.54	3.58	3.69
1	1	0	0	3.58	3.60	3.65	3.67	3.78
1	1	0	1	3.57	3.59	3.62	3.58	3.76
1	1	1	0	3.59	3.63	3.65	3.7	3.80
1	1	1	1	3.6	3.63	3.66	3.7	3.78

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