

# System Components and Design for OFDM-Based Broadcasting Receivers

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To Adriana my Beloved  
שימוני כחותם על לבך כחותם על זרועך  
כי עזה כמות אהבה קשה כשאל קנאה



# Abstract

Approaching the channel capacity limit has been the main goal of communication engineers since the pioneering work of Claude Shannon. This capacity depends primarily on the chosen schemes for channel coding and modulation, which need to be tailored to the specifics of the propagation environment. From an engineering perspective, it is important not only to maximize the channel capacity, but also to achieve this with the least complexity.

In addition to noise, a major impairment in terrestrial transmissions is the multipath nature of the channel, which affects the receiver performance dramatically. Over the past decade, orthogonal frequency-division multiplexing (OFDM) has emerged as the modulation of choice for such environments because of its inherent resilience to multipath effects and relative simplicity of the channel equalization, which allows for low-cost receivers. Nowadays, OFDM is a mature technology, being employed by various standards for both wireless networking and digital broadcasting.

The present doctoral thesis deals specifically with baseband receiver architectures for OFDM digital broadcasting, focusing on digital OFDM demodulation and to a lesser extent on forward error correction. The research scope includes the architectural exploration and optimization of several blocks at algorithmic and structural level: channel equalizer, QAM demapper, and Viterbi decoder. Because of their critical role, the channel equalizer and the Viterbi decoder are each treated in a dedicated chapter. The proposed architectures are optimized for area and take advantage of the new features found in modern FPGA's, such as embedded memories, multipliers, and shift registers.

Another important contribution of this thesis is the development of an efficient simulator for multipath channels with Doppler fading. Using an accurate channel simulator is essential for comparing simulation results between different teams. Especially critical is the modeling of the fading taps, since the fading process is much slower than the sampling rate. The proposed architecture is extremely scalable and suitable for both hardware and software implementation, the fading taps being generated by filtering white Gaussian noise. In this context, especially innovative are the solutions proposed for Gaussian noise generation and single-stage polyphase interpolation.

A final chapter of the thesis is dedicated to the functional modeling of OFDM receivers in SystemC and to the hardware design optimized for FPGA. The FFT block, which is the core of an OFDM demodulator, has been selected as a case study.



# Kurzfassung

Seit der grundlegenden Arbeit von Claude Shannon ist es zum Hauptziel jedes Nachrichtentechnikers geworden, die Kanalkapazitätsgrenze zu erreichen. Diese Kapazität hängt hauptsächlich von den verwendeten Kanalkodierungs- und Modulationsverfahren ab und muss den Gegebenheiten der Ausbreitungs Umgebung angepasst werden. Aus wirtschaftlicher Sicht ist es aber wichtig, nicht nur die Kanalkapazität zu maximieren, sondern dies mit dem geringsten Implementierungsaufwand zu erreichen.

Eine weitere Störung, die bei einer terrestrischen Übertragung neben dem Rauschen auftritt, ist die Mehrwegausbreitung des Kanals, die den Empfang sehr stark beeinträchtigt. In den letzten Jahren hat sich OFDM (Orthogonal Frequency Division Multiplexing) als bevorzugte Modulationsart durchgesetzt. Gründe dafür sind die inhärente Tauglichkeit für Mehrwegkanäle und die relative Effizienz dieses Kanalentzerrungsverfahrens, die die Implementierung preiswerter Empfänger ermöglicht. Heutzutage ist OFDM eine ausgereifte Technologie, die in verschiedenen Standards, sowohl drahtlose Netzwerke wie auch digitalen Rundfunk betreffend, angewandt wird.

Die vorliegende Doktorarbeit befasst sich besonders mit Basisband-Empfängerarchitekturen für OFDM-basierten digitalen Rundfunk, mit dem Schwerpunkt OFDM-Demodulation und, in geringerem Umfang, Fehlerkorrektur. Das Forschungsgebiet umfasst die Architekturuntersuchung und Optimierung verschiedener Empfängerbauelemente auf Algorithmenebene und Strukturebene: Kanalschätzer, QAM-Demapper, und Viterbi-Dekoder. Aufgrund ihrer kritischen Rolle werden dem Kanalschätzer und dem Viterbi-Dekoder eigene Kapitel gewidmet. Die vorgeschlagenen Architekturen sind optimiert hinsichtlich der benötigten Chipfläche und nutzen die Eigenschaften moderner FPGA-Bausteine wie eingebettete Speicherblöcke, Multiplizierer oder Schieberegister.

Ein weiterer wichtiger Beitrag dieser Dissertation ist der Entwurf eines effizienten Kanalsimulators, der die Mehrwegausbreitung und das Doppler-Fading richtig modelliert. Ein genauer Kanalsimulator ist für den Vergleich der Ergebnisse mehrerer an der Simulation beteiligter Teams unentbehrlich. Besonders wichtig ist die korrekte Fading-Modellierung der einzelnen Taps, da der Fadingprozess viel langsamer ist als die Abtastrate. Die entwickelte Architektur ist fein skalierbar und eignet sich besonders gut für Hardware- und Software-Implementierungen. Dabei werden die Fading-Taps durch Filterung unkorrelierter weißes Gaußsches Rauschens generiert. Besonders innovativ sind in diesem Zusammenhang die vorgeschlagenen Lösungen für die Generierung des Gaußschen Rauschens und für die einstufige Mehrphasen-Interpolation.

Das letzte Kapitel ist funktioneller SystemC-Modellierung von OFDM-Empfängern und dem FPGA-optimierten Hardware-Entwurf gewidmet. Der FFT-Baustein, der als Kern eines OFDM-Demodulators angesehen wird, wurde als Fallstudie gewählt.



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# List of Abbreviations

ACS	Add Compare Select
ADC	Analog-to-Digital Converter
AM	Amplitude Modulation
ASIC	Application-Specific Integrated Circuit
ASK	Amplitude Shift Keying
AWGN	Additive White Gaussian Noise
BER	Bit-Error Rate
CIR	Channel Impulse Response
COFDM	Coded OFDM
CORDIC	Coordinate Rotation Computer
CTF	Channel Transfer Function
DAB	Digital Audio Broadcasting
DAC	Digital-to-Analog Converter
DFT	Discrete Fourier Transform
DRM	Digital Radio Mondiale
DVB-T	Digital Video Broadcasting – Terrestrial
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FIFO	First In First Out
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
HF	High Frequency
IC	Integrated Circuit
ICI	Inter-Carrier Interference
IDFT	Inverse Discrete Fourier Transform
IEEE	Institute of Electrical and Electronic Engineers

IFFT	Inverse Fast Fourier Transform
IIR	Infinite Impulse Response
ISI	Inter-Symbol Interference
ITU	International Telecommunications Union
LAN	Local Area Network
LFSR	Linear Feedback Shift Register
LLR	Log-Likelihood Ratio
LS	Least Squares
LSB	Least Significant Bit
LSE	Least-Squares Estimation
MAC	Media Access Controller
MLC	Multi-Level Coding
MMS	Minimum Mean Square
MMSE	Minimum-Mean-Squares Estimation
MOC	Model of Computation
MSB	Most Significant Bit
MSE	Mean Square Error
OFDM	Orthogonal Frequency-Division Multiplexing
PRBS	Pseudo-Random Binary Sequence
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RAM	Random Access Memory
RMS	Root Mean Square
ROM	Read Only Memory
RTL	Register Transfer Logic
SNR	Signal-to-Noise Ratio
SOS	Second-Order Section
TDL	Tapped Delay Line
WGN	White Gaussian Noise
WSSUS	Wide-Sense Stationary with Uncorrelated Scattering
XOR	Exclusive OR Logical Operator